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EE 421 – 1001

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Switching Power Supply (12.5V) Using Boost Topology

Introduction

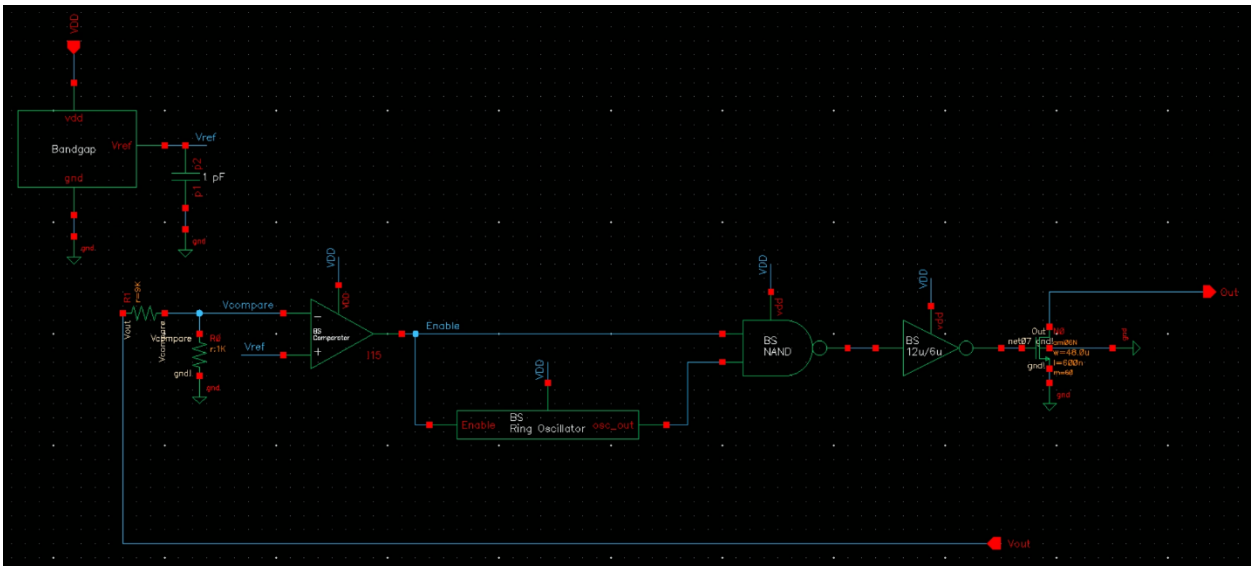
The focus of this project was to draft the designs for a boost converter using real CMOS in the C5 process. This is a form of switched-mode power supply, or SMPS, that is capable of stepping up a provided source voltage to a stable, desired target output voltage. The indicated spec for this design is such that the source voltage can vary between 4 and 5.25V while maintaining a stable 12.5V output at steady state. This is an incredibly valuable and prominent device in the modern age as it is utilized for charging a variety of important, everyday electronics from mobile phone chargers to medical test equipment. This report will consist of visual documentation and commentary for each major component utilized in the overall boost converter design, as well as delving into the reasoning behind certain design decisions.

The major components that I was required to draft in order to create the boost converter are a bandgap, comparator, and ring oscillator. The more minor components consist of a small inverter, slow inverter, NAND gate, and various-sized resistors and capacitors. Because these components are simpler, I will not be diving deep into them as they are drafted in accordance with their standard CMOS implementations and should not be focused on.

Boost Converter

As stated earlier, the boost converter is a switched-mode power supply, and it operates by simply driving an on-chip transistor between the cutoff and saturation states. The output voltage is sensed and constantly monitored to ensure that this transistor is switching states appropriately to maintain a steady 12.5V. When the transistor is in saturation, the circuit is closed. This enables the inductor to start building current, which is a positively sloped, linear relationship as indicated by the equation: $V = L\frac{di}{dt}$. When the transistor is in cutoff, and thus acting as an open, the current wants to continue to flow, but is now disconnected from the chip, so it begins to flow through a schottky diode which is connected to the load, and thus initiates charging. Additionally, there is a capacitor tied to ground after the schottky diode that builds a charge and is used as a filter to maintain the steady output value by supplying that charge to the load when the transistor is switched from cutoff to saturation.

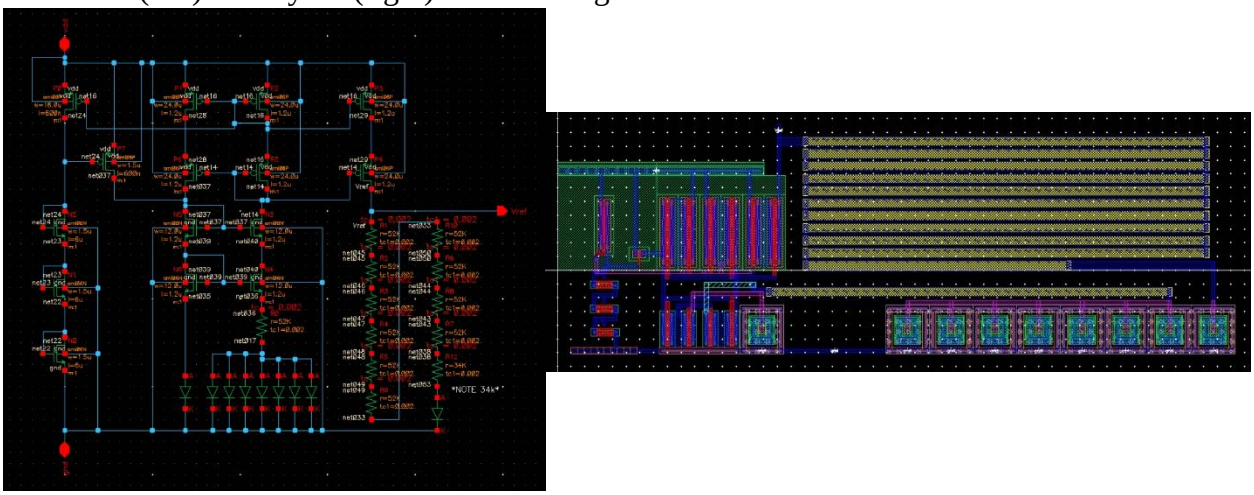
Boost Converter Schematic:



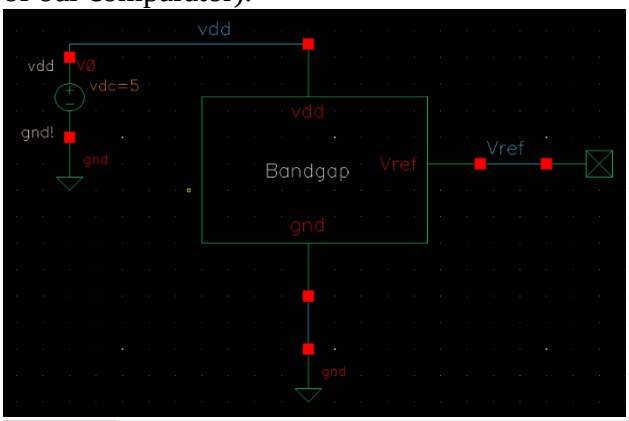
I will return to more images of and further commentary on the boost converter later in this document; however, here (above) is a schematic to provide a visualization of the previously explained circuit to give a rough idea of how each individual major component comes into play.

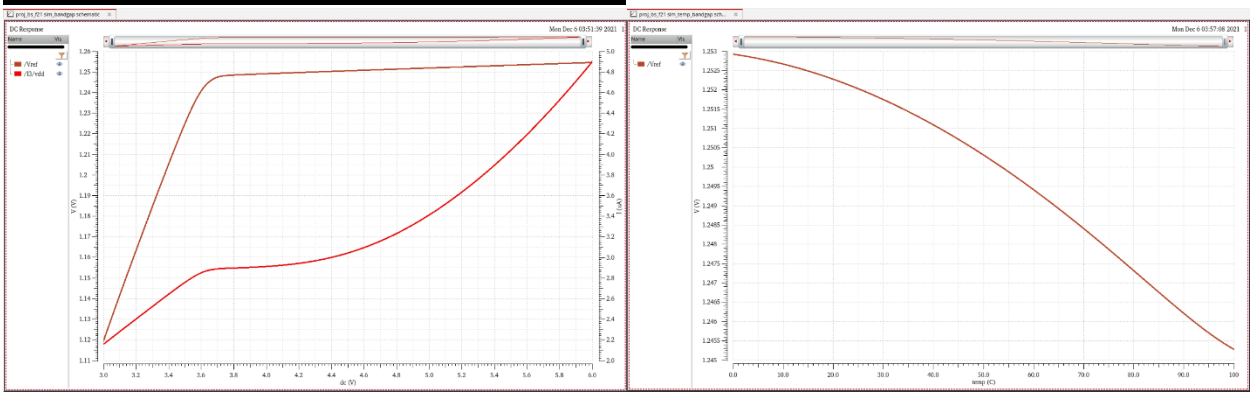
Bandgap

The bandgap is a critical element of this design as it provides the reference voltage that is used in the later designed comparator. This circuit is designed to provide a stable, steady 1.25V which will be compared to the diminished signal sensed from the output through the feedback loop. The schematic (left) and layout (right) for this design can be found as follows:



Additionally, I conducted simulations of this bandgap to display how it responds to changing VDD (left) and variance in temperature (right). The VDD varies from 3 to 6V (covering more than our spec's target range of 4 to 5.25V) and the temperature varies from 0 to 100 degrees Celsius. As can be observed in the resulting graphs below, this bandgap design is incredibly reliable even in both seemingly adverse situations, as the output voltage maintains a steady 1.25V under all conditions (with variance being in the millivolts, which is negligible in the eyes of our comparator).



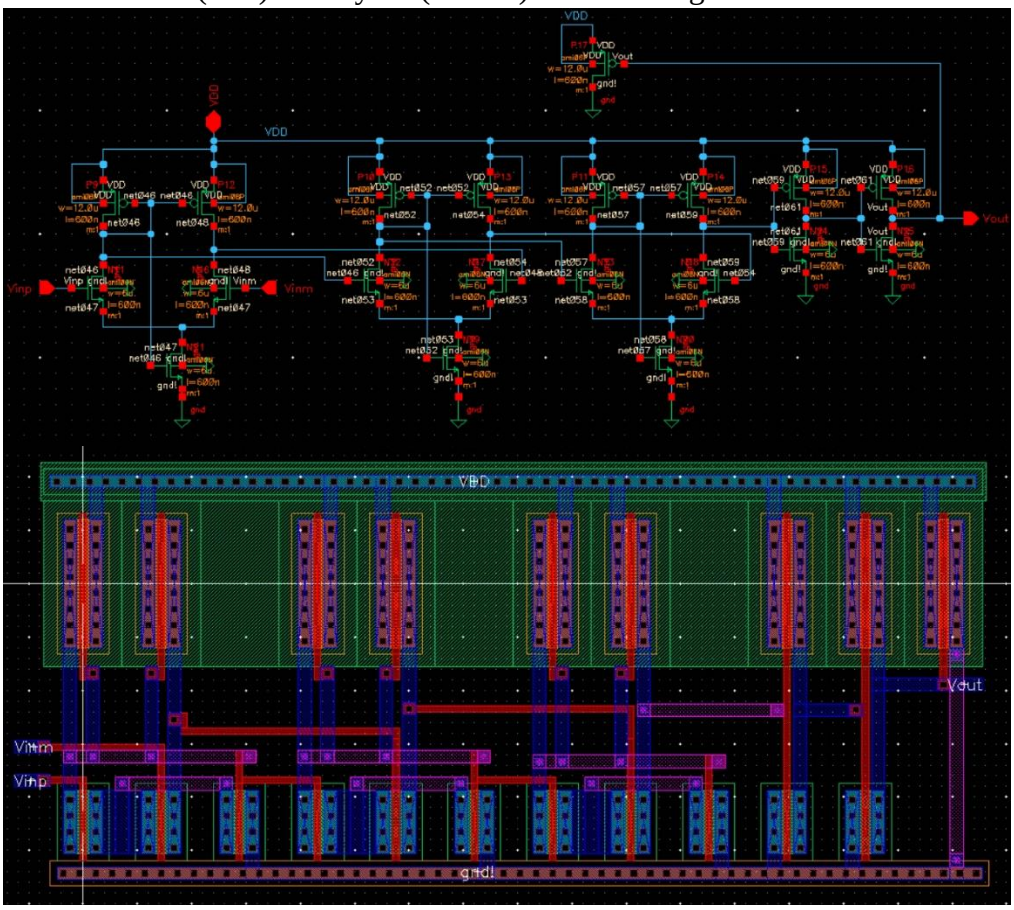


Comparator

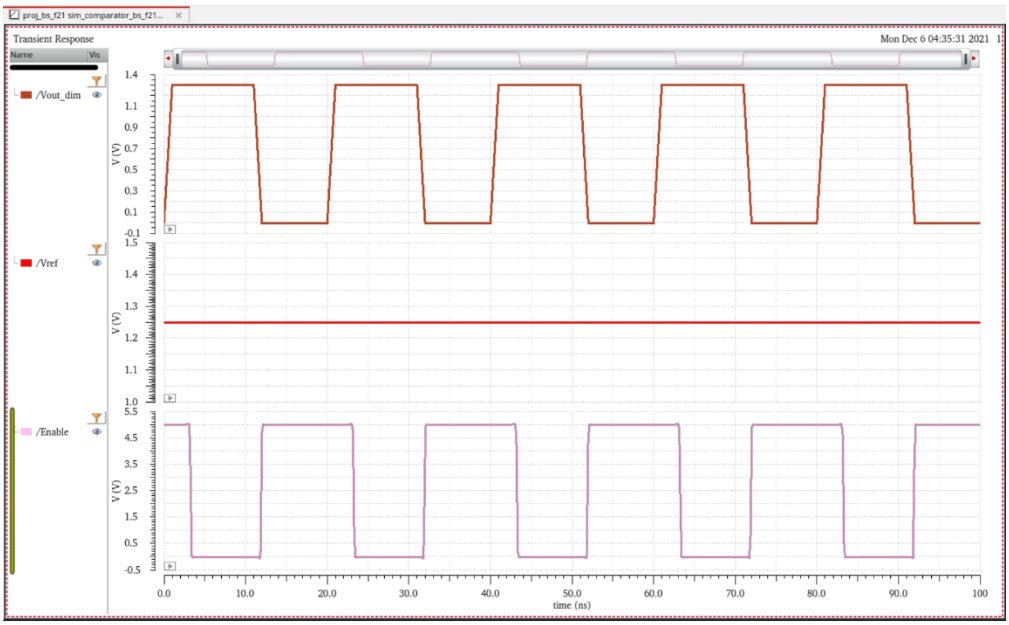
The comparator is a key device as it essentially conducts all of the sensing that makes this device's operation possible. It takes in the output voltage value, which is greatly diminished by a voltage divider, and compares that to the reference voltage supplied by the bandgap. A simple logic check occurs, in the which the comparator will only output an enable, or 1, signal when Vout drops below 12.5V (which would indicate that we need to enable the NMOS device to close the circuit and build up the current again). Otherwise, the signal sent with be a 0, which will leave the NMOS device disabled and acting as an open. This sensing and enabling management ensures that the NMOS is in the proper state to either boost the output voltage back up to 12.5V or keep it from exceeding 12.5V. Mathematically, this is why we designed our bandgap to provide a 1.25V reference, as with the voltage divider formed by our resistor values of 9k and 1k, the equation that gives us this threshold voltage is as follows:

$$V_{ref} = 12.5\frac{1k}{1k+9k} = 1.25V$$

The schematic (first) and layout (second) for this design can be found as follows:

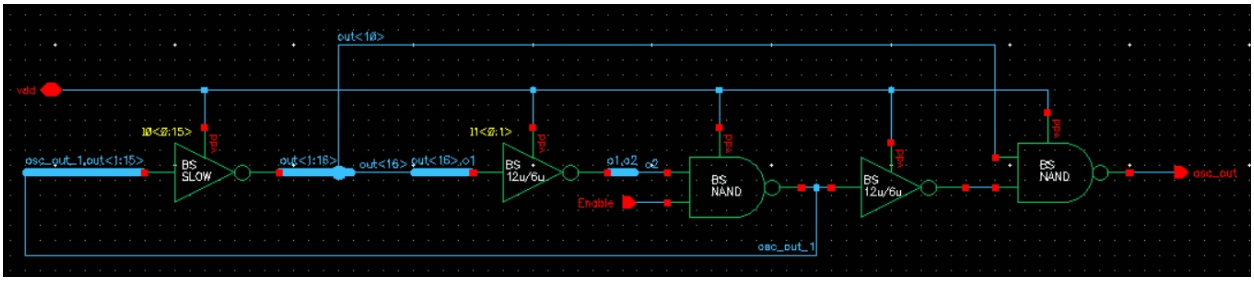


Additionally, I ran a rudimentary simulation of the comparator to showcase its operation. As stated, only once the negative terminal becomes larger than the positive terminal does the output enable signal become 1.



Ring Oscillator

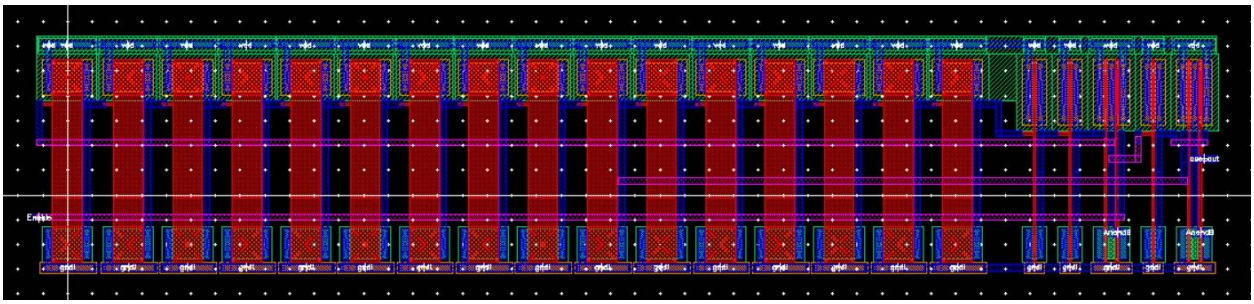
The ring oscillator is the last major component of this design. It is equally critical as it provides the circuit with both the duty cycle and hysteresis. The duty cycle is determined by changing which line we pull from the initial string of inverters shown in the following schematic image.



Currently out<10> is being utilized and it provides a duty cycle of about ~70%. This is the perfect target as this allows the output of the circuit to reach the target voltage of 12.5V even when the source is at the lowest spec voltage of 4V. This relationship can be observed through the following equation: $V_{out} = V_s * \frac{1}{(1-D)} = 4 * \frac{1}{(1-0.7)}$ =13.33V where Vs is the source voltage, and D is the on-time percentage of the duty cycle. For good design practice, I did not design to exact values and gave some leeway for even the minimum spec VDD value of 4V to be able to push a little past 12.5V.

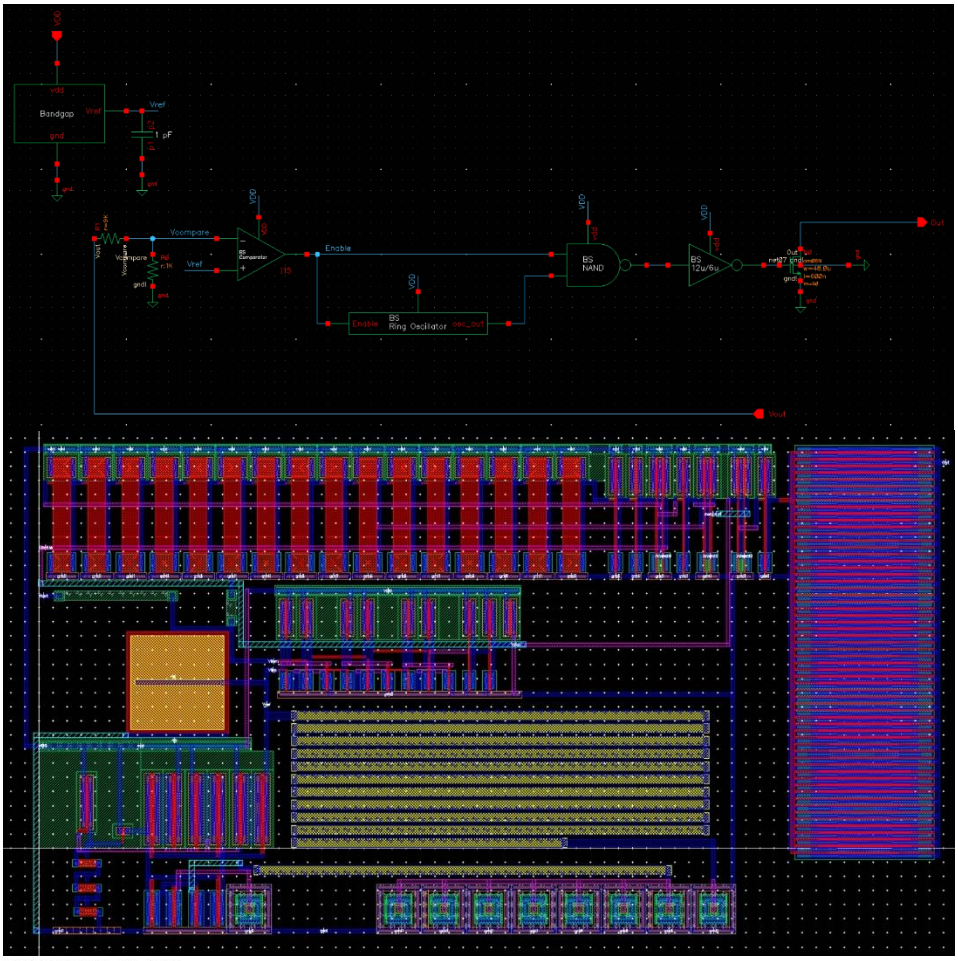
Regarding hysteresis, the frequency of this device determines the speed at which an enable signal from the comparator is actually able to enable the NMOS device.

Additionally, the straightforward layout can be observed below, in which I went back and redesigned my inverter and NAND gate layouts so that all of their VDDs and GNDs would each line up in one smooth strip.



Final Simulation and Testing

Now that the last major component has been implemented, it is time to return to the overall boost converter. As can be observed in the following images, the boost converter consists of every component that I previously drafted with some additional resistors and capacitors.




```
Compiling Diva LVS rules...

    Net-list summary for /home/staffier/CMOSedu/LVS/layout/netlist
       count
          67              nets
           4              terminals
          14              res
           1              cap
           9              diode
          43              pmos
          64              nmos

    Net-list summary for /home/staffier/CMOSedu/LVS/schematic/netlist
       count
          67              nets
           4              terminals
          14              res
           1              cap
           9              diode
          43              pmos
          45              nmos


    Terminal correspondence points
    N64       N10       Out
    N66       N8        VDD
    N65       N6        Vout
    N63       N0        gnd!

Devices in the netlist but not in the rules:
        res diode
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4

7 net-list ambiguities were resolved by random selection.

The net-lists match.
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Virtuoso® 6.1.8-64b - Log: /home/staffier/CDS.log.1
File  Tools  Options  Help                                   cadence

Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Mon Dec  6 12:42:30 2021
    completed ....Mon Dec  6 12:42:30 2021
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "BLS_proj_f21 layout"   *********
   Total errors found: 0

Getting layout propert bagGetting layout propert bagLoading techComp.cxt

mouse L: showClickInfo()        M: leHiSave()        R: _lxHiMousePopUp()
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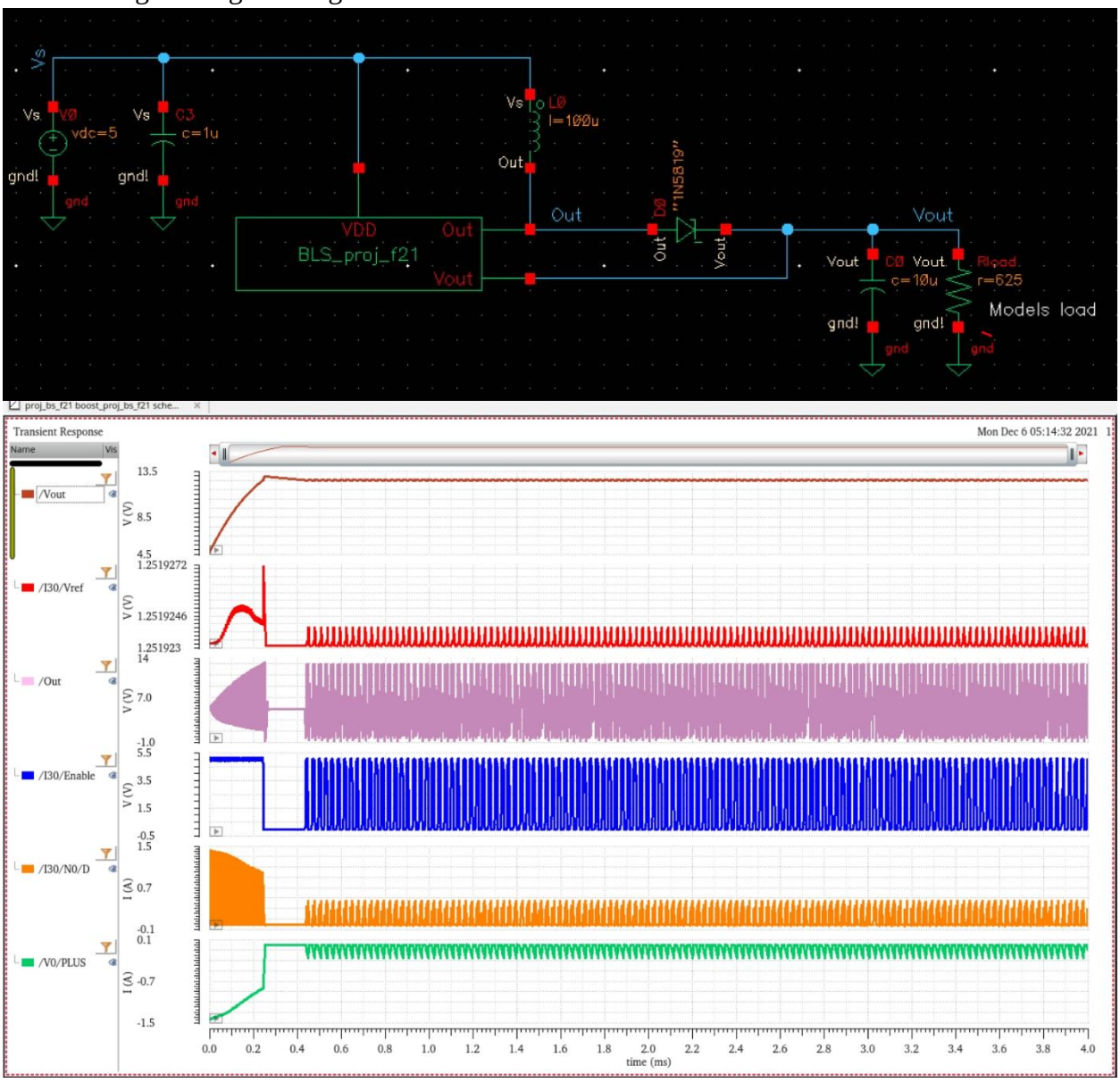
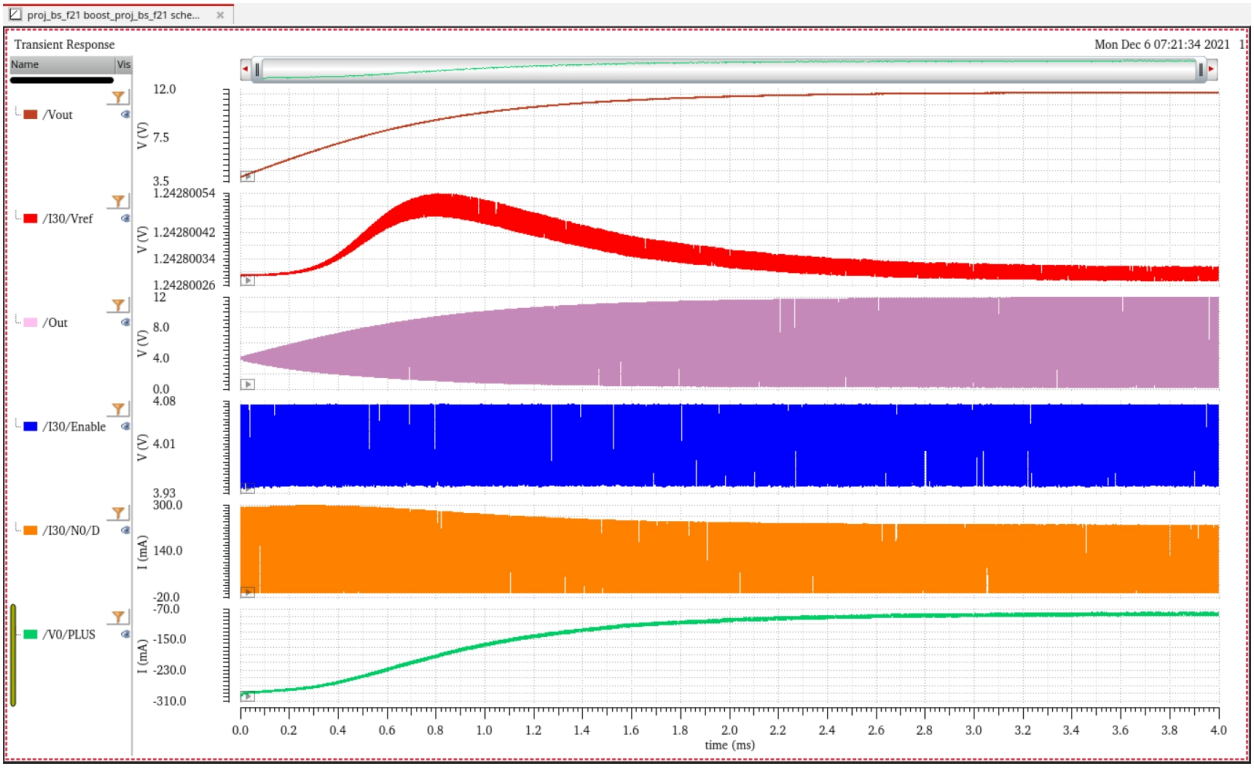
After performing and passing DRC and LVS checks on this layout, I then implemented it into the final schematic and performed a rudimentary simulation to verify that it is operating correctly and reaching the target voltage of 12.5V.



As can be observed in the simulation results, the voltage spikes up, then levels out at ~12.5V at steady state, which occurs quickly at around 0.4ms. The Out value is also much closer to 0 than with the provided NMOS device size. The provided size for the NMOS device was 48u/0.6u with a multiplier of 20, and the Out value approached around ~630mV as opposed to 0. I modified this to a multiplier of 40 and observed that the Out value approached much closer to 0 at around ~360mV. This makes sense as increasing the multiplier like this means that there are more transistors in parallel, which means that there is more resistance in parallel, which means that the total resistance value actually drops as indicated by the relationship $R_{total} = \frac{R1*R2}{R1+R2}$. This was further displayed as when I changed it to a multiple of 60, the resistance dropped further and

thus it approached even closer to 0 at around ~300mV. Of note here is that it did not decrease by as much as the first change, which makes sense because as you add more resistors in parallel, you get diminished returns in regard to how much smaller the total resistance gets every time.

Additionally, I performed another simulation to display that my circuit still operates under varying conditions. I adjusted the VDD from 5V to 4V which is the minimum value that this spec is meant to accept, and I also changed the temperature value from 27 up to 100 degrees Celsius.



As can be observed in this above simulation the behavior of the circuit is still near identical; however, the Vout value appears to take longer to reach steady state with the target voltage. Though the bandgap is designed to maintain its reference voltage output throughout various temperatures, other components are still affected by this severe temperature increase on a transistor level. This change is the transistors is the result of the higher temperature increasing the number of electron-hole pairs.

Reflecting on Design Decisions and Potential Future Improvements

For future reference, while my design is functional, there are certainly elements that can be fine-tuned and improved upon. The sizing of the NMOS transistor is an element that I sped past in this design. Though I did adjust it and take note of the resulting behavior change in the circuit, I did overall leave it and the inductor without proper fine tuning. Additionally, more fine tuning could be done in regard to the ring oscillator frequency. Similarly, I focused more on simply getting the appropriate duty cycle in order to get something that was functioning properly; however, future improvements could involve lowering the frequency in order to build a greater delay between the ring oscillator receiving its enable signal, and then enabling the NMOS device in order to create a better range of hysteresis.

Concluding Thoughts

Overall, I greatly appreciated this project. This was by far the largest scale design assignment that I have tackled using Cadence Virtuoso and I believe that I pulled from every piece of knowledge regarding it that I picked up throughout the semester in both the lecture course and the lab. I believe that I made mistakes and had lapses in design decision judgement that I have learned from and can use to improve for both future projects or even just revisions of this one. The trade-offs that one must make when drafting have been made much clearer to me. Glossing over an element has the potential to have a significant impact on the efficiency or even base operation of the circuit, and often problems will arise that I was not previously exposed to, and I needed to use critical thinking to work through or around it.