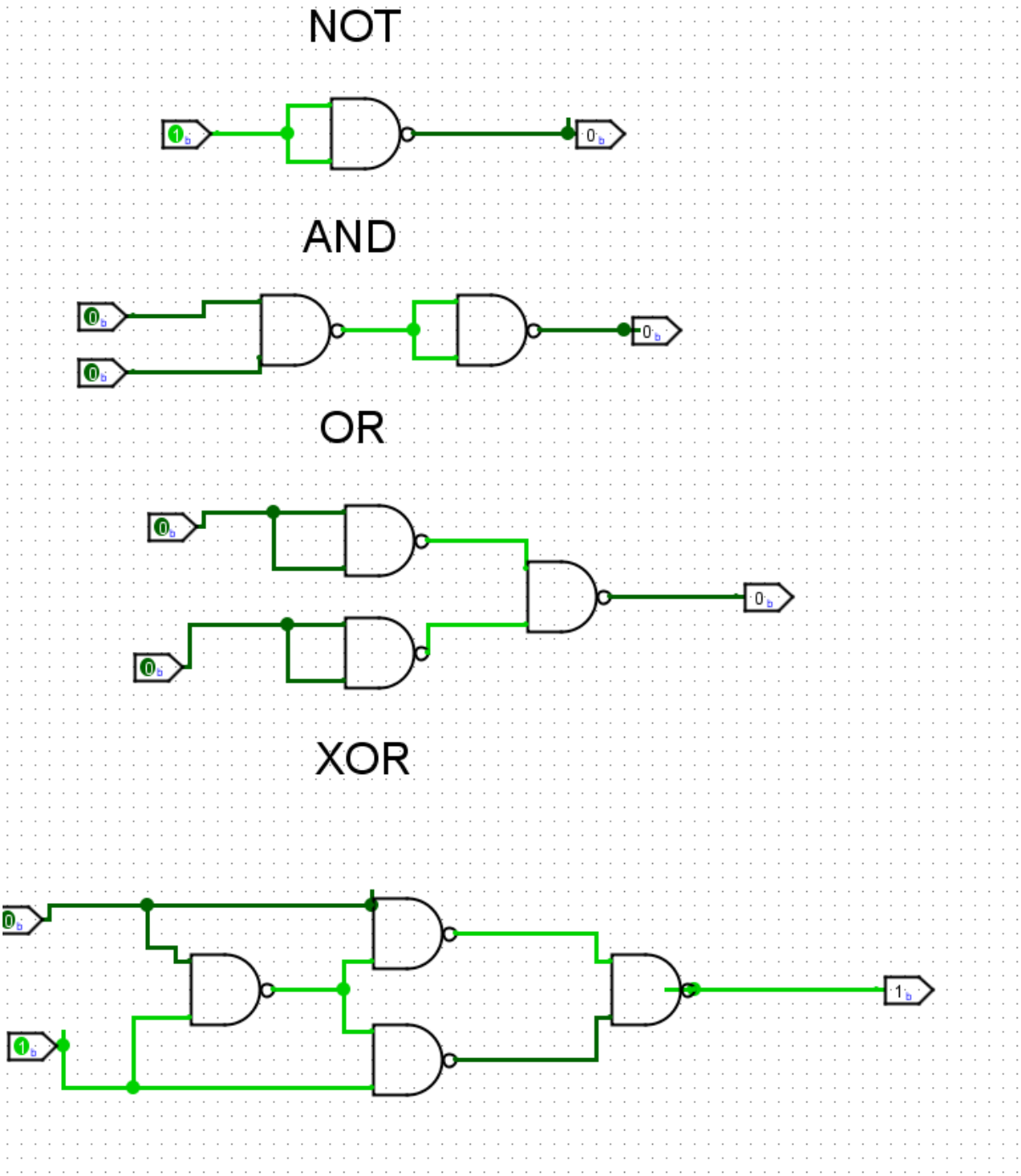
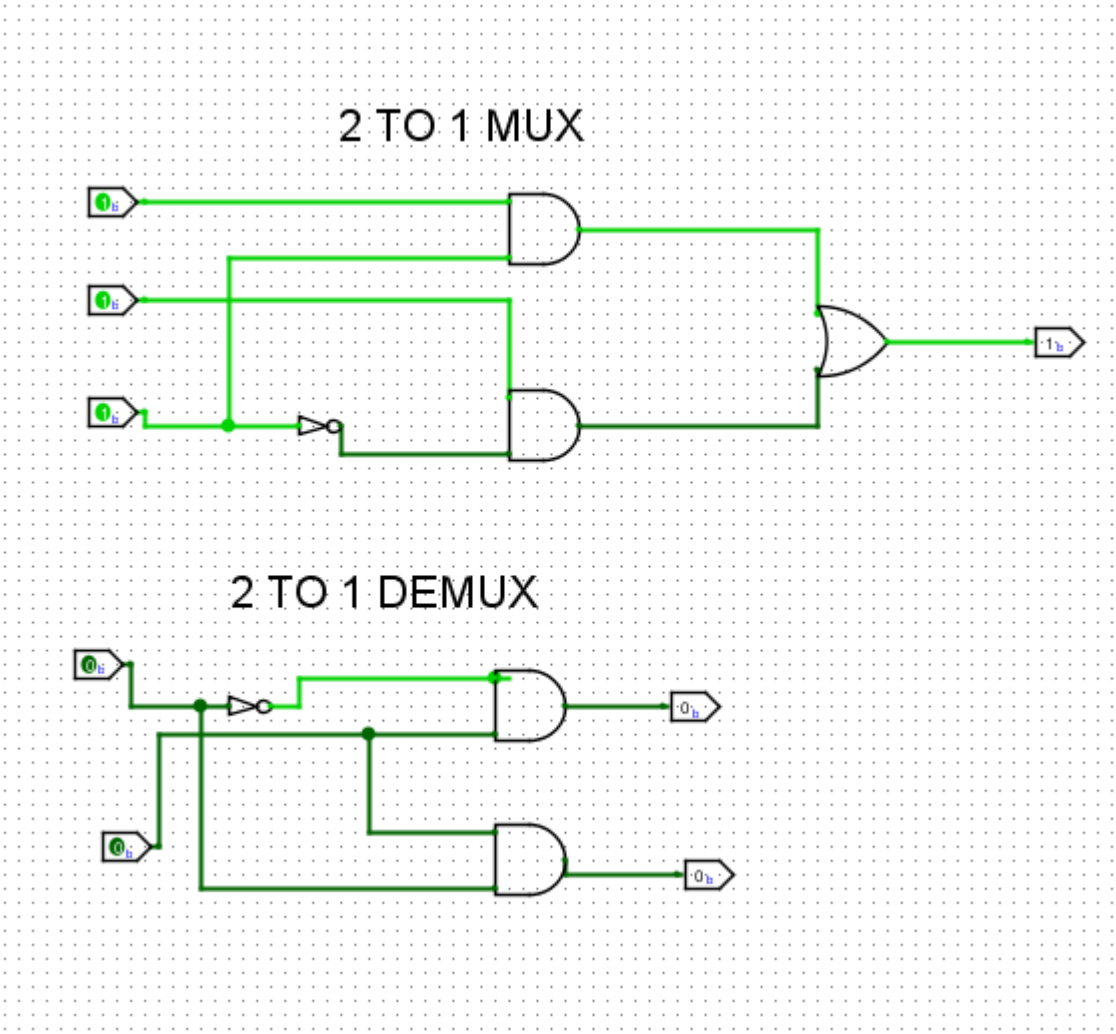
LAB 2

Q1



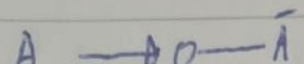
Q2



The digital multiplexer circuit known as a 2-to-1 multiplexer contains two data inputs, D 0 and D 1, one selects line S, and one output, Y

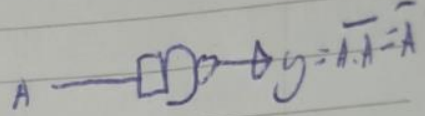
The1-to-2 demultiplexer, often known as a demux, has one select line, two output lines, and one input line.

(A)



A	Output
1	0
0	1

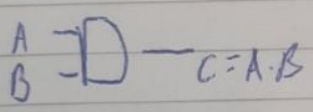
$\cong$



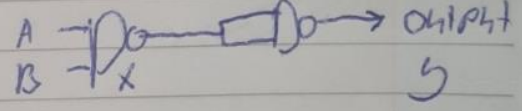
A	output
0	1
1	0

(B)

Built from nand gate

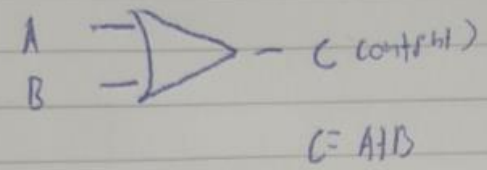


A	B	C (output)
0	0	0
0	1	0
1	0	0
1	1	1

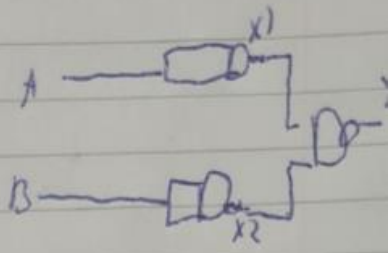


A	B	X (com)	Y (output ≥)
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

(C)



$C = A \cdot B$

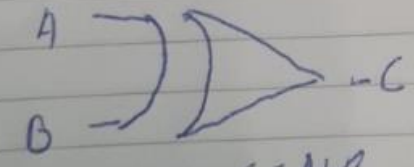


A	B	C
0	0	1
0	1	1
1	0	1
1	1	1

A	B	x_1	x_2	y_2
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

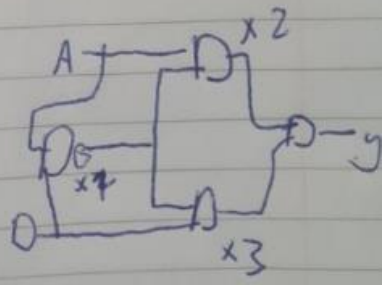
we built or gate with the help of 3 nand gate so we can control the output of

(D)



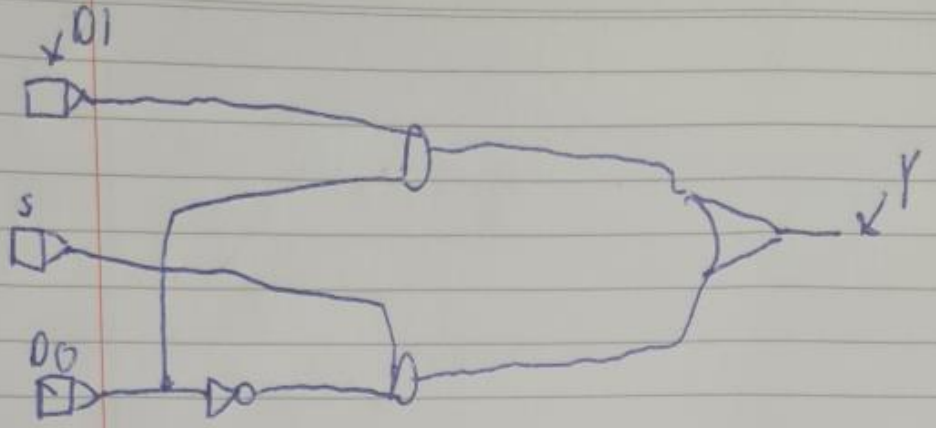
$C = A \cdot B$

$A \oplus B = A\bar{B} + \bar{A}B$



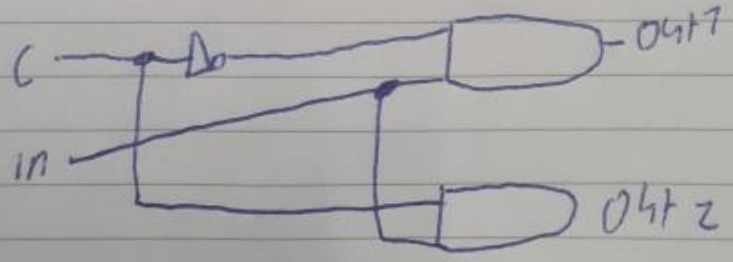
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

A	B	x_1	x_2	x_3	y
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0



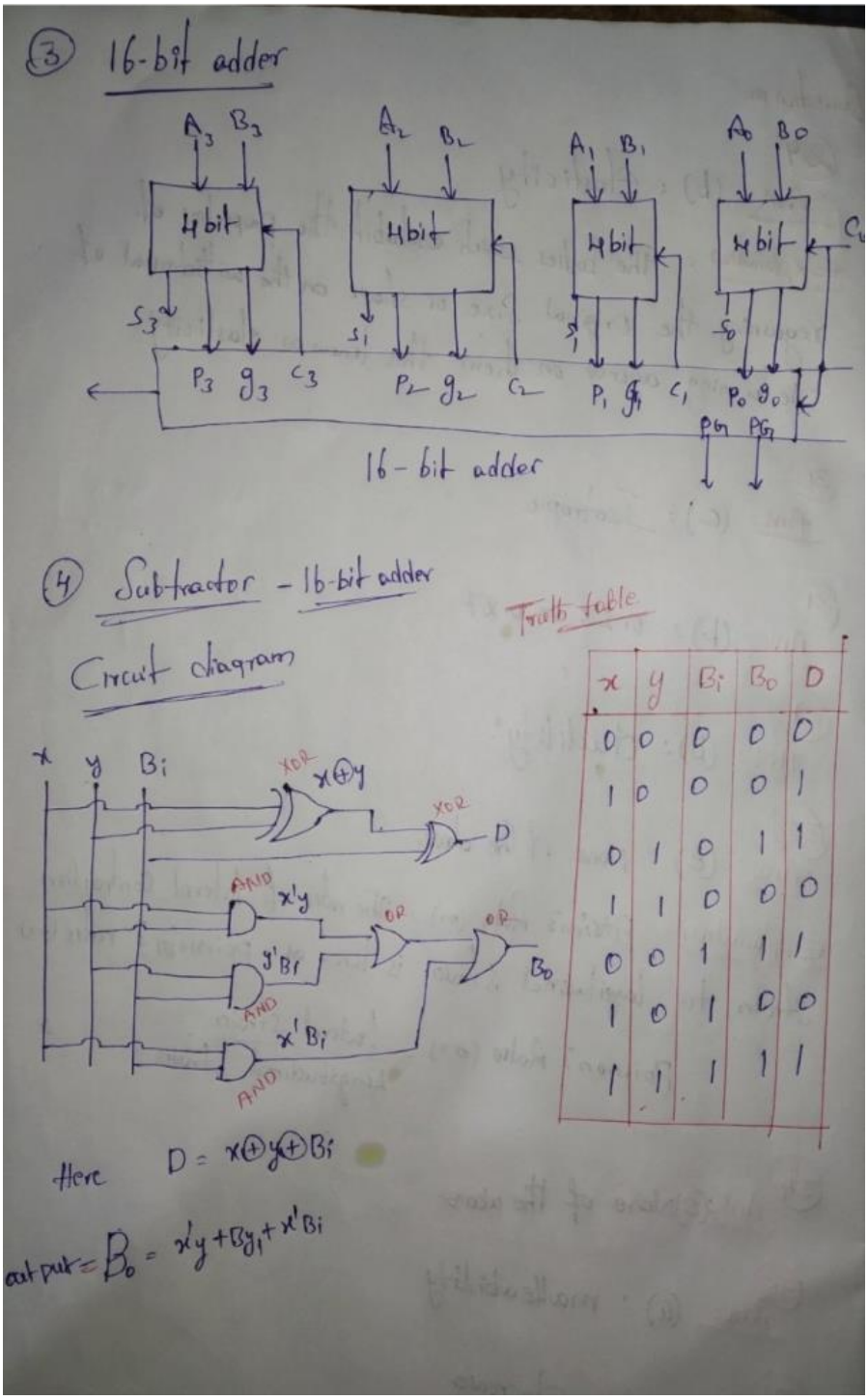
	input		output
Select line	D0	D1	Y
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

Q3



in	C	out1	out2
0	0	0	0
1	0	1	0
0	1	0	0
1	1	0	1

Q3.



x	y	Bi	Bo	D
0	0	0	0	0
1	0	0	0	1
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
1	1	1	1	1