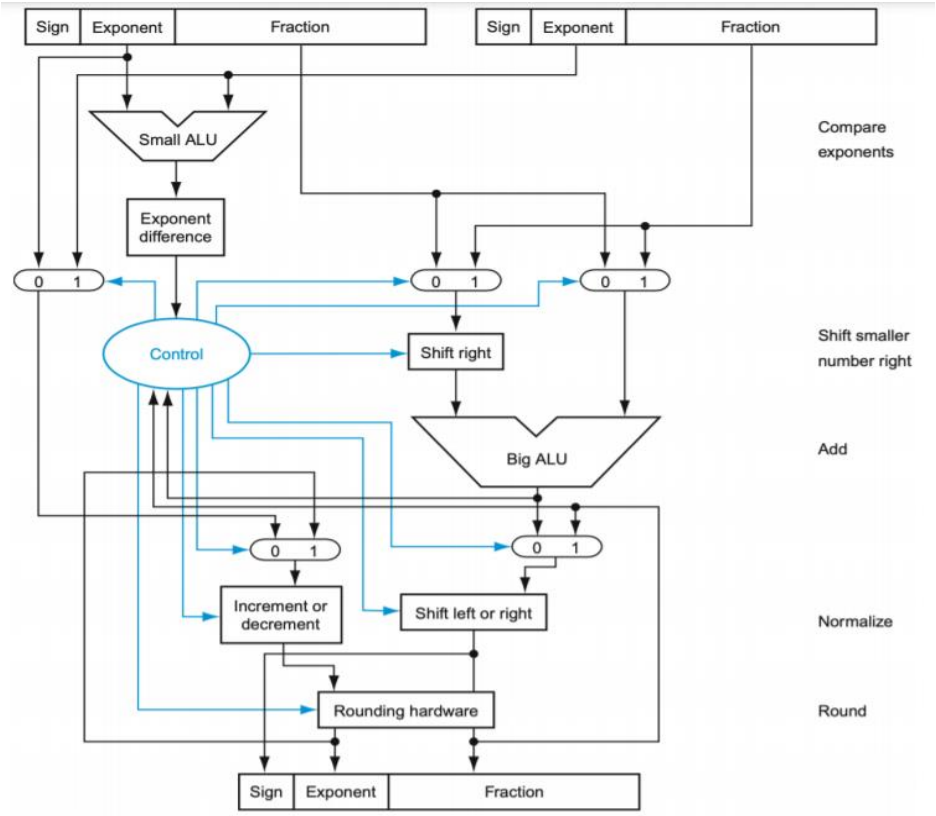
Report

ALU

According to the case, do the corresponding computation.

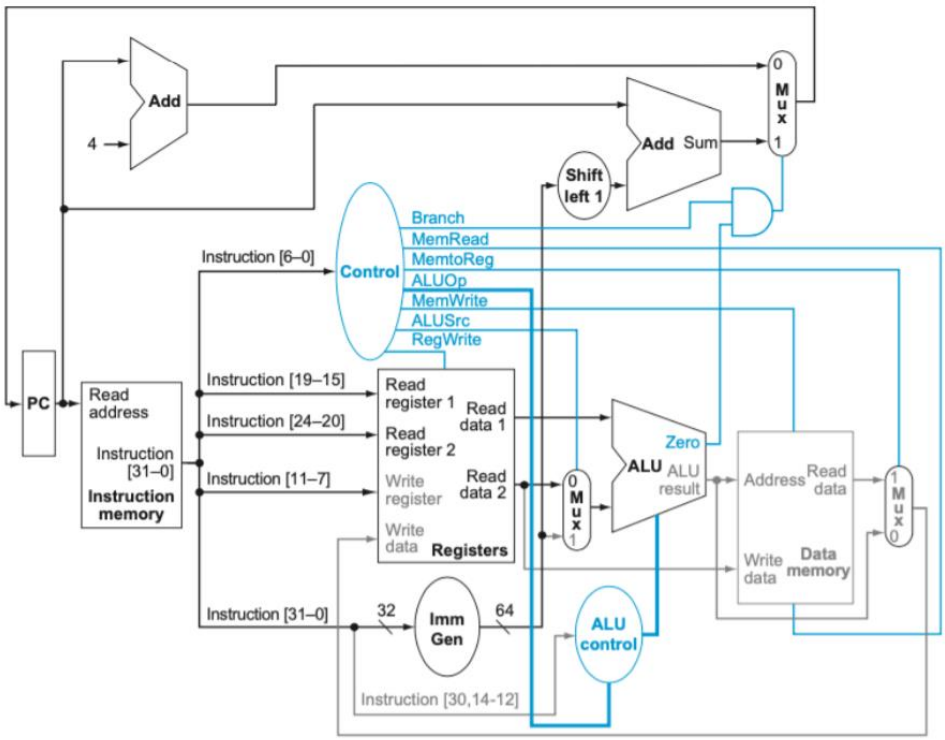
FPU




For addition, implement a module for every block shown in the figure, except for the part of renormalization after rounding.

For multiplication, make a multiply unit by changing the parts before normalization of adder. Those parts are changed into adding the exponents and multiply the fractions.

CPU




Implement a module for every block shown on the figure, except for integrating ALU control in Control. The last valid instruction will be buffered in Control, and the inputs of Registers and ImmGen come from the buffer in Control. Instruction and Control signals buffered in the Control Unit will remain the same value until a new valid instruction. CPU will send one cycle signal o_i_valid_addr every 15 cycles. For, ld and sd instruction, o_d_MemRead and o_d_Memwrite will be 1 while i_i_valid_inst is 1.

Reference: b07902080 for 15 cycle an o_i_valid_addr signal.