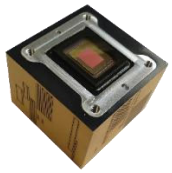
CASPEX 1.3M SWIR

1.3MPX SWIR SPACE CAMERA HEAD

3DCM880-1

Datasheet



1. PRODUCT OVERVIEW

The CASPEX 1.3M SWIR Space Camera Head is a high-density, high-performance, high-resolution SWIR Camera Head for space applications. It embeds a SWIR CMOS image sensor, offering multiples integrated readout features (sub-sampling, ROI, multi-parameters). The CASPEX 1.3M SWIR also embeds a high performance electronic architecture based on a reconfigurable FPGA associated with its TMR configuration memories, as well as volatile and non volatile memories. This allows for an efficient control of the sensor, as well as processing capacities for image pre-processing and formatting, making the 3DCM880 suitable for a large range of applications.

The CASPEX 1.3M SWIR electrical interface offers multiple LVDS User IOs, usable for interfaces such as CameraLink or SpaceWire, for an easy integration into complex systems requiring high-speed and flexible data and image transmission. All needed power supplies are embedded in the CASPEX 1.3M SWIR, which only requires a 5V input.

The CASPEX 1.3M SWIR Camera Head is based on 3D PLUS stacking technology, which is qualified for harsh environment, withstanding appreciable mechanical shock and vibrations, and 3D PLUS experience in space design and components choice, allowing for a high reliability and high density Camera Head.

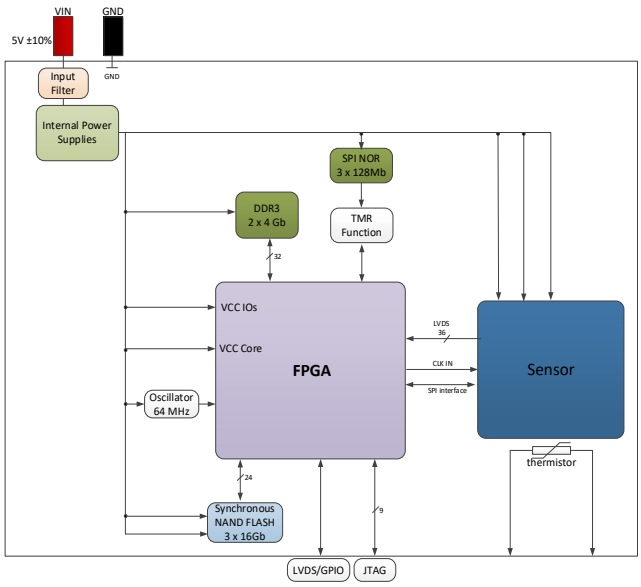
2. APPLICATIONS

- Earth observation, Atmosphere monitoring
- Planetary science
- Source Tracking
- Navigation & docking, Rendez-vous, Startracking,

3. KEY FEATURES

- 1.31 Mpixels SWIR global shutter CMOS image sensor
  - 1280 (H) x 1024 (V) 5µm active pixel array
  - Visible + SWIR Spectral Response: 0.4 - 1.7 µm
  - Read noise : 240e⁻, Dark current : < 28 ke⁻/s (25°C), Full Well Capacity > 170ke⁻
  - Multiple modes (All-pixel scan, Readout, subsampling, ROI), 8/10/12 bits modes
  - 134/125/71 fps acquisition speed in 8/10/12 bit full-frame
  - Up to 3270 fps acquisition speed for smaller ROI
- User-reconfigurable FPGA-Based Architecture
  - High-end FPGA (500K System Logic Cells)
  - 8Gb DDR3 and 48Gb NAND Flash memories
  - TMR SPI NOR configuration memory
  - LVDS, GPIO, JTAG
  - Average power consumption < 6 W at 25°C (Maximum < 10 W at 70°C)
- One single 5V input power supply needed
- Integrated temperature sensors
- Dedicated Thermal/Mechanical interfaces
- TID > 40 krads(si) / SEL immune up to LET > 60 MeV.cm2/mg
- Operating Temperature Range: -55°C to +70°C
- 40x40x45 mm, weight <140g with PGA package

4. BASIC SCHEMATIC



SCOPE

The CASPEX 1.3M SWIR Space Camera Head product family provides a reprogrammable space grade camera solution, integrating an InGaAs based SWIR Image Sensor sensitive in both visible and SWIR wavelength domains, and the associated electronic architecture needed to operate the sensor in one single miniaturized package.

The SWIR image sensor embedded within CASPEX 1.3M SWIR is a high-performances image sensor with 1280 x 1024, 5µm-pitch pixel array. The sensor is a diagonal 8.2 (Type ½) global shutter CMOS active pixel type solid-state image sensor with a square pixel array and 1.31 M effective pixels. It integrates several built-in features such as subsampling, Region-Of-Interest readout, multiple bit-mode.

The FPGA based architecture associated to the CMOS image sensor offers a generic architecture to interface and control the sensor in the scope of a full imaging system. The high-performance Kintex Ultrascale KU040 embedded in the CASPEX 1.3M SWIR Space Camera Head offers high speed memory interface and IOs, as well as high computing capabilities to permit high frame rate, image handling and pre-processing, and communication with users platform.

A radiation tolerant 128Mbit NOR Flash memory layer is integrated in the architecture for configuration bitstream storage, using a specific Rad Hard By Design mechanism to enhance the memory protection against space radiations, offering SEE mitigation by TMR and TID performance enhancement by embedded power switch.

An 8 Gbit DDR3 SDRAM memory provides to the architecture high-speed memory for computing purposes, as well as access to radiation qualified memory devices through a 32-bit wide data bus. A 48 Gbit Synchronous NAND Flash memory is in the same way available for non-volatile storage purposes, providing access for the FPGA to radiation qualified memory devices through a 24-bit wide data bus.This all-in-One 3DCM880 SWIR Space Camera Head is designed for operating and being reprogrammed under harsh environment and space radiations, in order to be integrated as the core of full Camera Systems and is well suited for any high reliability and high performance space imaging applications.

The CASPEX 1.3M SWIR Camera Head is designed and manufactured by 3D PLUS Company using its space qualified stacking technology process and manufacturing line based in France.

This all–in-one solution provides several key benefits:

- Ready to use all-in-one solution, with all necessary components integrated,
- Generic high-performance camera architecture, able to target a wide range of imaging applications,
- Enhanced radiation performance achieved by technology and hardening by design technics (RHBD),
- High level of miniaturization – ideal to answer the needs of constrained space imaging applications and easily integrated in a compact Camera System,
- Space qualification.

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5. DOCUMENTS

5.1 APPLICABLE DOCUMENTS

[AD1] **3DPA-8357:** CASPEX 1.3M SWIR Detailed Specification P/N: 3DCM880-1
[AD2] **3DFP-0880:** CASPEX 1.3M SWIR Space Camera Head - 3DCM880 - Flyer
[AD3] **3315-XXXX:** Total Ionizing Dose (TID) Detailed Report – CASPEX 1.3M SWIR **– P/N :** 3DCM880-1 **(Confidential)**
[AD4] **3315-XXXX:** Single Event Effects (SEE) Detailed Report – CASPEX 1.3M SWIR Space Camera Head 3DCM880-1 **(Confidential)**
[AD5] **3250-0118-1 :** CE4 Package Footprint

5.2 REFERENCE DOCUMENTS

[RD1] Xilinx Ultrascale Architecture and Product Datasheet, DS890, Rev 3.7, February 2019
[RD2] Xilinx Ultrascale FPGAs Datasheet, DS892, Rev 1.19, September 2020
[RD3] Xilinx Ultrascale Architecture Configuration user's guide, UG570, Rev 1.11, September 2019
[RD4] Xilinx Ultrascale SYSMON User's Guide, UG580, Rev1.10.1, September 2021
[RD5] Xilinx Ultrascale Power Estimator XPE 2020-1
[RD6] Open NAND Flash Interface Standard, ONFI 2.1 Jan 2009
[RD7] DDR3 SDRAM Standard, JEDEC, JESD79-3F, July 2012

6. ACRONYMS

DDR:	Double Data Rate	**P/N:**	Part Number
DSP:	Digital Signal Processor	**PT1000:**	Platinium Thermistor, 1000 Ω at 0°C
ECC:	Error Correction Coding	**RAM:**	Random Access Memory
ESA:	European Space Agency	**RHBD:**	Radiation Hardened By Design
ESD:	Electro Static Discharge	**ROI:**	Region Of Interest
FPGA:	Field Programmable Gate Array	**SECE:**	Single Event Column Error
GND:	Ground	**SEE:**	Single Event Effect
HBM:	Human-Body Model	**SEFI:**	Single Event Functional Interrupt
I/O:	Input/Output	**SEL:**	Single Event Latch-up
LUT:	Look Up Table	**SERE:**	Single Event Row Error
LVDS:	Low Voltage Differential Signaling	**SEU:**	Single Event Upset
MBPS:	Megabit per second	**SDRAM:**	Synchronous Dynamic Random Access Memory
NC:	Not Connected	**SPI:**	Serial Peripheral Interface
NVB:	Non Valid Block	**SWIR**	Short Wave Infra Red
PGA:	Pin Grid Array	**TID:**	Total Ionizing Dose
PCB:	Printed Circuit Board	**TMR:**	Triple Modular Redundancy

7. INTRODUCTION

The CASPEX 1.3M SWIR Space Camera Head product provides a reconfigurable space grade miniaturized camera core.

The CASPEX 1.3M SWIR Space Camera Head described in this datasheet embeds a 1.3 MPixels VIS-SWIR image sensor, an AMD-Xilinx Kintex Ultrascale SRAM based FPGA core, a radiation hardened by design 128 Mbit NOR FLASH memory for configuration bitstream storage, and additional 8Gbit DDR3 SDRAM volatile and 48 Gbit synchronous NAND Flash non-volatile memory.

The image sensor is a high-resolution, high-performance image sensor, providing a 1280 by 1024 (approx. 1.31 MPixels) active sensor array on a 1/2" format.

The FPGA core is a Kintex XCKU040 FPGA from the AMD-Xilinx Ultrascale family and is the center of the architecture, providing CASPEX 1.3M SWIR Space Camera Head high-computing power and high-speed interfaces.

The 128 Mbit NOR Flash Configuration Memory is radiation-hardened by design with a protection against potential SEE ensured by TMR mitigation and an enhanced TID performance controlled by a power on/off switch.

The additional NAND Flash and DDR3 SDRAM memory layers uses space-qualified components to provide reliable integrated non-volatile memories for storage purpose and volatile memories for computing purpose.

The CASPEX 1.3M SWIR Camera Head is designed and manufactured by 3D PLUS Company using its space qualified stacking technology process and manufacturing line based in France.

This all–in-one solution provides several key benefits:

- Ready to use all-in-one solution, with all necessary components integrated,
- Generic high-performance camera architecture, able to target a wide range of imaging applications,
- Enhanced radiation performance achieved by technology and hardening by design technics (RHBD),
- High level of miniaturization – ideal to answer the needs of constrained space imaging applications and easily integrated in a compact Camera System,
- Space qualification.

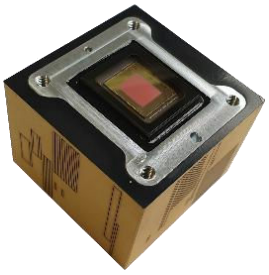


Figure 1: 3DCM880 SWIR Space Camera Head

8. QUALITY GRADES

Different operating temperature ranges and screening levels are available and are described in Table 1.

Variant – Part Number	Operating Temperature Range	Screening
3DCM880-1 SB	-40°C to +70°C	Industrial
3DCM880-1 FB	-55°C to +70°C	Industrial
3DCM880-1 SS	-40°C to +70°C	Space
3DCM880-1 FS	-55°C to +70°C	Space

Table 1: CASPEX 1.3M SWIR Camera Heads quality grades

9. FUNCTIONAL DESCRIPTION AND INTERNAL ARCHITECTURE

9.1 CAMERA ARCHITECTURE

9.1.1 Functional Block Diagram

The functional block diagram of the CASPEX 1.3M SWIR Space Camera Head is presented in Figure 2.

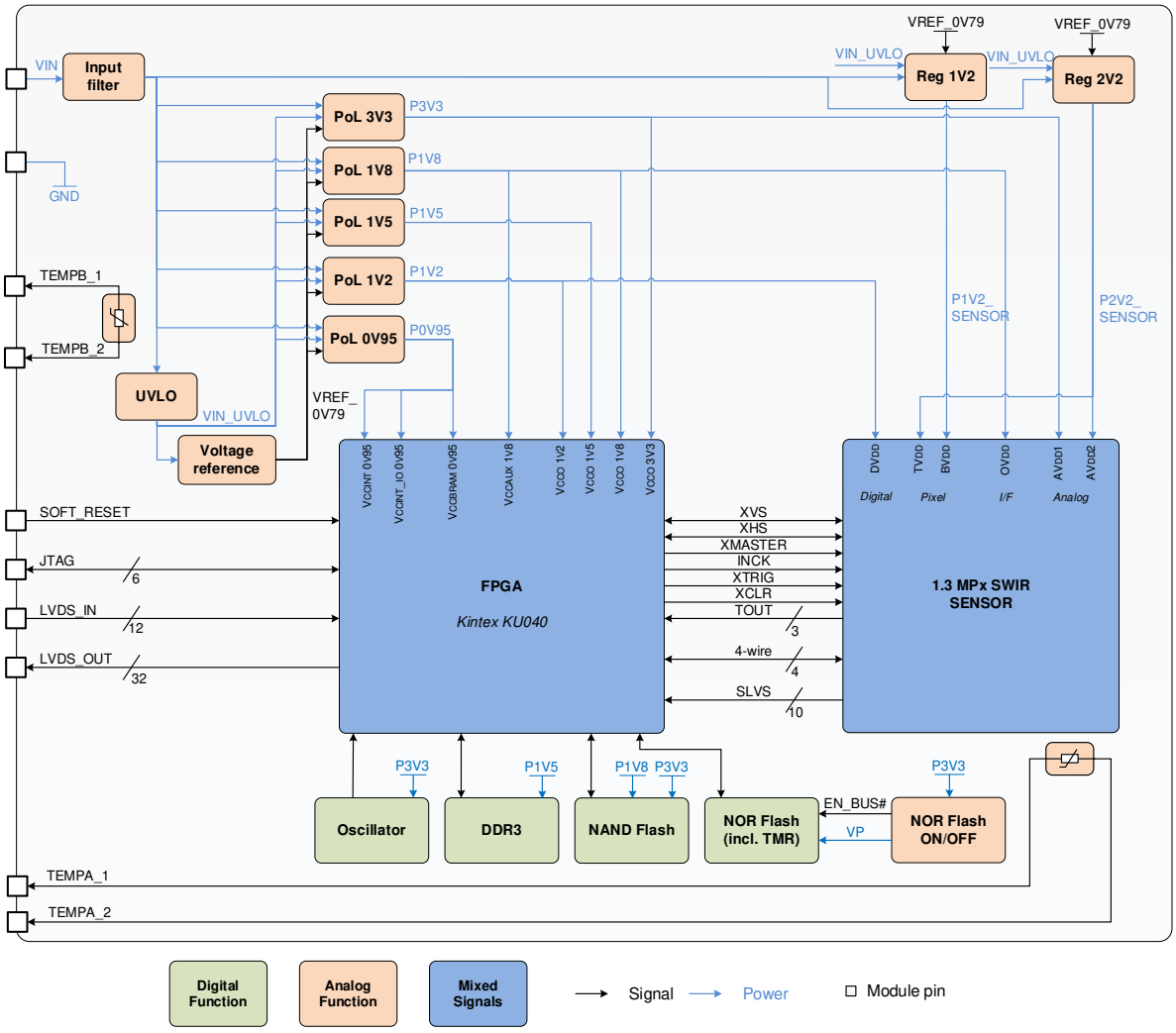


Figure 2: Functional block diagram

9.1.2 Power Supply

The CASPEX 1.3M SWIR Space Camera Head only requires one input power supply:

Name	Description	Value
V_{IN}	Input power supply	5V ±10%

Table 2: Power supply descriptions

Additional details on power supply are given in §11 Electrical Characteristics.

For I/O description, please refer to §10 PIN Assignment and Description.

9.2 EMBEDDED CMOS IMAGE SENSOR

9.2.1 Description

The CASPEX 1.3M SWIR Space Camera Head embeds a high-performance SWIR sensor with 1280 x 1024 pixel array. The sensor is a 8.2 mm (Type 1/2) CMOS active pixel type solid state image sensor with a square pixel array and 131 M effective pixels. This sensor features a global shutter with variable charge-integration time.

9.2.1.1 Main features

The main features of the embedded Image Sensor In the CASPEX 1.3M SWIR Space Camera Head are listed below:

- CMOS active pixel type dots,
- Global shutter function,
- Visible + SWIR (0.4 to 1.7µm)
- 1280 (H) x 1024 (V) approx.1.31 Mpixels
- Read noise : 240 electrons
- Dark current : < 28k electrons/sec @25°C
- Full Well Capacity > 165k electrons
- Multiple modes :
    - Readout mode
    - All-pixel scan mode
    - Vertical/Horizontal ½ subsampling mode
    - ROI mode
    - Vertical/Horizontal – Normal/Inverted readout mode
- 8-bit / 10-bit / 12-bit A/D converter
- Maximum frame rate in all pixel scan mode :
    - 135 frame/s in 8-bit per pixel mode
    - 120 frame/s in 10-bit per pixel mode
    - 71 frame/s in 12-bit per pixel mode

9.2.2 Sensor Interface and pins assignment

The interface between the FPGA and the SWIR image sensor is described in the table below:

Signal Name	Direction	Fpga Pin	Fpga Bank	Type	Comment
SENSOR_SDI	OUT	D9	66	LVCMOS 1V8	
SENSOR_SDO	IN	B14	66	LVCMOS 1V8	
SENSOR_SCK	OUT	F13	66	LVCMOS 1V8	
SENSOR_INCLK	OUT	A14	66	LVCMOS 1V8	
SENSOR_XTRIG	OUT	D15	66	LVCMOS 1V8	
SENSOR_XVS	IN/OUT	F14	66	LVCMOS 1V8	
SENSOR_XCE	OUT	F15	66	LVCMOS 1V8	
SENSOR_XHS	IN/OUT	E15	66	LVCMOS 1V8	
SENSOR_XCLR	OUT	G14	66	LVCMOS 1V8	
SENSOR_TOUT0	IN	J13	66	LVCMOS 1V8	
SENSOR_TOUT1	IN	H12	66	LVCMOS 1V8	
SENSOR_XMASTER	OUT	H13	66	LVCMOS 1V8	
SENSOR_TOUT2	IN	H14	66	LVCMOS 1V8	
SENSOR_CLK1_N	IN	F12	66	SLVS	SWIR sensor SLVS Signals (P : positive, N : negative)
SENSOR_CLK1_P	IN	G12	66	SLVS	
SENSOR_SLVS_00_N	IN	G9	66	SLVS	
SENSOR_SLVS_00_P	IN	G10	66	SLVS	
SENSOR_SLVS_01_N	IN	D11	66	SLVS	
SENSOR_SLVS_01_P	IN	E11	66	SLVS	
SENSOR_SLVS_02_N	IN	H8	66	SLVS	
SENSOR_SLVS_02_P	IN	H9	66	SLVS	
SENSOR_SLVS_03_N	IN	F8	66	SLVS	
SENSOR_SLVS_03_P	IN	F9	66	SLVS	

Table 3: FPGA / Image Sensor interface

9.2.3 Pixel arrangement

The pixels of the image sensors are arranged as shown in the figure below:

The interface between the FPGA and the SWIR image sensor is described in the table below:

Signal Name	Direction	Fpga Pin	Fpga Bank	Type	Comment
SENSOR_SDI	OUT	D9	66	LVCMOS 1V8	
SENSOR_SDO	IN	B14	66	LVCMOS 1V8	
SENSOR_SCK	OUT	F13	66	LVCMOS 1V8	
SENSOR_INCLK	OUT	A14	66	LVCMOS 1V8	
SENSOR_XTRIG	OUT	D15	66	LVCMOS 1V8	
SENSOR_XVS	IN/OUT	F14	66	LVCMOS 1V8	
SENSOR_XCE	OUT	F15	66	LVCMOS 1V8	
SENSOR_XHS	IN/OUT	E15	66	LVCMOS 1V8	
SENSOR_XCLR	OUT	G14	66	LVCMOS 1V8	
SENSOR_TOUT0	IN	J13	66	LVCMOS 1V8	
SENSOR_TOUT1	IN	H12	66	LVCMOS 1V8	
SENSOR_XMASTER	OUT	H13	66	LVCMOS 1V8	
SENSOR_TOUT2	IN	H14	66	LVCMOS 1V8	
SENSOR_CLK1_N	IN	F12	66	SLVS	SWIR sensor SLVS Signals (P : positive, N : negative)
SENSOR_CLK1_P	IN	G12	66	SLVS	
SENSOR_SLVS_00_N	IN	G9	66	SLVS	
SENSOR_SLVS_00_P	IN	G10	66	SLVS	
SENSOR_SLVS_01_N	IN	D11	66	SLVS	
SENSOR_SLVS_01_P	IN	E11	66	SLVS	
SENSOR_SLVS_02_N	IN	H8	66	SLVS	
SENSOR_SLVS_02_P	IN	H9	66	SLVS	
SENSOR_SLVS_03_N	IN	F8	66	SLVS	
SENSOR_SLVS_03_P	IN	F9	66	SLVS	

Table 4: FPGA / Image Sensor interface

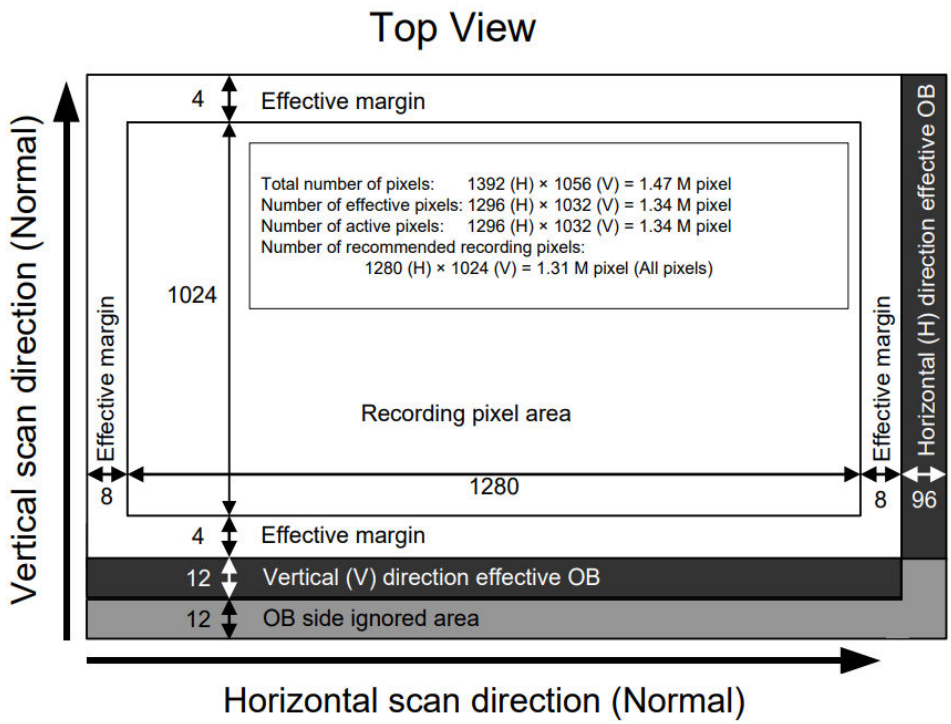


Figure 3 : SWIR sensor pixel arrangement

9.2.4 Sensor Relative Response

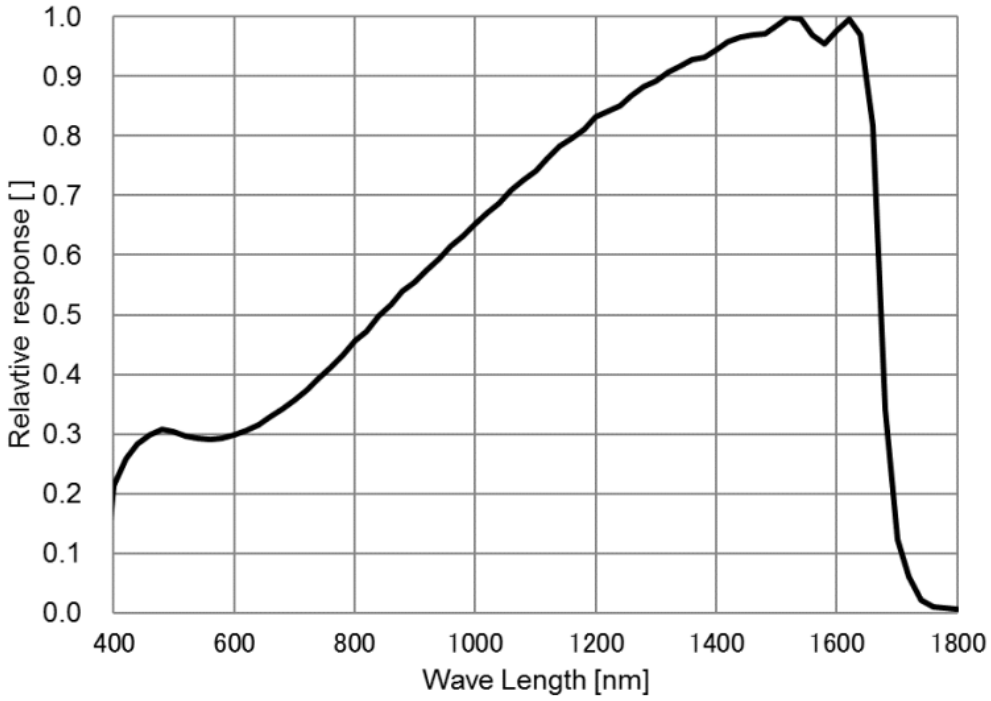


Figure 4 : Image sensor spectral sensitivity at 15°C

9.2.5 Image sensor electro-optical characteristics

The image sensor electro-optical characteristics are presented in the table below.

Parameter	Typical Value	Unit
Readout Noise	240	e^{-}
Dark current	30 000	e^{-}/s
Charge to Voltage conversion Factor	0.025	LSB/e^{-}
Full Well Capacity	170 000	e^{-}

Table 5: 3DCM880 Optoelectronics Characteristics

9.2.6 Sensor Configuration Interfaces and Operation

9.2.6.1 Sensor Configuration

The CMOS Image sensor embedded in the CASPEX 1.3M SWIR Space Camera Head has a total of 5376 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 0Ch, 10h to 19h. Some of those registers initial value must be changed. To access and configure these register, two serial communication interfaces are available: 4-wire serial link and I²C serial link.

9.2.6.2 Readout Modes and frame rate

The table below lists the available operating modes available with the SWIR Image Sensor integrated in the 3DCM880 SWIR Space Camera. Those performances are given for normal data rate configuration.

Drive Mode	Frame Rate (Frame/s)	Data Rate [Gbps]	SLVS ch[1]	A/D conversion	Number of recording pixels		Total number of pixels	
					H	V	H	V
All pixels	134.73	2.376	4	8	1280	1024	2064	1068
	92.69	1.188	2				1500	
	125.27	2.376	4	10			1776	
	74.76	1.188	2				1488	
	71.53	2.376	4	12			2592	
	62.97	1.188	2				1472	
All pixel (Vertical / Horizontal ½ subsampling)	260.68	2.376	4	8	640	512	2064	552
	260.68	1.188	2				1032	
	242.36	2.376	4	10			1776	
	242.36	1.188	2				888	
	138.39	2.376	4	12			2592	
	138.39	1.188	2				1296	
ROI	*2	2.376	4	8	*1	*1	2064	*2
	*2	1.188	2				1500	
	*2	2.376	4	10			1776	
	*2	1.188	2				1488	
	*2	2.376	4	12			2592	
	*2	1.188	2				1472	

Table 6: Sensor Readout Modes Performances

Note 1: Designated cropping area.

Note 2: See ROI mode below.

9.2.6.3 ROI Modes

This sensor offers ROI function that allows signals to be cut and read out in multiple arbitrary positions. Cropping positions can be set to a maximum 64 areas, specified by 8 horizontal points and 8 vertical points, regarding pixel start position at origin (0,0) in all pixel scan mode. ROI Modes are only available in all-pixel scan modes.

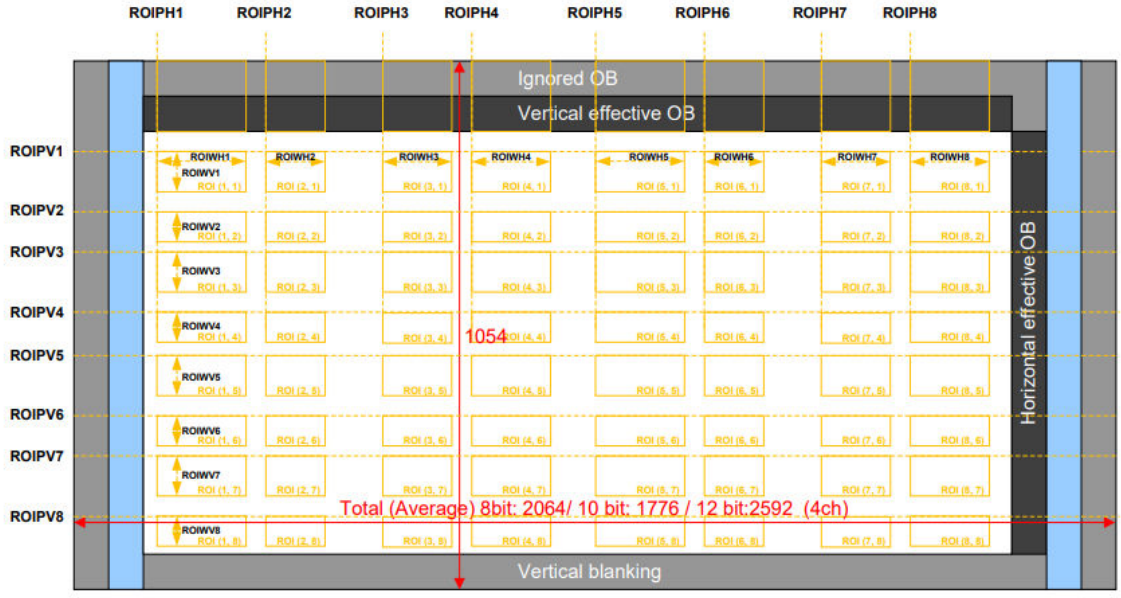


Figure 5 : Designated areas in ROI mode

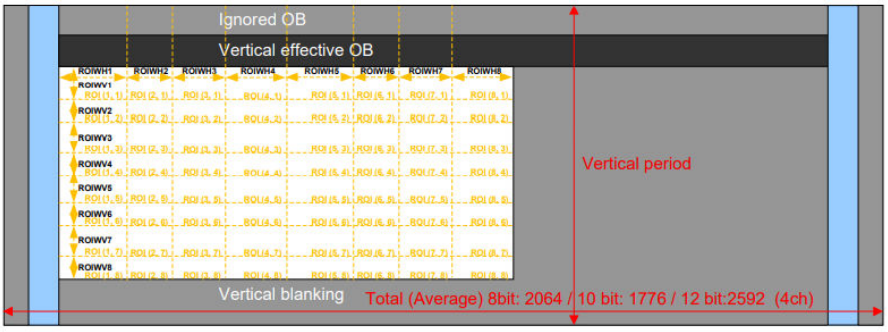


Figure 6 : resulting image in ROI mode

Basic ROI mode limitations:

- Basic ROI mode forbid overlapping of ROI designated areas.
- Horizontal and vertical settings must be multiple of 4
- Minimum width of ROI window :
    - ROI horizontal width:
        - ROIWH1 + ROIWH2 + … + ROIWH8 > 8 pixels
    - ROI Vertical width :
        - ROIWV1 + ROIWV2 + … + ROIWV8 > 8 pixels

ROI Mode frame rate :

$$framerate = \frac{1}{(number\ of\ line\ per\ frame)x(line\ period)}$$

For example, with number of lines of 600, maximum frame rate achievable is 226 frame/s. With a minimum number of line of 8, the frame rate increase up to 3270 frame/s.

9.2.6.4 Integrated Sensor Functions

The Image Sensor embedded in the CASPEX 1.3M SWIR Space Camera Head offers the following integrated functions:

- Standby mode: Configurable to reduce power consumption of the sensor. The communication interface of the sensor still operate in standby mode.
- Master/Slave mode: The sensor can be switched between master and slave mode to allow the user to operate synchronization signals for image readout.
- Gain adjustment: a Programmable Gain Control (PGC) is provided to configure analog and digital blocks of the sensor. The total of analog gain and digital gain can be set up to 48 dB as shown in the figure hereafter.

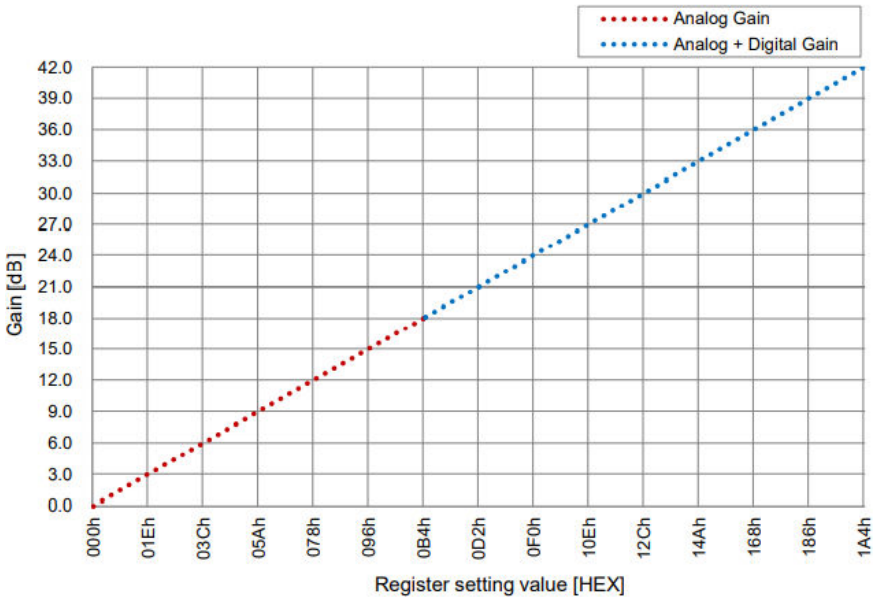


Figure 7 : Gain Settings

- Black Level adjustment: A black level offset can be added relative to the data in which the digital gain modulation was performed.
- Horizontal/Vertical Normal and Inverted Operation: The sensor readout direction (normal/inverted) in horizontal and vertical direction can be switched. The figures hereafter show the different modes of sensor readout.

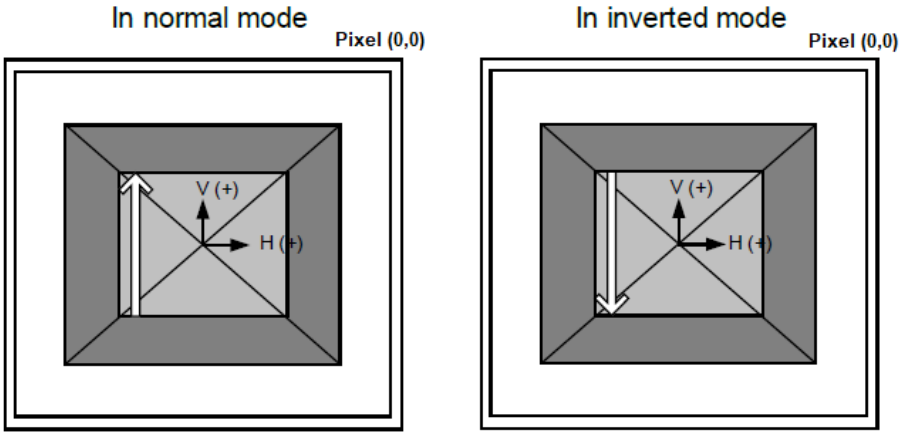


Figure 8 : Normal and Inverted Drive Outline in Vertical Direction (Top View)

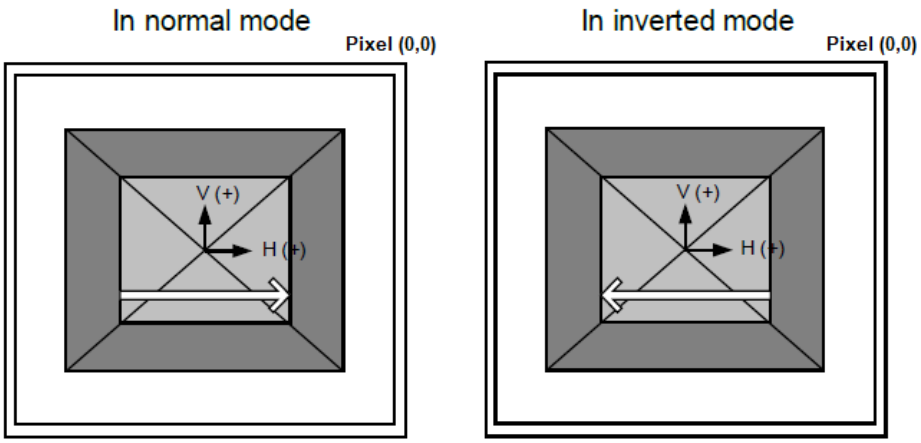


Figure 9 : Normal and Inverted Drive Outline in Horizontal Direction (Top View)

- Shutter and integration Time Settings: The sensor uses a global shutter function that integrates all lines collectively by using memory in each pixel. It has a variable electronic shutter function that can control the integration time in line units to adjust the exposure time. The sensor also has a trigger mode to control exposure start timing and memory transfer timing.

  For integration time control, an image which reflect the setting is output after setting changes.

  The shutter operation and storage time are shown in the figure below. For simplification, shutter and readout operation are noted in line units.

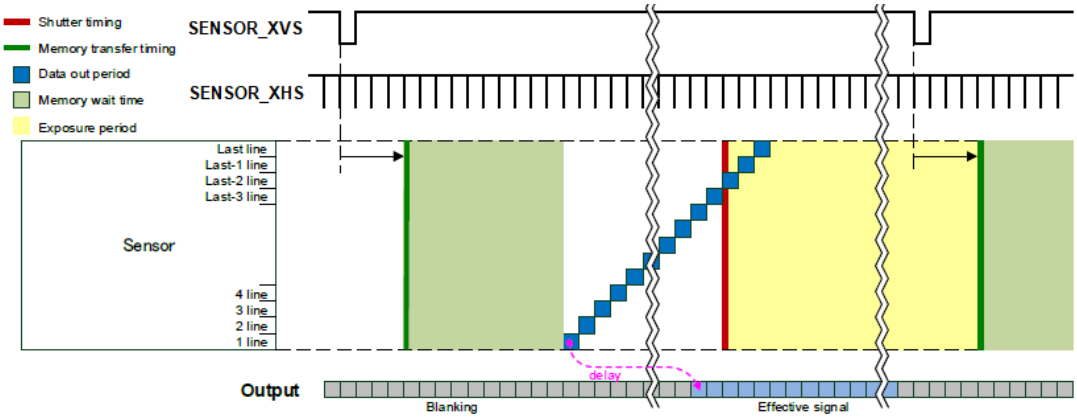


Figure 10 : Global Shutter (Normal mode) Operation

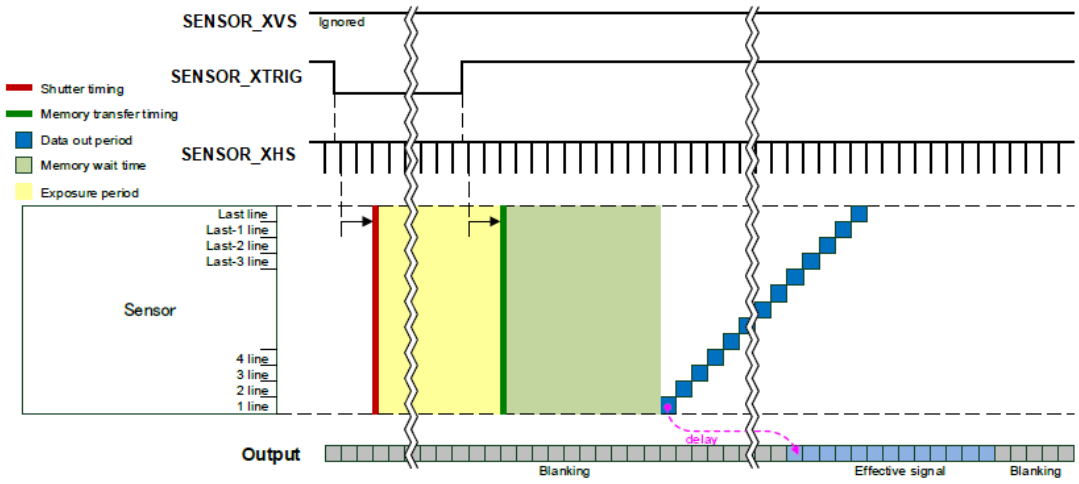


Figure 11 : Global Shutter (Sequential Trigger mode) Operation

The following shutter modes are available:

- Normal Mode: The integration time can be controlled by varying the electronic shutter timing. The Exposure time is given by the following formula :

$$Exposure\ time\ [s] = (1H\ period) * (Number\ of\ line\ per\ frame - SHS) + 7.372\ [\mu s]^1$$

Note 1: Exposure time error

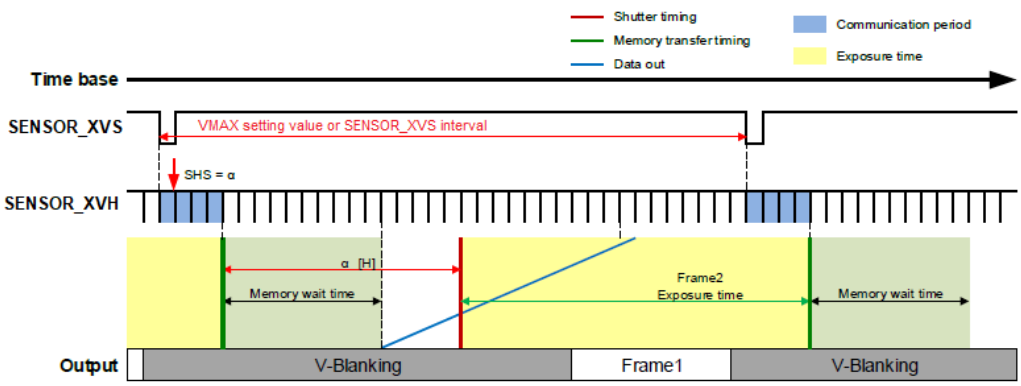


Figure 12 : Global Shutter (Normal mode)

- Sequential Trigger Mode: The integration time can be controlled by varying the pulse width that is input to SENSOR_XTRIG external trigger. This function is usable in slave mode only. The number of lines per frame differs according to the operating mode. The Exposure time is given by the following formula :

$$Exposure\ time\ [s] = (SENSOR\_XTRIG\ low\ level\ pulse\ width\ [H]^{*2}) + 7.372\ [\mu s]^{*1}$$

Note 1: Exposure time error (t_{OFFSET})

Note 2: Low level pulse width is counted by SENSOR_XHS pulse.

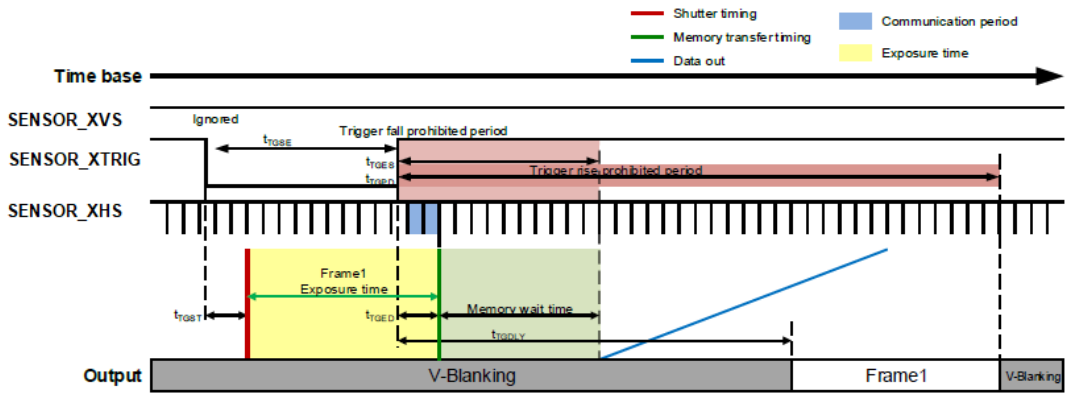


Figure 13 : Global Shutter (Sequential Trigger mode)

- Fast Trigger Mode: Fast Trigger Mode is a trigger mode that starts exposure at the fall of the external trigger signals immediately. The Exposure time is given by the following formula :

$$Exposure\ time\ [s] = (SENSOR\_XTRIG\ low\ level\ pulse\ width\ [\mu s]) + 7.372\ [\mu s]^{*1}$$

Note 1: Exposure time error (t_{OFFSET})

- Signal Output: The sensor supports multiple output modes at different levels:
  - Output configuration: 4/8/16 ch/annels modes, Data rate modes,/
  - Output bit width configuration: 8/10/12 bit modes
  - Output signal range configuration

The Sensor also benefits from the additional functions below:

- Multi-Frame Set Output mode (2 / 4 frame)
- Multi Exposure Trigger Mode
- Multi Frame ROI (Multi Exposure + ROI) mode
- Driving Low Power Consumption at longtime exposure
- Simple Thermometer
- Gradation Compression
- Pattern Generator

9.2.6.5 Sensor Initialization Sequence

The following sequence must be followed to initialise the CMOS Image Sensor:

- After Power-On, register values are undefined. Thus, the system must be cleared. Hold SENSOR_XCLR at Low level for 500 ns or more to set all registers to their default values. In addition, hold SENSOR_XCE to High level during this period until SENSOR_INCK is input.
- Start the input of SENSOR_INCK after setting SENSOR_XCLR to High level.
- Set the sensor register through I2C or 4-Wire communication interface after the system having been cleared. A period of more than 21 µs must be provided after setting SENSOR_XCLR to High level before enabling communication through the setting of SENSOR_XCE Low.

The following diagram illustrate the initialization sequence:

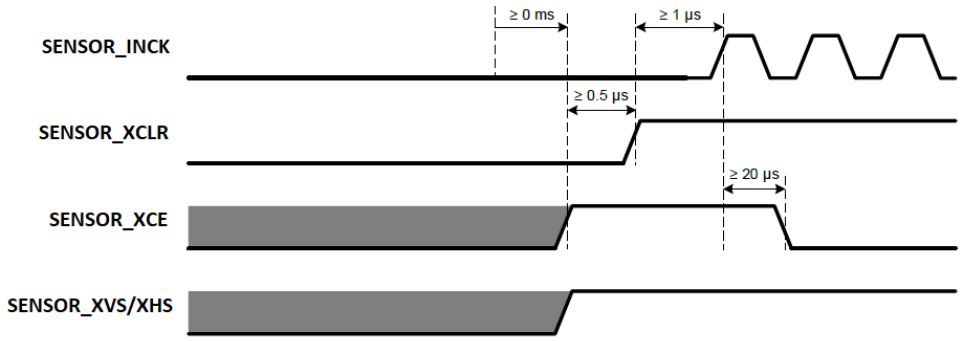


Figure 14 : CMOS Image sensor Initialization Sequence

Before powering down the CMOS Image sensor, each digital input (SENSOR_INCK, SENSOR_XCE, SENSOR_SCK, SENSOR_SDI, SENSOR_XCLR, SENSOR_XMASTER, SENSOR_XTRIG, SENSOR_SLAMODE, SENSOR_XVS, SENSOR_XHS) must be set to high impedance.

9.2.6.6 Sensor Setting Flow

9.2.6.7 Slave Mode

The figure below shows the operating flow of the sensor in slave mode. Standby setting can be enabled by setting the STANDBY register to “1” during operation of the sensor.

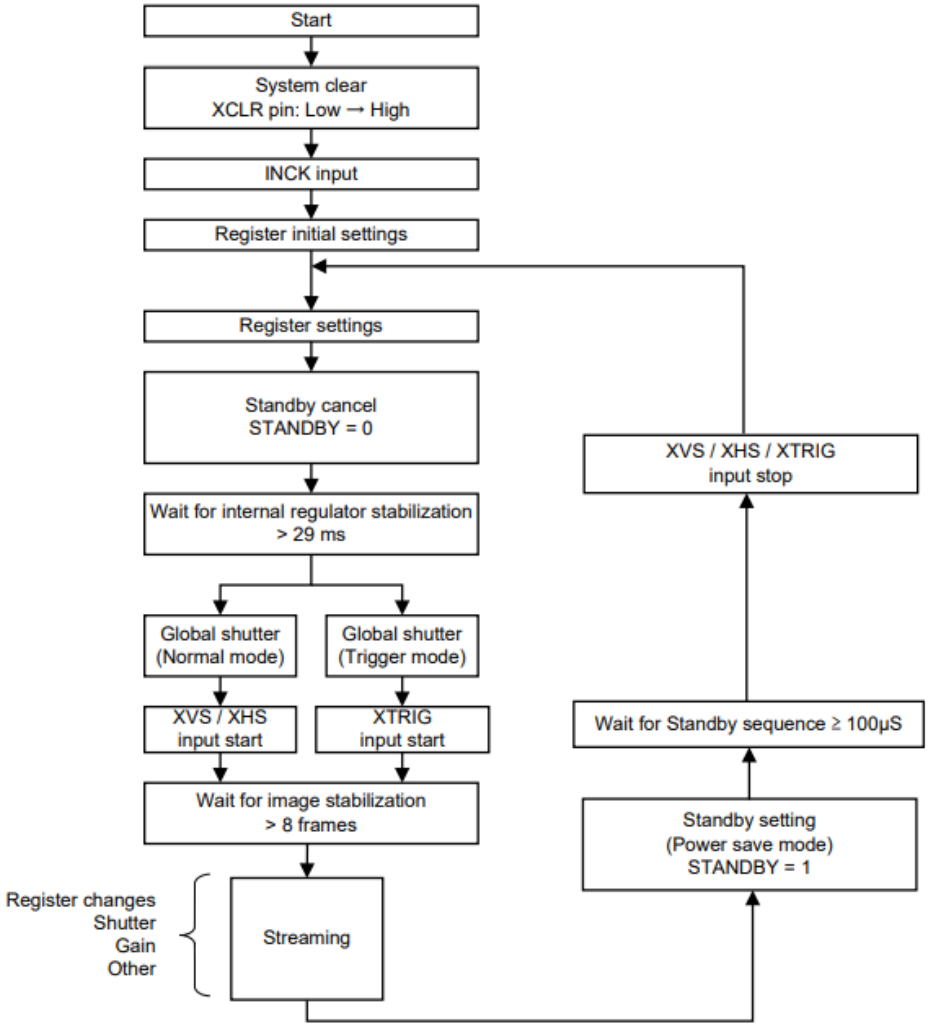


Figure 15 : Slave Mode Sensor Setting Flow

9.2.6.8 Master Mode

The figure below shows the operating flow of the sensor in master mode.

The Master mode starts by setting the master mode start register XMSTA to “0” after waiting for internal regulator stabilization (> 1 ms).

Standby setting (power save mode) can be enabled by setting the STANDBY register to “1” during operation of the sensor. Set XMSTA to “1” before the standby mode.

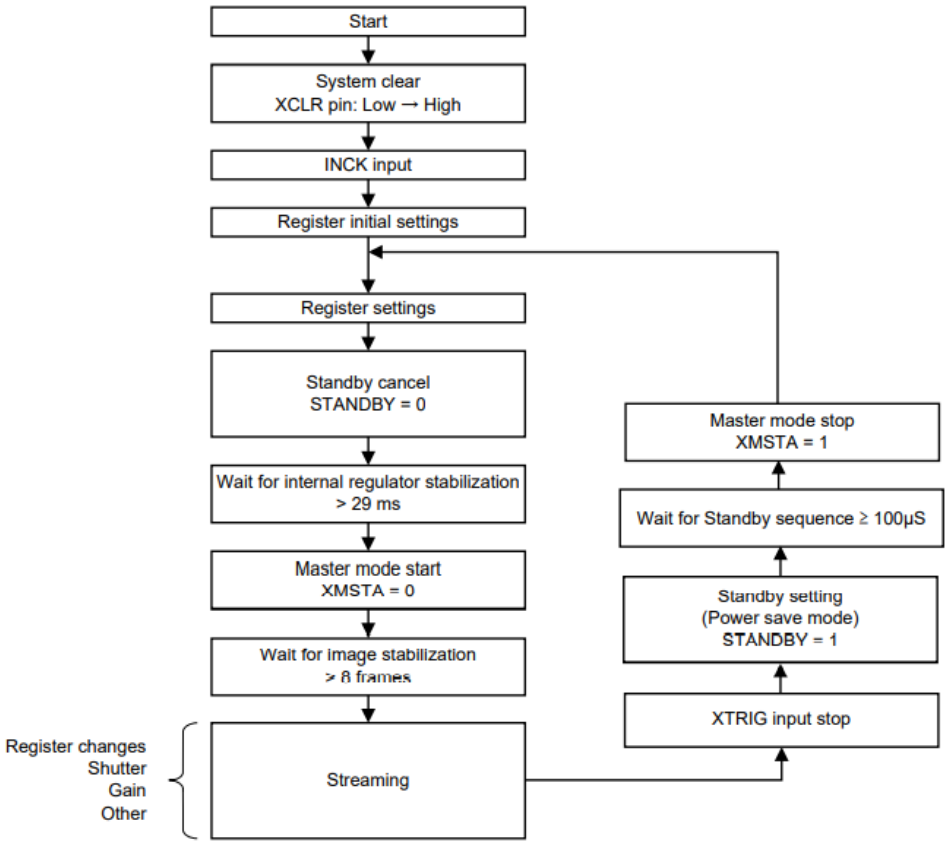


Figure 16 : Master Mode Sensor Setting Flow

9.3 EMBEDDED FPGA

The FPGA Core Embedded in the CASPEX 1.3M SWIR Space Camera Head is taken from the Xilinx Ultrascale family. The device is the Kintex Ultrascale XCKU040-2FBVA676I, in FBVA676 package. This FPGA is a high-performance FPGA Core benefiting from radiation tested process technology (20nm TSMC), and providing a performance/power ratio for such an application. For more information on the component and on how to use it, please refer to its documentation (RD1 to RD3). Interface between FPGA and PGA Pinout of the 3DCM880 Space Camera Head is detailed in section 10.1.1.

9.3.1 FPGA Main Features summary

- 20 nm TSMC process technology,
- 530 K System Logic Cells,
- 1920 DSP slices,
- 21.1 Mbit of RAM blocks,
- 6-input look-up tables (LUTs) and flip-flop
- High-speed memory interfaces (DDR3),
- On-chip thermal monitoring capability accessible through Xilinx SYSMON [RD4].

9.3.2 FPGA Resources

Device	Xcku040
Capacity	
System Logic Cells	530 250
Modules	
Configurable logic blocks LUTs	242 400
Configurable logic blocks flip-flop	484 800
Embedded RAM	
Maximum Distributed RAM	7 Mbits
Block RAM blocks	600
Block RAM	21.1 Mbits
Embedded DSP slices	1920
Clocks Management Tiles (1 MMCM, 2 PLLs)	10

Table 7: FPGA Resources

9.3.1 FPGA Analog Telemetries interface

The camera can be used to acquire telemetries of analog signals through FPGA SYSMON.

Signal name	Fpga pin	Type	Comments
AD0P	M20	Analog auxiliary inputs, unipolar	P3V3 (FPGA bank, sensor and NAND flash memories power supply) telemetry
AD0N	L20	Analog auxiliary inputs, unipolar	P3V3 telemetry ground
AD1P	K20	Analog auxiliary inputs, unipolar	VP (NOR Flash memories power supply) telemetry
AD1N	K21	Analog auxiliary inputs, unipolar	VP telemetry ground
AD2P	J21	Analog auxiliary inputs, unipolar	P2V2_SENSOR (sensor analog power-supply) telemetry
AD2N	H21	Analog auxiliary inputs, unipolar	P2V2_SENSOR telemetry ground
AD8P	M19	Analog auxiliary inputs, unipolar	P1V5 (FPGA bank and DDR memories power supply) telemetry
AD8N	L20	Analog auxiliary inputs, unipolar	P1V5 telemetry ground
AD9P	L18	Analog auxiliary inputs, unipolar	P1V2 (sensor digital power-supply telemetry
AD9N	K18	Analog auxiliary inputs, unipolar	P1V2 telemetry ground
AD10P	G21	Analog auxiliary inputs, unipolar	P1V2_SENSOR (sensor analog power-supply telemetry
AD10N	G22	Analog auxiliary inputs, unipolar	P1V2_SENSOR telemetry ground
AD11P	H19	Analog auxiliary inputs, unipolar	VREF_1 (board voltage reference*) telemetry
AD11N	G20	Analog auxiliary inputs, unipolar	VREF_1 (board voltage reference*) telemetry ground

Table 8: FPGA Analog Telemetries interface

Note : VREF_1 reference is not used for ADC acquisition, FPGA on-chip reference is used.

9.4 EMBEDDED CONFIGURATION MEMORY

The CASPEX 1.3M SWIR Space Camera Head uses three characterized, rad tolerant 128Mbit NOR Flash memories with a TMR implementation.

To increase the radiation tolerance of the NOR flash memories, it is recommended to switch off the memories after FPGA is loaded.

The signal CTRL_SWITCH_N (FPGA pin AB16) connected to one of the embedded FPGA Core User IOs is used to switch off the power supply.

The standard LVCMOS33 should be applied for the corresponding pin, and 16 mA mode should be used, to be able to provide enough current to have a fast start up.

When the signal CTRL_SWITCH_N is high, the power supply of the configuration memory is switched off. The signal CTRL_SWITCH_N shall be set to '1' in the FPGA firmware.

Each output of the NOR Flash memories before TMR is available to the FPGA Core for verification purpose via the following IOs:

- SO1: W20,
- SO2: W18,
- SO3: AB17.

Users are then able to access each memory output by using the SPI interface and these 3 output pins as User IO after FPGA configuration.

The standard LVCMOS33 should be applied for the corresponding pin, and 16 mA mode should be used for the CTRL_SWITCH_N signal, to be able to provide enough current to have a fast start up.

The interface between the FPGA and its configuration memory is described in the table below.

Signal Name	Direction	Fpga Pin	Type	Comment
SCK	OUT	U9	LVCMOS33	
CS_N	OUT	N7	LVCMOS33	
MOSI	OUT	U7	LVCMOS33	
MISO	IN	T7	LVCMOS33	
SO1	IN	W20	LVCMOS33	
SO2	IN	W18	LVCMOS33	
SO3	IN	AB17	LVCMOS33	
CTRL_SWITCH_N	OUT	AB16	LVCMOS33	16 mA mode configured, to be able to provide enough current to have a fast start up

Table 9: FPGA / Configuration memory interface

9.5 EMBEDDED ASYNCHRONOUS/SYNCHRONOUS NAND FLASH MEMORY

The CASPEX 1.3M SWIR Space Camera Head integrates a 48 Gbit synchronous NAND Flash memory. This NAND Flash memory can operate in synchronous and asynchronous mode and is organized as three 16 Gbit NAND Flash memories devices interfaced to the bank 64 of the FPGA Core through a 24-bit wide data bus.

For details description of the devices operation and configuration, refer to Open NAND Flash Interface Standard ONFI 2.1 [RD6].

9.5.1 Embedded NAND Flash Memory FPGA Interface

For this memory organization, all flash signals, except FLASH_DQ data bus and FLASH_DQS signals, are the same for all devices.

Pins DQS-1 and DQS-2 are paired for each device and interfaced to the FPGA through 3 signals FLASH_DQS1, FLASH_DQS2, FLASH_DQS3, one for each device.

Data interface with the FPGA is organized in a 24 bits wide data bus, with DQ[0:7] of each device interfaced to FLASH_DQ[0:7], FLASH_DQ[8-15] and FLASH_DQ[16:23].

The schematic of the NAND Flash Memory layer is presented as follow:

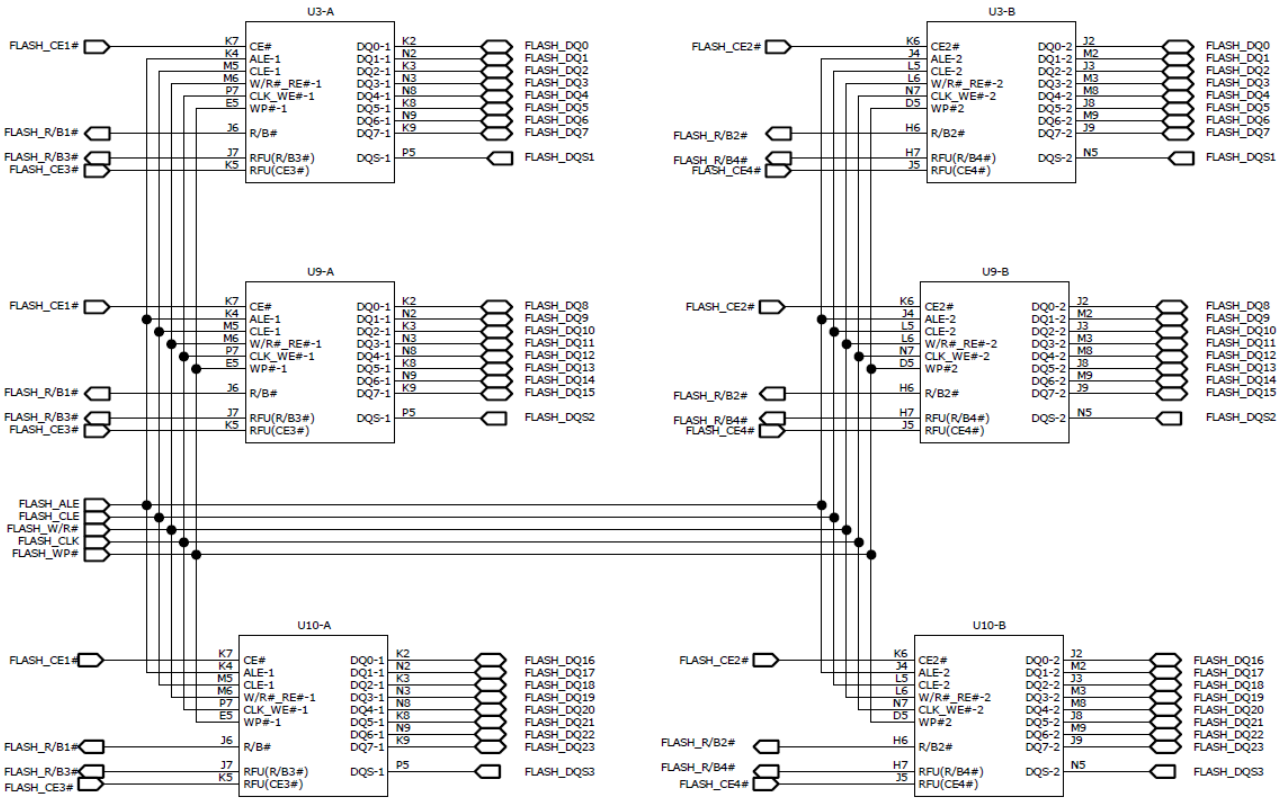


Figure 17 : NAND Flash Memory Organization

9.5.2 Embedded NAND Flash Memory FPGA pins assignment

The following pin assignment is mandatory as the FPGA Core and the NAND Flash memory are hard wired internally in the module. Thus, signal standards shall be configured to LVCMOS 1V8.

Please, refer to Electrical Characteristics for more details on specific operating conditions and power on/off sequencing.

Nand Flash Signal	Fpga Pin And Bank	Nand Flash Signal	Fpga Pin And Bank	Nand Flash Signal	Fpga Pin And Bank
FLASH_DQ0	AA15, Bank 64	FLASH_DQ15	AE11, Bank 64	FLASH_CE1#	AB11, Bank 64
FLASH_DQ1	AA14, Bank 64	FLASH_DQ16	AF10, Bank 64	FLASH_CE2#	AC11, Bank 64
FLASH_DQ2	AB15, Bank 64	FLASH_DQ17	AE10, Bank 64	FLASH_CE3#	AB12, Bank 64
FLASH_DQ3	AC14, Bank 64	FLASH_DQ18	AD9, Bank 64	FLASH_CE4#	Y12, Bank 64
FLASH_DQ4	AD15, Bank 64	FLASH_DQ19	AC9, Bank 64	FLASH_R/B1#	AA13, Bank 64
FLASH_DQ5	AE15, Bank 64	FLASH_DQ20	AD8, Bank 64	FLASH_R/B2#	V12, Bank 64
FLASH_DQ6	AD14, Bank 64	FLASH_DQ21	AC8, Bank 64	FLASH_R/B3#	Y10, Bank 64
FLASH_DQ7	AF15, Bank 64	FLASH_DQ22	AB9, Bank 64	FLASH_R/B4#	W10, Bank 64
FLASH_DQ8	AF14, Bank 64	FLASH_DQ23	AA8, Bank 64	FLASH_W/R#	Y11, Bank 64

Nand Flash Signal	Fpga Pin And Bank	Nand Flash Signal	Fpga Pin And Bank	Nand Flash Signal	Fpga Pin And Bank
FLASH_DQ9	AB14, Bank 64	FLASH_DQS1	AE16, Bank 64	FLASH_WP#	Y15, Bank 64
FLASH_DQ10	AC13, Bank 64	FLASH_DQS2	AE12, Bank 64		
FLASH_DQ11	AD13, Bank 64	FLASH_DQS3	AA9, Bank 64		
FLASH_DQ12	AF13, Bank 64	FLASH_ALE	W15, Bank 64		
FLASH_DQ13	AF12, Bank 64	FLASH_CLE	AC12, Bank 64		
FLASH_DQ14	AD11, Bank 64	FLASH_CLK	V11, Bank 64		

Table 10: FPGA / NAND Flash memory interface

Table 9 hereafter gives a description of each signal:

Signal Name	Device Signal Name	Type	Description	Comments
FLASH_ALE	ALE	Input	Address latch enable	Loads an address from DQx into the address register.
FLASH_CLE	CLE	Input	Command latch enable	Loads a command from DQx into the command register.
FLASH_CLK	CLK / WE#	Input	Write Enable and Clock	WE# transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLK latches command and address cycles.
FLASH_CEn#	CE#	Input	Chip enable	Enables or disables one or more die (LUNs) in a target.
FLASH_W/R#	RE# / W/R#	Input	Read enable and Write/Read	RE# transfers serial data from the NAND Flash to the FPGA when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQx and DQS.
FLASH_R/Bn#	R/B#	Output	Ready/busy	An open-drain, active-low output. This signal indicates target activity. A hardwired pull-up is embedded in the camera head
FLASH_DQ_x	DQx	I/O	Data inputs/outputs	The bidirectional I/Os transfer address, data, and command information.
FLASH_DQSn	DQS	I/O	Data Strobe	Provides a synchronous reference for data input and output
FLASH_WP#	WP#	Input	Write protect	Enables or disables array PROGRAM and ERASE operations.

Table 11: NAND FLASH Device Signals Description

Note 1: FLASH_R/Bn# is OR-tied to each of the NAND Flash device, as presented in Figure 17.

9.5.3 Embedded NAND Flash Initialization

WP# signal supports additional hardware protection during power transitions, this prevents data corruption during power transitions. After Power Up of the CASPEX 1.3M SWIR Space Camera Head, use the following procedure to initialize the device:

1- The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure below).

2- If not monitoring R/B#, the host must wait at least 200µs reset of the camera. If monitoring R/B#, the host must wait until R/B# is HIGH.

3- The asynchronous interface is active by default for each target. Each LUN draws less than an average of IST measured over intervals of 1ms until the RESET (FFh) command is issued.

4- The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for tPOR after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.

5- The device is now initialized and ready for normal operation.

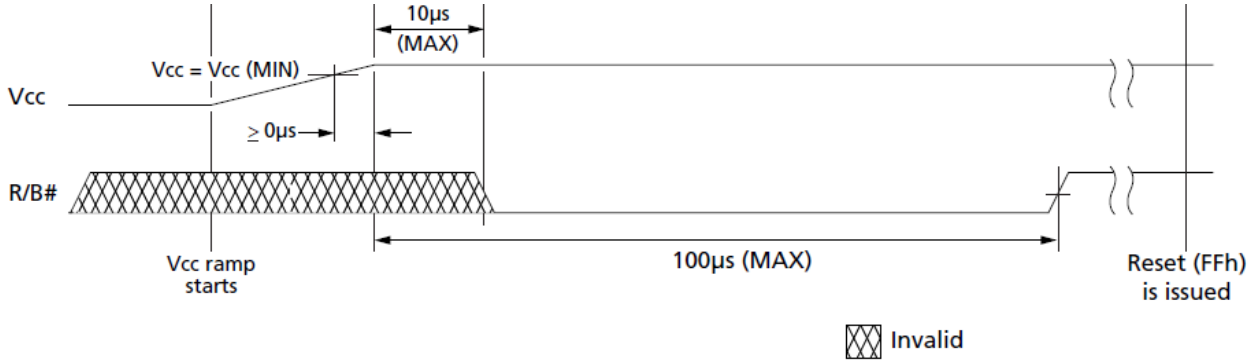


Figure 18 : Power on sequence

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETET PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

9.5.4 Embedded NAND Flash Operations

The following operations are detailed for individual device. The organization of the embedded NAND Flash memory of the CASPEX 1.3M SWIR Space Camera Head, described in 9.5.1 must be taken into account in order to use efficiently each NAND Flash devices.

Each NAND Flash device is organized as follow:

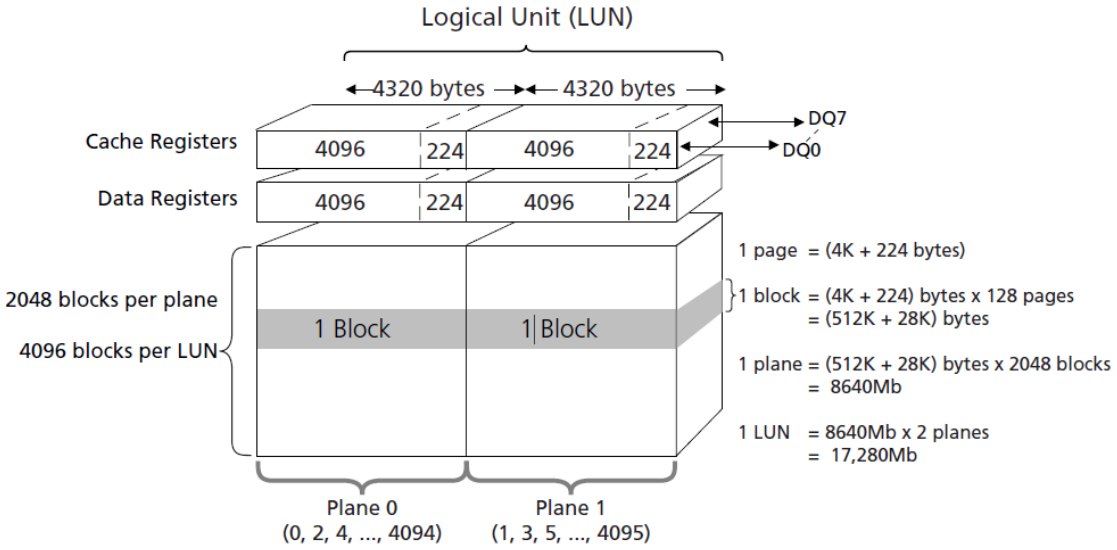


Figure 19 : Array organization per device

CYCLE	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CAO[2]
Second	LOW	LOW	LOW	CA12[3]	CA11	CA10	CA9	CA8
Third	BA7[4]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	BA18	BA17	BA16

Table 12: Array addressing for each device

Note 1: CAx= column address, PAx= page address, they are collectively called row addresses

Note 2: When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

Note 3: Column address number 4320 (10E0h) through 8191 (1FFFh) are invalid, out of bounds, do not exist in the device and cannot be addressed.

Note 4 : BA[7] is the plane select bit. Plane 0: BA[7] = 0; Plane 1: BA[7] = 1

All NAND operations supported are listed in Table 13: NAND Flash command set. Always refer to [RD6] for commands and sequence description.

Cycle	Command Cycle #1	Number Of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected Lun Is Busy[1]	Valid While Other Luns Are Busy[2]	Note
Reset Operations							
RESET	FFh	0	-	-	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	-	-	Yes	Yes	
Identification Operations							
READ ID	90h	1	-	-	-		3
READ PAREMETER PAGE	ECh	1	-	-	-		
READ ID UNIQUE	Edh	1	-	-	-		
Configuration Operations							
GET FEATURES	EEh	1	-	-	-		3
SET FEATURES	EFh	1	4	-	-		4
Status Operations							
READ STATUS	70h	0	-	-	Yes		
READ STATUS ENHANCED	78h	3	-	-	Yes	Yes	
Column Address Operations							
CHANGE READ COLUMN	05h	2	-	E0h	-	Yes	
CHANGE READ COLUMN ENHANCED	06h	5	-	E0h	-	Yes	
CHANGE WRITE COLUMN	85h	2	Optional	-	-	Yes	
CHANGE ROW ADDRESS	85h	5	Optional	-	-	Yes	5
Read Operations							
READ MODE	00h	0	-	-	-	Yes	
READ PAGE	00h	5	-	30h	-	Yes	6
READ PAGE MULTI-PLANE	00h	5	-	32h	-	Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	-	-	-	Yes	7
READ PAGE CACHE RANDOM	00h	5	-	31h	-	Yes	6,7
READ PAGE CACHE LAST	3Fh	0	-	-	-	Yes	7
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h	-	Yes	
PROGRAM PAGE MULTI-PLANE	80h	5	Yes	11h	-	Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h	-	Yes	8
Erase Operations							
ERASE BLOCK	60h	3	-	D0h	-	Yes	
ERASE BLOCK MULTI-PLANE	60h	3	-	D1h	-	Yes	
Copyback Operations							
COPYBACK READ	00h	5	-	35h	-	Yes	6
COPYBACK PROGRAM	85h	5	Optional	10h	-	Yes	

Cycle	Command Cycle #1	Number Of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected Lun Is Busy[1]	Valid While Other Luns Are Busy[2]	Note
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h	-	Yes	

Table 13: NAND Flash command set

Note 1: Busy means ready status RDY = 0.

Note 2: These commands can be used for interleaved die (multi-LUN) operations.

Note 3: The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.

Note 4: The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.

Note 5: Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) for more details.

Note 6: This command can be preceded by up to one READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous two-plane array operation.

Note 7: Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.

Note 8: Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.

9.5.5 Embedded NAND Flash error management

Each NAND Flash device is specified to have a minimum number of valid blocks (NVB) of the total available block. This means the device could have block that are invalid when shipped from the factory. An invalid Block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per device will not fall below NVB during the endurance life of the product.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark. The first block (physical block address 00h) for each device is guaranteed to be valid with ECC when shipped from the factory.

Description	Value
Minimum number of valid blocks (NVB) per device	4016
Total available blocks per device	4096
First spare area location	Byte 4096
Bab-block mark	00h
Minimum required ECC	4-bit ECC per 540 bytes of data

Table 14: Error management details

9.6 EMBEDDED DDR3 SDRAM MEMORY

The 3DCM880 SWIR Space Camera Head integrates an 8 Gbit DDR3 SDRAM memory in its architecture for processing purspose.

This DDR3 SDRAM memory layer is organized as two 4 Gbit DDR3 SDRAM memory devices (256M x 16 bits) interfaced to the banks 44 and 45 of the FPGA Core through a 32-bit wide data bus.

9.6.1 Embedded DDR3 SDRAM Memory Organization

All address signals DDR3_A[15:0] and DDR3_BA[2:0], as well as the command signals (DDR3_RAS#, DDR3_CAS#, DDR3_CS#, DDR3_WE#, DDR3_CKE0, DDR3_ODT0 and DDR3_CK/CK#) are shared between the two devices.

Each 16-bit wide data interface are interfaced with the FPGA Core in one 32-bit wide data but DDR3_DQ[31:0].

The signals UDM, LDM, UDQS/UDQS# and LDQS/LDQS# of each device signals are interfaced with the FPGA to each byte of the 32-bit wide data bus as follow:

- DDR3_DM0 (LDM), DDR3_DQS0/DDR3_DQS0# (LDQS) to DDR3_DQ[7:0],
- DDR3_DM1 (UDM), DDR3_DQS1/DDR3_DQS1# (UDQS) to DDR3_DQ[15:8],
- DDR3_DM2 (UDM), DDR3_DQS2/DDR3_DQS2# to DDR3_DQ[23:16],
- DDR3_DM3 (UDM), DDR3_DQS3/DDR3_DQS3# to DDR3_DQ[31:24].

The VREF_DDR3 pin of each device is connected to à 0.75V reference voltage.
The ZQ pin of each device is connected to the ground through a 240 Ohms pull-down resistor.

The DDR3 SDRAM memory is organized as follows:

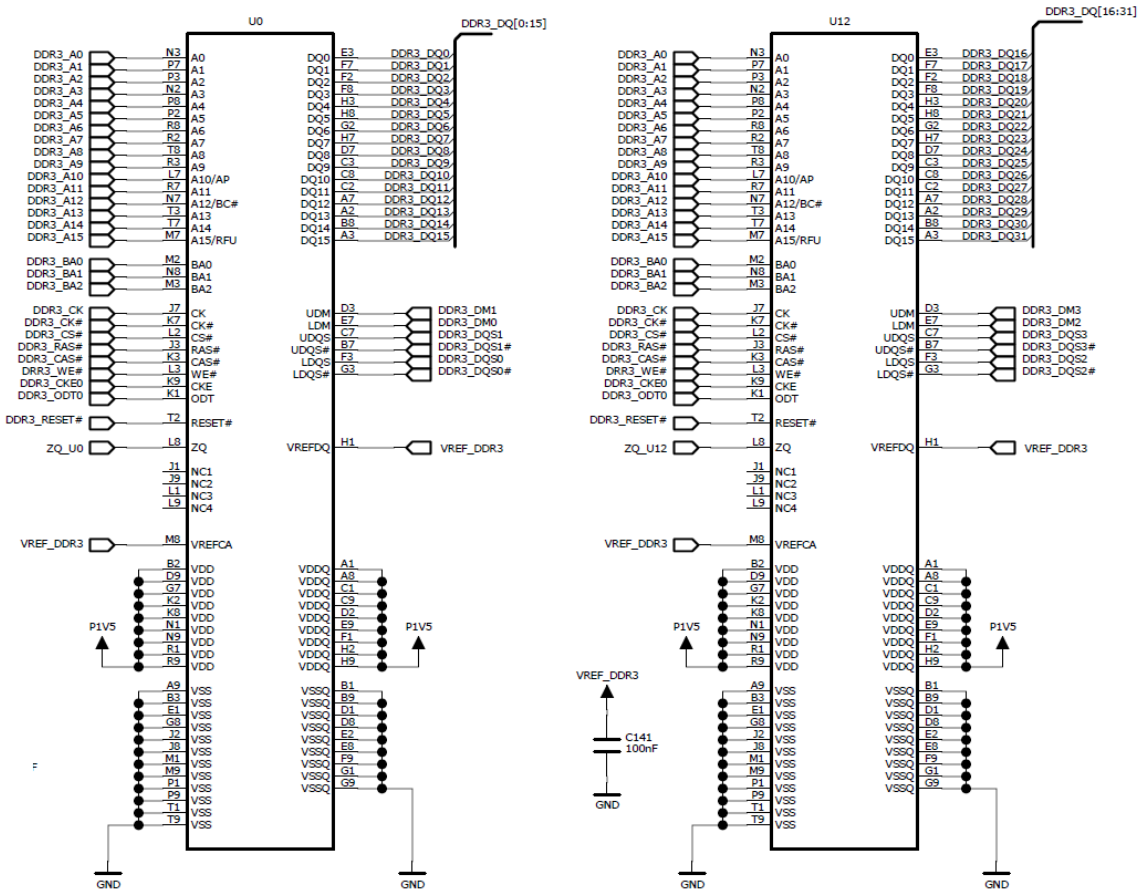


Figure 20 : DDR3 SDRAM Organization

9.6.2 Embedded DDR3 SDRAM Memory FPGA pins assignment

The following pin assignment is mandatory as the FPGA Core and the DDR3 SDRAM memory devices are hard wired internally in the module. Please, refer to §11 for more details on specific operating conditions and power on/off sequencing.

Memory Signal	Fpga Pin	Fpga Bank	Memory Signal	Fpga Pin	Fpga Bank	Memory Signal	Fpga Pin	Fpga Bank
DDR3_A0	R21	44	VREF_44_45	N18	45	DDR3_DQ8	AC26	44
DDR3_A1	T23	44	VREF_44_45	U19	44	DDR3_DQ9	AA23	44
DDR3_A2	P24	44	DDR3_ODT0	P19	44	DDR3_DQ10	AB26	44
DDR3_A3	P23	44	DDR3_DQS0	U26	44	DDR3_DQ11	Y23	44
DDR3_A4	T25	44	DDR3_DQS0#	V26	44	DDR3_DQ12	AC23	44
DDR3_A5	R22	44	DDR3_DQS1	AA25	44	DDR3_DQ13	AA22	44
DDR3_A6	U25	44	DDR3_DQS1#	AB25	44	DDR3_DQ14	AC24	44
DDR3_A7	P26	44	DDR3_DQS2	K26	45	DDR3_DQ15	AB22	44
DDR3_A8	AB24	44	DDR3_DQS2#	J26	45	DDR3_DQ16	L25	45
DDR3_A9	R25	44	DDR3_DQS3	F22	45	DDR3_DQ17	M22	45
DDR3_A10	U20	44	DDR3_DQS3#	F23	45	DDR3_DQ18	M25	45
DDR3_A11	T24	44	DDR3_CK	T19	45	DDR3_DQ19	N22	45
DDR3_A12	T22	44	DDR3_CK#	T20	45	DDR3_DQ20	N26	45
DDR3_A13	R26	44	DDR3_DM0	W23	44	DDR3_DQ21	M24	45
DDR3_A14	W24	44	DDR3_DM1	AA24	44	DDR3_DQ22	M26	45
DDR3_A15	R23	44	DDR3_DM2	N23	45	DDR3_DQ23	L24	45
DDR3_BA0	P21	44	DDR3_DM3	E25	45	DDR3_DQ24	H26	45
DDR3_BA1	U22	44	DDR3_DQ0	V22	44	DDR3_DQ25	G26	45
DDR3_BA2	R20	44	DDR3_DQ1	W25	44	DDR3_DQ26	J25	45
DDR3_RAS#	P18	44	DDR3_DQ2	V23	44	DDR3_DQ27	G25	45
DDR3_CAS#	P20	44	DDR3_DQ3	Y25	44	DDR3_DQ28	H24	45
DDR3_CS#	R18	44	DDR3_DQ4	U24	44	DDR3_DQ29	F25	45
DDR3_WE#	T18	44	DDR3_DQ5	Y26	44	DDR3_DQ30	J24	45
DDR3_RESET#	V21	44	DDR3_DQ6	V24	44	DDR3_DQ31	G24	45
DDR3_CKE0	U21	44	DDR3_DQ7	W26	44			

Table 15: 3DCM880 embedded DDR3 SDRAM memory interface

Table 16 hereafter gives a description of each signal:

Signal Name	Device Signal Name	Type	Function
DDR3_CK/CK#	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
DDR3_CKE	CKE	Input	Clock enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
DDR3_CS#	CS#	Input	Chip select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
DDR3_ODT	ODT	Input	On die termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT
DDR3_RAS#, DDR3_CAS#, DDR3_WE#	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DDR3_DM[3:0]	DM (DMU, DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
DDR3_BA[2:0]	BA0-BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle
DDR3_A[15:0]	A0-A15	I/O	Address Inputs: Provide the row address for Active commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands
DDR3_A10	A10/AP	Input	Auto-Precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
DDR3_A12	A12/BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details

Signal Name	Device Signal Name	Type	Function
DDR3_RESET#	RESET#		Active Low Asynchronous Reset: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
DDR3_DQ[31:0]	DQ (DQL,DQU)		Data Input/Output: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail- to-rail signal with DC high and low at 80% and 20% of VDD, i.e., 1.20V for DC high and 0.30V for DC low.
DDR3_DQS/DQS#[3:0]	DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#		Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

Table 16: DDR3 SDRAM device Signals Description

9.6.3 Embedded DDR3 SDRAM Description

9.6.3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

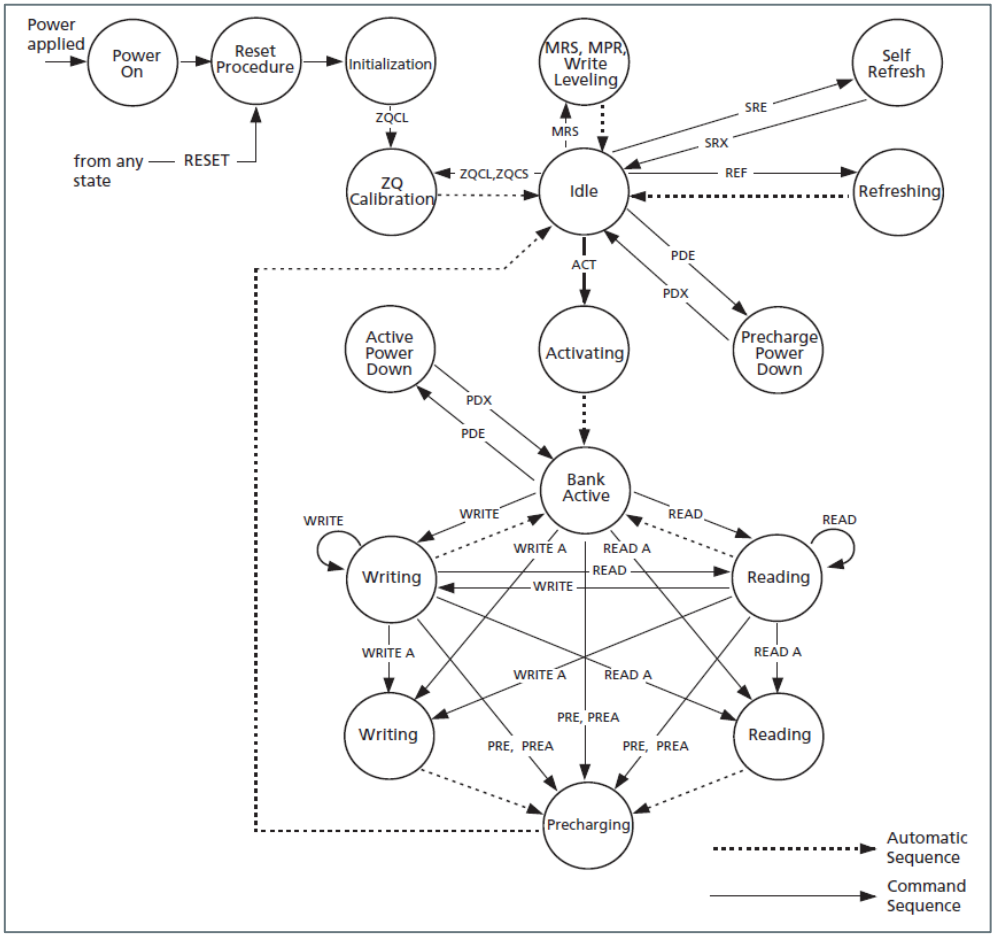


Figure 21 : Simplified DDR3 SDRAM State Diagram

9.6.3.2 Basic functionality

The DDR3 SDRAM devices integrated in the CASPEX 1.3M SWIR Space Camera Head are 4Gb DDR3 SDRAM devices. DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization.

For More details regarding the DDR3 SDRAM devices operations, please refer to the device datasheet referred in the CASPEX 1.3M SWIR Space Camera Head Detailed Specification [AD1] and to the DDR3 SDRAM Standard JEDEC Documentation [RD7].

9.6.3.3 Reset and Initialization Procedure

9.6.3.4 Power-Up and initialization sequence

The following sequence is required for Initialization after power-up of the CASPEX 1.3M SWIR Space Camera Head :

1- After RESET# is de-asserted, wait for another 500 µs until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

2- Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

3- The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

4- After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=max (tXS ; 5 x t_{CK})

5- Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)

6- Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)

7- Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).

8- Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).

9- Issue ZQCL command to starting ZQ calibration.

10- Wait for both tDLLK and tZQinit completed.

11- The DDR3 SDRAM is now ready for normal operation.

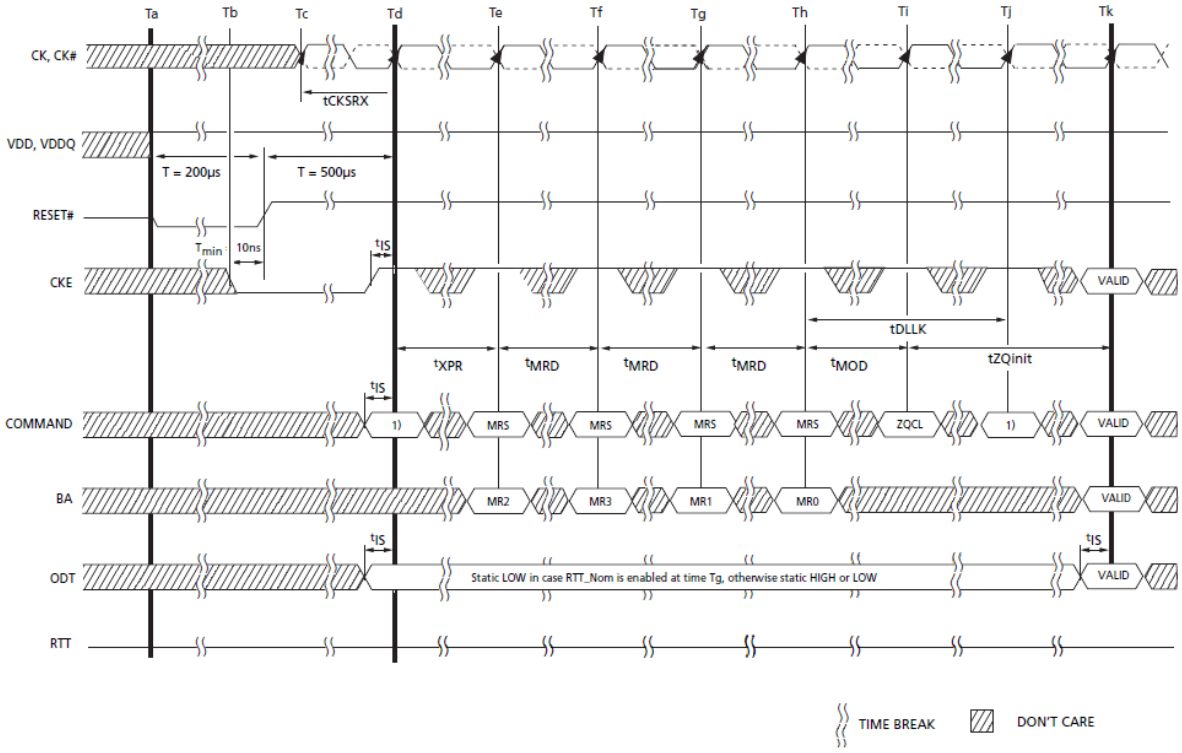


Figure 22 : Reset and Initialization Sequence at Power-on Ramping

9.6.3.4.1 Reset and Initialization with stable Power

The following sequence is required for RESET at no power interruption initialization.

1- Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled “LOW” before RESET being deasserted (min. time 10 ns).

2- Follow Power-up Initialization Sequence steps 1 to 10.

3- The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.

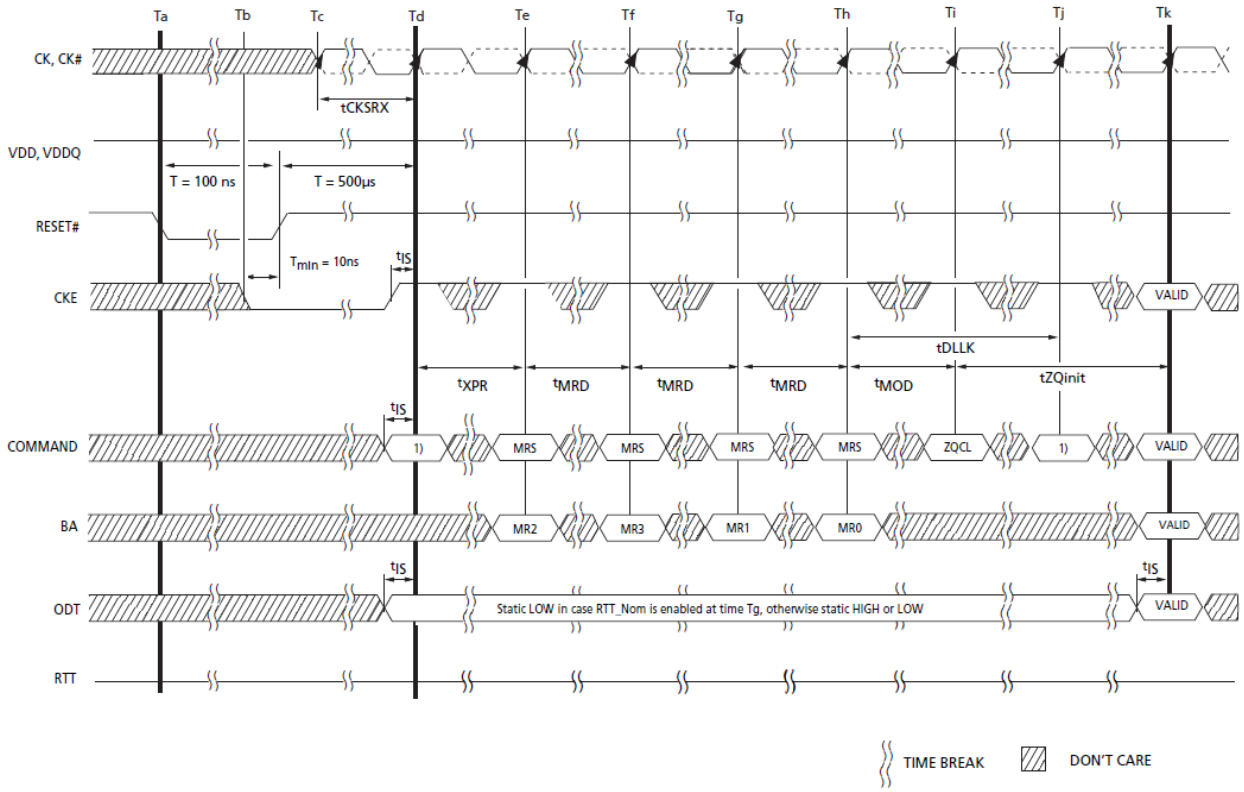


Figure 23 : Reset and Initialization Sequence at Power-on Ramping

9.7 EMBEDDED OSCILLATOR

The camera uses a 64 MHz oscillator which generates the input clock of the FPGA.

The interface between the FPGA and its configuration memory is described in the table below.

Signal Name	Direction	Fpga Pin	Fpga Bank	Type	Comment
OSC_CLK	IN	Y17	65	LVCMOS33	Input clock from oscillator

Table 17: FPGA / NAND Flash memory interface

10. PIN ASSIGNMENT AND DESCRIPTION

10.1 MODULE PIN-OUT

The electrical interface of the CASPEX 1.3M SWIR Space Camera Head has 72 electrical connections and 4 additional mechanical pins, as described in Table 18 hereafter.

Signal Name	Direction	Number of pins	Description
Power Supply			
Power Supply	-	6	External 5V Power Supply
GND	-	11	Global ground
LVDS Interface			
LVDS_IN_n_P/N	I/O	12	LVDS Differential I/Os
LVDS_OUT_n_P/N	I/O	32	
JTAG Interface and FPGA configuration pins			
SOFT_RESET	I/O	1	User I/O connected to pin Y21 of the camera head FPGA component. This pin is used in standard flight code 3DIPCC0838 as active low reset to the camera FPGA design. As opposed to the FPGA_Prog reset, it does not cause a FPGA configuration logic reset. An internal pull-up in the FPGA forces the SOFT_RESET pin High state by connecting it to the 3.3V power supply.
FPGA_TCK	I	1	Clock for all devices on a JTAG chain The FPGA_TCK pin is internally connected to a 3.3V pull-up resistor.
FPGA_TMS	I	1	Mode select for all devices on a JTAG chain. The FPGA_TMS pin is internally connected to a 3.3V pull-up resistor.
FPGA_TDI	I	1	JTAG chain serialized data input
FPGA_TDO	O	1	JTAG chain serialized data output
FPGA_DONE	O	1	A High signal on the FPGA_DONE pin indicates completion of the configuration sequence. The FPGA_DONE pin is internally connected to a 3.3V pull-up resistor.
FPGA_PROG	I	1	Active-Low reset to configuration logic. When FPGA_PROG is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset is initiated upon the falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge. FPGA_PROG can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. Dedicated pins remain disabled while FPGA_PROG is held Low. FPGA_PROG pin is internally held high through a 3.3V pull-up resistor.
Thermistors interface			
SENSOR_TEMPA_n	I/O	2	Direct electrical connection to PT1000 internal Thermistors SENSOR_TEMPA pins (H1 and H2 of the PGA package), located below the image sensor package in the camera head module.
FPGA_TEMPB_n	I/O	2	Direct electrical connection to PT1000 internal Thermistors FPGA_TEMPB pins (G1 and G2 of the PGA package) are connected to the PT1000 thermistor on the internal thermal

			drain attached to the internal FPGA die of the camera head.
Miscellaneous			
Mechanical pins	-	4	Mechanical pins placed at each corner of the PGA matrix
TOTAL	**-**	**76**	

Table 18: CASPEX 1.3M SWIR Space Camera Head functional pin-out

The SOFT_RESET signal is a user I/O connected to pin Y21 of the camera head FPGA component. This pin can be used as active low reset for a FPGA design. This can be done by using a P3V3 powered FPGA pin from bank 65. By default, an internal pull-up in the FPGA will force this SOFT_RESET input to the high state (inactive), the equipment driving the camera will be connected to this input via an open collector or open drain output,

This avoids problems of electrical compatibility and allows the camera's SOFT_RESET to be controlled from several controllers (see example below).

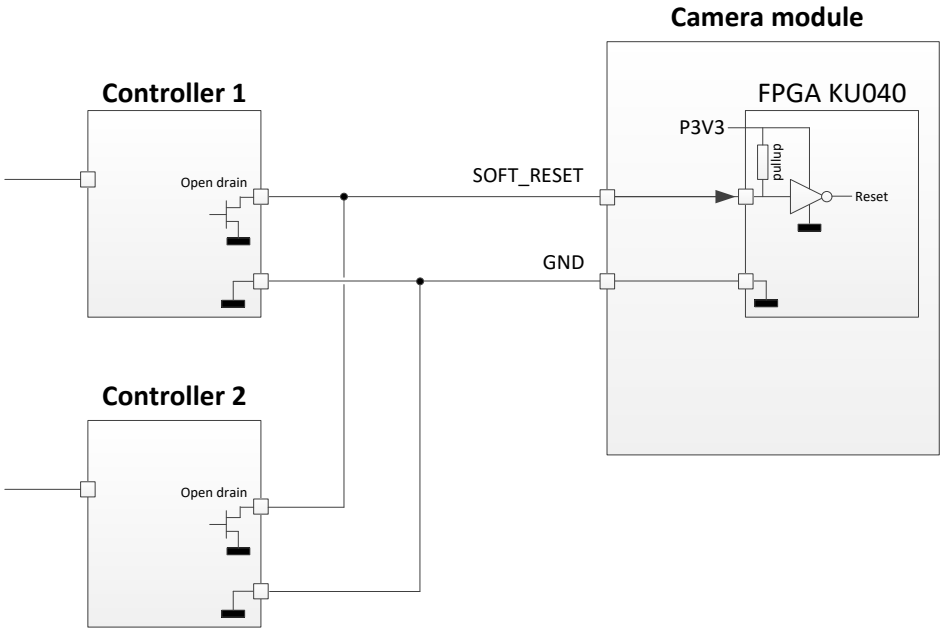


Figure 24: Example of SOFT_RESET signal use

The FPGA_PROG signal is an active-Low reset to configuration logic. When FPGA_PROG is pulsed Low, the FPGA configuration is cleared, and a new configuration sequence is initiated. Configuration reset is initiated upon the falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge. FPGA_PROG can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. Dedicated pins remain disabled while FPGA_PROG is held Low. FPGA_PROG pin is internally held high through a 3.3V pull-up resistor.

A High signal on the FPGA_DONE pin indicates completion of the configuration sequence. The FPGA_DONE pin is internally connected to a 3.3V pull-up resistor FPGA to Oscillator

10.1.1 FPGA to PGA Pinout Interface

Signal Name	Direction (seen from FPGA)	FPGA Pin	PGA Pin	FPGA Bank	Type	Comments
LVDS Interface						
LVDS_OUT_0_N	IN/OUT	A23	G6	46	LVDS	
LVDS_OUT_0_P	IN/OUT	A22	G7	46	LVDS	
LVDS_OUT_1_N	IN/OUT	A20	G5	46	LVDS	
LVDS_OUT_1_P	IN/OUT	B20	G4	46	LVDS	
LVDS_OUT_2_N	IN/OUT	B22	F6	46	LVDS	
LVDS_OUT_2_P	IN/OUT	B21	F7	46	LVDS	
LVDS_OUT_3_N	IN/OUT	C22	E4	46	LVDS	
LVDS_OUT_3_P	IN/OUT	C21	E5	46	LVDS	
LVDS_OUT_4_N	IN/OUT	E21	D4	46	LVDS	
LVDS_OUT_4_P	IN/OUT	E20	D5	46	LVDS	
LVDS_OUT_5_N	IN/OUT	D21	E6	46	LVDS	
LVDS_OUT_5_P	IN/OUT	D20	E7	46	LVDS	
LVDS_OUT_6_N	IN/OUT	C19	F5	46	LVDS	
LVDS_OUT_6_P	IN/OUT	D19	F4	46	LVDS	
LVDS_OUT_7_N	IN/OUT	C18	H5	46	LVDS	
LVDS_OUT_7_P	IN/OUT	D18	H4	46	LVDS	
LVDS_OUT_8_P	IN/OUT	A17	K7	46	LVDS	
LVDS_OUT_8_N	IN/OUT	A18	K6	46	LVDS	
LVDS_OUT_9_N	IN/OUT	A19	H7	46	LVDS	
LVDS_OUT_9_P	IN/OUT	B19	H6	46	LVDS	
LVDS_OUT_10_N	IN/OUT	B16	K5	46	LVDS	
LVDS_OUT_10_P	IN/OUT	C16	K4	46	LVDS	
LVDS_OUT_11_N	IN/OUT	B17	J7	46	LVDS	
LVDS_OUT_11_P	IN/OUT	C17	J6	46	LVDS	
LVDS_OUT_12_N	IN/OUT	F20	C5	46	LVDS	
LVDS_OUT_12_P	IN/OUT	G19	C4	46	LVDS	
LVDS_OUT_13_N	IN/OUT	F17	J5	46	LVDS	
LVDS_OUT_13_P	IN/OUT	G17	J4	46	LVDS	
LVDS_OUT_14_N	IN/OUT	F19	D6	46	LVDS	
LVDS_OUT_14_P	IN/OUT	F18	D7	46	LVDS	
LVDS_OUT_15_N	IN/OUT	G16	L6	46	LVDS	
LVDS_OUT_15_P	IN/OUT	H16	L5	46	LVDS	
LVDS_IN_0_N	IN/OUT	A25	B7	46	LVDS	
LVDS_IN_0_P	IN/OUT	A24	C7	46	LVDS	
LVDS_IN_1_N	IN/OUT	D26	A3	46	LVDS	
LVDS_IN_1_P	IN/OUT	D25	B3	46	LVDS	
LVDS_IN_2_N	IN/OUT	B25	A5	46	LVDS	
LVDS_IN_2_P	IN/OUT	B24	B5	46	LVDS	
LVDS_IN_3_N	IN/OUT	C23	A2	46	LVDS	
LVDS_IN_3_P	IN/OUT	D23	B2	46	LVDS	
LVDS_IN_4_N	IN/OUT	C24	A4	46	LVDS	
LVDS_IN_4_P	IN/OUT	D24	B4	46	LVDS	

Signal Name	Direction (seen from FPGA)	FPGA Pin	PGA Pin	FPGA Bank	Type	Comments
LVDS_IN_5_N	IN/OUT	B26	A6	46	LVDS	
LVDS_IN_5_P	IN/OUT	C26	B6	46	LVDS	
JTAG interface						
FPGA_TCK	IN	L9	L2	N/A	LVCMOS 3V3	Pullup 3.3V
FPGA_TMS	IN	P9	J3	N/A	LVCMOS 3V3	Pullup 3.3V
FPGA_TDI	IN	N9	K3	N/A	LVCMOS 3V3	
FPGA_TDO	OUT	L9	L3	N/A	LVCMOS 3V3	
FPGA Configuration and Reset interface						
FPGA_PROG	IN	M7	K2	N/A	LVCMOS 3V3	Pullup 3.3V
FPGA_DONE	OUT	V7	J2	N/A	LVCMOS 3V3	Pullup 3.3V
SOFT_RESET	IN	Y21	J1	65	LVCMOS 3V3	Pullup 3.3V

Table 19: CASPEX 1.3M SWIR Camera head FPGA to PGA Pin Interface

10.2 PIN ASSIGNMENT

The Grid Array is constituted of 76 pins, 11 x 7 with pin B1 missing for fool-proof. (refer to Figure 25).

The pin pitch is 2.54 mm.

Refer to footprint for Package CE4 ([AD5]).

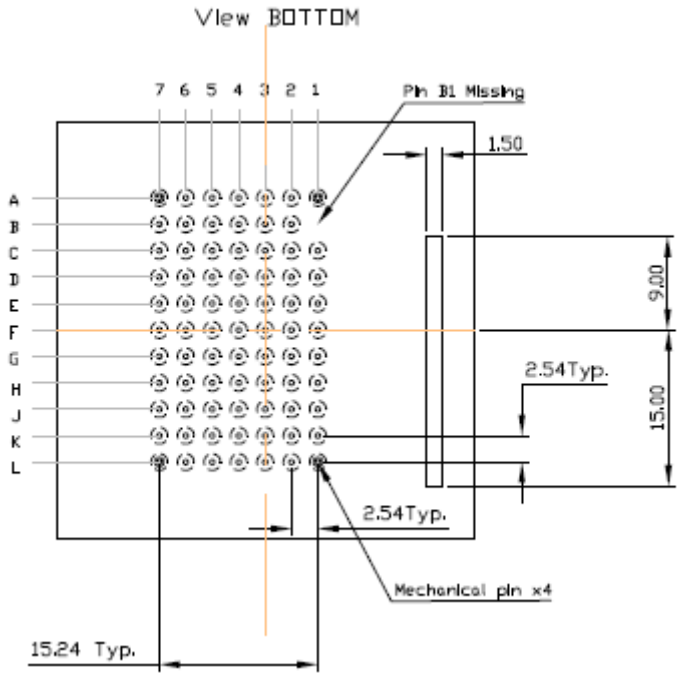


Figure 25: CASPEX 1.3M SWIR Camera Head Bottom View

10.2.1 PGA pins assignment (Top view)

	1	2	3	4	5	6	7
A	Mechanical pin	LVDS_IN_3_N	LVDS_IN_1_N	LVDS_IN_4_N	LVDS_IN_2_N	LVDS_IN_5_N	Mechanical pin
B	NC *(pin not present)*	LVDS_IN_3_P	LVDS_IN_1_ P	LVDS_IN_4_ P	LVDS_IN_2_N	LVDS_IN_5_ P	LVDS_IN_0_N
C	VIN	VIN	VIN	LVDS_OUT_12_P	LVDS_OUT_12_N	GND	LVDS_IN_0_ P
D	VIN	VIN	VIN	LVDS_OUT_4_N	LVDS_OUT_4_P	LVDS_OUT_14_N	LVDS_OUT_14_P
E	GND	GND	GND	LVDS_OUT_3_N	LVDS_OUT_3_P	LVDS_OUT_5_N	LVDS_OUT_5_P
F	GND	GND	GND	LVDS_OUT_6_P	LVDS_OUT_6_N	LVDS_OUT_2_N	LVDS_OUT_2_P
G	FPGA_TEMPB_2	FPGA_TEMPB_1	GND	LVDS_OUT_1_P	LVDS_OUT_1_N	LVDS_OUT_0_N	LVDS_OUT_0_P
H	SENSOR_TEMPA_2	SENSOR_TEMPA_1	GND	LVDS_OUT_7_P	LVDS_OUT_7_N	LVDS_OUT_9_P	LVDS_OUT_9_N
J	SOFT_RESET	FPGA_DONE	FPGA_TMS	LVDS_OUT_13_P	LVDS_OUT_13_N	LVDS_OUT_11_P	LVDS_OUT_11_N
K	GND	FPGA_PROG	FPGA_TDI	LVDS_OUT_10_P	LVDS_OUT_10_N	LVDS_OUT_8_N	LVDS_OUT_8_P
L	Mechanical pin	FPGA_TCK	FPGA_TDO	GND	LVDS_OUT_15_P	LVDS_OUT_15_N	Mechanical pin

Power supply	GND	Thermistor interface
JTAG, FPGA configuration and Reset signals	LVDS interface	Mechanical pins

Table 20 : CASPEX 1.3M SWIR Camera Head PGA Pin Assignment

11. ELECTRICAL CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, are as described in the following table:

N°	Characteristics	Symbol	Maximum Ratings	Unit	Remarks
1	Voltage on VIN Supply relative to GND	VIN	-0.3 to 6.5	V	
2	JTAG voltage	V_{JTAG}	-0.400 to 3.950	V	
3	Voltage on LVDS pins relative to GND	V_{LVDS}	-0.55 to 2.35	V	
4	3.3 LVCMOS IO Voltage and configuration I/O relative to GND	V_{3V3}	-0.3 to 3.6	V	
5	Input current	I_{IN}	2.7	A	
6	Current through thermistors	I_{therm}	1	mA	
7	Storage Temperature Range	T_{STG}	-55 to +125	°C	
8	Power Dissipation	P_{DMAX}	12.7	W	Maximum power dissipation at 70°C End-of-Life. Highly dependent on the FPGA Configuration and module usage
9	Junction Temperature	T_J	125	°C	

Table 21: Absolute Maximum Ratings

Note: Permanent module damage, including package and Die, may occur if Absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

11.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Input Voltage	4.5	5	5.5	V
$V_{IDIFF\ LVDS}$	Differential input voltage on LVDS		See Table 24		
$V_{ICM\ LVDS}$	Common mode input voltage on LVDS		See Table 24		
TEMP	Operating temperature	-55	-	+70	°C

Table 22: Recommended operating conditions

Note: Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

11.3 POWER SUPPLY INTERFACE

11.3.1 Power-up

Inrush current on input power supply does not exceed nominal module consumption.

11.3.2 Power Consumption

The average power consumption (Beginning Of Life) of the CASPEX 1.3M SWIR space camera heads are described Table 23. This table considers the use of 3D PLUS Standard FPGA design 3DIPCC0848, further described in §13 of this datasheet.

Symbol	Parameter	-55°C	25°C	+70°C	Unit
P_{No_Prog}	No prog mode (FPGA_PROG asserted low)	1	1.2	2	W
P_{Idle}	Idle mode	3.5	4	6	W
P_{acq}	Image acquisition mode	5	5.5	9	W

Table 23: Average power budget for CASPEX 1.3M SWIR Camera Head with 3DIPCC0848 FPGA Design

These values are dependent on the FPGA design used to configure the FPGA core of the CASPEX 1.3M SWIR camera head and should be recalculated using Xilinx Power estimator tools for Kintex Ultrascale KU040 [RD5] when considering a custom FPGA design.

11.3.3 Internal Power Supply Switching Characteristics

All internal voltages provided to the camera head electronics components are generated by several Point-of-Load switching converters, with specific switching frequency of 600 kHz.

11.3.4 Decoupling and Input Filter

The CASPEX 1.3M SWIR Space Camera Head module embeds an input filter to ensure a good current rejection from the POL to the main supply at the switching frequency. In addition, the internal POLs of the camera are protected from high frequency perturbation from the main supply. Furthermore, the input filter

allows being dependent free from the parasitic inductance coming from the wire length between the DC/DC converter that provides the main supply (5V) and the camera.

Input filter is constituted by a serial inductor (10µH, L9), 1 tantalum capacitor (1 x 330µF) with 2 damping resistors (2 x 1Ω), followed by a ceramic capacitor close to each DC-DC converter (10µF).

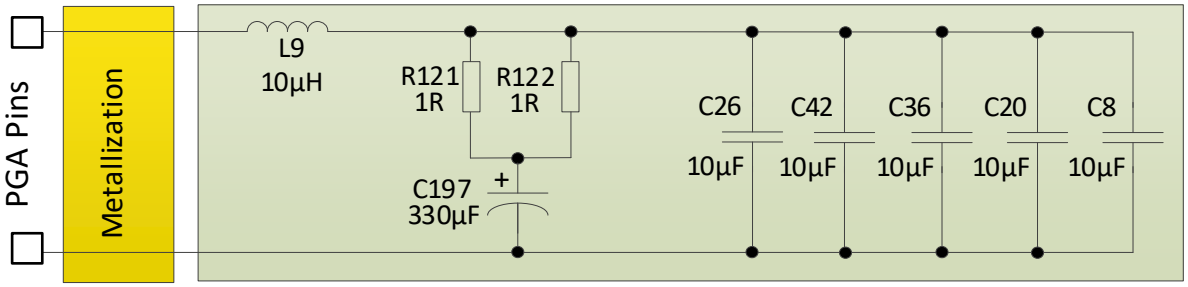


Figure 26: CASPEX 1.3M SWIR Camera Head Input filter

11.4 LVDS AND CONFIGURATION INTERFACES

The CASPEX 1.3M SWIR Space Camera Head module provides 22 LVDS pairs, directly connected to the FPGA component. All those pairs can be configured as input or output at FPGA level.

When configured as input, it is recommended for the user to connect a 100 Ω resistor between two pairs of each pins or use 100 Ω termination configurable in the FPGA. For outputs, the user shall connect a 100 Ω resistor between the two wires of each link to ensure the current loop.

LVDS interface of the FPGA for 3DCM880 are given in the table hereafter:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcco	Internal supply voltage to LVDS bank	-	-	1.8	-	V
Vodiff	Differential Output Voltage	Rt = 100 Ω across N and P signals	247	350	600	mV
Vocm	Output Common-mode Voltage	Rt = 100 Ω across N and P signals	1.000	1.250	1.425	V
Vidiff	Differential Input Voltage		100	350	600	mV
VICM_DC	Input Common-mode Voltage (DC coupling)		0.300	1.200	1.425	V
VICM_AC	Input Common-mode Voltage (AC Coupling)		0.600	-	1.100	V

Table 24 : LVDS pins interface specifications

12. RADIATION PERFORMANCES

The radiation performances of the CASPEX 1.3M SWIR Space Camera Head are defined both by the radiation performances of the semiconductor devices embedded in the module, and by the system level radiation hardening technics (RHBD) chosen in the module design.

The following sections are giving an overview of the main radiation characteristics of the semiconductor devices used in the CASPEX 1.3M SWIR Space Camera Head and RHBD technics and protection mechanisms integrated in the module hardware architecture. Detailed radiations report for SEE and TID testing campaigns of the CASPEX 1.3M SWIR space camera heads are detailed in [AD3] and [AD4], as company confidential documents. Those are only consultable on 3D PLUS premises for 3D PLUS customers.

12.1 3D PLUS RADIATION HARDNESS ASSURANCE

3D PLUS modules, including the CASPEX 1.3M SWIR camera heads, have complex electrical design embedding multiples heterogeneous components. Radiation hardness is guaranteed be several layers of design considerations:

- Base components radiation performances: Each component from passives to complex FPGA are evaluated for their performances, either by 3D PLUS, or by publicly available reports. Additional testing is also performed regarding TID performances (radiation LAT) to guarantee the module base components performances, for most component (FPGA is excluded for target TID range of the camera heads).
- System level analysis and radiation mitigation: The electronic design of 3D PLUS modules takes into consideration the radiation performances in its design hypothesis based on ECSS Space Product Assurance standards, especially at Design Justification and Worst Case Analysis, choosing suitable design margins to guarantee the module performance during its whole life and targeted environment. This also includes hardware mitigation technics when needed to reduce or suppress occurrence rate of radiation events.
- Algorithm/Architecture adequation: For FPGA base architecture, 3D PLUS provides FPGA design solution, either standalone IP Cores, or full FPGA design. The section of this datasheet describes the available solution for the 3DCM880 camera heads. The development of these IPs is made based on ECSS-Q-ST-60-02C standard, including radiation aspect analysis. Mitigation technics such as TMR or EDAC algorithm are integrated in order to reduce SEE occurrence rate when needed.

12.2 EEE COMPONENTS RADIATION PERFORMANCES

12.2.1 CMOS Image Sensor

The CASPEX 1.3M SWIR Space Camera Head embeds a High-resolution high-performance CMOS Image Sensor. This device is space qualified, and has been submitted to radiation testing campaigns.

12.2.1.1 Single Event Effects

The 3DCM880 camera head image sensor have been evaluated for SEE/SEFI performances, as based on the same pixel and readout circuit as the CASPEX 12M camera heads. Preliminary SEE parameters are considered to be as follow (TBC) :

Parameter	Value
W	20
S	1
σ_{sat}	3.10^{-5} cm²/device
LETth	0.4 MeV.cm²/mg

Table 25: Image sensor Weibull parameters

12.2.1.2 Dose Effects

The image sensor of the CASPEX 1.3M SWIR camera head have been submitted to protons irradiation campaign to characterize dose effects on its performances.

Increase of dark current is the main dose effect on the optoelectronic performances of the sensor. Conversion gain, saturation sees slight degradation at high irradiation level.

The following table summarize main parameters measurement before and after irradiation with 62 MeV protons :

Equivalent Dose	Fluence	Dark current	Read noise	CVF	Saturation
rad	p/cm²	ke⁻/s	e⁻	LSB/e⁻	ke⁻
0	0	30	240	0.025	170
1343	1.10^{10}	85	240	0.03	170
4028	3.10^{10}	165	245	0.04	160
13427	1.10^{11}	335	250	0.1	150

Table 26 : Measurement summary before and after gamma/protons irradiation

Note: Proton irradiation has been performed with 62 MeV energy level.

12.2.2 FPGA Core

The CASPEX 1.3M SWIR Space Camera Head embeds an AMD-Xilinx Kintex Ultrascale XCKU40 FPGA Core. The Ultrascale (TSMC 20nm) technology has been proved to be efficient for radiative environment with available performances results, including by Xilinx Company. The FPGA Core has shown validated TID (>100 krad (Si)) and SEL (> 80 MeV.cm²/mg) performances.

12.2.2.1 Single Events Effects

The FPGA Core has been SEE characterized, focusing on multiple internal components by implementing related design (shift registers, counter designs, etc). No Latch-up Events are observed below a LETth of 80 MeV.cm²/mg.

The table below gives SEU Weibull parameters for Configuration RAM (CRAM) and Block Ram (BRAM) components of the FPGA Core, and occurrence rate for a typical GEO environment (in and out of flare).

Component	Weibull Parameters	Total rate (out-of-flare)	Total rate (in-flare)
CRAM	W = 5 S = 1.3 σ_{sat} = 8.10^{-10} cm²/bit LET_{th} = 0.5 Mev.m²/mg	$1.01.10^{-8}$ /bit/day	$4.74.10^{-06}$ /bit/day
BRAM	W = 2 S = 0.98 σ_{sat} = $9.6.10^{-10}$cm²/bit LET_{th} = 0.9 MeV.cm²/mg	$1.80.10^{-08}$ /bit/day	$8.33.10^{-06}$ /bit/day

Table 27 : SEU Weibull Parameters and error rate in typical GEO environment for CRAM and BRAM

12.2.2.2 Dose Effects

The FPGA core has been evaluated up to 120 krad(Si) with full functionality and showed an average of 7% increase in the fabric core increase and less than 2% increase in the BRAM, GTM, I/O and DSP leakage currents. The maximum TID induced propagation delay increase is less than 1% and all devices tested passed AC characteristics tests and functionals test within less than 1 week of annealing.

12.2.3 Embedded Configuration Memory

The CASPEX 1.3M SWIR Space Camera Head includes three 128 Mbit NOR Flash configuration memories. This component used in 3D PLUS modules has been evaluated for its radiation performances and shown validated TID (>40 krad(SI) not polarized) and SEL (>62.5 MeV.cm²/mg) performances.

This memory is Radiation Hardened By Design with a protection against potential SEE ensured by TMR mitigation and an enhanced TID performance (40 krad (Si)) made possible by the integrated power switch of the module (15 krad – ON all time of irradiation). In order to reach these TID performances, users must switch off the configuration memory after the FPGA is configured in order to permit low duty-cycle for the NOR Flash memory devices. The configuration memory is sensitive to SEFF

12.2.3.1 Single Events Effects

The SPI NOR Flash component used in CASPEX 1.3M SWIR camera heads have been SEE characterized. It showed Latch-up immunity up to SEL LET threshold of 62.5 MeV.cm²/mg.

SEFF have been observed above a LET threshold of 46 MeV.cm²/mg at room temperature, with a saturated cross section of 5.10^{-6} cm²/device, for ERASE and PROGRAM modes only. No SEFF can occur when the device is powered off, in IDLE mode, or in READ mode. In the intended use as configuration memory, the failure rate is negligible (read mode at power-up and powered off).

The table below gives the SEU/SEFI parameters for the SPI NOR FLASH :

Type	Weibull Parameters
SEFI	W = 10 S = 3 σ_{sat} = 5.10^{-6} cm²/bit LET_{th} = 2 MeV.cm²/mg
SEU	W = 50 S = 5 σ_{sat} = $7.5.10^{-11}$ cm²/bit LET_{th} = 15 MeV.cm²/mg

Table 28 : SEU/SEFI performances for SPI NOR Flash component

SEU can occur with memory powered on and off. TMR is used to correct these effects. SEFI can only occur with the memory powered on, with a negligible occurrence rate with a duty cycle near zero.

12.2.3.2 Dose Effects

The SPI NOR Flash configuration memory used as the base component in the CASPEX 1.3M SWIR camera head has been characterized for TIP performances. Depending on the duty cyle, TID performances are varying. With a duty cycle of 100% (always turned ON, Vcc = 3.3V), the component can perform up to 15 krad(Si). With a duty cycle of 0% (always OFF, Vcc = 0V), the component can perform up to 40 krad (Si).This is the intended use in the 3DCM880 camera head, the SPI NOR FLASH being used only during FPGA configuration, then able to be powered off via an internal power switch.

12.2.4 Embedded NAND Flash Memory

The CASPEX 1.3M SWIR Space Camera Head embeds a 48 Gbit NAND Flash Memory accessible by the FPGA Core through a 24-bit wide data bus. The devices used to provide this memory layer are space qualified, with validated TID (>60 krad(Si)) and SEL LET threshold (> 62.5 MeV.cm²/mg) performances. SEU events can be mitigated by the use of a dedicated ECC or Radiation Intelligent Memory Controller.

12.2.4.1 Single Event Effects

The NAND Flash memory used in the CASPEX 1.3M SWIR camera head has been characterized for is SEE performance. The table below give Weibull parameters and occurrence rate for a typical GEO environment.

Type	Weibull Parameters	Total Rate (out-of-flare)	Total Rate (in-flare)
SEU	W = 39 S = 1.3 σ_{sat} = 1.6e^{-10} cm²/bit LET_{th} = 1.2 MeV.cm²/mg	9.54.10^{-11} /bit /day	9.08.10^{-08} /bit /day
SEFI	W = 39 S = 1.3 σ_{sat} = 1.6e^{-10} cm²/bit LET_{th} = 1.25 MeV.cm²/mg	8.13.10^{-04} /device /day	4.55.10^{-01} /device /day

Table 29: SEU/SEFI Weibull parameters and occurance rate for NAND Flash memory

12.2.4.2 Dose Effects

The NAND Flash memory used in the CASPEX 1.3M SWIR camera head has been characterized for is TID performance. Functional and parametric tests were performed guaranteeing the memory component up to 75 krad(Si).

12.2.5 Embedded DDR3 SDRAM Memory

The CASPEX 1.3M SWIR Space Camera Head includes a 2 Gbit SDRAM Memory accessible by the FPGA Core through a 32-bit wide data bus. The devices used to provide this memory layer are space qualified, with validated TID (>75 krad(Si)) and SEL LET threshold (> 67.2 MeV.cm²/mg) performances. SEU events can be mitigated by the use of a dedicated ECC or Radiation Intelligent Memory Controller.

12.2.5.1 Single Events Effects

The DDR3 SDRAM memory used in the CASPEX 1.3M SWIR camera head has been characterized for is SEE performance. The table below give Weibull parameters and occurrence rate for a typical GEO environment.

Type	Weibull Parameters	Total Rate (out-of-flare)	Total Rate (in-flare)
SEU	W = 57 S = 4.08 σ_{sat} = 1.05.10^{-11} cm²/bit LET_{th} = 0.4 MeV.cm²/mg	2.52.10^{-14} /bit /day	1.70.10^{-11} /bit /day
SERE	W = 44.9 S = 3.11 σ_{sat} = 6.56.10^{-3} cm²/bit LET_{th} = 0.4 MeV.cm²/mg	1.07.10^{-02} /device /day	8.63.10^{+00} /device /day
SECE	W = 17.7 S = 0.999 σ_{sat} = 4.29.10^{-3} cm²/bit LET_{th} = 2.18 MeV.cm²/mg	1.06.10^{-01} /device /day	1.41.10^{+02} /device /day
SEFI	W = 34.2 S = 2.33 σ_{sat} = 6.18.10^{-6}cm²/bit LET_{th} = 0.4 MeV.cm²/mg	1.74.10^{-05} /device /day	5.53.10^{-03} /device /day

Table 30: SEU/SERE/SECE/SEFI Weibull parameters and occurrence rate for DDR3 SDRAM memory

12.2.5.2 Dose Effects

The DDR3 SDRAM memory used in the CASPEX 1.3M SWIR camera head has been characterized for is TID performance. Functional and parametric tests were performed guaranteeing the memory component up to 75 krad(Si).

12.3 CONFIGURATION MEMORY HARDENING

As the SPI NOR Flash configuration memory is a critical part of the CASPEX 1.3M SWIR camera head, its performances must be guaranteed during its life. Two aspects of radiation effects have been considered as described in §9.4: TMR for SEU/SEFI mitigation and Power Switch for TID functional performances enhancement.

Indeed, the SPI NOR Flash of the CASPEX 1.3M SWIR camera head is intended to store the configuration bitstream for the KU040 FPGA Core. As the camera module can be switched off multiple time during a mission, the SRAM-based FPGA Core requires to be configured each time. For this purpose, the FPGA design integrity, and thus reliability of the reading of the SPI NOR Flash configuration memory must be guaranteed.

In order to avoid any error in the loaded bitstream caused by a potential SEU after module power-up and FPGA configuration, Three base components are used in a TMR configuration, and a majority voting is performed on read data.

An internal power switch function has also been embedded in the CASPEX 1.3M SWIR camera head to allow the user to switch off the SPI NOR Flash power supply, enhancing with low duty cycle its radiation performances.

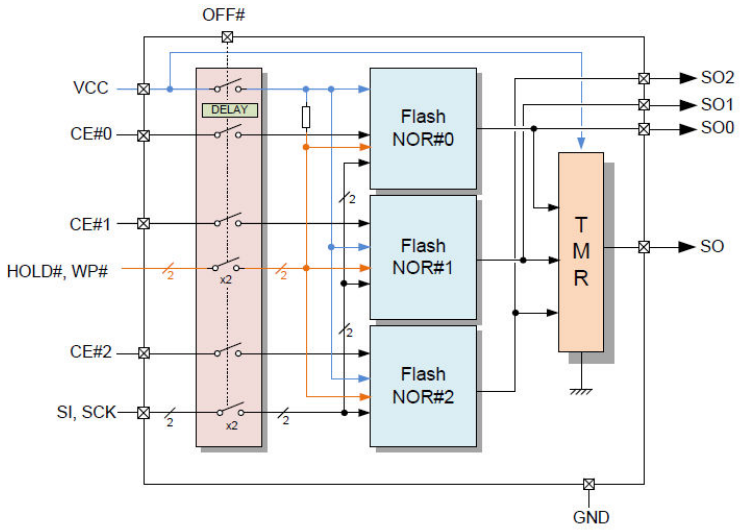


Figure 27 :SPI NOR Flash TMR configuration of CASPEX 1.3M SWIR camera head

12.4 RADIATION PERFORMANCES SUMMARY

The radiation tolerant CASPEX 1.3M SWIR Space Camera Heads are guaranteed for Total Ionizing Dose (TID) of 40 krad(Si) and Single-Event-Latch-ups (SELs) immunity up to 60 MeV.cm²/mg. Intrinsic hardness to Single-Event Effects (SEEs) provided by the semiconductor technology is strengthen by specific radiation-hardened by design (RHBD) strategy to meet the requirements of space applications, as detailed in the previous sections.

13. FPGA DESIGN AND IP CORES

The CASPEX 1.3M SWIR CMOS Space Camera Head architecture is FPGA based. Thus, the development of an associated FPGA design to allow users to operate the Space Camera Head is required. 3D PLUS provides several catalogue options to answer the need for a ready-to-use solution, as well as building blocks for a custom firmware development.

13.1 3DIPCC0848 SPACE QUALIFIED FPGA DESIGN

As a ready-to-use FPGA design solution to operate the CASPEX 1.3M SWIR Space Camera Head, 3D PLUS offers as a catalogue product (P/N 3DIPCC0848), a full flight FPGA design developed based on ESA's ECSS-Q-ST-60-02C Standard.

It provides an efficient interface to support camera applications by integrating all required hardware controllers (CMOS Image sensor, Memories), IP Cores, and Communication to operate the CASPEX 1.3M SWIR Space Camera Head to its full capabilities.

This firmware's communication interface is based on a SpaceWire Interface to provide the user access to:

- Telecommands (for dynamic configuration of internal IPs and components, frames or video requests)
- Telemetries (Temperature sensors, Health monitoring, status registers)
- Output images or videos data.

Main features:

- Full Camera operation, compatible to the Image Sensor functionalities
- Low level image processing (binning, averaging, windowing)
- Dynamic configuration of the registers through telecommands: Integration time, Gain, Window position and size
- Provides telemetry: Integration time, Gain, Window position and size (X/Y offsets and width/height), Test mode, Health status and Self-test
- Complete access to the configuration registers of the sensor
- Adjustable frame rate through dedicated registers
- Compatible with the maximum frame rate of the CMOS sensor
- Space wire interface:
    - Up to 64 Mbps for reception (telecommands and configuration)
    - Up to 128 Mbps for transmission (telemetries and video streaming):
        - Up to 6 Mpixels/s in 10/12 bits mode
        - Up to 12 Mpixels/s in 8-bit mode
- Internal DDR3 SDRAM and NAND Flash Memory Management with radiation effect mitigation (ECC, scrubbing mechanisms) Associated IP Cores

For specific applications for which additional or different algorithms would be needed, 3D PLUS proposes several catalogue IP Cores to help the CASPEX 1.3M SWIR Space Camera users develop their own FPGA design.

13.1.1 3DIPCC0835 DDR3 SDRAM Controller IP Core

The 3DIPCC0835 DDR3 SDRAM Controller is a fully configurable DDR3 SDRAM memory controller IP core designed for CASPEX 12M and CASPEX 1.3M SWIR Space Camera Heads.

The 3DIPCC0835 is designed to achieve radiation tolerance improvement in the use of the Space Camera DDR3 SDRAM internal memory. It contains all standard functions of a DDR3 memory controller, includes memory devices Single Event Upset (SEU) mitigation and Single Event Functional Interrupt (SEFI) protection in order to answer the need of applications subjected to radiative environments, and provides standard AMBA compatible interfaces for easy integration in a custom design.

Main features:

- Configurable via AMBA architecture interface (AHB User Interface bus / AXI3 protocol)
- Integrated DDR PHY interface
- Selectable Enable/Disable EDAC (Hamming Error Correcting Code (ECC))
- Selectable Burst Access (4 – 8)
- Configurable DRAM refresh time
- Scrubbing function
    - Selectable Enable/Disable scrubbing
    - Configurable scrubbing frequency

13.1.2 3DIPCC0847 SWIR Image Sensor Controller IP Core

The 3DIPCC0847 SWIR Image Sensor Controller IP Core is specifically designed to provides an IP Core solution to operate the CASPEX 1.3M SWIR Space Camera image sensor.

The 3DIPCC0847 allows the operations of all built-in functionalities of the CMOS image sensor, providing access to all configuration registers to operate the sensor depending on the application. It is compatible with the sensor's maximum performances (frame rate, pixel bit depth, resolution), and handle the datastream from the sensor to allow a standard AMBA architecture interface for easy integration in a custom design. The 3DIPCC0847 provide image data in a specific format, providing additional telemetry data to the user.

Main features:

- Generate frame and video requests and read-out of the sensor
- Configuration of main parameters of the Sensor :
    - Exposure time
    - Gain
    - Offset
    - Bit mode (8/10/12-bit pixels)
- Low level image processing:
    - Windowing
    - Multi ROI
    - Configurable binning up to 8x8 pixels
        - Additional analog binning of the sensor compatible
- Telemetry including :
    - Exposure time/Gain/Offset
    - On-board Time
    - CIS Temperature
    - Window/ROI parameters
- Standard AXI3 Master interconnect interface for image data transmission to the FPGA main design
- Standard AHB Slave interface
- Standard APB Slave interface

13.2 CUSTOM FPGA DESIGN DEVELOPMENT OPTION

For details on 3D PLUS FPGA development options for the CASPEX 1.3M SWIR Space Camera Head, please contact your 3D PLUS Sales representative and/or the associated Product Manager.

14. EVALUATION KIT

The 3DEV0830 Space Camera Head Evaluation Kit is a tool designed to support the development and testing of systems and firmware centered around the CASPEX 1.3M SWIR CMOS Space Camera Head. It allows the user to simply interface with the Space Camera Head to evaluate the multiple functionalities of its architecture.

The 3DEV0830 Space Camera Head Evaluation Kit consists of the following:

- A Generic electrical interface board based on the CASPEX 1.3M SWIR Space Camera Head pinout, with an adapted camera socket and a generic connector for flex-rigid PCB and camera module assembly, Camera link and Space Wire interface connectors, Power supply connectors,
- A National instrument CameraLink® PC interface board
- A StarDundee SpaceWire-USB Interface Brick
- A 3D PLUS developed Camera Interface PC software (for communication and control of the camera)
- An evaluation camera FPGA design for the CASPEX 1.3M SWIR Space Camera Head, to allow communication with the PC Software and operating of the camera.

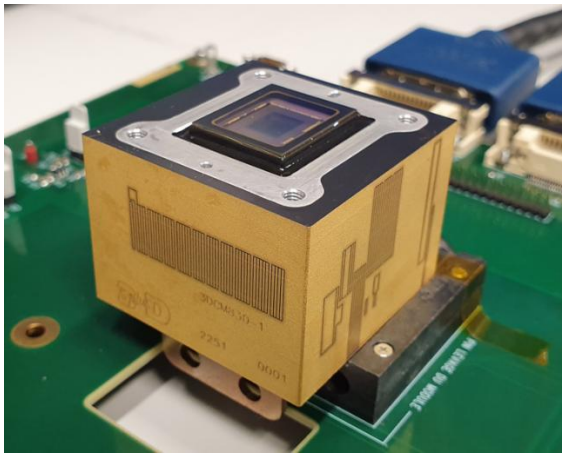


Figure 28: CASPEX 1.3M SWIR camera head on associated test board an socket

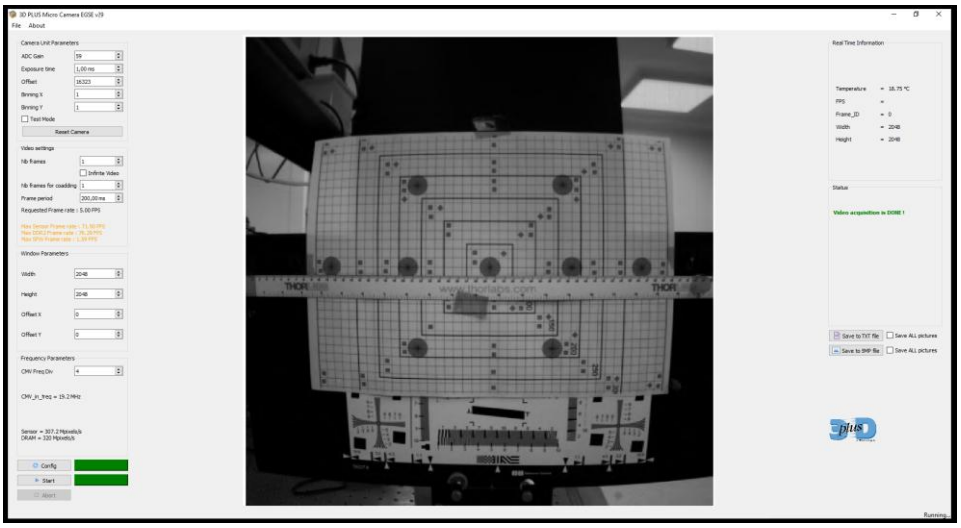


Figure 29: 3DEV0830 preliminary PC user interface

The 3DEV0830 Space Camera Head Evaluation Kit allows the user to configure the camera parameters (exposure time, acquisition modes, binning, windowing, etc) to evaluate its functionalities and the operating modes of the sensor, request video sequence acquisition for image quality evaluation.

The 3DEV0830 Space Camera Head Evaluation Kit mechanical drawing will be available to help users integrate the CASPEX 1.3M SWIR Space Camera Head on their optical bench.

15. FLEX-RIGID PCB ELECTRICAL INTERFACE

The bottom of CASPEX 1.3M SWIR Space Camera Head contains a pin grid array (PGA) area where a flex-rigid PCB connector enables robust electro-mechanical connections between the camera head and the interfaced system.

This type of interface allows generic connectors to be used to interface the CASPEX 1.3M SWIR Space Camera Head to answers the specific requirements of each mission, for both the electrical interface and its shape.

Both generic and custom flex-rigid PCB connector solution are available and can be tailored to fit the mission requirements, according to ECSS-Q-ST-70-12C. This includes the interface PCB board to operate the camera head assembled on the flex-rigid PCB with the 3DEV0830 Evaluation Kit.

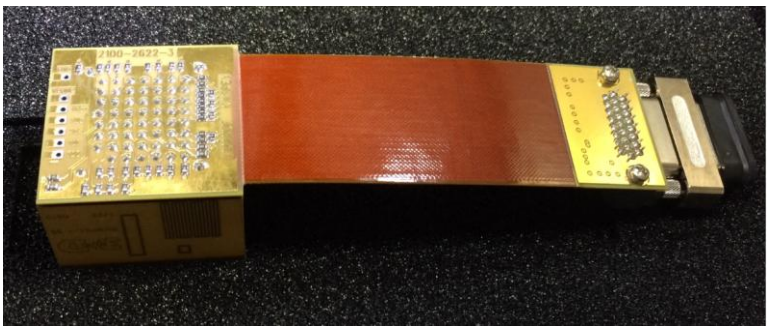


Figure 30: Example of Flex-Rigid PCB with connector adapted on a 3DCM734 Space Camera Head

16. PACKAGING

16.1 PACKAGE DESCRIPTION

The CASPEX 1.3M SWIR Space Camera Head package is a parallelepiped with a section of 40mm x 40mm and a height of 45 mm. The pins height is of 2.5 mm, the thermal drain is 15 mm, bringing the total height of the module to 45 mm. The 3D PLUS Package reference associated is CE4 (See.[AD5]).

The camera module dimensions are given in the following drawings:

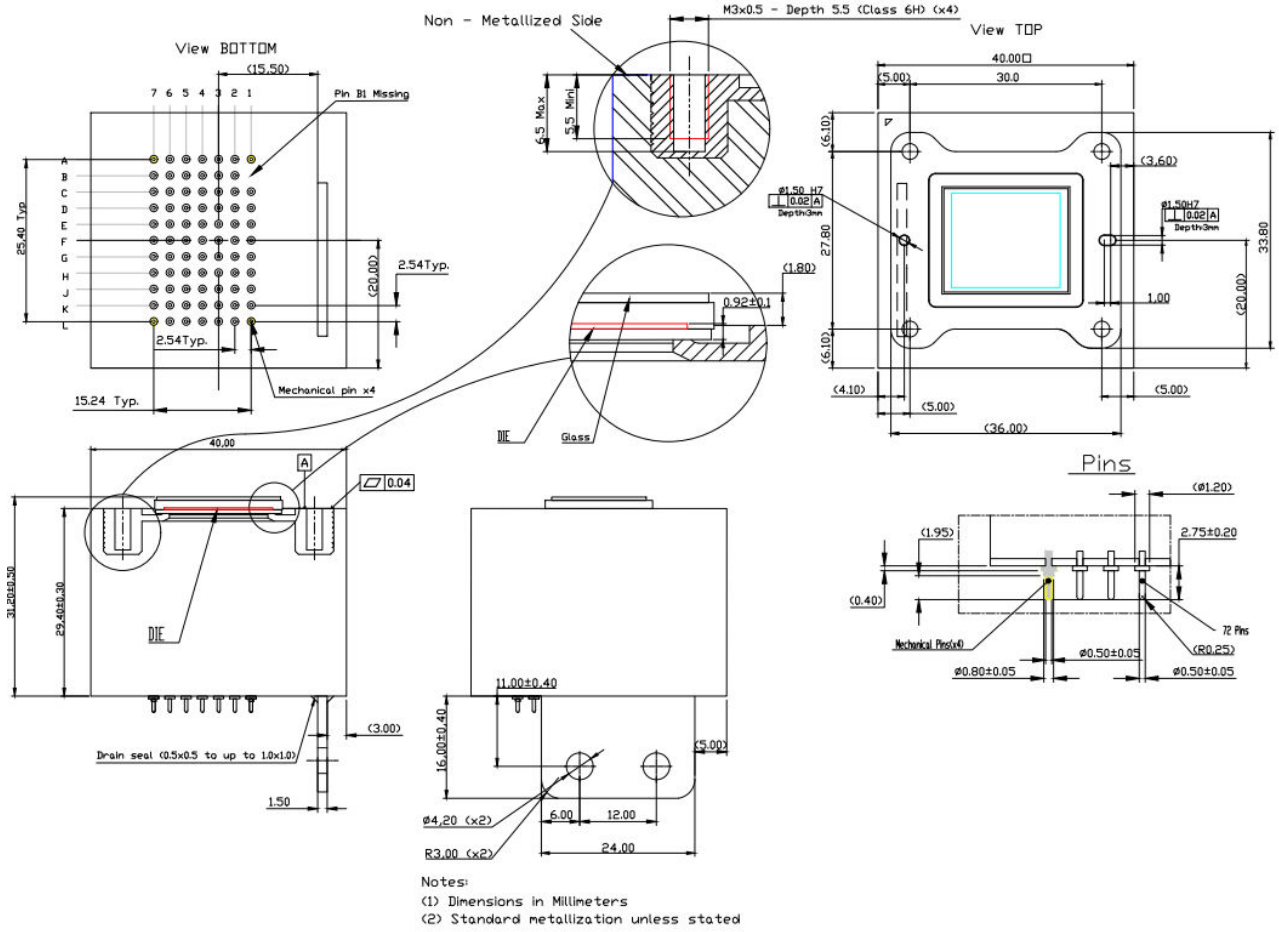


Figure 31: CASPEX 1.3M SWIR Camera Head Mechanical Drawing

Notes:

Dimensions are in mm.
Mass of the module is 140 ±5 g

16.2 OPTICAL INTERFACE

The sensor active area is made with 1280 columns x 1024 rows with a pitch of 5 µm. Its package is embedded in a metallic cradle functioning as a mechanical, thermal and optical interface for the CASPEX 1.3M SWIR Space Camera Head.

The optical center is defined in the following drawing:

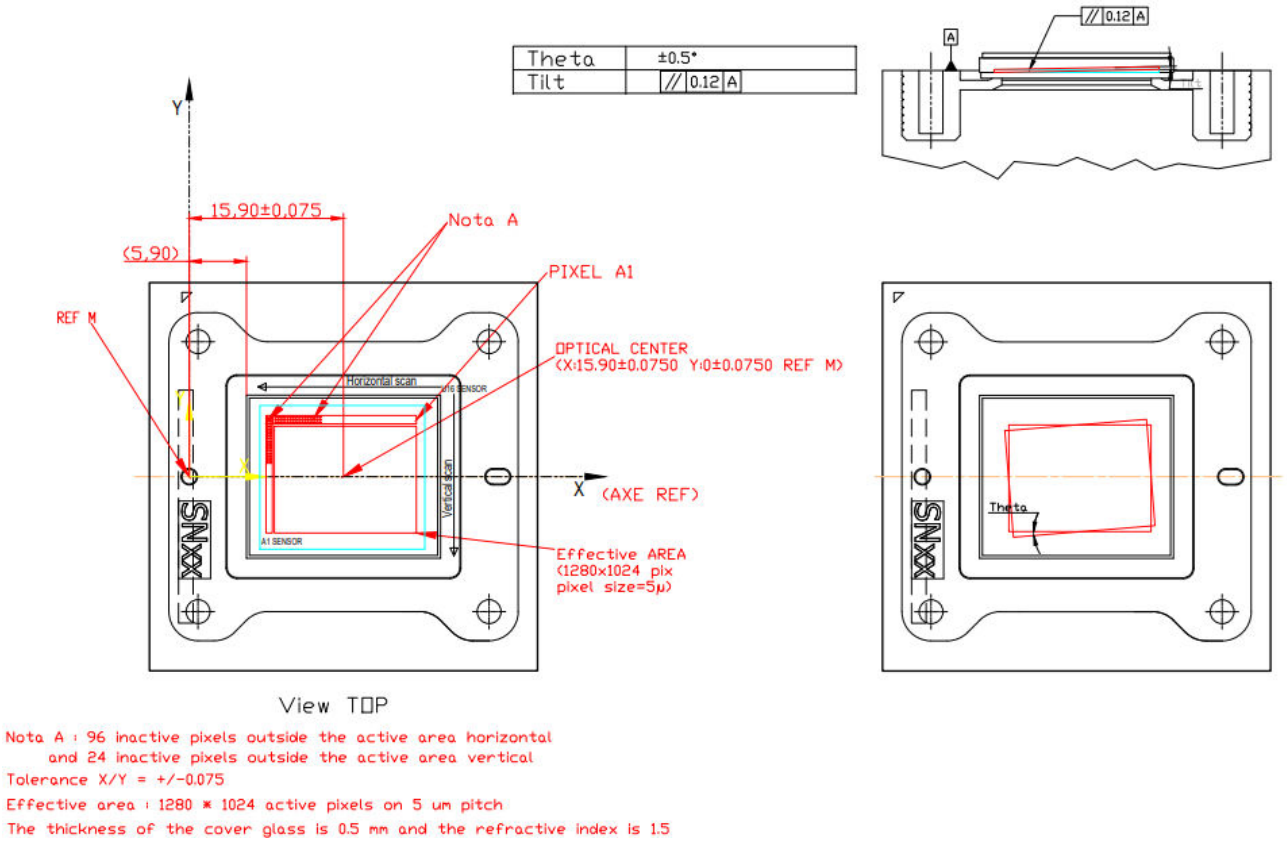


Figure 32: CASPEX 1.3M SWIR Sensor Optical Reference

Maximum rotation of the pixel matrix with regards to the cradle: Theta = ±1°.

16.3 THERMAL INTERFACE

The CASPEX 1.3M SWIR Space Camera Head provides two distinct thermal interfaces. The first thermal interface is the metallic cradle in which the image sensor is located.

A specific thermal interface is also available on the bottom of the CASPEX 1.3M SWIR module. This thermal interface is a 1.5 mm thick copper drain, linked internally to the FPGA Core package and placed near all internal power supply components.

17. HANDLING AND ASSEMBLY RECOMMENDATIONS

Detailed recommendations concerning 3D PLUS Modules storage and assembly conditions are available in **[AD1]**. Module assembly on board must follow reflow guidelines as defined at:

https://www.3d-plus.com/customer-service/#assembly_recommendation.

17.1 PACKING

Modules are packed in antistatic boxes.

Each box is sealed with antistatic bag under vacuum with desiccant sachet.

Each packing is marked at least with:

- 3D PLUS Logo
- Module description: CASPEX 1.3M SWIR – 1.3 MPixels SWIR Space Camera Head
- Module P/N: 3DCM0880-1
- Quantity

17.2 HANDLING

3D PLUS modules must be handled with antistatic gloves and ESD wrist strap. The use of tools that could damage sides of components is prohibited.

The module thermal drain when being handled must be tied to ground to allow discharge. It is recommended to handle the module under ionizing flux.

Refer to [AD1] for details.

17.3 GROUNDING

Electrical ground and mechanical ground of the CASPEX 1.3M SWIR Space Camera Heads are not connected internally to the same potential.

It is recommended to connect the metallic cradle, thermal drain and mechanical pins of the module to non-floating potentials of the instrument/spacecraft (electrical or mechanical ground) through fixation screws or soldering on the PGA pins interface.

The thermal drain is internally connected by a 1 MΩ isolation resistor to the internal electrical ground of the camera head.

17.4 STORAGE

3D PLUS recommends to store the modules in dry environment (dry sealed bags, dry cabinet) for a better use of its products. Refer to [AD1] for details.

17.5 MODULE ASSEMBLY

After sealed bag opening, 3D PLUS modules have to be baked 24 hours at 125°C. The maximum storage duration under environmental conditions ≤ 30°C and < 60% RH is 6 hours. Beyond 6 hours, a new 24-hour bake at 125°C has to be performed on modules.

The use of any adhesive tape (e.g. Kapton®) on the side of the module during assembly is prohibited.

Recommendation for module assembly is to use flex-rigid PCB to avoid hyperstaticity when fixed through the top mechanical interface. Module assembly on board must follow guidelines described in [AD1].

Maximum body temperature must not exceed 183°C for a maximum exposure time of 4 s (measured at module side level.

Module cleaning after assembly must be done with isopropylic alcohol preferentially, or with de-ionized water otherwise. For other cleaning products, please consult 3D PLUS for further information.

Module reinforcement and coating operation are described in [AD1].

17.6 MECHANICAL ASSEMBLY

The mounting cradle material is AW-7175-T7351.

The recommended screws for assembly are A2 grade 70 property class, with a threaded length of 4 mm inside the cradle (4 screws). The minimum threaded length of the holes inside the cradle is 4mm.

The recommended tightening torque is Cs = 86 cN.m **(TBC)**

(Pretension load = 1378N (0.7 safety coefficient), friction coefficient μ = 0.15) **(TBC)**

17.7 ELECTROSTATIC DISCHARGE SENSITIVITY

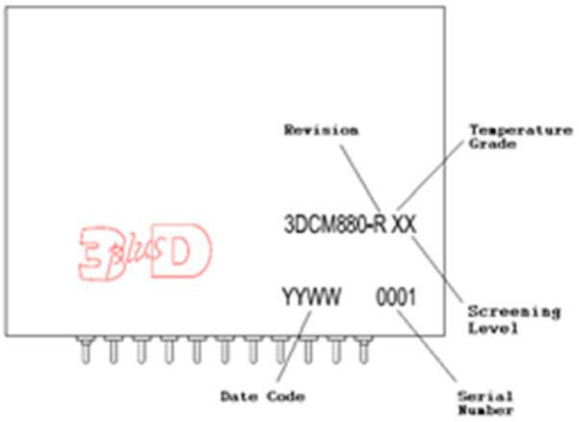
In order to avoid ESD damage and to guarantee reliable assembling of the CASPEX 1.3M SWIR Space Camera Head, ESD protections methods have to be applied.

Human Body Model (1B Class) and Charged Device Model (C4 class) is 1000 V.

18. ORDERING INFORMATION

The CASPEX 1.3M SWIR Space Camera Head is available with a combination of Temperature Ranges and Screening Levels to serve a broad range of applications and customers' requirements:

- «SB» Quality Grade to address Engineering Models,
- «SS» Quality Grade to address Flight Models.



3DCM880-1 X X

Temperature range

S = (-55°C to +70°C)
F = (-40°C to +70°C)

Screening level

B = Industrial grade
S = Space Grade

A Specific Source Control Drawing (SCD#) referenced in [AD1] is available for the space qualified product and shall be used for its procurement.

19. REVISION HISTORY

ED./REV.	DATE (DD/MM/YYYY)	DESCRIPTION
1	07/01/2025	Revision 1.0 Datasheet : - Creation for 3DCM880-1 modules equipped with long thermal drain - replacing 3DCM830-1 with short thermal drain. - Integrating new Family name CASPEX in the document

Table 31: Revision history