## 2.7 Hardware-Based Protection

The bq40z50-R2 device has three main hardware-based protections—AOLD, ASCC, and ASCD1,2—with adjustable current and delay time. Setting ***AFE Protection Configuration[RSNS]*** divides the threshold value in half. The ***Threshold*** settings are in mV; therefore, the actual current that triggers the protection is based on the $R_{SENSE}$ used in the schematic design.

In addition, setting the ***AFE Protection Configuration[SCDDx2]*** bit provides an option to double all of the SCD1,2 delay times for maximum flexibility towards the application's needs.

For details on how to configure the AFE hardware protection, refer to the tables in *Appendix A*.

All of the hardware-based protections provide a Trip/Latch Alert/Recovery protection. The latch feature stops the FETs from toggling on and off continuously on a persistent faulty condition.

In general, when a fault is detected after the ***Delay*** time, the CHG and DSG FETs will be disabled (Trip stage), and an internal fault counter will be incremented (Alert stage). Since both FETs are off, the current will drop to 0 mA. After ***Recovery*** time, the CHG and DSG FETs will be turned on again (Recovery stage).

If the alert is caused by a current spike, the fault count will be decremented after ***Counter Dec Delay*** time. If this is a persistent faulty condition, the device will enter the Trip stage after ***Delay*** time, and repeat the Trip/Latch Alert/Recovery cycle. The internal fault counter is incremented every time the device goes through the Trip/Latch Alert/Recovery cycle. Once the internal fault counter hits the ***Latch Limit***, the protection enters a Latch stage and the fault will only be cleared through the Latch Reset condition.

The Trip/Latch Alert/Recovery/Latch stages are documented in each of the following hardware-based protection sections.

The recovery condition for removable pack (***[NR]*** = 0) is based on the transition on the $\overline{\text{PRES}}$ pin, while the recovery condition for embedded pack (***[NR]*** = 1) is based on the ***Reset*** time.

#### 9.2.2.1.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ40Z50-R2 device. Select the smallest value possible to minimize the negative voltage generated on the BQ40Z50-R2 $V_{SS}$ node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor.

The BQ40Z50-R2 ground scheme is different from that of the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the $R_{SENSE}$ resistor pad. In the BQ40Z50-R2 device, however, it connects the low-current ground on the SRP side of the $R_{SENSE}$ resistor pad close to the battery 1N terminal (see *Section 9.2.2.1.3*). This is because the BQ40Z50-R2 device has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.

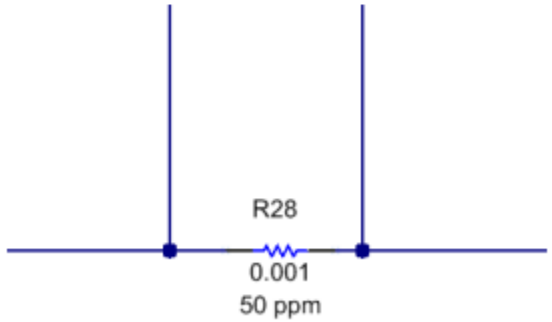


**Figure 9-5. Sense Resistor**

We have two parallel 3w m2Ω as a sense resistor

If you have two **parallel resistors** with the same value of $0.002\,\Omega$ (2 mΩ), their **effective resistance** ( $R_{\text{eff}}$) is halved because resistors in parallel combine as follows:

## Formula for Parallel Resistors:

$$R_{\text{eff}} = \frac{R_1 \times R_2}{R_1 + R_2}$$

For two identical resistors ($R_1 = R_2 = 0.002\,\Omega$):

$$R_{\text{eff}} = \frac{0.002\,\Omega \times 0.002\,\Omega}{0.002\,\Omega + 0.002\,\Omega} = \frac{0.002}{2} = 0.001\,\Omega\,(1\,\text{m}\Omega)$$

## New RSENSE Value:

- The effective sense resistance $R_{\text{eff}}$ is $1\,\text{m}\Omega$.

Default 0xF4 (hex)
- 1111 0100
- 0x0f 0x04
- 31ms -19.42mV

Update 0xF6 (hex)
- 1111 0110
- 0x0f 0x06
- 31ms -24.98mV

#### 15.9.10.5 Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | AOLD | Threshold | H1 | 0x0 | 0xFF | 0xF4 | Hex |

**Description**: ***AOLD:Threshold*** Setting
Bits 7–4: OLDD: AOLD delay time
Bits 3–0: OLDV: AOLD threshold

## A.1 Overload in Discharge Protection (AOLD)

### Table A-1. Overload in Discharge Protection Threshold (Settings:AFE:AFE Protection Control [RSNS] = 0)(1)

### A.1 Overload in Discharge Protection (AOLD)

| | |
|---|---|
| 0x06 | –24.98 mV |

### Table A-3. Overload in Discharge Protection Delay(1)

| | |
|---|---|
| 0x0F | 31 ms |

Default 0x77 (hex)
- 0111 0111
- 0x07 0x07
- 427µs 100mV

#### 15.9.11.5 Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | ASCC | Threshold | H1 | 0x0 | 0xFF | 0x77 | Hex |

**Description**: ***ASCC:Threshold*** Setting

Bits 7–4: SCCD: SCC delay time
Bit 3: Reserved
Bits 2–0: SCCV: SCC threshold

Default 0x72 (hex)
- 0111 0010
- 0x07 0x02
- 427µs 44.4mV

## A.2 Short Circuit in Charge (ASCC)

### Table A-4. Short Circuit in Charge Threshold (Settings:AFE:AFE Protection Control [RSNS] = 0)(1)

| | |
|---|---|
| 0x02 | 44.4 mV |

### Table A-6. Short Circuit in Charge Delay(1)

| | |
|---|---|
| 0x07 | 427 µs |

### 15.9.12.5 Thresholds 1 and 2

Default ASCD1 0x77 (hex)
- 0111 0111
- 0x07 0x07
- 427µs -100mV

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | ASCD | Threshold 1 | H1 | 0x0 | 0xFF | 0x77 | Hex |
| Protections | ASCD | Threshold 2 | H1 | 0x0 | 0xFF | 0xE7 | Hex |

**Threshold 1 Description**: ***ASCD:Threshold 1*** Setting
Bits 7–4: SCD1D–SCD1 delay time
Bit 3: Reserved
Bits 2–0: SCD1V: SCD1 threshold

**Threshold 2 Description**: ***ASCD:Threshold 2*** Setting
Bits 7–4: SCD2D–SCD2 delay time
Bit 3: Reserved
Bits 2–0: SCD2V: SCD2 threshold

Update ASCD1 0x72 (hex)
- 0111 0010
- 0x07 0x02
- 427µs -44.4mV

Default ASCD2 0xE7 (hex)
- 1110 0111
- 0x0E 0x07
- 854µs -100mV

Update ASCD2 0xE4 (hex)
- 1110 0100
- 0x0E 0x04
- 854µs -66.65mV

## A.3 Short Circuit in Discharge (ASCD1 and ASCD2)

**Table A-7. Short Circuit in Discharge Threshold (Settings:AFE:AFE Protection Control [RSNS] = 0)(1)**

| | | | | |
|---|---|---|---|---|
| ASCD1 | 0x02 | –44.4 mV | 0x07 | 427 µs |
| ASCD2 | 0x04 | –66.65 mV | 0x0E | 854 µs |

Updated:
AOLD: Latch Limit: 5
ASCD: Latch Limit: 3
ASCC: Latch Limit: 3

Other Parameters:
AOLD, ASCD, ASCC

Using Default:
Counter Dec Delay: 10secs
Recovery: 5secs
Reset: 15secs

Default:
AOLD: Latch Limit: 0
ASCD: Latch Limit: 0
ASCC: Latch Limit: 0