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Repeater Insertion in SFQ Interconnect

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***Abstract*—Superconductive passive transmission lines (PTL) are widely used for signal routing in large scale rapid single flux quantum (RSFQ) circuits. Due to the imperfect matching of the transmission lines between the driver and receiver, SFQ pulses are partially reflected. The round trip propagation time of these reflections can coincide with the following SFQ pulse, resulting in a decrease in bias margins or incorrect circuit behavior. This resonant effect depends upon the length of the PTL and the clock frequency of the signal. A methodology to reduce and manage this effect is the focus of this paper. A closed-form expression describing the dependence of the resonance frequency on the length of the PTL is presented. This expression describes a set of forbidden lengths for PTL interconnect segments in RSFQ circuits. The proposed methodology and algorithm insert active PTL-based repeaters into long superconductive interconnect while ensuring the length of the line segment is outside the forbidden region while increasing bias margins.**

***Index Terms*—Single flux quantum, electronic design automation, computer aided design, superconducting integrated circuits, superconductive digital electronics.**

I. Introduction

CONVENTIONAL integrated circuit technology is based on CMOS devices and standard copper interconnects. The scaling of CMOS technology, however, has significantly slowed in recent years. Advanced nanoscale fabrication facilities have become prohibitively expensive, and the energy consumption of CMOS circuits has greatly increased. An attractive alternative to advanced semiconductor technologies for large scale ultra-high speed and ultra-low power digital applications is Josephson junction (JJ) based digital superconductive circuits [1]. Superconductive IC technology has produced the highest performance digital circuits [2]. Rapid single flux quantum (RSFQ) is a widely used digital logic family within this promising superconductive technology. In RSFQ, information is represented in the form of single flux quantum (SFQ) pulses – picosecond wide voltage pulses with a quantized area. Recent research efforts suggest the use of this technology for high performance, energy efficient supercomputers to achieve DoE exascale computing objectives [3], [4].

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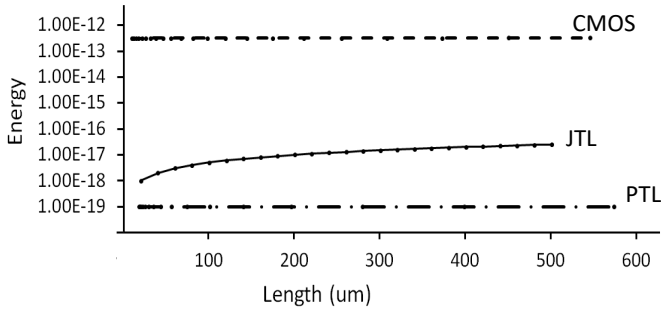

Fig. 1. Energy vs. interconnect length of 16 nm CMOS (dash line), SFQ JTL (solid line), and SFQ PTL (dash-dotted line) for 10 kA/cm^2 [6].

Some primary advantages of RSFQ circuits are high speed digital logic with low power dissipation, ideal (no DC resistance) interconnects, quantum accuracy, scalability, and relatively low manufacturing complexity [2]. SFQ circuits utilize two distinct types of interconnect - active Josephson transmission lines (JTL) and passive transmission lines (PTL), composed of a microstrip or a stripline with a matched driver and receiver [5]–[7]. A comparison of the energy dissipated by point-to-point interconnects for CMOS and SFQ is shown in Fig. 1. The energy of a 16 nm CMOS interconnect technology is evaluated with an RLC model [8]. The energy of the CMOS interconnect is approximately six orders of magnitude greater than the energy dissipated by a passive superconductive interconnect.

With only a modest number of researchers worldwide, significant progress in the design and manufacture of superconductive electronics has resulted in device densities of over 600,000 JJ/cm^2 [9]–[12]. Due to differences between SFQ and CMOS technologies, many electronic design automation (EDA) tools developed for CMOS can not be used for SFQ technology; however, general synchronization principles and techniques commonly used in CMOS are applicable to SFQ technology [13], [14]. Pulse-based logic in SFQ, different active and passive components, certain interconnect structures, and sub-terahertz clock frequencies present unique challenges in many stages of the SFQ circuit design process. Quantitative guidelines are needed to support the development of SFQ-based EDA tools. Combined with recent efforts to develop EDA tools for superconductive electronics [15], [16], the complexity of RSFQ circuits is expected to greatly increase.

One of the primary concerns of automated routing methodologies in integrated SFQ circuits is the interconnect characteristics. Specialized algorithms and guidelines in SFQ-based

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automated routing tools are needed to determine the optimal interconnect length for each line and driver/receiver configuration when propagating a signal along a passive interconnect [5], [17]–[21].

Due to the imperfect match between the driver and receiver, resonant effects occur in long PTL lines [22]–[24]. These effects are caused by the coincidence of the input SFQ pulse with the reflection of the previous pulse in a transmission line, and depends upon the characteristics of the PTL and the clock frequency of the input signal. In this paper, a methodology is proposed to manage and mitigate these effects.

In this paper, different types of SFQ interconnects are discussed in section II. A physical model of a PTL line is described in section III. The resonant effects of the PTL line which introduces a forbidden region of length, and a closed-form expression for the resonance behavior are presented in section IV. In section V, an algorithm is introduced to avoid resonance effects in long lines driven by a PTL repeater system. The paper is concluded in section VI.

II. SFQ SIGNAL ROUTING

Clock and data signals are distributed within an SFQ circuit to the SFQ sinks. To propagate a signal within the interconnect between RSFQ gates, JTLs or PTLs are typically used [17]. The JTLs in RSFQ interconnects consume power and add delay due to the additional JJs. Furthermore, the JTLs are placed within the standard cell layers, resulting in greater congestion. Although not a significant issue in current MSI RSFQ circuits, the greater power, delay, and area of a JTL pose a significant challenge in future VLSI RSFQ circuits.

A PTL is another type of SFQ interconnect, consisting of a superconductive microstrip [22], [25], [26] or a stripline, connected to a matched driver and receiver. The SFQ pulses ballistically propagate along a PTL at the speed of light within the medium. Utilizing PTLs rather than JTLs for long lines in VLSI RSFQ circuits reduces the output delay, power consumption, and congestion [18]–[20].

Many models for interconnect routing and delay estimation are utilized in conventional CMOS-based routing tools including inductively resonant networks [27]. Multiple techniques exist to reduce or increase the wire delay to achieve a target delay, such as wire sizing [28] and wire snaking [29]–[32]. Since the delay of a PTL with specific cross sectional dimensions for a target technology depends mostly on the line length, and the pulse propagation speed of a PTL approaches the speed of light in the medium, CMOS-like routing techniques are inappropriate for superconductive VLSI circuits. If necessary, pulses can be delayed by inserting JTL stages within the signal and clock lines. Impedance matching is required for both CMOS RF, microwave, and RSFQ transmission line interconnects. The unavoidable presence of reflections in SFQ transmission lines, however, is of greater concern than in CMOS due to the nonlinear behavior of JJs and the large impedance mismatch between a transmission line and the load JJ. The purpose of this paper is to introduce a routing methodology to mitigate the effects of these reflections on superconductive microstrip lines.

III. SFQ INTERCONNECT MODEL

A superconductive microstrip is a standard SFQ transmission line due to the simple geometry, adjustable size, and scalability. Based on the phase velocity of the transmission line, a resonance behavior occurs in a microstrip when the roundtrip time of the reflections coincides with the clock period of the signal. This behavior is related to the impedance characteristics of the line. The impedance characteristics and phase velocity of a microstrip are discussed in this section.

The structure of a superconductive microstrip is depicted in Fig. 2(a). The line consists of a superconductive strip on a dielectric substrate placed above a ground plane. Due to the London penetration depth λ of the superconductive material, the propagation of an SFQ signal slows, causing a delay of up to several per cent of the speed of light [33]. The interconnect is represented by a lossless distributed LC transmission line, which depends upon the interconnect length. L and C are, respectively, the inductance and capacitance per unit length.

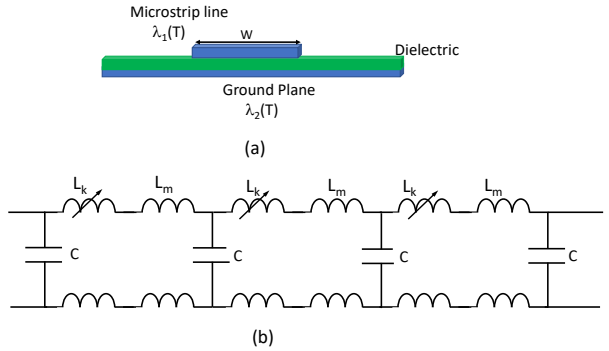

Fig. 2. Lossless superconductive transmission line, (a) microstrip, and (b) equivalent circuit.

An equivalent circuit of a superconductive transmission line is shown in Fig. 2(b). L_m is the magnetic inductance per unit length due to the magnetic flux within the superconductive line, and L_k is the kinetic inductance per unit length due to the motion of the paired electrons. The total inductance per unit length due to the contribution of the inductances, L_m and L_k, and the capacitance of a superconductive microstrip are [34], [35], respectively,

$$L = \frac{\mu_0 h}{Kw}[1 + \frac{\lambda_1}{h} coth(\frac{t_1}{\lambda_1}) + \frac{\lambda_2}{h} coth(\frac{t_2}{\lambda_2})] \quad , \tag{1}$$

$$C = \frac{\epsilon_0 \epsilon_r w}{h} \quad , \tag{2}$$

where w is the width of the superconductive microstrip, and t_1, t_2, and h are, respectively, the thickness of the microstrip, ground plane, and dielectric. λ_1 and λ_2 are, respectively, the penetration depth of the microstrip and ground plane. K is the fringing field factor [34], [36], [37]. The total inductance of a transmission line is proportional to the penetration depth; a deeper penetration depth produces a larger inductance.

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The kinetic inductance is an important factor reducing the phase velocity in microstrips. For a lossless line, the relative phase velocity is

$$v_{phase} = \frac{1}{\sqrt{LC}} \quad . \tag{3}$$

The phase velocity can be changed since the internal inductance is inversely proportional to the Cooper pair density [38].

IV. Frequency dependence of PTL interconnect

An important property of superconductive passive transmission lines is the resonance effects produced when the reflections of the SFQ signal from the receiver or driver coincide with an input SFQ pulse. The effects of the frequency of the SFQ signals on the optimal length of a microstrip transmission line are discussed in this section.

An analysis of the lower bias margin for a PTL including the driver, transmission line, and receiver is presented in Fig. 3. At a specific frequency, a lower bias margin of the PTL receiver is determined for different interconnect lengths. A PTL is evaluated as a lossless transmission line with a characteristic impedance of 8 ohms. In this figure, the dependence of the bias margins of the receiver [5] on the PTL length is depicted. The set of resonance lengths of a PTL system depends on the clock frequency of the applied SFQ signal which peaks at the lowest margins, see Fig. 3. When the effective line length is a multiple of half of a wavelength, a resonance occurs. The relationship between the resonant frequencies and the length of an interconnect line is

$$f_{resonance} = \frac{nv_{phase}}{2L_l} \quad , \tag{4}$$

which is directly related to the phase velocity of the interconnect. L_l is the physical length of the PTL interconnect, and n is an integer multiplier that determines the harmonic of the resonance frequency.

By considering an applied frequency as the resonance frequency for an imperfectly matched transmission line, a closed-form expression for the resonance length of a PTL line is determined. The resonance frequency and resonance length for a given impedance depend upon the fabrication characteristics and are an integer multiple of the primary resonance frequency. The resonance effect in a PTL with a single JJ receiver [5] is depicted in Fig. 3. The impedance of a lossless transmission line for the 10 kA/cm^2 technology is based on the MIT Lincoln Laboratory SFQ5ee fabrication process [6], [7]. The resonance behavior of the interconnect at 20 GHz occurs at 2.9 mm (see Fig. 3).

To determine the harmonics of the resonance frequency, the Fourier transform of an SFQ pulse is required. An SFQ pulse can be approximated by a Gaussian pulse [39],

$$V(t) = V_0 exp(-\frac{t^2}{2s^2}) \quad , \tag{5}$$

where s is the standard deviation. The Fourier transform of this pulse is

$$V(\omega) = (2\pi)^{\frac{1}{2}} s V_0 exp(-\frac{1}{2}\omega^2 s^2). \tag{6}$$

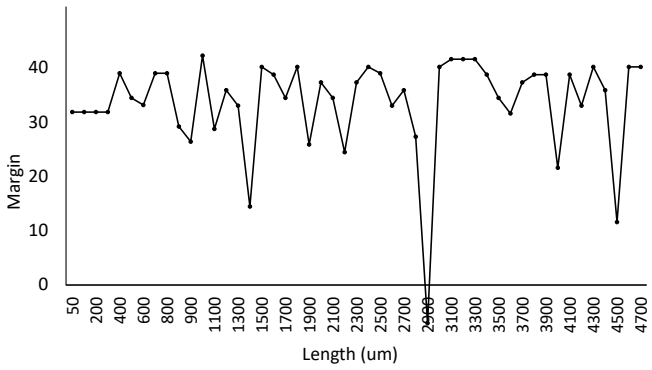

Fig. 3. Resonance effect in a lossless superconductive transmission line at 20 GHz (for the 10 kA/cm^2 technology [6]).

Note that the frequency spectrum of an SFQ pulse is also Gaussian. Harmonic frequencies of the SFQ pulse are derived from (6), which correspond to the resonant frequencies and lengths, as described by (4).

The dependence of the lower bias margins of the receiver [5] on the length of the PTL line is shown in Fig. 4 for two different frequencies of the input SFQ signal – 20 and 40 GHz. The first sharp decrease in bias margins at 40 GHz (the dashed line) occurs at 1.35 mm, a second decrease occurs at 2.9 mm. The first resonance length is approximately half of the second resonance length. The second resonance length at 40 GHz occurs at the same length as the first resonance effect at 20 GHz, consistent with (4). These resonance behaviors affect the bias margins and can cause a circuit to not function properly. Changing the impedance of the PTL line slightly shifts the resonance peak, but preserves the general trend.

The dependence of frequency on the first forbidden length of a PTL is shown in Fig. 5. The precise resonance length depends upon the fabrication technology and PTL impedance, and the trend is consistent with experimental results [40]. At low frequencies, the resonance occurs in extremely long lines. In these cases where the lines are supplied with a low frequency signal, correct operation is preserved as the resonance peak occurs in longer lines. For high frequency lines due to the shorter resonance length, additional constraints on the PTL interconnect exist.

An unsafe region X for a given resonance length is the region of line length in which the circuit operates incorrectly and resonance behavior occurs. This unsafe region is determined by the width of the resonance peaks (see Fig. 4), width and shape of the reflected pulse, technology characteristics, and overlap of the SFQ data pulse with the reflected pulse. In high frequency PTLs, multiple reflected pulses gradually accumulate. The shape of the accumulated reflections in a microstrip is uncertain, and depends upon the shape of the reflected SFQ pulse, round trip length of the PTL, and time of the reflections. The width of the unsafe region also depends upon the expected target margin for a PTL. A lookup table is therefore used for the bias margins for each PTL length and frequency for each receiver and driver pair in a cell library. Based on a margin analysis of a lossless transmission line, the forbidden region in this paper is approximately +10% of the

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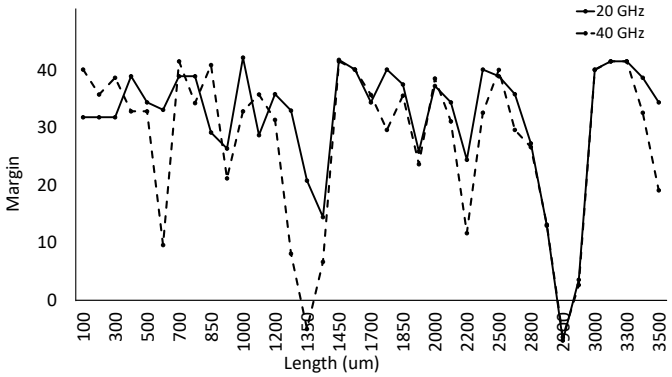

Fig. 4. Resonance effect in a lossless superconductive transmission line at 20 GHz and 40 GHz (for the 10 kA/cm^2 technology [6]).

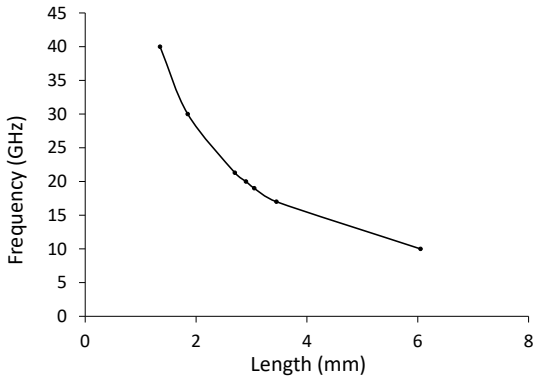

Fig. 5. Dependence of resonance frequency on the length of a PTL.

length due to the additional reflection delay of the JJ in the receiver.

For any frequency of an applied SFQ signal, a set of forbidden PTL lengths is produced, which corresponds to the main resonant length and harmonic multiples of this length. This set of forbidden lengths should be avoided. To prevent this resonance effect from affecting circuit operation, the length of a PTL segment is constrained to be shorter than the resonant length. Similar to conventional CMOS circuits, repeaters are inserted into these long transmission lines to partition the lines into shorter sections [41], [42]. A superconductive transmission line with and without repeaters is shown in Fig. 6. The repeaters are located to ensure that the length of each interconnect segment is outside the forbidden region.

V. Algorithm for Repeater Insertion in SFQ Interconnect

An algorithm is presented here to insert repeaters within PTL interconnect to prevent resonance effects in long PTL lines. The repeater insertion process is described in section V-A. An algorithm for inserting repeater in PTL interconnect is discussed in section V-B.

A. Problem definition

The problem of inserting repeaters in SFQ interconnect to minimize a target cost function is described in this subsection.

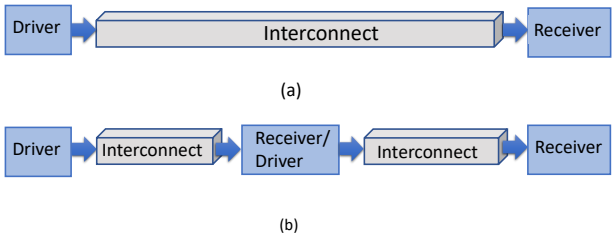

Fig. 6. SFQ interconnect, a) no repeater, and b) with repeaters.

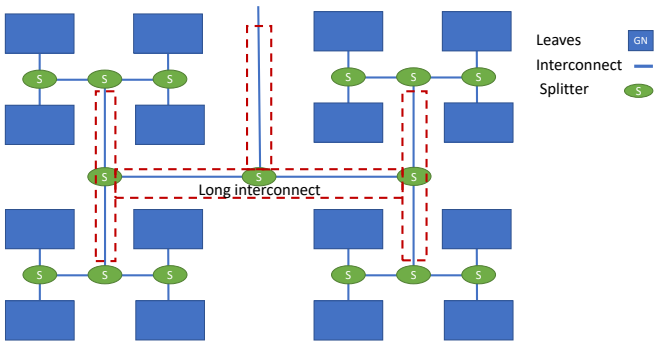

Fig. 7. An H-tree with n wires. The possible repeater positions are represented by the dashed rectangles.

An H-tree interconnect topology is shown in Fig. 7. The tree consists of h interconnect segments with multiple fanout. Each segment is connected between a driver and a receiver. The interconnect has n leaves, each leaf corresponds to one of the sinks of the tree. At each sink $1 \leq i \leq n$, the propagation delay t_{di} is the path delay from the source to the sink i of the tree. The delay of a PTL consists of the propagation delay of the PTL line and the input-to-output delay of the receiver and driver. Increasing the number of repeaters increases t_{di}. Within a tree, there are m interconnect segments which may require a repeater, where $0 \leq m \leq h$ and the repeaters are inserted to minimize a given cost function. An example of possible repeater positions for a long line is represented by the dashed rectangles shown in Fig. 7.

The repeater insertion process determines the number of repeaters j and length of partitions $l_{m(j+1)}$ that minimize a cost function C (l_{11}, l_{12}, $l_{1(j+1)}$, l_{21}, l_{22}, $l_{2(j+1)}$, ..., l_{m1}, l_{m2}, $l_{m(j+1)}$). $l_{m(j+1)}$ is the length of each interconnect partition within an interconnect segment m. The length of the partition is in the range $l_{min} < l_{j_m} < l_{int_m}$ where l_{int_m} is the length of the original interconnect segment without repeaters. The minimum length l_{min} of a PTL interconnect is the length where a PTL is faster than a JTL [5].

B. Repeater insertion algorithm

The objective is to determine the optimal number of repeaters and length of segments in an interconnect by minimizing a target cost function with different weights for the metrics, such as the area, power, and delay. Pseudocode describing the algorithm is shown in Pseudocode 1. The algorithm starts

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with zero repeaters, j_h = 0, in each of the interconnect segments, corresponding to an initial tree without repeaters. To determine the m possible positions of the repeaters, the length of the interconnect segments is compared to the first resonance length and the related forbidden region. If the length of an interconnect segment is longer than the first resonance length, this segment is a possible position for a repeater; otherwise, no repeater is required in this segment. The first resonance length longer than the length of an interconnect segment determines the largest number of harmonics N. From (4) and the lookup table, a set of resonance interconnect lengths l_{r_N} and frequency harmonics of the interconnect f_{r_N} are determined for $N \geq 1$. If $l_{r_N} \leq l_{max_m} \leq Xl_{r_N}$, repeaters are inserted into this interconnect segment. Otherwise, no repeaters are inserted within this segment. An interconnect segment without repeaters provides the lowest cost, and the number of repeaters remains zero. These interconnects are labeled to indicate that no repeaters should be inserted.

If the number of harmonics N is odd, the interconnect segment is split into two parts with equal lengths. If the number of harmonics N is even, the interconnect section is divided into two parts corresponding to the length outside the forbidden region, and the number of repeaters is j_m = 1. In this paper, 30% and 70% of the total length of a segment are arbitrarily selected to demonstrate the algorithm. For these harmonics, the halfway length falls within the forbidden region. The algorithm iterates until all m possible repeater positions are evaluated. During each iteration of the algorithm, the length of the interconnect segments and resonance lengths are scanned to determine the number and position of the repeaters that decrease a target cost function. The iterations are repeated until there is no change in the number of repeaters as compared to the previous iteration.

C. Application of algorithm to long PTLs

Repeaters can be inserted into an SFQ interconnect composed of PTL lines and splitters, such as a clock network. An example structure of a clock network is depicted in Fig. 7. The topology of the clock distribution network is an H-tree network.

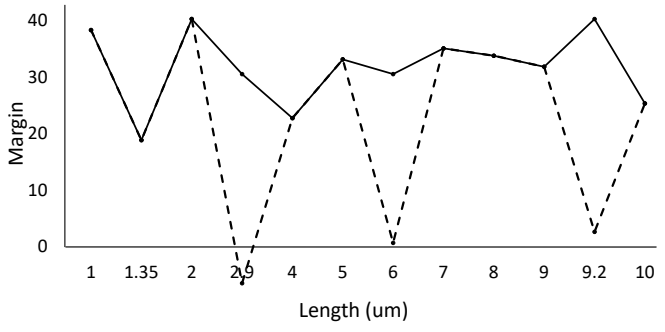

Fig. 8. The effect of resonance on the bias margins of a receiver in a lossless PTL at 20 GHz with (solid line) and without (dashed line) repeaters.

Pseudocode 1 Pseudocode of algorithm for inserting repeaters into an interconnect line.

Input: Number of interconnect segment h, length of interconnects, frequency, number of repeater $j = 0$, inductance and capacitance of a superconductive micro stripline,

Output: Definition file

Calculate phase velocity in microstrips by $v_{phase} = \frac{1}{\sqrt{LC}}$
Calculate a set of resonance length of interconnect by $l_{rN} = \frac{nv_{phase}}{2f}$;
Determine number of repeater in m possible position of interconnect;
Determine largest number of harmonics N;
INT = Write (l_m)
for $l_m \; in \; l_{r_N} \leq l_m \leq Xl_{r_N}$ **do**
  if N *is odd* **then**
    $l_{m1,2} = \frac{l_m}{2}$
    INT$_{lm}$ = Write ($l_{m1,2}$)
  if N *is even* **then**
    $l_{m1} = 0.3l_m$, $l_{m2} = 0.7l_m$;
    INT$_{lm}$ = Write ($l_{m1,2}$);
    j=j+1;
  if $Xl_{r_N} \leq l_m \leq Xl_{r_{N+1}}$ **then**
    Go step 15
Determine delay and margin;
Cost = Write (delay, margin)
$Definitionfile \leftarrow j, INT, Cost$

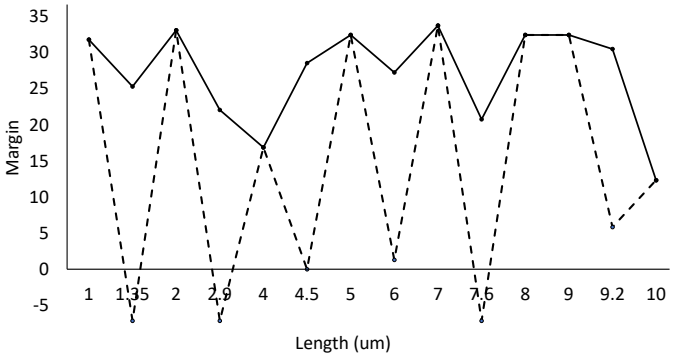

Fig. 9. The effect of resonance on the bias margins of a receiver in a lossless PTL at 40 GHz with (solid line) and without (dashed line) repeaters.

Assuming a lower margin for the receiver, the algorithm is applied to a PTL line with different lengths and frequencies to determine the minimum number of repeaters. Any resonance effects in the PTL interconnect at 20 GHz and 40 GHz (for a 10 kA/cm^2T technology) are depicted, respectively, in Figs. 8 and 9 without (dashed line) and with repeaters (solid line).

A lower margin of the receiver for different lengths is listed in Tables I and II. The results of the algorithm are compared with interconnect without repeaters and depict the improvement in bias margins of an interconnect due to the inserted repeaters.

The first resonant length of the interconnect occurs at 1.35 mm and 2.9 mm at, respectively, 40 GHz and 20 GHz.

The resonant behavior of the interconnect results in incorrect operation, where an SFQ pulse cannot pass through the interconnect. Since N is an odd number, this interconnect is divided into two equal parts, improving the bias margins to approximately 25%. This improvement is obtained for all odd harmonics, as listed in Tables I and II.

A 6 mm PTL line exhibits a resonance behavior at both 20 GHz and 40 GHz. This forbidden region corresponds to the second and fourth harmonic of the resonance frequency at, respectively, 20 GHz and 40 GHz. When one repeater is inserted, splitting the interconnect segment into two equal length PTLs, the length of these lines is within the forbidden region. When the interconnect section is divided into two parts, corresponding to 30% and 70% of a 6 mm line, correct functionality with wide bias margins and low delay is observed. The advantages of the algorithm (improved functionality with wider margins) are demonstrated on multiple examples of resonant frequency harmonics, see Tables I and II.

VI. Conclusions

Interconnects for prospective large scale RSFQ circuits are a significant issue in the automated routing of high speed integrated SFQ circuits. The interconnect and clock frequency produce resonance effects in superconductive transmission lines. A methodology for inserting PTL-based repeaters into superconductive interconnects is proposed to prevent resonance effects in long PTL lines. These resonance effects produce constraints on the length (forbidden regions) which should be avoided. The proposed repeater insertion methodology improves bias margins while slightly increasing the area and delay of the interconnect. The proposed algorithm provides guidelines for EDA tools and enables routing of robust, long superconductive interconnects.

TABLE I
Tradeoffs among configurations for different interconnect segments, at 20 GHz.

Length of interconnect (mm)	Delay (ps)	Length of repeaters (mm)	Margin	Comments
1	15	–	-38%, +28%	No repeaters
1.35	18	–	-19%, +29%	No repeaters
2	23	–	-40%, +25%	No repeaters
2.9	–	–	–, +29%	No repeaters
2.9	40	1.45, 1.45	-22%, +26%	Equal repeater lengths
4	36	–	-22%, +24%	No repeaters
5	47	–	-33%, +25%	No repeaters
6	–	–	-0.6%, +30%	No repeaters
6	65	3, 3	-6%, +25%	Equal repeater lengths
6	65	1.8, 4.2	-30%, +25%	Different repeater lengths
7	63	–	-35%, +25%	No repeaters
8	71	–	-34%, +25%	No repeaters
9.2	–	–	-2%, +27%	No repeaters
9.2	90	4.6, 4.6	-40%, +25%	Equal repeater lengths
10	87	–	-25%, +25%	No repeaters
13	111	–	-35%, +25%	No repeaters

TABLE II
Tradeoffs among configurations for different interconnect segments, at 40 GHz.

Length of interconnect (mm)	Delay (ps)	Margin	Comments
1	15	-32%, +27%	No repeaters
1.35	–	–, +27%	No repeaters
1.35	27	-25%, +25%	Equal repeater lengths
2	23	-33%, +25%	No repeaters
2.9	–	–, +27%	No repeaters
2.9	40	-22%, +25%	Different repeater lengths
4.5	–	–, +27%	No repeaters
4.5	53	-28%, +25%	Equal repeater lengths
5	47	-32%, +25%	No repeaters
6	–	–, +27%	No repeaters
6	65	-27%, +24%	Different repeater lengths
7	73	-33%, +25%	No repeaters
7.6	–	–, +27%	No repeaters
7.6	77	-21%, +25%	Equal repeater lengths
8	71	-32%, +28%	No repeaters
9	79	-32%, +25%	No repeaters
9.2	–	–, +27%	No repeaters
9.2	90	-30%, 25%	Different repeater lengths
10	87	-15%, +25%	No repeaters

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