SP&R: Simultaneous Placement and Routing framework for standard cell synthesis in sub-7nm

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Abstract— Standard cell synthesis requires careful engineering approaches to ensure routability across various digital IC designs since physical design (PD) for sub-7*nm* technology nodes demands holistic efforts to address urgent and nontrivial design challenges. The smaller number of routing tracks and more complex design rules due to the sophisticated multi-patterning technology make place-and-route (P&R) for designing a standard cell extremely hard and time-consuming. Many conventional approaches have been suggested for improving transistor-level P&R and pin accessibility, nonetheless insufficient because of the heuristic/divide-and-conquer manners.

In this paper, we propose a novel framework, *SP&R*, which simultaneously solves P&R for designing standard cell's layout without deploying any sequential procedures (between place and route steps) by using dynamic pin allocation-based cell synthesis. The proposed *SP&R* utilizes the Optimization Modulo Theories (OMT), an extension of the Satisfiability modulo theories (SMT), to obtain optimal standard cell layout by virtue of SAT (Boolean Satisfiability)-based fast reasoning ability. We validate that our SP&R framework achieves 10.5% of reduction on average in terms of metal length compared to the sequential approach, through practical standard cell designs targeting sub-7*nm* technology nodes.

I. Introduction

Standard cell synthesis has become a critically challenging problem because technology nodes of the integration process are continuously shrinking below 7*nm*. In sub-7*nm* technology nodes, the gap between the device and metal pitches becomes larger, thus the number of routing tracks becomes smaller. As a result, the conditional design rules introduced by sophisticated multiple-patterning technologies such as LELE (litho-etch-litho-etch), SADP (self-aligned double patterning) and SAQP (self-aligned quadruple patterning) are getting more complex than before [1]. The standard cell layout design procedure can be described by three items: (1) Transistor-level placement, (2) in-cell routing among the transistors, and (3) pin-accessibility optimization for PD.

Due to the complex design rules, standard cell synthesis has complicated constraints to achieve a high-performance cell layout. Since exploring an optimal layout has enormously large search space introduced by highly-combined complicated constraints of transistor-level placement, in-cell routing, and pin-accessibility improvement, the given problem is nontrivial and critically challenging. On top of the discussed difficulties above, most of previous works focus on the divide-and-conquer-style sub-problems and/or heuristic approaches of the standard cell layout problem, limiting the solution space and optimality (e.g., transistor-level placement, in-cell routing, pin-accessibility, etc.).

For transistor-level placement problem, many approaches have been proposed to reduce the solution space by adopting heuristic approaches such as "Eulerian trail" [2] and "Branch and Bound" [3]. For in-cell routing problem, several approaches based on conventional "Maze Routing algorithm" [4], [5] are suggested but inapplicable to recent multi-pattern technologies. Recently, SADP-aware optimized routing solution has been presented [6]. Due to the complex design rule in recent sub-7*nm* technology, several approaches propose pin-accessibility optimization techniques to improve pin-accessibility [7], [6]. However, these approaches for solving sub-problems are hard to reach the optimal solution of standard cell layout because of the intractable solution space partitioning and the intrinsic limitation of heuristic methodology.

For full automation of standard cell layout design, a few [8], [9] approaches which cover transistor-level placement and in-cell routing together are reported. However, these approaches are not suitable for the multiple-patterning technologies in sub-7*nm*. Recently, a sub-7*nm* applicable standard cell synthesis automation framework has been proposed [10], [11]. However, the framework includes the sequential/heuristic approaches in place-and-route phase as well.

Recently, several SMT (Satisfiability modulo theories) solvers including the optimization methodology (i.e., OMT) are released [12], [13]. SMT is more expressive language containing non-Boolean variables (e.g., integer, bit-vector, etc.) and predicate symbols as described in [14]. Based on the fast reasoning ability of SAT, SMT methodology empowers us to represent the given standard cell layout design problem with much richer modeling language.

In this paper, we propose a novel framework that Simultaneously attacks Place-and-Route (SP&R) of standard cell layout with an innovative lever, dynamic pin allocation (DPA) scheme which enables a simultaneous P&R optimization without deploying any sequential procedures (between place-and-route steps). Our framework SP&R utilizes the OMT (optimization modulo theories)-included SMT solver [12] to achieve optimal standard cell layout compared to conventional approaches such as ILP-based methods.

The main contributions of this paper are listed as follows:

- We propose an efficient framework SP&R that simultaneously solves place-and-route (P&R) optimization problem. We devise an innovative dynamic pin allocation

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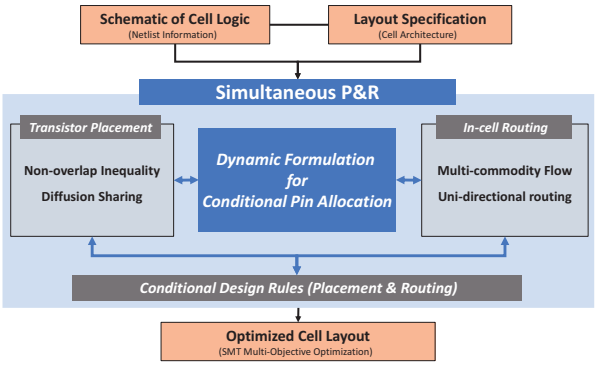

Fig. 1. An overview of SP&R framework.

(DPA) scheme to integrate placement and routing steps into a single optimization procedure.

- SP&R utilizes an OMT (Optimization modulo theories) feature equipped a state-of-the-art SMT (Satisfiability modulo theories) solver in multi-objective optimization, capable of SAT-based fast reasoning.
- SP&R covers a wide variety of conditional design rules for DFM, e.g., multiple-patterning techniques, resulting in routability-aware and pin-accessibility-aware layouts.
- We demonstrate our method's feasibility on the 7nm cell architectures, indicating practical applicability.

The remaining sections are organized as follows. Section II describes our SP&R framework. Section III discusses our experimental results. Section IV concludes the paper.

II. SP&R: Simultaneous Place & Route

In this section, we describe the detailed functionalities of SP&R: (i) Overview of SP&R; (ii) Cell Architecture; (iii) Combination of Multiple Objectives; and (iv) SMT Formulation.

A. Overview of SP&R

We adopt the state-of-the-art *lazy* approach SMT solver *Z3* to solve the given optimization problem. Fig. 1 shows an overview of the proposed SP&R framework. Given netlist information and cell architecture, our SP&R framework executes both transistor placement and in-cell routing concurrently with various design rule violation (DRV) check through the conditional design rule formulation. Combination of placement and routing is achieved by our novel dynamic formulation for conditional pin allocation (i.e., DPA scheme). The notations are shown in Table I.

B. Cell Architecture

Our framework employs the 7nm ASAP7 standard cell architecture (e.g., the layer/track information) [15], [10] and netlist information of [16] in generation of our practical cell examples as depicted in Fig. 2. Inspired by [17], [18], we adopt supernodes to cover the multiple candidates for each pin which is either the pin of FET (i.e., internal pin) or the I/O pin of standard cell (i.e., external pin).

Layout Configuration. We define the grid-based placement and routing graph composed of four metal layers (i.e., TS/PC, $M0$, $M1$, and $M2$) and each layer is defined as uni-directional edges. In practice, the metal elements in $M2$ layer are minimally used for the routing because the upper layers

TABLE I
Notations for the SP&R framework.

Term	Description
T	Set of FETs
t	t^{th} FET
x_t	X coordinate of lower-left corner of t
w_t (or h_t)	Width (or height) of t
P^t	Set of internal pins in t
p_i^t	i^{th} pin of t
$n(p)$	Net information of pin p
$G(V, E)$	Three-dimensional (3D) routing graph
V	Set of vertices in the routing graph G
V_i	Set of vertices in i^{th} metal layer of the routing graph G
v	A vertex with the coordinate (x_v, y_v, z_v)
v_d	A d-directional adjacent vertex of v
$a(v)$	Set of adjacent vertices of v
$e_{v,u}$	An edge between v and u, $u \in a(v)$
$w_{v,u}$	Weighted cost for metal segment on $e_{v,u}$
N	Set of multi-pin nets in the given routing box
n	n^{th} multi-pin net
s^n	A source of n
D^n	Set of sinks in n
d_m^n	m^{th} sink of n
v^n	0-1 indicator if v is used for n
$e_{v,u}^n$	0-1 indicator if $e_{v,u}$ is used for n
$f_m^n(v,u)$	0-1 indicator if $e_{v,u}$ is used for commodity f_m^n
$m_{v,u}$	0-1 indicator if there is a metal segment on $e_{v,u}$
$C_m^n(v,u)$	Capacity variable for $e_{v,u}$ of commodity f_m^n
$g_{d,v}$	0-1 indicator if v forms d-side EOL of a metal segment

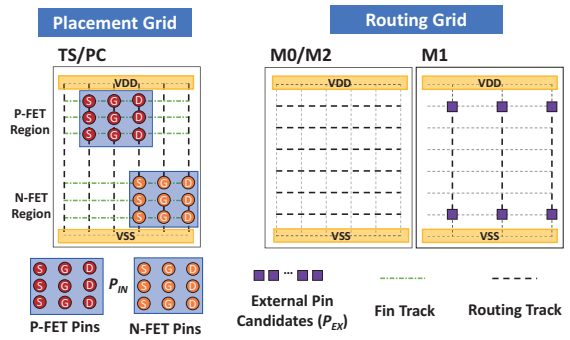

Fig. 2. Grid-based placement & routing graph.

of $M1$ are main resource for detailed routing (i.e., we set the weighted cost $w_{v,u}$ of $M2$ metal by four times higher than that of other metal layer.). In placement layer (i.e., TS/PC), there are three placement tracks (i.e., fin tracks) for transistor allocation in the corresponding pMOS (resp. nMOS) region. The upper layers of TS/PC (i.e., $M0/1/2$) are the routing tracks for the in-cell routing and each layer has 6 horizontal tracks.

Internal pin (P_{IN}) for FET. P_{IN} (i.e., source, drain, and gate of each FET) is defined in placement graph as described in Fig. 2. The position of each pin is dynamically selected by placement formulation (Section II-D1) and is connected to the pin layout for routing through our DPA scheme (Section II-D2).

External pin (P_{EX}) for I/O pin accessibility. P_{EX} is defined for representing the I/O pin of the standard cell. Our framework guarantees the pin accessibility of the optimized standard cell layout by defining the vertices (i.e., purple squares in Fig. 2) connected to P_{EX} in $M1$. The routed metals in $M1$ represent the I/O pin of standard cell layout for next procedures.

C. Combination of Multiple Objectives

The proposed SP&R minimizes both placement and routing objectives. The cell size can be defined as the maximum right corner of used resources (i.e., both transistors and routed metal elements) as represented in Expression (1) since we assume that the minimum of left corner and the number of placement track are always 0 and 6 in the 7*nm* cell architecture [15]. The total metal length is the weighted sum of routed metal segments as shown in Expression (2). Our SP&R comprehends multiple objectives by using "lexicographic" minimization (Expression (3)), a feature of OMT.

Placement (Cell Size) :

$$\max\left(\max\left\{x_t + w_t \mid t \in T\right\}, \max\left\{x_v, x_u \mid m_{v,u} = 1\right\}\right) \quad (1)$$

Routing (Total Metal Length) :

$$\sum_{e_{v,u} \in E} \left(w_{v,u} \times m_{v,u}\right) \quad (2)$$

LexMin : [1] Cell Size, and [2] Total Metal Length. (3)

With multiple objectives (i.e., cell size and total metal length), SP&R explores the optimal standard cell layout that satisfies complicated constraints defined in following sections.

D. SMT Formulation

On top of the efficient solving ability of SAT, SMT formula provides us to get the optimal standard cell layout through their OMT feature. Furthermore, SMT formula supports a much richer modeling language (e.g., a more expressive language that includes integer type variables and predicate symbols) than Boolean SAT formula. These key features of SMT accomplish exhaustive searching for the optimal solution with the efficient expression of constraints compared to the conventional ILP formula.

Our SMT formulation consists of four subsections, *(i) Placement Formulation*, *(ii) DPA* (*Dynamic Pin Allocation*), *(iii) Routing Formulation*, and *(iv) Design Rule Constraints*. All constraints are connected and concurrently executed in a single execution.

*1) **Placement Formulation**:* We utilize the conventional floorplanning design approaches (i.e., *Relative Positioning Constraint*) for the transistor placement problem. We only consider relative positioning in x coordinate because we restrict "both stacks" in each FET region (i.e., N-FET / P-FET) due to the limited number of fin tracks in sub-7nm. The efficient selection schemes for *Diffusion Sharing* and *Active-to-Active Rule* are also included to further enhance practicality of our framework. Especially, we consider "neighboring diffusion effect (NDE)" related to diffusion sharing [19]. For multi-finger selection scheme, our framework always chooses the minimum number of fingers according to the SP&R objectives (i.e., the minimization of cell size and metal length). The placement formulation is connected to the routing formulations through our novel DPA scheme (Section II-D2).

Relative Positioning Constraint (RPC). All transistor positions can be represented by four RPCs as shown in Expression (4).

$$\begin{aligned} \textbf{Right:}\quad & x_t \geq x_s + w_s, \\ \textbf{Left:}\quad & x_t + w_t \leq x_s, \end{aligned} \qquad \forall t, s \in T, t \neq s \quad (4)$$

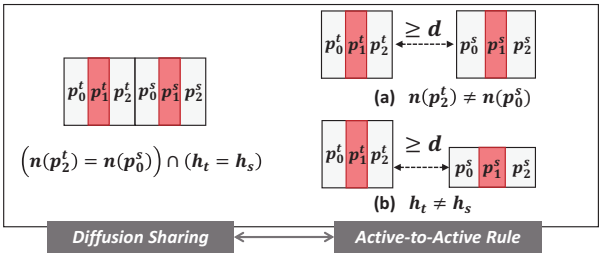

Fig. 3. Examples of DS and AA Rule. (a) Different net between the closest pins of two FETs. (b) Different heights between two FETs.

ALGORITHM 1: 1-D Relative Positioning Constraint with Diffusion Sharing (FET t, FET s)

if *t is on the right side of s without diffusion sharing* **then**
  $x_t \geq x_s + w_s + d$;
else if *t is on the right side of s with diffusion sharing* **then**
  $x_t = x_s + w_s$;
else if *t is on the left side of s without diffusion sharing* **then**
  $x_t + w_t + d \leq x_s$;
else if *t is on the left side of s with diffusion sharing* **then**
  $x_t + w_t = x_s$;
else
  Unsatisfiable condition ;
end

At least one of the two inequalities holds for each pair where $t \neq u$ through the SMT expression as described in Algorithm 1. These geometric conditions determine the position and the flip status of the transistor.

Diffusion Sharing (DS) and Active-to-Active (AA) Rule. DS is a common placement technique when the net information is the same between pins of different FETs. However, DS technique is not useful when the net information between the closest pins of two FETs is different (Fig. 3(a)) or two FETs have different heights (Fig. 3(b)). The distance between FETs t and s can be either 0 or larger than minimum distance d (d = 2 in our formulation) depending on DS & AA conditions as shown in Fig. 3 and Algorithm 1.

*2) **Dynamic Pin Allocation (DPA)**:* We devise a dynamical scheme for the conditional pin allocation as an interface between the placement and routing. In TS/PC layer, the placement tracks (grids) are not on grids of routing tracks. Thus, we need to determine a pin layout of TS/PC layer on routing grid to utilize our on-grid routing formulation as shown in Fig. 4. Routing formulation utilizes the dynamically-determined pin layout to achieve the optimal in-cell routing solution.

From Placement (Pin Allocation). Based on the transistor placement result from the placement formulation, we dynamically determine the pin layout on routing grid by controlling the flow capacity of each routing grid (edge). Each internal pin p has its own set of flow capacity variable $C_m^n(p, r)$ for all corresponding routing grids on TS/PC layer. The detailed control algorithm is shown in Algorithm 2. For certain net n and commodity m, $C_m^n(p, r)$ is set as 0 if the vertex r is not in the range of p.

For example, each internal pin (i.e., source/gate/drain) of Fig. 5(a), (b), and (c) has only two feasible vertices (blue circles) for pin access through the flow capacity control algorithm. All feasible sets of vertex r in TS/PC layer can

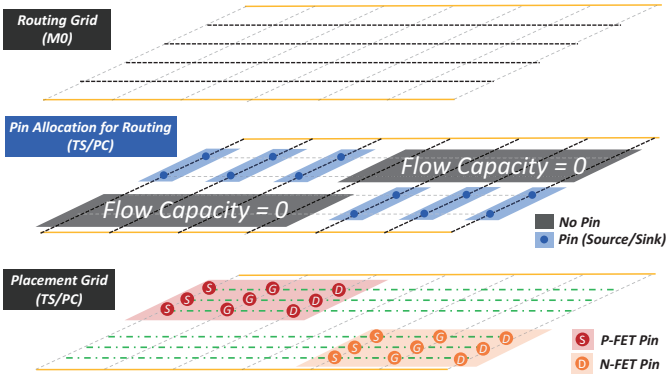

Fig. 4. Dynamical pin allocation using routing grid in TS/PC layer.

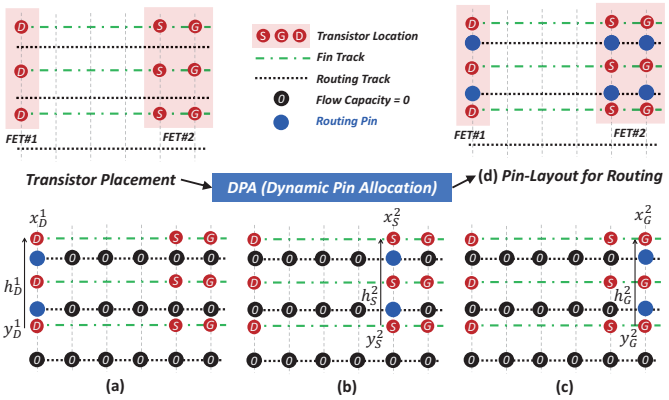

Fig. 5. An example of pin allocation through DPA. Capacity control for (a) drain pin of FET#1, (b) source pin of FET#2, and (c) gate pin of FET#2. (d) Selected pin-layout for routing.

ALGORITHM 2: Flow Capacity Control Constraint

/* X coordinate/Y coordinate of a routing grid r : x_r/y_r*/
/* Height/X coordinate/Y coordinate of a pin p : $h_p/x_p/y_p$*/
/* Single column pin only : Set of x is singleton*/
/* p is either source or sink of net n and commodity m */

if $(x_r \neq x_p) \quad \vee \quad (y_r < y_p) \quad \vee \quad (y_r > y_p + h_p)$ **then**
  $C_m^n(p,r) = 0$;
else
  $C_m^n(p,r)$ is determined by the Routing Formulation (CFC);
end

be either the source s^n or sink d_m^n in the routing formulation by connecting the flow capacity variable $C_m^n(p,r)$ to flow variable $f_m^n(v,u)$ as follow.

To Routing (Flow Capacity Connection). Expression (5) is the connection constraint between flow variable $f_m^n(v,u)$ (in Expression (6) of routing formulation) and flow capacity variable $C_m^n(p,r)$. Each $f_m^n(v,u)$ is less than or equal to $C_m^n(p,r)$ when vertex v is the internal pin p, and the adjacent vertex u is the adjacent vertex r of p in TS/PC (i.e., V_0). Thus, routing formulation can analyze the routability using only feasible sets of r in V_0 layer.

$$f_m^n(v=p, u=r) \leq C_m^n(p,r), \quad \forall r \in a(p),\ \forall r \in V_0 \tag{5}$$

By 0-1 manner of the flow capacity variable $C_m^n(p,r)$, the flow $f_m^n(v,u)$ is excluded when r is not located in the range of p. Thus, only feasible pin layout for each pin is dynamically determined for the in-cell routing as described in Fig. 5(d) (blue circles).

*3) **Routing Formulation**:* Our SP&R utilizes the conditional design rule-aware multi-commodity flow network theory for the in-cell routing problem as described in [17]. We reduce the solution search space in our formulation by using the uni-directional edges only. Compared to [17], constraints for *commodity flow conservation* and *exclusiveness use of vertex* are refined by adopting the undirected edge. Similar to the placement formulation, the routing formulation is also connected/controlled by the DPA formulation (Section II-D2) in concurrent way.

Commodity Flow Conservation (CFC). Expression (6) is the modified CFC constraint regardless of the flow direction. In case of source s^n or sink d_m^n, the summation of commodity flow indicator $f_m^n(v,u)$ between a certain vertex v and its adjacent vertices $a(v)$ is set as 1.

$$\sum_{u \in a(v)} f_m^n(v,u) = \begin{cases} 1, & \text{if } v = s^n, d_m^n \\ 2x, x = \{0,1\}, & \text{otherwise} \end{cases} \quad \forall v \in V,\ \forall n \in N,\ \forall d_m^n \in D^n \tag{6}$$

Vertex Exclusiveness. Constraint (7) ensures that there are no intersecting nets on any vertices except P_{EX}. For P_{EX}, Exactly-k constraint is set because the supernode of external pins should be shared as many as the number of P_{EX}.

$$\sum_{n \in N} v^n \begin{cases} = 1, & \text{if } v = P_{IN} \\ = \text{ the number of } P_{EX}, & \text{else if } v = P_{EX} \\ \leq 1, & \text{otherwise} \end{cases}, \quad \forall v \in V \tag{7}$$

When $v = P_{IN}, P_{EX}$, the only one edge indicator must be used as represented in Constraint (8) (i.e., exactly-one (EO) constraint).

$$v^n = \sum_{u \in a(v)} e_{v,u}^n, \quad v = P_{IN}, P_{EX}, \quad \forall n \in N \tag{8}$$

When $v \neq P_{IN}, P_{EX}$, we allow multiple use of edges against vertex v for a certain net. Constraint (9) is logically ORing all adjacent edges of the vertex v to preserve multi-commodity flows in the net.

$$v^n = \bigvee_{u \in a(v)} e_{v,u}^n, \quad v \neq P_{IN}, P_{EX}, \quad \forall n \in N \tag{9}$$

*4) **Design Rule Constraints**:* Our SP&R is performing metal-layer-aware optimization. The design rules of TS/PC layer are mainly related to the placement thus we apply placement-related design rules such as *DS (Diffusion Sharing)*, *AA (Active-to-Active)*, and *End-of-Line (EOL) Spacing* rule. For the other layers (i.e., $M0/1/2$), we also consider various conditional design rules such as *Minimum Area Rule (MAR)*, *End-of-Line Spacing Rule*, and *Via Rule* by utilizing the same methodology of [18]. Furthermore, our framework includes multi-pattern-aware design rules such as *Parallel Run Length (PRL) rule* and *Step Height Rule (SHR)* [20], [21]. To ensure the pin-accessibility of the cell layout, we consider the *Minimum I/O Pin Length Rule* as well.

PRL (Parallel Run Length) Rule. PRL rule is one of the important design rules to avoid "single-point-contact" in

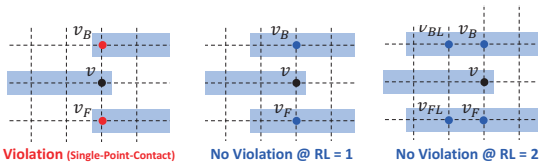

Fig. 6. An example of PRL.

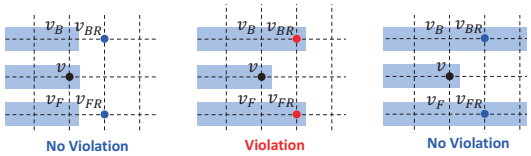

Fig. 7. An example of SHR @ Step Height = 2.

manufacturing SADP mask [21]. Fig. 6 and Constraint (10) represent the PRL rule and the corresponding formulation when run length (RL) is 2.

$$g_{R,v} + g_{L,v_B} + g_{L,v_{BL}} \leq 1; g_{R,v} + g_{L,v_F} + g_{L,v_{FL}} \leq 1, \forall v \in V_0, V_2 \quad (10)$$

SHR (Step Height Rule). SHR is a design rule to avoid "the small step" in manufacturing SADP mask [21]. Fig. 7 and Constraint (11) illustrate the SHR and the corresponding formulation when step height is 2.

$$g_{R,v} + g_{R,v_{BR}} \leq 1; \quad g_{R,v} + g_{R,v_{FR}} \leq 1, \quad \forall v \in V_0, V_2 \quad (11)$$

III. Experimental Result

The proposed SP&R (Simultaneous Place-and-Route) framework is implemented in *Perl/SMT-LIB* 2.0 standard-based formula and validated on a Linux workstation with 2.4GHz Intel Xeon E5-2620 CPU and 256GB memory. The multi-threaded SMT Solver *Z3* (version 4.8.5) is used to produce the optimized solution through the proposed SP&R formulation. SP&R generates the "design layout" file including the information for the transistors (i.e., FETs), nets (i.e., target nets for in-cell routing), and I/O pins (i.e., P_{EX}) by using schematic information of cell logic.

A. Sequential- vs. Simultaneous-P&R

Since SP&R exhaustively searches the solution in combined solution search space between placement and routing, our simultaneous optimization of P&R can guarantee optimal solutions with respect to multiple objectives (i.e., cell size and total metal length) by utilizing the lexicographic minimization. We compare our simultaneous approach to the conventional sequential optimization of P&R. To simulate sequential P&R of [10], we first find a placement with minimum cell size satisfying only the routing formulation described in Section II-D3. Then we find an optimized solution with respect to the total metal length of in-cell routing by utilizing all routability-related formulation (i.e., routing formulation and design rule constraints). Fig. 8 shows the difference in term of the metal length between SP&R and sequential approach. Through our DPA scheme, we can get the optimal standard cell layout with 239 metal length as shown in Fig. 8(b). Compared to the sequential approach (Fig. 8(a)), simultaneous approach reduces by 18.2% (292 → 239) of the metal length for in-cell routing. Furthermore, SP&R minimizes the number of

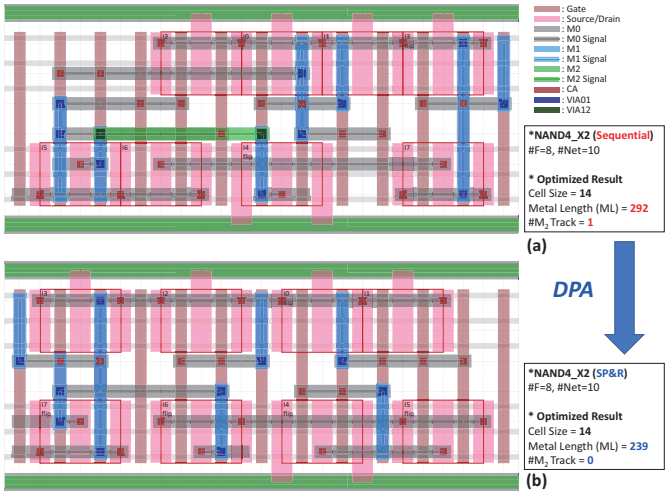

Fig. 8. The comparison between (a) sequential (ML = 292) and (b) simultaneous P&R (ML = 239) using NAND4_X2.

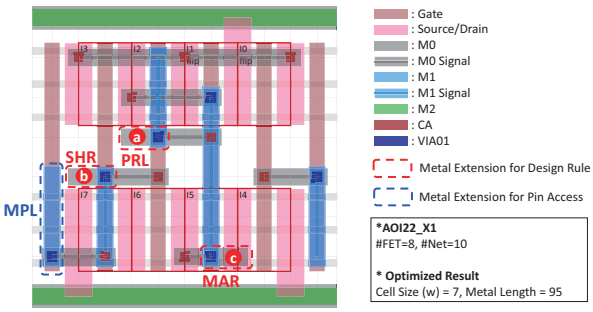

Fig. 9. An example of corrected cell layout for DFM and I/O pin-accessibility.

$M2$ track from 1 to 0. The minimal use of $M2$ tracks is an important goal of the standard cell synthesis because the minimal use of $M2$ resource can dramatically improve the routability in detailed routing procedure of PD.

B. Optimization for DFM and Pin-accessibility

Our SP&R implements various design rule constraints for DFM-aware cell layout automation. Fig. 9 shows an example of corrected cell layout generated by SP&R. All routed metal segments are successfully satisfying all pre-discussed conditional design rule constraints as depicted in Fig. 9[1]. The metals (a), (b), and (c) (red dashed region) are successfully extended to satisfy conditional design rule PRL, SHR, and MAR, respectively. The blue dashed region shows that the metal is extended for I/O pin accessibility.

C. Experimental Statistics

Table II presents our experimental results with respect to SMT formulation, cell layout optimization for 9 standard cells, and reference data of [10] for the comparison. As shown in Table II, SP&R reduces the metal length by 10.5% (18.2%) on average (best case) compared to sequential P&R. Moreover, SP&R reduces the number of consumed $M2$ tracks from 1.3 to 0.8 on average. SP&R obtains the optimal cell layout within 7 minutes for 8 out of 9 standard cells. For LHQ_X1 cell, the optimal cell layout is found within 24 minutes (T_O). In

[1]In this research, we attack a couple of the representative design rules. By virtue of on-grid nature of routing, the authors firmly believe that all other conditional design rules can be properly formulated and integrated.

TABLE II

EXPERIMENTAL STATISTICS: P&R = NUMBER OF VARIABLES AND CONSTRAINTS FOR PLACEMENT AND ROUTING RESPECTIVELY, DPA = NUMBER OF VARIABLE/CONSTRAINT FOR DPA(DYNAMIC PIN ALLOCATION), W = CELL WIDTH IN TRACKS, ML = TOTAL METAL LENGTH, M_2 = NUMBER OF USED M_2 TRACKS, ML IMPR. = ($ML_{sequential}$ - $ML_{simultaneous}$) / $ML_{sequential}$, T_O = EXECUTION TIME OF SP&R, T_D = TOTAL P&R EXECUTION TIME WITH OPTIMAL MANUFACTURABILITY OF [10] (I.E., $t3 + t5$ OF [10]). ALL TIME IS IN [MM:SS].

Cell Specification			SMT Formulation				Cell Layout Optimization								[10] (Sequential/ILP[2])				
Name	#FET	#Net	#Variable		#Constraint		Sequential P&R			Simultaneous P&R				ML					
			P&R	DPA	P&R	DPA	w	ML	M_2	w	ML	M_2	T_O	Impr.[%]	#	#FET	#Net	w	T_D
AOI22_X1	8	10	10,268	314	17,908	145	7	104	0	7	95	0	00:31	8.7	1	8	11	6	00:06
NAND4_X1	8	10	9,885	294	17,160	135	7	79	0	7	79	0	02:06	-	2	8	10	6	00:08
NAND4_X2	8	10	35,770	1,424	65,766	672	14	292	1	14	239	0	06:25	18.2	3	8	11	12	00:29
AOI22_X2	8	10	38,638	1,538	72,660	723	15	308	1	15	303	1	02:53	1.6	4	8	11	12	00:52
OAI22_X2	8	10	38,638	1,538	72,660	723	15	355	2	15	303	1	03:46	14.6	5	14	16	12	05:07
XOR2_X1	10	9	13,110	476	23,008	222	8	125	0	8	125	0	00:20	-	6	8	11	16	06:19
MUX2_X1	12	12	20,044	674	33,770	320	10	253	1	10	253	1	01:42	-	7	17	22	12	02:50
HA_X1	14	11	25,141	950	43,094	450	11	308	2	11	271	1	01:29	12.0	8	11	15	12	00:56
LHQ_X1	16	17	41,386	1,524	74,986	742	15	658	5	15	553	3	23:50	16.0	9	8	11	16	03:12
Average	10.2	11.0	22,613.6	838.0	40,624.9	395.6	11.3	275.8	1.3	**11.3**	**246.8**	**0.8**	**04:47**	**10.5**		10.0	13.1	11.6	02:13

SMT formulation, the number of variables and constraints with respect to P&R dominantly relies on the number of FETs and nets. The overhead of variables and constraints for DPA is about 3.7%, 1.0% on average of P&R variables and constraints, respectively. With small overhead, DPA successfully combines the placement and routing. The reference data of [10] represents the cell specification (i.e., #FET and #Net) and P&R result (i.e., w and T_D) of cells which have similar complexity with our standard cell examples. This demonstrates that our SP&R produces the optimal cell layout solution with reasonable time overhead.

IV. CONCLUSION

We have described our simultaneous placement and routing framework, a new standard cell design automation framework with the simultaneous place-and-route (i.e., DPA) scheme. SP&R provides fully automated optimal solutions for standard cell layout design through exploring the combined search space between placement and routing. We validate that the proposed SP&R is capable of generating the cell layout through the OMT feature of SMT solver for the practical standard cell examples, successfully avoiding DRVs.

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REFERENCES

[1] A. P. Jacob, R. Xie, M. G. Sung, L. Liebmann, R. T. Lee, and B. Taylor, "Scaling challenges for advanced cmos devices," *International Journal of High Speed Electronics and Systems*, vol. 26, no. 01n02, p. 1740001, 2017.

[2] X. Xu, N. Shah, A. Evans, S. Sinha, B. Cline, and G. Yeric, "Standard cell library design and optimization methodology for asap7 pdk," in *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 999–1004, IEEE, 2017.

[3] B. Taylor and L. Pileggi, "Exact combinatorial optimization methods for physical design of regular logic bricks," in *2007 44th ACM/IEEE Design Automation Conference*, pp. 344–349, IEEE, 2007.

[4] N. Ryzhenko and S. Burns, "Standard cell routing via boolean satisfiability," in *Proceedings of the 49th Annual Design Automation Conference*, pp. 603–612, ACM, 2012.

[5] C. J. Poirier, "Excellerator: custom cmos leaf cell layout generator," *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 8, no. 7, pp. 744–755, 1989.

[2]All experiments of [10] were executed on a single-threaded 2.20GHz Intel Xeon E5-2699 v4 machine and using CPLEX 12.6.

[6] W. Ye, B. Yu, D. Z. Pan, Y.-C. Ban, and L. Liebmann, "Standard cell layout regularity and pin access optimization considering middle-of-line," in *Proceedings of the 25th edition on Great Lakes Symposium on VLSI*, pp. 289–294, ACM, 2015.

[7] J. Seo, J. Jung, S. Kim, and Y. Shin, "Pin accessibility-driven cell layout redesign and placement optimization," in *2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC)*, pp. 1–6, IEEE, 2017.

[8] M. Guruswamy, R. L. Maziasz, D. Dulitz, S. Raman, V. Chiluvuri, A. Fernandez, and L. G. Jones, "Cellerity: A fully automatic layout synthesis system for standard cell libraries," in *Proceedings of the 34th annual Design Automation Conference*, pp. 327–332, ACM, 1997.

[9] A. M. Ziesemer and R. A. da Luz Reis, "Simultaneous two-dimensional cell layout compaction using milp with astran," in *2014 IEEE Computer Society Annual Symposium on VLSI*, pp. 350–355, IEEE, 2014.

[10] P. Cremer, S. Hougardy, J. Schneider, and J. Silvanus, "Automatic cell layout in the 7nm era," in *International Symposium on Physical Design*, pp. 99–106, ACM, 2017.

[11] Y.-L. Li, S.-T. Lin, S. Nishizawa, H.-Y. Su, M.-J. Fong, O. Chen, and H. Onodera, "Nctucell: A dda-aware cell library generator for finfet structure with implicitly adjustable grid map," in *Proceedings of the 56th Annual Design Automation Conference 2019*, p. 120, ACM, 2019.

[12] N. Bjørner, A.-D. Phan, and L. Fleckenstein, "νz-an optimizing smt solver," in *International Conference on Tools and Algorithms for the Construction and Analysis of Systems*, pp. 194–199, Springer, 2015.

[13] R. Sebastiani and P. Trentin, "Optimathsat: A tool for optimization modulo theories," in *International conference on computer aided verification*, pp. 447–454, Springer, 2015.

[14] C. Barrett and C. Tinelli, "Satisfiability modulo theories," in *Handbook of Model Checking*, pp. 305–343, Springer, 2018.

[15] V. Vashishtha, M. Vangala, and L. T. Clark, "ASAP7 predictive design kit development and cell design technology co-optimization," in *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 992–998, IEEE, 2017.

[16] M. Martins, J. M. Matos, R. P. Ribas, A. Reis, G. Schlinker, L. Rech, and J. Michelsen, "Open cell library in 15nm freepdk technology," in *Proceedings of the 2015 Symposium on International Symposium on Physical Design*, pp. 171–178, ACM, 2015.

[17] I. Kang, D. Park, C. Han, and C.-K. Cheng, "Fast and precise routability analysis with conditional design rules," in *Proceedings of the 20th System Level Interconnect Prediction Workshop*, p. 4, ACM, 2018.

[18] D. Park, I. Kang, Y. Kim, S. Gao, B. Lin, and C.-K. Cheng, "ROAD: Routability analysis and diagnosis framework based on SAT techniques.," in *ISPD*, pp. 65–72, 2019.

[19] C. Han, K. Han, A. B. Kahng, H. Lee, L. Wang, and B. Xu, "Optimal multi-row detailed placement for yield and model-hardware correlation improvements in sub-10nm vlsi," in *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 667–674, IEEE, 2017.

[20] X. Xu, B. Cline, G. Yeric, B. Yu, and D. Z. Pan, "Self-aligned double patterning aware pin access and standard cell layout co-optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 5, pp. 699–712, 2015.

[21] Y. Ma, J. Sweis, H. Yoshida, Y. Wang, J. Kye, and H. J. Levinson, "Self-aligned double patterning (SADP) compliant design flow," in *Design for Manufacturability through Design-Process Integration VI*, vol. 8327, p. 832706, International Society for Optics and Photonics, 2012.