Novel Global Interconnect structure with improved Elmore Delay Estimation for Low-Power Applications

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Novel Global Interconnect structure with improved Elmore Delay Estimation for Low-Power Applications

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Abstract

With advancements in technology, size and speed have been the important facet in VLSI interconnects. Interconnects are known as the basic building block that provide a connection between two or more blocks and have scaling problems that an IC designer faces while designing. As scaling increases, the impact of interconnect in the VLSI circuits became even more important. It controls all the important electrical characteristics on the chip. With scale-down technology, interconnects not only become closer with each other but their dimensions also change which can directly impact the circuit parameters. Certain RC structures have already been defined to control these parameters but in this paper, authors have proposed a new interconnect structure with improved Elmore delay estimation to reduce delay and power consumption in lumped and distributed interconnect circuits using Pulse and Ramp inputs. Further, the proposed model is estimated and verified theoretically. The linear relationship of power consumption and delay for the RC structure has been observed. The proposed structure with improved Elmore delay estimation shows improvement in delay by 64.25% in lumped circuits and 68.75% in distributed circuits in comparison to existing Elmore delay calculations which help in increasing the overall speed of the interconnect circuit.

Keywords: Interconnects; Delay; Power consumption; Copper; VLSI

1. Introduction

Interconnects are considered the basic building blocks of integrated circuits nowadays. These are the metal wiring which provide electrical connections among the active devices to transmit and distribute signals and power across the circuit. The rapid advancement of technology has resulted in more refined Integrated Circuits (IC) with minimum feature size requirements. But when the feature size of interconnecting wires scale down, the signal integrity issues start to dominate while improving

the speed, power, area, and cost characteristics. As per International Technology Roadmap for Semiconductors (ITRS), future nanoscale circuits will contain more than a billion transistors and operate at a speed of over 10GHz [1]. During the process of chip making, the individual components are fabricated on the chips after which these components are connected. But there remains no room to create all the connections so the manufacturers build vertical layers or levels of interconnect. A complex IC can have 10 or more layers of interconnects. These multilevel metal structures not only rose higher and higher but also started to dominate the anatomy of integrated circuits. And due to this, interconnects started controlling the power, noise, timing, design functionality, and even reliability of the circuits. Interconnects can be local or global depending upon the performing function. Local interconnects are the first or the lowest level of interconnects which do not travel a long distance that is connecting two transistors within the same block. Whereas global interconnects are the highest level of interconnects and runs long distances. These generally include clocks, buses, power, or ground lines. With the increasing metal layers, it is important to connect the interconnect levels from one layer to the other. This connection is provided by vias which allow signals and power to be transmitted from one level to the other. Distribution of these long wires can be a challenging task as the performance parameters of high-speed IC highly depend on interconnects size and placement properties. Also, for the enhancement of performance parameters, different techniques can be approached.

Along with timing and power parameters, reduction in area is also considered to be an important factor. Also, the area is considered to obtain the approximate average length of the global interconnect. The length of interconnect depends on the area and the area depends on the geometry. If considered long wires, the time constant becomes quadratic concerning length. Along with the parameter degradation, many issues also arise from the layout designing. For a small size chip processing, interconnects are modelled first so that they consume less space and optimize the performance of the circuit. Still, as the feature size decreases many placement, floor planning and routing issues can occur in the circuit. To reduce these issues, different design levels and optimization techniques have been adopted. After proper wire sizing, interconnects can be modelled using different lumped interconnect models like L, π, and T-models. Generally, the π-model is preferred for distributed RC lines because of its advantages over the other two [2] [3]. When compared with L-model, π-model's delay tends to decrease by half, and when compared with T-model, though the delay is the same T-model has an extra node which complicates the delay calculations [2]. These lumped RC lines can be converted into distributed RC lines. In distributed RC lines, the long wire is divided into segments and each segment is modelled as L or π-type of RC circuit. For each segment, the total length (L) is also divided into individual segment length (Δl) according to the distribution and the value of total resistance and capacitance also gets distributed into individual segment values. These models can not only assist in determining the power consumption or delay of the system but also the crosstalk noise present in the system. The noise has also become one of the major factors in degrading the efficiency of the system.

Along with the minimum noise factor, fast-speed circuits are of major significance as the technology gets improved. For today's technology, the circuit performance mostly depends on the performance of interconnects to achieve projected clock frequencies. For fast circuit designs, interconnect delay is the cognitive factor to determine circuit performance. For an *RC* line, the RC delay (τ) is calculated as the product of total resistance (R) and total capacitance (C). The most commonly used delay estimation model is the Elmore delay model. It provides an accurate estimation of delay in lumped models and can also be used for n-segments of a long wire.

Although Elmore delay estimation is the fastest estimation with less complexity, the only first moment of the impulse response is taken into account for delay calculations. There are other approaches in which higher-order moments are also considered for more accurate delay calculations with more analytical effort. Also, many other different models are taken into account other than the Elmore delay model for fast and accurate computation of the circuits. In [1], the authors have proposed an encoding scheme to achieve an overall reduction in power dissipation, delay, and coupling activity for on-chip buses. This encoding scheme reduces the number of overall transitions which reduces the worst-case crosstalk by reducing the coupling and switching activity. This reduction in switching activity also reduced the dynamic power dissipation of the system as compared to the initial sequence. In [3], various interconnect models and techniques adopted by different researchers to reduce the problem of crosstalk in circuits are reviewed. In [4], authors have reviewed the overall design flow of interconnect modelling in IC design including interconnect characterization, various 2D/3D field solvers, interconnect model library generation, and parameter extraction. They have also discussed statistical interconnect modelling. In [5], wire width planning has been studied for interconnects performance optimization in an interconnect-centric design flow. The authors have presented two simplified wire sizing schemes for VLSI optimization. In [6], authors have developed a set of interconnect delay estimation models with consideration of various layout optimizations including optimal wire-sizing (OWS), simultaneous driver and wire-sizing (SDWS), and simultaneous buffer insertion/sizing and wire-sizing (BISWS). In [7], a new algorithm is proposed for optimizing Elmore delay and layout design based on alphabetic trees. The alphabetic tree framework is quite general and can be used to solve routing problems such as power supply net routing. Further, they have compared different models and concluded that their algorithm runs much faster and can be used in a layout system for performance-driven interconnect design. In [8], authors have presented a 2π-model as a closed-form crosstalk structure. This approach helped them in solving layer assignment problems which further reduced the crosstalk noise. In [9], a wire sizing problem (WSP) is proposed using the Elmore delay model. In [10], the authors have analyzed the determinants of interconnect delay with the Elmore delay model. Further, the experiments are carried out at the stage of physical circuit design. In [11], the authors provide a generalized approach to linear RLC/RC circuit response approximation. In this approach, the transient response is approximated by matching the initial boundary conditions and uses higher-order moments to construct

a q-pole model which is also known as the Asymptotic Waveform Evaluation method. Although, this method can be accurate for delay estimation it also provides numerical instability. In [12], the D2M RC delay metric is proposed which is as simple and fast as the Elmore delay model but more accurate. The proposed metric behaves like the Elmore delay metric which generally overestimated delay but with consistently less error. It can be used in time-driven placements, interconnect synthesis, and global routing. In [13], authors have extended probability interpretation to circuit homogeneous response without requiring the time shift parameter. They have used gamma distribution to characterize a normalized homogeneous portion of the step response. Further, they demonstrated that when a table model is carefully constructed, the h-gamma approximation provides excellent improvement to that from model-order reduction but with run time complexity comparable to Elmore delay approximation with very little additional cost in terms of CPU time. It is probably stable for any RC mesh response. In [14], the authors have introduced a new boundary limiting the Elmore delay. This new improved Elmore delay problem is derived according to the compound interest problem of Jacob Bernoulli. In [15], the authors have presented some commonly used interconnect models and a set of interconnect designs and optimization techniques for improving interconnect performance and reliability. They have also presented a comparison of different optimization techniques in terms of their efficiency and optimization results. They have also discussed the trends and challenges of interconnect design as the technology feature size rapidly decreases to below 0.1 microns. In [16], a comparative study is done by the researchers about 3 different Elmore delay-based methodologies which provide better results as compared to the simple Elmore delay estimation model. First, the Scaled Elmore delay model which is the scaled version of the simple Elmore delay model by the factor of ln (2). Second, the effective capacitance model tries to deal with an effect that has become more evident in new technologies due to the rising of interconnect resistance. Last, the Fitted Elmore delay model is an attempt to adjust Elmore delay by adding coefficients to terms of the Elmore delay formula to get closer results with that of SPICE results. In [17], authors have presented an equivalent Elmore delay model for RLC trees. Closed-form solutions were observed for 50% delay, rise time, overshoot, and settling time of signals in RLC trees. The solutions presented have the same accuracy characteristics as compared to the Elmore delay model. In [18], a simple closed-form delay estimation interconnect structure is presented based on first and second-order moments that handle arbitrary voltages and conductance effects for a lumped and distributed line. In [19], authors have proved that the Elmore delay is an absolute upper bound on the 50% delay of an RC tree response. A lower bound on the delay is also developed using Elmore delay and the second moment of the impulse response. In [20], authors have outlined the importance of layer assignment over wire sizing and present efficient techniques to perform concurrent buffer insertion and layer assignment to fix electrical and timing problems while maintaining speed. In [22], the author discusses the Elmore delay model which provides simplistic delay analysis that avoids time-consuming numerical integration/differential equations of RC network. In [23], the authors have proposed an improved Elmore delay model. This model is extracted by applying the Least Mean Square method on

SPICE simulation results. Although the speed of the circuit matters, power consumption and dissipation of the circuit matters equally. Excess dissipation of power which is generated as heat in the circuits can lead to system failure. There are many ways to control the power factor in the circuits which can reduce the power considerably. One such method can be applying ramp signal as an input. In [24], authors have presented a new method to calculate time-varying response for a finite-length distributed RC line with ramp as an input supply. In [25], authors have used adiabatic array logic to design some fundamental logic gates. Adiabatic array logic is an adiabatic logic family which helps in reducing the power consumption in the circuits.

It is well known that circuit efficiency depends upon the performance of the system. A chip may contain many different blocks connected with each other. When one block performs its function faster, the performance of other blocks can vary due to the heat dissipation or functionality of each block. This performance variation can depend on various factors. But the major performance factors for deep sub-micron technologies depend on the interconnects which connect these blocks. With the scaling of circuit parameters, the major issues occurring in the device depend highly on interconnects. Wires are not only used to connect these blocks with each other but also connect two or more transistors that are present inside these blocks. One of the main problems present in the circuits is a delay. The interconnect delay is calculated using resistance (R) and capacitance (C). Interconnect introduces some resistive and capacitive parasitic. These parasitic affect the performance of the circuits. Interconnect parasites increase the propagation delay of the circuit, can increase power dissipation and can add some extra noise to the circuits. One way to optimize the circuit performance is to properly design the layout of the interconnect system. The main and basic idea for the minimum delay is to keep the wire as short as possible. Although, interconnect layout design and wire sizing are two different things but both are studied altogether because wire sizing also focuses on reducing the parameters of the interconnects as small as possible. There can be different types of wire sizing namely uniform, non-uniform, tapered wire sizing, or continuous wire sizing [6][20] which can enhance the speed of the system as well as solve the layer assignment problem for the circuit. Π-model is also considered for layer assignment problems [8]. It not only reduces delay but can also reduce the number of layers in a chip. For simple π-RC interconnect circuits, Elmore delay estimation is used widely which is one of the simple and accurate methods for delay calculation. To optimize circuit performance more, this delay can be enhanced by using different techniques or methods [12] [13]. Besides Elmore delay uses only first moment of the impulse response but it can also be calculated using higher order of the response [11]. Optimizing only delay is not sufficient to boost a circuit's performance. Power consumption and power dissipation both must be considered equally for proper functioning. Power dissipation is the maximum power that can be released without disturbing the performance of the system and released in the form of heat. Power dissipation depends on the switching activity of the response. Due to more fast switching, the power also reduces which will reduce the thermal energy in the circuit thereby improving the

reliability of the device. This switching can be controlled directly by using encoding methods [1]. Power consumption is one of an important factor considered for a system's performance [18]. It is well learned that by proper wire sizing and improved Elmore delay estimation the propagation delay can be reduced. Also, by varying voltages the power consumption reduces. Other than varying voltage, changing the nature of input response can also reduce the power consumption in the circuits for example using ramp signal as an input. Unlike the switching behaviour of step response, ramp signal varies steadily and linearly with respect to time.

It has been seen that Elmore delay estimation gives the accurate results of delay for monotonic step response. Also, the delay of interconnects can be improved using different techniques and can be structured differently to get maximum optimized results for the time constant. Moreover, it was seen that only delay was improving by using these techniques. Therefore, the focus of this paper is to re-structure the interconnect circuit to optimize delay as well as power consumption by preserving the characteristics of the Elmore delay estimation model. In this paper, a new interconnect structure with improved Elmore delay estimation has been proposed for interconnects to reduce the time constant as well as power consumption using pulse and ramp as inputs. Also, power consumption is given a priority to reduce with the decrease in interconnect length. In this research article, the authors have focused on the following:

- Wire geometry along with the shrinking size of the circuits
- Spacing between interconnects
- Dielectric permittivity used for making interconnects
- The resistivity of the material which is used to manufacture interconnects

This paper comprises of the following sections: Section 2 explains the proposed methodology, Section 3 explains results and discussions, and lastly Section 4 explains conclusion and future scope.

2. Proposed Methodology

According to Moore's law, the number of transistors per silicon chip doubles every year. This law suggests faster, smaller, and more efficient circuits. With the advancement in technology, the size is also shrinking which increases the metal layers in the circuit. At this stage, interconnects control the timing, power, delay, noise even reliability of the circuits. This leads to the importance of interconnects. There are many reasons to stress the significance of interconnects in the circuits. Firstly, the authors have considered the wire geometry along with the shrinking size of the circuits. The main issues which are seen in the circuits are due to global interconnects. The scaling of global interconnects depends on the scaling factors. Three parameters are considered for wire sizing i.e. length (L), width (W), and thickness (T). The length of the long wires is independent of scaling and only width and thickness

reduces by the factor *s*. Hence, the resistance of the long wires increases but the capacitance remains the same. This increase in wire resistance brings out an *RC* delay phenomenon. Second, the spacing issues which occur with technology scale down. As the technology size decreases, the spacing between the interconnects also decreases. Today, the spacing between interconnects has been reduced to such an extent that the problem of coupling has started to degrade the performance of the circuits. This coupling not only introduces additional delay but also noise issues that can cause permanent circuit failure and to re-spin silicon [7]. This re-spin process is very expensive and time-consuming because if an error occurs in the design after fabrication, then the whole process must be repeated again. Third, interconnects are separated from each other by dielectric layers. The dielectric permittivity depends on the material used for making interconnects. Low-k dielectrics are preferred for wire insulation. Low-k material means materials with relatively low dielectric constant as compared to silicon-di-oxide. These materials are responsible for the continued scaling of technology. Replacing SiO_2 with low-*k* materials enables faster switching and low heat dissipation. SiO_2 was used as dielectric but many other materials when doped with SiO_2 gave lower dielectric constant values and are being used for better performance. The permittivity of unity that is air is also being used which is effective but produces fabrication and production cost challenges. Lastly, the resistivity of the material is used to manufacture interconnects. Previously, aluminium was used to make interconnects but later was switched to copper because copper provides better electrical conductivity as well as low resistivity. Due to this material change, some relaxation was seen in terms of power dissipation and delay but as technology further scaled down the problem of delay persisted. Now the technology has scaled down so much that the resistivity of copper seems to be high enough to generate performance problems. To promote the better performance of the systems new materials must be tested and applied so that the circuits have faster switching and low power consumption.

The better performance also depends upon the structure used for interconnects. There can be three possible lumped models used for modelling interconnect structures that are *L*, *π,* and *T*. The *L* model is the simplest lumped model with total resistance (*R*) and total capacitance (*C*). The delay (τ) for the *L* model is computed as the product of total resistance and total capacitance (*RC*) which does not satisfy the Elmore delay estimation for long wires. So, this model is avoided. For the π-model, the capacitance is divided in half but the resistance remains the same. The delay for π-model is the product of total resistance and half of the total capacitance resulting τ as *RC*/2 which perfectly satisfies the Elmore delay estimation. Similarly, for the T model, the resistance gets divided by 2 but the capacitance remains the same. The delay for the *T* model also satisfies the Elmore delay estimation. The only difference between π and *T* model is that the *T* model has an extra node that may increase the number of calculations or make it more complex. As a result, the π-model is the popular model for a distributed RC line. Fig.1. shows the methodology used in this paper.

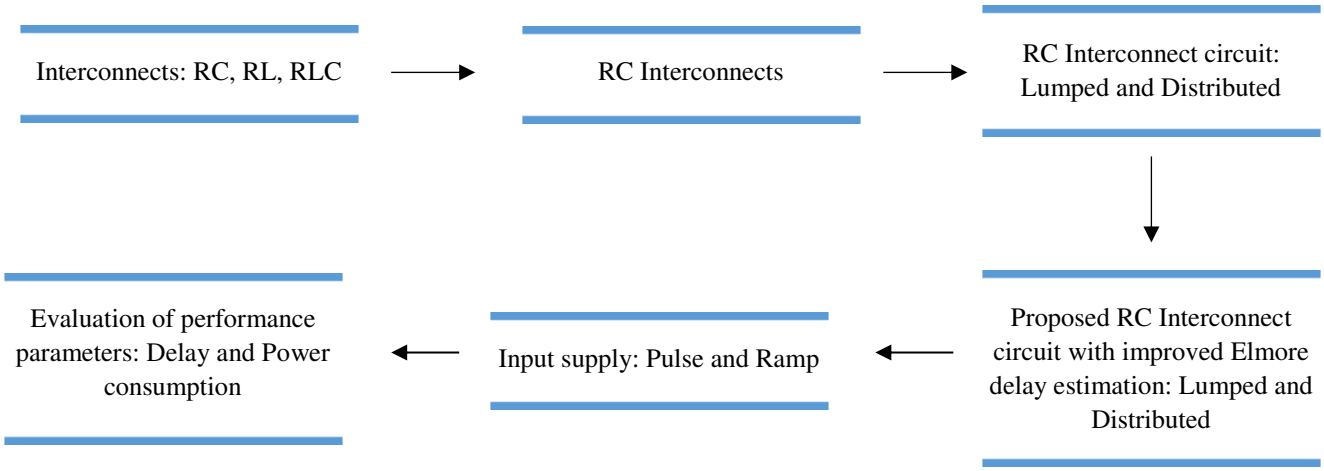


Fig. 1. Proposed Methodology

All these factors if computed correctly can reduce the time constant and can enhance the efficiency of the circuits. Also, power consumption must be considered because if power consumption becomes larger, circuits will tend to dissipate more heat which will ultimately cause a system failure. To evaluate delay for the circuits, the Elmore delay model is considered as it is simple and accurate. It allows us to explicitly express signal delay as a simple algebraic function of geometric parameters of interconnects so that it can be easily used for interconnect optimization [2]. Elmore delay gives results for input signal which is of a step function type. If the step response of the circuit is $h(t)$, 50% point delay of monotonic step response is the time T_d which satisfies Eq. (1) [14].

$$\int_0^{T_d} t\, h(t)dt = 0.5 \tag{1}$$

In the Elmore delay model, T_d is approximated as the mean of the impulse response $h(t)$. If the impulse response is taken as the probability density function (pdf), the mean is defined as the first moment of the impulse response which is called τ_d is given by Eq. (2) [14].

$$\tau_d = \int_0^{\infty} t\, h(t)dt \tag{2}$$

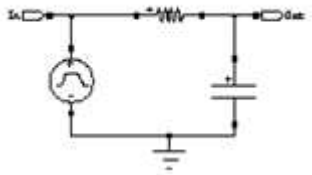
The first moment of the impulse response is commonly referred to as the Elmore delay. It represents the dominant time constant and a good estimate of delay in the circuit. Thus, for an *RC* ladder, the Elmore delay can be computed as given by Eq. (3) [7].

$$\tau_i = \sum_k (C_k \times R_{ik}) \tag{3}$$

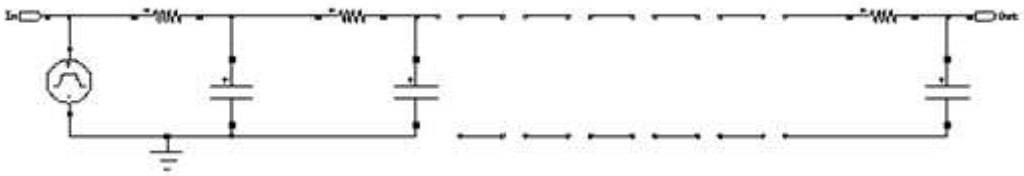
Where the node of interest is node i, C_k is the capacitance at node k, and R_{ik} is the sum of all the resistances in common from source to node i to the source to node k. Eq. (4) illustrates the Elmore delay estimation for n number of segments.

$$\tau = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + - - - - + (R_1 + R_2 + R_3 + - - + R_n)C_n \tag{4}$$

Delay can be estimated for lumped as well as distributed RC line. Fig. 2 shows the lumped and distributed RC network. For lumped model, the total delay can be expressed as the product of resistance and capacitance i.e. τ = RC. Fig. 2 (a) shows the lumped network of a wire. If step input is applied, 50% point delay for lumped network is equivalent to 0.7RC [7-26]. For long distributed wires, the *RC* delay can be computed in terms of total wire resistance (*R*) and total wire capacitance (*C*). Fig.2. (b) represents the *RC* ladder with *n* segments consisting of total wire length *L.*If step input is applied, 50% point delay for distributed network is equivalent to 0.4RC [7-26].



(a)



(b)

Fig. 2.(a) Lumped RC network (b) Distributed RC network

In this paper, the simple RC structure is considered for evaluating performance parameters. Also, power consumption is observed to be increasing and decreasing w.r.t. interconnect length. To obtain a more strict relation function of power for length, authors have proposed a new interconnect structure with improved Elmore delay estimation with pulse and ramp as input supply. The evaluation of the proposed structure is done for both the networks i.e. lumped as well as distributed.

2.1 Proposed Interconnect structure with improved Elmore Delay Estimation

From the above study, it has been revealed that the distributed network is considered better for parameters performance. The interconnect circuits can be further divided into sub circuits or more to get more optimized values of power but delay remains almost constant. To get optimized values for both, the authors have proposed a new interconnect structure with Elmore delay estimation. The proposed structure consists of a resistance and a capacitance which are divided into two parts with their half values. It has almost negligible complexity in structure and easy to simulate. The circuits are combined in such a way that one is combined in an upside-down position with the other one which not only substitutes the value of capacitance but of resistance also. Fig.3. shows the proposed (lumped)

interconnect structure. For lumped interconnect structure, the resistances and capacitances are connected in such a way that they form the alphabet T.

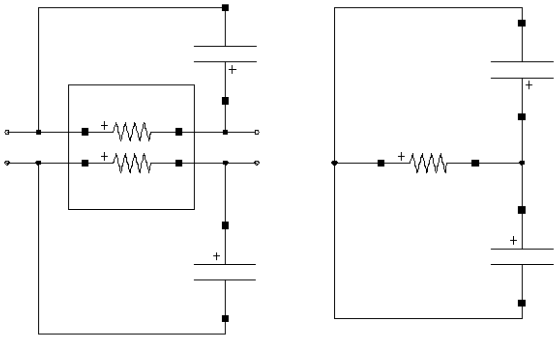


Fig. 3. Proposed lumped interconnect structure

The performance parameters are evaluated for different lengths of interconnect circuits which are considered from 1mm to 10mm. The wire geometry is shown in Table 1 for 45nm technology with dielectric as 2 for all different lengths of interconnects. The values of total resistance and total capacitance are taken for different interconnect lengths are shown in Table 2 which are derived from Predictive Technology Models (PTM) [21].

Table 1. Wire geometry for 45nm technology

Parameters	Values (μm)
Width	0.2
Height	0.1
Spacing	0.4
Thickness	1

Table 2. Different values of total resistance and capacitance for different lengths of interconnect

Length	Parameters	
(mm)	*Resistance* (Ω)	*Capacitance* (*fF*)
1	110	191
2	220	383
3	330	575
4	440	767
5	550	959
6	660	1150
7	770	1342
8	880	1534
9	990	1726

10	1100	1918

When the two circuits are connected, the resistance of the proposed structure is reduced by the factor of four. With the technology size decreasing, resistance plays an important role. With increased resistance, delay and power both increase because both have a direct relationship with resistance. In proposed structure, when two circuits are connected parallel with each other, the resistance also becomes parallel with each other. As the single circuit is divided into two different circuits, the value of resistance gets divided among them. And, with the decrease in resistance, the performance parameters get optimized because power and delay directly depend on resistance. The total resistance of the proposed structure can be calculated as given by Eq. (5).

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} \tag{5}$$

Similarly for capacitance, although the total capacitance value remains the same for the circuit for each segment the value gets divided equally among them further reducing the capacitance value. Also, for long wires length remains constant only thickness and width reduces with technology scaling. This reduction results in the reduction of area. If area reduces capacitance also reduces because of the direct relationship between area and capacitance. This improves the overall speed of the circuits. The total capacitance of each segment is calculated using Eq. (6):

$$C = C_1 + C_2 \tag{6}$$

For example, for a 1mm wire, the total resistance (R) as 110Ω and total capacitance (C) as 191fF are considered. When the interconnect circuit is modelled using the proposed interconnect structure, then according to Fig.3, the resistance gets divided into two halves resulting in 55Ω as each resistance value. The total value of resistance for the circuit is evaluated using Eq. (16) resulting in 27.5Ω. Similarly, for capacitance, the value gets divided equally resulting 95.5fF as each capacitance. The delay for proposed lumped interconnect structure can be calculated using the reduced value of the resistance and the capacitance. The Elmore estimation for the lumped network is given by Eq. (7):

$$m_\upsilon = \left[\frac{R}{4} * C\right] = \frac{RC}{4} = 0.25RC \tag{7}$$

Similarly, the Elmore delay can be computed for distributed network. Fig.4. shows the distributed structure of interconnect with n-segments. For distributed interconnect structure, the resistances and capacitances are connected in such a way that they form the alphabet H. Algorithm 1 explains the formation of the RC ladder using the proposed interconnect structure.

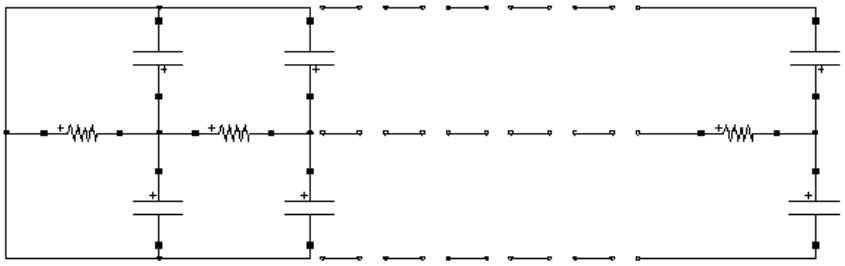


Fig. 4. Proposed distributed interconnect structure

Algorithm 1: Novel Interconnect Structure for Delay and Power consumption.

Input: Interconnect

Output: Delay, Power consumption

Start

Step-1: Consider an interconnect length and evaluate total resistance and total capacitance for the circuit.

Step-2: Model a distributed RC line by distributing segments.

Step-3: Simulate the RC ladder using the proposed structure for the considered length.

Step-4: Divide each segment into half.

Step-5: Place one segment in an upside-down position with the other remaining half segment in upright-position to form the alphabet H.

Step-6: Divide the value of resistance of each segment and evaluate the total resistance of each segment when connected in parallel.

Step-7: Distribute the value of total capacitance equally for each segment.

Step-8: Repeat steps 3 to 7 for all the segments in the RC ladder as shown in Fig.4.

End

With the reduction in the total resistance of the interconnect circuit, the delay also reduces. This reduced delay does not match with the proposed Elmore delay estimation but provides the improved Elmore delay calculation. To evaluate the new improved Elmore delay, let's consider a distributed RC network using the proposed structure as shown in Fig.4. The length (L) of interconnect remains the same. If the reduced total resistance (R/4) and total capacitance (C) expands into n equal segments, then the Elmore delay can be computed as:

$$R_1 = R_2 = - - - - - - - - = R_n = \frac{R}{4n} \tag{8}$$

$$C_1 = C_2 = - - - - - - - - = C_n = \frac{C}{n} \tag{9}$$

Using Elmore estimation:

$$\tau = \frac{RC}{4n^2} + \frac{2RC}{4n^2} + - - - - - - - + \frac{NRC}{4n^2} \tag{10}$$

$$\tau = \frac{RC}{4n^2}[1 + 2 + - - - - - - - + N] \tag{11}$$

$$\tau = \frac{RC}{4n^2}\sum_{i=1}^{N} n \tag{12}$$

$$\tau = \frac{RC}{4n^2}\left[\frac{n(n+1)}{2}\right] \tag{13}$$

$$\tau = \frac{RC(n+1)}{8n} \tag{14}$$

If step response applied, then 50% delay for n→∞ is:

$$\tau = \frac{RC}{8} = 0.125RC \tag{15}$$

Thus, for a distributed RC ladder the improved Elmore delay can be computed by Eq. (19):

$$\tau_i = \sum_k (2C_k \times R_{ik}) \tag{16}$$

Where the node of interest is node *i*, $2C_k$is the sum of all capacitances at node *k*, and R_{ik} is the sum of all the resistances in common from source to node *i* and source to node *k*. The Elmore delay estimation for *n* number of segments is given by Eq. (20).

$$\tau = R_1(C_A + C_a) + (R_1 + R_2)(C_B + C_b) + (R_1 + R_2 + R_3)(C_C + C_c) + - - - - + (R_1 + R_2 + R_3 + - - + R_n)(C_N + C_n) \tag{17}$$

The proposed structure with improved Elmore delay estimation shows improvement in delay by 64.25% in lumped circuits and 68.75% in distributed circuits as compared to existing Elmore delay calculations which help in increasing the overall speed of the interconnect circuit. Also, the reduction

in resistance value by four times even when the capacitance remains the same for the circuit clearly shows the reduction in power consumption. This evidenced calculation shows the up-gradation of the interconnect circuits. Hence, it can be said that along with the delay parameter power consumption also plays a vital role in circuit efficiency and reliability. Power consumption in a circuit can be reduced by supplying the ramp as an input. Ramp is a type of signal which increases steadily and linearly with time. Ramp supply reduces the charging time of the capacitor which eventually helps in low power dissipation as well as consumption. Less power consumption will lead to less heat dissipation which will make the circuit live longer. Also, the circuit's reliability can be seen in terms of resistance and the time for which the current flows. The more the resistance and time constant, more will be the heat dissipation and this resistance and delay can be made smaller with proper distribution of the wire.

All the simulations were carried out in a system with Intel(R) Core(TM) i7-10700 CPU @ 2.90GHz processor, 16.0 GB RAM using LTSPICE software.LTSPICE is software that is best suited for faster simulation of electronic circuits and power electronics. LTSPICE has good online community support. It is the widely used SW tool for simulation purposes, extremely simple to use, Light Weight, Rich in Component library, and free. It also allows adding off-the-shelf-components. Users just need to find or write the SPICE model of the respective component. LTSPICE is a whole other software tool that also uses SPICE to do its simulations but uses better algorithms, methods, and tricks to get simulations done faster with high accuracy than PSPICE.

3. Results and Discussions

Considering uniform distribution i.e. distribution of segments per unit length, different lengths along with each segment resistance and capacitance values used for estimation of performance parameters for the proposed lumped and distributed structures are shown in Table 3 and 4 respectively. The total values of resistance and capacitance are derived from Predictive Technology Models (PTM) [21]. The individual values of resistance and capacitance can be obtained by dividing equal values to each capacitance and equal value of each resistance divided by four. For example, for 2mm wire total resistance is 220Ω, and the total capacitance value is 383fF. Considering uniform distribution, the individual resistance (R/4) value will be 27.5Ω and the individual capacitance (C/4) value will be 95.75fF because the total capacitance value gets divided among all the capacitances equally.

Table 3. Different lengths with individual resistance and capacitance values for proposed lumped interconnect structure

Lengths (mm)	Total Resistance ($\frac{R}{4}$) (Ω)	Total capacitance (fF)
1	27.5	191
2	55	383

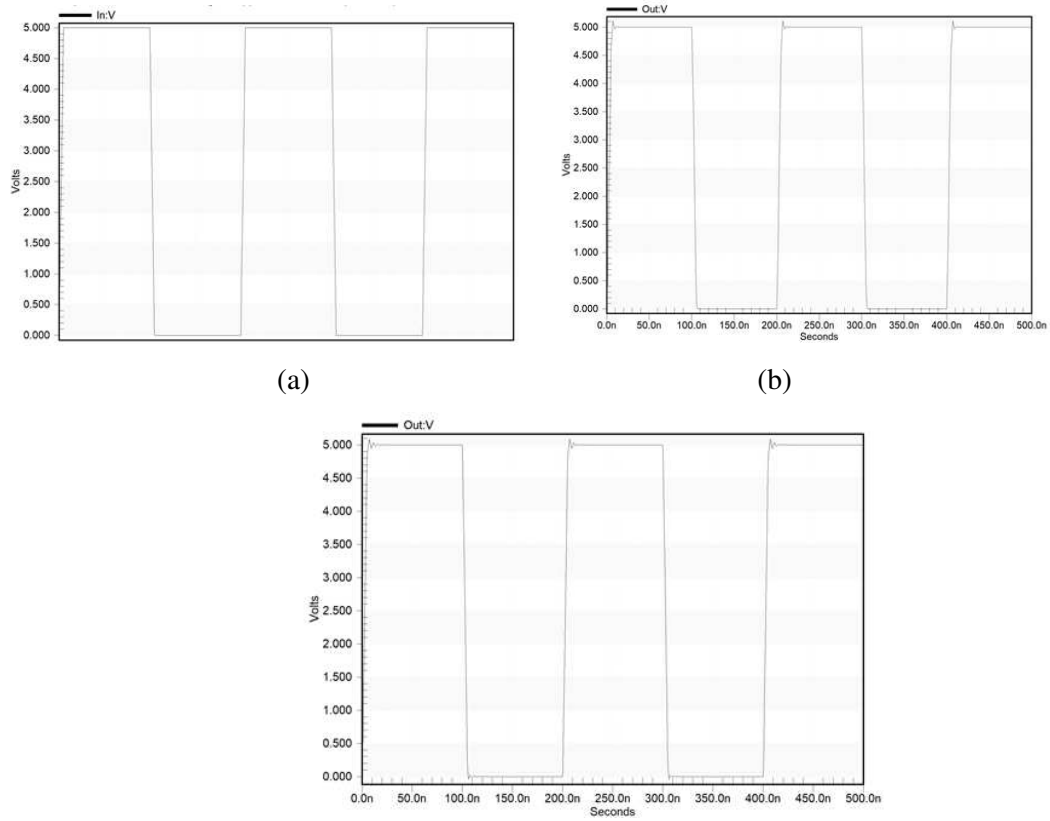
3	82.5	575
4	110	767
5	137.5	959
6	165	1150
7	192.5	1342
8	220	1534
9	247.5	1726
10	275	1918

Table 4. Different lengths with individual resistance and capacitance values for proposed distributed interconnect structure

Lengths (mm)	Total Resistance (Ω)	Total capacitance (fF)	Individual Resistance (Ω)	Individual Capacitance (fF)
1	110	191	27.5	95.5
2	220	383	27.5	95.75
3	330	575	27.5	95.83
4	440	767	27.5	95.875
5	550	959	27.5	95.9
6	660	1150	27.5	95.83
7	770	1342	27.5	95.85
8	880	1534	27.5	95.875
9	990	1726	27.5	95.88
10	1100	1918	27.5	95.9

The simulations are performed using SPICE. Fig.5 and 6 shows the waveforms for the lumped and distributed wire network for pulse and ramp input respectively. Further, the performance parameters from length 1mm to 10mm for both lumped and distributed network with pulse input supply are estimated and tabulated in Table 5 and Table 6 respectively and with ramp input supply in Table 7 and 8 respectively. The structures are modelled considering values calculated in Table 3 and 4. Also, the simulated values are theoretically verified with the Elmore delay estimation.

The results for different inputs applied are different. For pulse input, the output is observed to be somewhat distorted. This can be due to delay or power consumption. For ramp input, the output holds its initial shape by reducing the power consumption in the circuit with slow switching process.

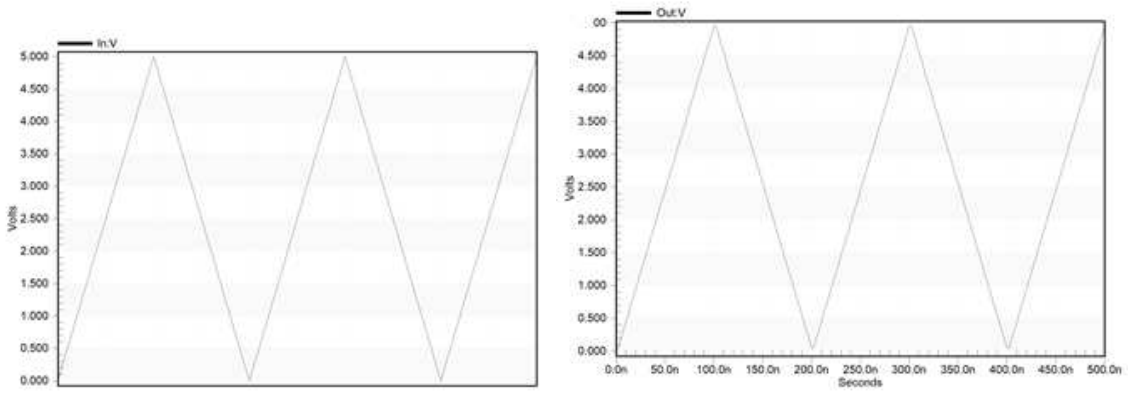


(a) (b)

(c)

Fig. 5. (a) Input pulse signal (b) Lumped structure Output with overshoot problem (c) Distributed structure Output with significant distortion

Fig.5 represents the waveform for lumped and distributed circuits when pulse input is applied. It can be observed in both the waveforms that there is an overshoot in the signal at every rise of the signal. This overshoot represents a distortion in the output signal which means when the transient value exceeds its final value. But the signal stabilizes itself with the rise time of the signal to change the output as little as possible.



(a) (b)

Fig. 6. (a) Ramp Input (b) Output with no distortion

Fig.6 represents the waveform for the circuit with ramp input. It can be observed that there is no distortion in the output of the circuit and the power can be reduced considerably.

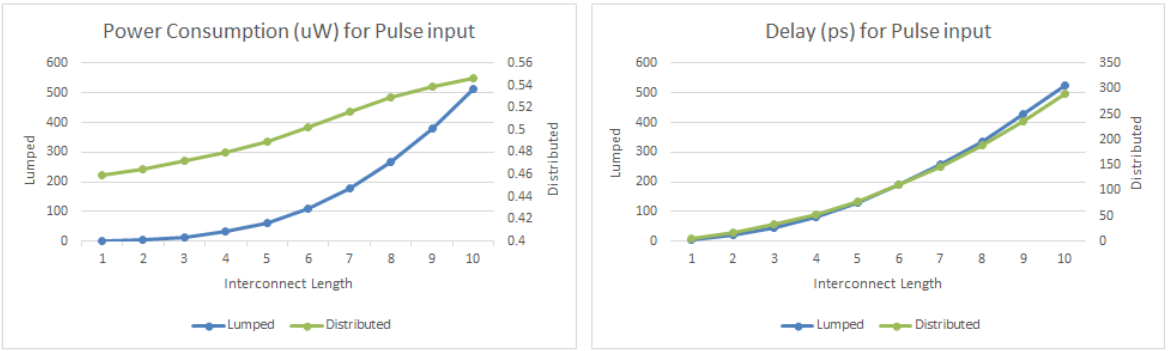
Table 5. Performance evaluation for proposed lumped interconnect structure for Pulse input

Length (mm)	Theoretical delay for lumped network (ps) Eq. (7)	Simulated delay lumped network (ps)	Power (µW)
1	5.25	5.41	0.45
2	21.06	21.01	3.47
3	47.43	46.64	12.8
4	84.37	81.81	31.5
5	131.86	130.34	63.3
6	189.75	189.61	111.69
7	258.33	258.33	179.71
8	337.48	337.48	268.91
9	427.18	427.17	379.50
10	527.45	526.99	512.18

Table 6. Performance evaluation for proposed distributed interconnect structure for Pulse input

Length (mm)	Theoretical delay for lumped network (ps) Eq. (17)	Simulated delay lumped network (ps)	Power (µW)
1	5.25	5.41	0.459
2	15.79	16.36	0.465
3	31.62	32.44	0.472
4	52.73	52.69	0.480
5	79.11	78.96	0.490
6	110.68	110.47	0.502
7	147.60	147.37	0.516
8	189.83	189.43	0.529
9	237.30	236.51	0.539
10	290.09	289.36	0.546

Table 5 and 6 tabulates the delay and power consumption in the lumped and distributed RC interconnect circuit for different lengths. The calculated values using Elmore delay estimation show the better computation of the interconnect circuits with less delay as compared to the simulated ones, though both the values are somewhat similar. Also, from the evaluated values, the performance parameters can be varied according to the lengths of interconnects. Fig.7 and 8 shows the variations of power to interconnect length and delay to interconnect length for both lumped and distributed circuits for different input supplies.



(a) (b)

Fig. 7.For pulse input signal (a) Power vs Length (b) Delay vs Length

Fig 7 (a) and Fig 7 (b) shows the linear relationship with the increase in interconnect length. For power vs length graph, lumped interconnect circuits power increases with the increase in length whereas distributed circuits power also increases with increase in length but marginally. The longer the wire more will be the power consumption which can also be observed from Fig 7. For delay vs length, lumped circuits and distributed interconnect circuit with different lengths delay strictly increases linearly with the increase in interconnect length. Also, the linear relationship represented in the graphs shows a positive slope. A strictly linear increase of delay verifies the monotonic nature of the impulse response.

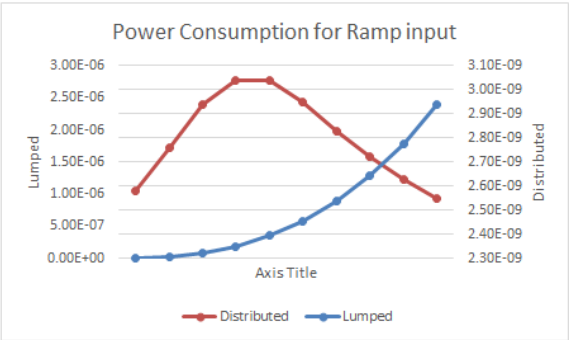
Table 7. Performance evaluation for proposed lumped interconnect structure for Ramp input

Length (mm)	Theoretical delay for lumped network (ps) Eq. (7)	Simulated delay lumped network (ps)	Power (µW)
1	5.25	5.15	0.002
2	21.06	20.54	0.02
3	47.43	46.97	0.07
4	84.37	84.23	0.18

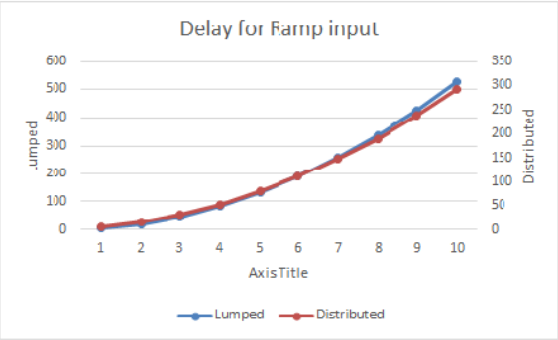
5	131.86	131.84	0.35
6	189.75	189.74	0.57
7	258.33	258.33	0.88
8	337.48	337.48	1.28
9	427.18	427.18	1.78
10	527.45	527.45	2.40

Table 8. Performance evaluation for proposed distributed interconnect structure for Ramp input

Length (mm)	Theoretical delay for lumped network (ps) Eq. (15)	Simulated delay lumped network (ps)	Power (nW)
1	5.25	5.15	2.58
2	15.79	15.37	2.76
3	31.62	30.93	2.94
4	52.73	52.13	3.04
5	79.11	78.82	3.04
6	110.68	110.65	2.95
7	147.60	147.74	2.83
8	189.83	190.06	2.72
9	237.30	237.60	2.63
10	290.09	290.43	2.55



(a)



(b)

Fig. 8. For ramp input signal (a) Power vs Length (b) Delay vs Length

Fig 8 (a) and Fig 8 (b) show the linear relationship with the increase in interconnect length. For power vs length graph, lumped interconnect circuits power increases with the increase in length whereas distributed circuits power first increases with increase in length then decreases with the length. The

longer the wire more will be the power consumption for lumped circuit and less power consumption for distributed circuit which can also be observed from Fig 8. For delay vs length, lumped circuits and distributed interconnect circuit with different lengths delay strictly increases linearly with the increase in interconnect length. The delay does not change much when compared with pulse input response but power consumption is affected greatly. Also, the linear relationship represented in the graphs shows a positive slope. A strictly linear increase of delay verifies the monotonic nature of the impulse response.

4.1 Comparison

Lastly, a comparison of the proposed model is done with the other state of art techniques and is tabulated in Table 6.

Table 6. Comparison of proposed model with other state of art technique

Models/Technique			Power (μW)	Delay (ps)
Proposed interconnect structure (for max *L*=10mm)	Pulse supply (5V and 5ns rise time)	RC Lumped RC Distributed	512.18 0.546	526.99 289.36
Proposed interconnect structure (for max *L*=10mm)	Ramp supply (5V and 100ns rise time with 200ns time period)	RC Lumped RC Distributed	2.40 2.35nW	537.45 290.43
Ramadass *et al*[18] (for 5V)		RC Lumped RC Distributed	0.451 0.546	20.138ns 42.564ns
Gupta [19] (for 5ns rise time)		At node A At node B At node C	- - -	0.018ns 1.06ns 1.48ns

The maximum length of the proposed interconnect structure is considered for the comparison of delay and power values with other state of art techniques. For the proposed structure, the input voltage is kept constant to 5V with a rising time of 5ns. When compared with the novel interconnect model as mentioned in [18] with second-order moments, more optimized values were observed for distributed network from the proposed interconnect structure while the delay for lumped circuit was observed to be decreased and power consumption increased. Although, the authors in [18] have simulated their model on different voltages but when compared with the proposed structure, the lumped network power has increased for both the inputs applied but for distributed network power remains the same for pulse input and decreases for ramp input. In [19], authors have evaluated delay at 5ns rising time for different nodes in the RC interconnect circuit. Though authors of the proposed model have not calculated at each node but for the end node, our model shows more speed in comparison to Gupta [19] with the same rising time.

4. Conclusion and Future scope

In this paper, an innovative interconnect structure with improved Elmore delay estimation model was simulated. Further, Elmore delay calculations for long wires with pulse and ramp inputs have been observed for lumped and distributed distribution segments for different lengths of interconnect. It was concluded that for pulse input signal lumped RC network, the delay and power both increases linearly with a significant value with increasing interconnect length whereas in distributed RC network, delay increases with interconnect length but power increases slightly. For ramp input, the delay remains almost similar in comparison with pulse input supply for both lumped and distributed network but for power consumption, it rises linearly with increase in interconnect length for lumped circuits and for distributed circuits the power first increases then decreases with the increase in interconnect length. Thus, the performance parameters for distributed network show better efficiency as compared to the lumped network. An optimized Elmore delay calculation was performed to reduce the time constant of the interconnect circuits. Apart from delay, power consumption was also of major concern which was seen to be optimized while using an enhanced RC model. A linear relationship of power consumption and delay for both the RC networks was observed and it has been observed. Although, the computation cost will increase a little but the proposed structure gives better results when it comes to reducing power consumption in the circuits. Further, for future aspects, different materials can be used to evaluate the performance parameters for the circuits and a comparison can be done with copper material. Also with the decreasing size of the technology, inductance gets introduced in the interconnect structures which can also be considered.

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2. Conflict of Interest: Not applicable
3. Code available: Not applicable
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