Multi-objective optimization for heat transfer performance of micro-fins and signal integrity of key interconnect technologies in 3D integrated chips

Wei He[1], Ershuai Yin[1], Qiang Li[*]

MIIT Key Laboratory of Thermal Control of Electronic Equipment, School of Energy and Power Engineering, Nanjing University of Science and Technology, Nanjing 210094, China

Abstract: This paper is devoted to the synergistic design of the thermal management and signal integrity for 3D integrated chips. The structure parameters of the micro-fin and interconnected components are optimized to obtain a balanced performance of chip heat dissipation and signal integrity. The three-dimensional integrated chip flows heat transfer model under the action of electrothermal coupling is developed. A full-wave electromagnetic simulation model of the signal interconnection components is proposed with the same structural parameters. The effects of various structural factors on the heat transfer performance and signal integrity of 3D integrated chips are investigated. A genetic algorithm multi-objective optimization is carried out to simultaneously reduce the total thermal resistance of the 3D integrated chip and the signal transmission losses of the critical interconnect components. The results show that the total thermal resistance of the 3D IC becomes lower with larger TSV diameter, micro-fins height and micro-fine radius, and smaller oxide thickness. When the TSV diameter and oxide thickness increase, the height and radius of the micro fins are reduced to facilitate the signal transmission of the chip interconnected components. A multi-objective optimization approach significantly improves the chip's heat transfer performance and signal integrity. The chip designer can determine the optimal solution by deciding the weights of the two optimization objectives depending on the practical requirements.

Keywords: 3D integrated chips, Thermal management, Signal integrity, through-silicon via (TSV), Electrothermal coupling, Multi-objective optimization.

1. Introduction

With the rapid development of the chip manufacturing industry, integrated chip packaging technology has developed from a two-dimensional plane to a three-dimensional space. The three-dimensional integrated circuit has been widely considered a technical choice beyond Moore's law. Compared with the traditional two-dimensional chip, the three-dimensional chip makes full use of the vertical direction of the chip substrate, which makes the chip have higher integration, shorter interconnection time and faster transmission speed[1]. In addition, the interconnection of electrical signals in the vertical direction of the 3D integrated chip is mainly achieved utilizing silicon through-via (TSV) technology[2]. Although the growth momentum is good, the development of new technologies will also bring new problems. First and foremost, thermal management is a complex problem in chip high-density integration, which is also a critical challenge restricting the development of 3D integrated chips. The heat generated in the actual chip work is mainly the Joule heat effect of internal transistors, interconnect solder joints, and metal interconnects under the action of the external electric field. If the heat is not taken away, the regular operation of the chip will be

*Corresponding author. E-mail address: liqiang@njust.edu.cn (Q. Li)

1. Denotes equal contribution

seriously affected. To solve the thermal management problem of the three-dimensional integrated chip, effective heat dissipation methods need to be adopted. Microchannel cooling technology has the characteristics of high heat dissipation efficiency and compact structure. This cooling method has been widely used in the field of electronic heat dissipation, and semiconductor manufacturing technology has been mature enough to manufacture different microchannel structures on the silicon wafer. On the other hand, with the advent of the 5G era, the 3D integrated chip will be in the high-frequency signal transmission environment, a significant challenge to the signal transmission of heterogeneous high-density integrated chips. There are complex coupling parasitic effects between TSV, substrate, transistor, and TSV, which will affect the quality of TSV signal transmission. Therefore, it is necessary to analyze various signal integrity problems such as signal crosstalk, loss, reflection, and so on[3]. In addition, introducing a microchannel heat sink structure can solve the thermal management problem of a three-dimensional integrated chip and will have a specific impact on the signal transmission efficiency in the chip. Therefore, when studying the thermal management of a three-dimensional integrated chip, it is essential to consider the signal integrity analysis of key interconnects components in the chip. Researchers have carried out relevant research on thermal management and signal integrity analysis of three-dimensional integrated chips.

For 3D integrated chip thermal management studies. Calvin R[4, 5] designed and manufactured a three-dimensional integrated chip cooling system, the manufacturing and assembly processes were introduced. This heat dissipation method is achieved by machining microchannel structures on the wafer and then assembling the wafers through a flip-flop soldering process. Moreover, electrical and fluid flow tests prove the feasibility of the system. Remco van ERP[6] designs microchannels and electronic devices on silicon substrates, significantly reducing the thermal resistance between chips. The manifold microchannel structure can achieve the heat dissipation of 1.7 kW/cm2. At present, it is only limited to single-layer chip cooling. D Bing[7], [8]built a simulation model of a processor with a micro-fin heat sink structure. The microfine flow and heat transfer characteristics are analyzed, and the temperature peak in the core area is reduced by optimization design. Meanwhile, the distribution of temperature field and thermal stress under liquid cooling conditions in the double-layered closed microchannel was studied, and the results showed that the alternating flow mode in the double-layered microchannel has little effect on temperature reduction. Shuai F[9, 10] proposes an embedded gradient-distributed micro-fin array heat sink. The heat transfer characteristics of micro fins with different densities are analyzed by numerical simulation, and experiments verify the heat transfer advantages of gradient micro fins. Pankaj Srivastava[11] analyzed the heat transfer characteristics of a double-layer microchannel structure by numerical simulation and studied the effects of different flow directions of the upper and lower layers and whether there are fins in the microchannel on the heat transfer performance. The results show that the microchannels with fin structure have the best heat transfer performance, and the flow direction of the upper and lower microchannels is counter-flow which helps to distribute the temperature

uniformly. The above research shows that microchannel cooling technology plays a vital role in the heat dissipation of electronic devices. In addition, the micro-fins heat sink structure has the advantages of large heat dissipation area, compact structure and high heat transfer efficiency. More importantly, TSV can be embedded in the micro fin to isolate the coolant. The micro-fins is embedded between the layers of the three-dimensional integrated chip as a heat sink structure and does not hinder the signal transmission in the vertical direction in the chip. Therefore, the application of micro fin structure has great research significance for the research of thermal management of three-dimensional integrated chip.

However, all the above studies set the heat flux on the fixed surface, and the actual situation needs to consider the electrothermal problem. Because during the operation of the actual chip, the electronics, transistors, and metal transmission lines interact with each other in the presence of an applied electric field, generating large amounts of heat through Joule heating. In addition, the change of temperature will change the thermal conductivity and electrical properties of the material and finally achieve the coupling equilibrium state. Therefore, the electrothermal coupling effect of the chip cannot be ignored. The above research does not consider the electrothermal coupling effect in the chip, whether it is a single-layer microchannel or double-layer structure. The analysis of chip electrothermal coupling is very important for the compatibility between internal components. For example, X P Wang[12] investigates multi-physics field effects during stacked TSV transients. The results show that the insulation parameters of TSV are sensitive to temperature. J Y Zhou [13] developed a finite element simulation model of a multilayer chip stack, including TSV and interconnecting micro bumps. The electrothermal effect of the whole chip under current load is analyzed. Meanwhile, the temperature field and electric field distribution of the chip and the thermal stress distribution at the solder joints are analyzed. J R Chai[14, 15] analyses the electrothermal effects of TSV arrays and considers the effect of Gaussian pulse voltage loading on the temperature of TSV arrays. A radial point interpolation method is proposed to analyze the transient electrothermal effect of TSV. The method is characterized by high computational accuracy and short computational time. Furthermore, the influence of TSV structural parameters on the electrothermal coupling effect is analyzed, and the electrothermal effects of bonded micro-bumps and transmission lines are considered. From the above study, it is clear that the large amount of heat generated in the chip due to Joule heating cannot be ignored. The effect on temperature changes is less by changing the internal structural parameters of the chip. Therefore, combining micro fins cooling technology is necessary to obtain greater cooling capacity. In the previous work, the author studied the electrothermal coupling effect of TSV embedded in micro fins when coolant flowed and analyzed the heat generation mechanism of TSV embedded in micro fins.

Meanwhile, the heat transfer performance of the micro-fin is improved by changing the structure of the micro-fins. Although microfluidics can take away a large amount of heat in the chip, it will also affect the parasitic parameters of semiconductor media and change the signal

transmission efficiency of interconnection components in the chip. Oh, Hanju[16–18] investigated the electrical characteristics of TSV in microfluidic pin-fin heat sinks. The results show that the microfluidic structure dramatically influences the electrical parasitic value of silicon substrate. Furthermore, the ring grounded TSV array is designed as a shielding structure in the micro fin to reduce the interference of coolant to signal transmission. In summary, the high-density integration of three-dimensional integrated chips and the high-frequency signal transmission characteristics bring severe challenges to chip development. Therefore, it is necessary to study the thermal management of a three-dimensional integrated chip and the signal integrity of key interconnect components in the chip. Unfortunately, research on such has not been reported.

Based on the above analysis, the research gap between the available literature and the present work could be concluded. The research on the electrothermal coupling of components in the chip allows solving thermal management problems from an actual situation. In addition, the study of chip thermal management and signal integrity of critical interconnect components has become key to ensuring the performance and reliability of electronic devices and the development of new electronic devices. Although many scholars have studied the heat transfer characteristics of micro fins, research into the thermal management of 3D IC and the signal integrity of critical interconnect components has not been carried out simultaneously. To realize this requirement, In this paper, the thermal management of 3D ICs and the signal integrity of key interconnected components in the chip are studied simultaneously, considering electrothermal coupling effects. The effects of TSV diameter, oxide thickness, micro-fine height, and radius on the chip's heat transfer performance and signal integrity were investigated. To balance the heat transfer performance of the heat sink in the chip and the signal integrity of the interconnected components, multi-objective optimization of two performance parameters was carried out. This paper achieves the optimal set of Pareto solutions by response surface-genetic algorithm optimization and verifying the reliability of the results.

Nomenclature

D_{tsv}	Silicon via diameter (um)
d_{sio2}	Insulation thickness (um)
R_{fin}	Micro fin diameter (um)
H_{fin}	Micro fin height (um)
D_h	Hydraulic diameter(m)
Lr	The perimeter of fluid inlet cross-section(m)
Ar	Microchannel cross-sectional area(m^2)
K(T)	Thermal conductivity
Rt	Total thermal resistance (k/w)
Re	Reynolds number

V	Voltage (v)
R	Resistance (Ω)
I	electric current (A)
σ(T)	Electro conductibility
S21	insertion loss
S11	Callback loss
Greek symbol	
μ_f	Fluid dynamic viscosity (Pa·s)
ρ	fluid density (kg/m^3)
β	temperature coefficient of conductor

2 Theoretical model

2.1 Simulation model description

In order to study the thermal management of three-dimensional integrated chips from a realistic perspective, a simulation model has been developed in this paper, as shown in Figure 1. where Figure 1(a) shows the entire model diagram. Previous studies by scholars [8]have shown that the heat transfer efficiency of staggering fins is better than that of parallel fins. Therefore, staggered micro fins are used as the research object in this research work. Figure 1 (b) shows the local calculation model due to the complex structure of the calculation model and multiple physical situations to be considered. Therefore, the local model was chosen as the simulation object to save computational time. Fig. 1 (c) is a sectional view of a local calculation model, which includes a silicon substrate, micro fins, TSV embedded in micro fins, bonding micro bumps between upper and lower chips, and fillers between chips. The filler is a BCB (Benzo-Cycle-Butene) polymer that bonds and strengthens the chip's upper and lower connections [19, 20]. The bonding between chips is through copper and copper at the TSV port under a specific temperature change. In addition, as shown in Fig. 1 (c), the outer surface of TSV is wrapped with an oxide layer to prevent the diffusion of copper metal into the silicon substrate, the diffusion of copper metal into silicon substrate will affect the parasitic electrical properties, and then affect the signal transmission.[21] The dimensions of the calculation model are shown in Table 1, where the horizontal and vertical spacing are equal.

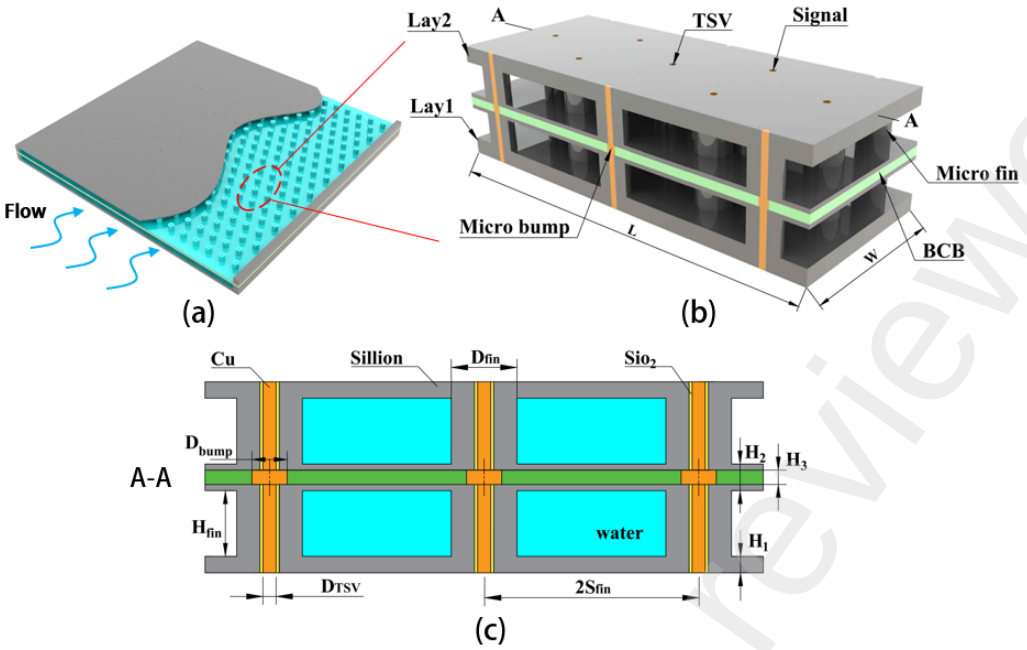

Fig.1 Schematic diagram of 3D integrated chip (a) Overall model (b) Local model (c) cutaway view

Table1 Structural parameters of 3D-IC electrothermal coupling model

parameters	Unit(mm)	parameters	Unit(mm)
Edge width (W)	1.0	Micro fin diameter (D_{fin})	0.2
Edge length (L)	2.5	Micro fin spacing (S_{fin})	0.5
Silicon substrate (H_1)	0.1	SiO_2 thickness (d_{sio2})	0.001
Micro fin height (H_{fin})	0.2	TSV diameter (D_{tsv})	0.04
Bonding layer (H_2)	0.1	BCB layer (H_3)	0.05

In this research work, deionized water flows into the channel of the micro-fine structure as a coolant, and the TSV is embedded in the micro-fin to insulate it from water. The fluid inlet temperature is 293.15K, and the outlet is the pressure outlet boundary condition. The external surface is set up as an adiabatic wall surface, as the chip is in a closed environment after encapsulation. In addition, the lower end of the TSV is connected to the voltage load and the upper end to the ground. To achieve coupled analysis of electrothermal effects and fluid heat transfer models, a three-dimensional IC embedded micro fin calculation model is established using Finite element analysis. Furthermore, in the calculation model, material parameters are sensitive to temperature changes, such as thermal conductivity K(T) and conductivityσ(T). When the temperature changes, the temperature-dependent properties of the material lead to the changes of conductivity and thermal conductivity, which then affect the heat production, and finally achieve the coupling steady state. By setting the material parameters with variable temperature, the influence of electrothermal coupling in the chip can be analyzed more specifically. The change of material properties with temperature can be expressed as：

$$X(T)=\sum_{n=0}^{4} C_n T^n, T \in (T_0, T_{\max}) \tag{1}$$

Where C represents the fitting coefficient of material properties. T is Temperature. Different material properties can be found in the literature[12].

2.3 Governing equations

In this paper, the physical fields of the model include heat conduction, heat convection, and electromagnetic heat, and the heat is Joule heat generated by applying voltage load TSV. Besides, In the simulation calculation, it is assumed that the fluid flow model in the 3D IC embedded micro fin is laminar flow. The density does not change when the fluid moves, and only heat conduction and convective heat transfer are considered in the process of heat conduction. By assuming the flow mode, the governing equation can be expressed as follows [22, 23]:

$$\nabla \cdot (\rho \cdot U) = 0 \tag{2}$$

Where ρ is the density of coolant, U is viscosity.

$$\nabla \cdot (\rho \cdot C_p \cdot U \cdot T_f) = \nabla \cdot (K_f \cdot \nabla \cdot T_f) \tag{3}$$

$$\nabla (\rho \cdot U \cdot U) = -\nabla P + \nabla \cdot (\mu \cdot \nabla \cdot U) \tag{4}$$

Where C_p is the specific heat capacity, P is the pressure, T_f is the fluid temperature, K_f is the fluid thermal conductivity.

For solid domain, the energy equation is expressed as:

$$\nabla \cdot (K\mathrm{s} \cdot \nabla \cdot T\mathrm{s}) = 0 \tag{5}$$

Where K_S is the thermal conductivity of the solid domain.

In addition, the electrothermal coupling effect is an interactive process. As current is applied to the TSV, a large amount of heat is generated due to Joule heat, and the increase in temperature leads to a decrease in the resistivity of the TSV, which in turn affects Joule heat eventually reaches coupling equilibrium. Meanwhile, the change of temperature will affect the change of material parameters such as conductivity, affect the electric field, interact with each other and finally achieve stability. In this regard, the equation of electric heat generation can be obtained as:

$$R(\mathrm{t}) = [1 + \beta \cdot T(\mathrm{t})] \cdot R_0 \tag{6}$$

$$P(t) = I(t) \bullet I(t) \bullet R(\mathrm{t}) \tag{7}$$

Where *R*, *β*, *T*, *P*, *I*, and *t* are the resistance, temperature coefficient of conductor, temperature, Thermal power consumption, electric current, and time.

2.4 Analysis parameters

In this work, the flow velocity of the fluid inlet is estimated using the calculation formula of the Reynolds number. For the present fluid calculation model, the micro-fine structure micro-channel inlet Reynolds number can be expressed as:

$$\mathrm{Re} = \frac{\rho v D_h}{\mu_f} \tag{8}$$

Re can describe the fluid flow state. It can be seen from the formula that re is directly proportional to ρ fluid density), v (fluid inlet velocity), D_h (hydraulic diameter), and inversely

proportional to μ_f(dynamic viscosity), Moreover, D_h can be expressed as：

$$D_h = \frac{4Ar}{Lr} \tag{9}$$

The average Nusselt number (Nu) is used to reflect the heat transfer performance of the microchannel heat sink and can be expressed as:

$$Nu_{avg} = \frac{h_{avg} \cdot D_h}{K_f} \tag{10}$$

$$h_{avg} = \frac{q_{w,avg}}{(T_{w,avg} - T_{f,avg})} \tag{11}$$

Where Nu_{avg} is the average Nusselt number of the microchannel heat sink, h_{avg} is the average heat transfer coefficient of the fluid, K_f is the thermal conductivity of the fluid. $q_{w,avg}$ is the average heat flux density of the wall. $T_{w,avg}$ and $T_{f,avgare}$ the average temperature of the chip surface and fluid, respectively.

In this research work, the total thermal resistance Rt[24] of the 3D IC is defined as：

$$Rt = \frac{\Delta T \max}{Q} = \frac{T \max - Tin}{Q} \tag{12}$$

Where T_{max} is the maximum temperature in the calculation model, T_{in} is the fluid inlet temperature, and Q is the total thermal power consumption in the calculation model.

The signal integrity is the quality of the signal in the transmission path. The transmission path is not limited to wires but includes the components that carry the signal[25, 26]. This research mainly takes TSV as the signal transmission carrier, and the signal transmission process needs to follow the transmission line theory[27]. The signal transmission needs a transmission path and returns the path. Therefore, the typical signal transmission mode is adopted, and the ground signal (G-S) paired TSV is taken as the research object. The S parameter can describe the signal integrity index, and the matrix equation of the S parameter can be defined as:

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix} \tag{13}$$

The matrix equation's parameters S11, S22, S21, and S22 represent the relationship between the incident wave and the reflected wave at each port. According to a Two-port network diagram shown in Fig. 2, the incident wave A1 at port 1 causes the reflected wave B1, and the rest of the energy is transmitted to port 2. Similarly, the incident wave A2 and the reflected wave B2 at port 2 transmit the rest of the energy to port 1.

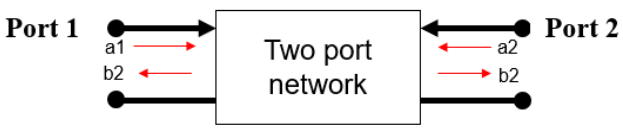

Fig.2 Two-port network

Where S11 represents the ratio of the reflected sinusoidal signal at port 1 to the input sinusoidal signal, in engineering applications, the smaller the S11 value, the smaller the network reflection loss; S21 represents the ratio of the sinusoidal signal received at port 2 to the input sinusoidal signal

at port 1. The greater the S21 value, the smaller the signal transmission loss. This paper mainly considers the S21 parameter：

$$S11 = \frac{b1}{a1}; S21 = \frac{b2}{a1} \tag{14}$$

2.5 Simulation method validation

The current research work investigates the heat transfer characteristics of micro fins and the electrothermal coupling effect of TSVs embedded in micro fins. A voltage load is applied to the TSV, and the generated heat is used as the heat source. For similar simulation methods. The simulation model of heat transfer in microchannel fluids under similar conditions was developed, the pressure drop and Nu values at different flow rates are calculated and compared with previous references[28]. The comparative results are shown in Figure 3, where the numerically simulated Nu and pressure drop values are consistent with the results in Ref. The numerical simulation results will be slightly different from the reference literature results due to deviations and unavoidable errors in the model structure parameters from the experimental specimen. Moreover, The electrothermal coupling method can set the temperature change material in the chip [29]. Therefore, the simulation method can be applied to this research work.

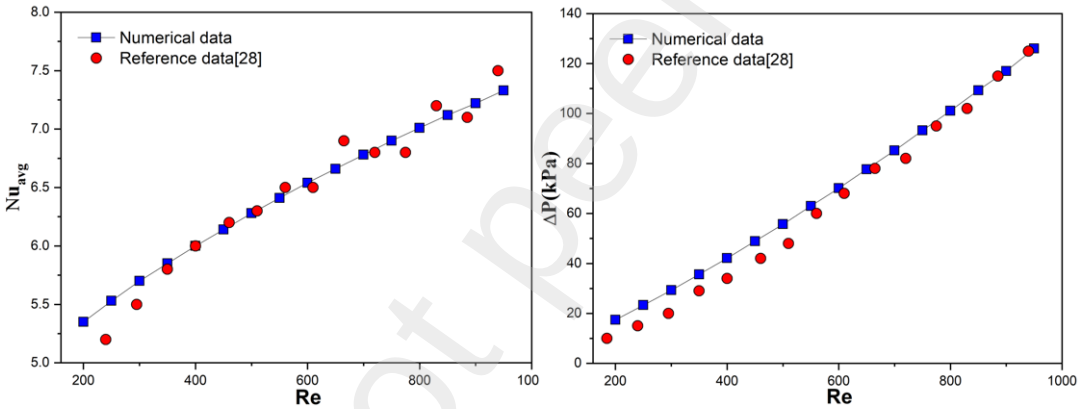

Fig.3 Comparison of numerical result and experimental result.

On the other hand, the number of grids in simulation calculation will affect the results. It is necessary to unify the number of meshes for different microchannel structure models to calculate the results accurately. The simulation model in 2.1section is used for grid independence analysis, and the pressure drops and maximum temperature value is calculated respectively based on the different number of grids. Moreover, the number of meshes of the simulation model is divided into 1.1, 1.2, 1.3, 1.4, 1.5, and 1.6 million, respectively. Due to the calculation configuration limitation, the grid with small errors can only be selected in the appropriate grid number range. Therefore, taking the calculation results of 1.6 million grids as the standard, the relative errors of the results of different grid numbers are compared respectively. The results show that the relative errors of pressure drop are 4.91%, 1.98%, 1.16%, 0.41%, 0.18%, respectively, and the maximum temperature relative errors are 1.15%, 0.71%, 0.5%, 0.24%, respectively. Therefore, a grid size of 1.5 million is used as the simulation criterion in this paper.

3 Results and discussion

3.1 Analysis of heat transfer characteristics

For the research of thermal management of 3D IC, the embedded microchannels between the chip layers can be used for cooling. To further investigate the heat transfer characteristics of micro fins in microchannels and the effects of TSV structure parameters, the effects of TSV diameter, oxide insulation thickness, micro fin height, and micro fin radius on the heat transfer performance of chips were analyzed, respectively. Other structural parameters remain unchanged when analyzing the influence of different structural parameter variables. Furthermore, the Reynolds coefficient of the coolant inlet changes from 200 to 1000. The results are shown in Figure 4. As shown in Fig. 4 (a), with the increase of RE, the thermal resistance of 3D IC with different insulation thickness decreases, and when it is at low Re, the thermal resistance drop is faster, and when it is at high re, the thermal resistance drop is slow. That is determined by the convective heat transfer capacity of the coolant. Increasing Re can improve the heat transfer capacity when the fluid is low Re. When the fluid is at high re, increasing the flow rate has a limited effect on improving the heat transfer capacity. In addition, under the same Re, the greater the thickness of the insulating layer, the higher the thermal resistance. That is because the thermal conductivity of the oxidized insulating layer of TSV is low, so the heat cannot be transmitted smoothly from TSV, Leading to an increase in the total thermal resistance of the 3D IC. As shown in Figure 4(b), with the increase of Re, the thermal resistance of three-dimensional integrated chips with different TSV diameters decreases, and when it is at low Re, the thermal resistance drop is faster, and when it is at high re, the thermal resistance drop is slow. Moreover, under the same Re, the larger the TSV diameter, the smaller the thermal resistance. That is because when the TSV diameter increases, the resistance decreases, and the Joule heat generated decreases. Furthermore, the voltage in the 3-D integrated chip remains constant, the resistance value decreases and the thermal power consumption increases. From the derivation of the thermal resistance formula, it can be seen that the total thermal resistance decreases as the thermal power consumption increases. As shown in Figure 4 (c), with Re's increase, the thermal resistance of three-dimensional integrated chips with different micro fin diameters decreases. Moreover, when it is at low Re, the thermal resistance drop is faster, and when it is at high Re, the thermal resistance drop is slow. The thermal resistance decreases with the increase of micro fin radius. That is because the increase of the micro fin radius between the channels narrows the fluid flow space, increases the local velocity, and also increases the fluid disturbance, which is beneficial to break the fluid boundary layer, to improve the convective heat transfer process between the fluid and the channel wall. However, compared with TSV structural parameters, the change of micro fin structural parameters has little effect on thermal resistance. Figure 4(d) shows the effect of micro-fine height variation on the total thermal resistance of the 3D IC. It can be seen from the figure that with the increase of Re, the total thermal resistance of the chip decreases with different micro fin heights, and when it is at low Re, the thermal resistance drop is faster, and when it is at high Re, the thermal resistance drop is slow. In addition, when Re is the same, the higher the fin height, the lower the total thermal resistance of the chip. That is because the height of the micro fin increases, the length of TSV increases, the resistance decreases and the Joule heat decreases, and the current decreases, the voltage load remains unchanged, the thermal power consumption increases, and the total thermal resistance decreases. Moreover, when the inlet height of the microchannel decreases, the inlet

velocity increases and the local temperature decreases so that the total thermal resistance is close when the height of the micro fin is 180um and 200um. In general, appropriately increasing the microchannel height can reduce the total thermal resistance of the chip.

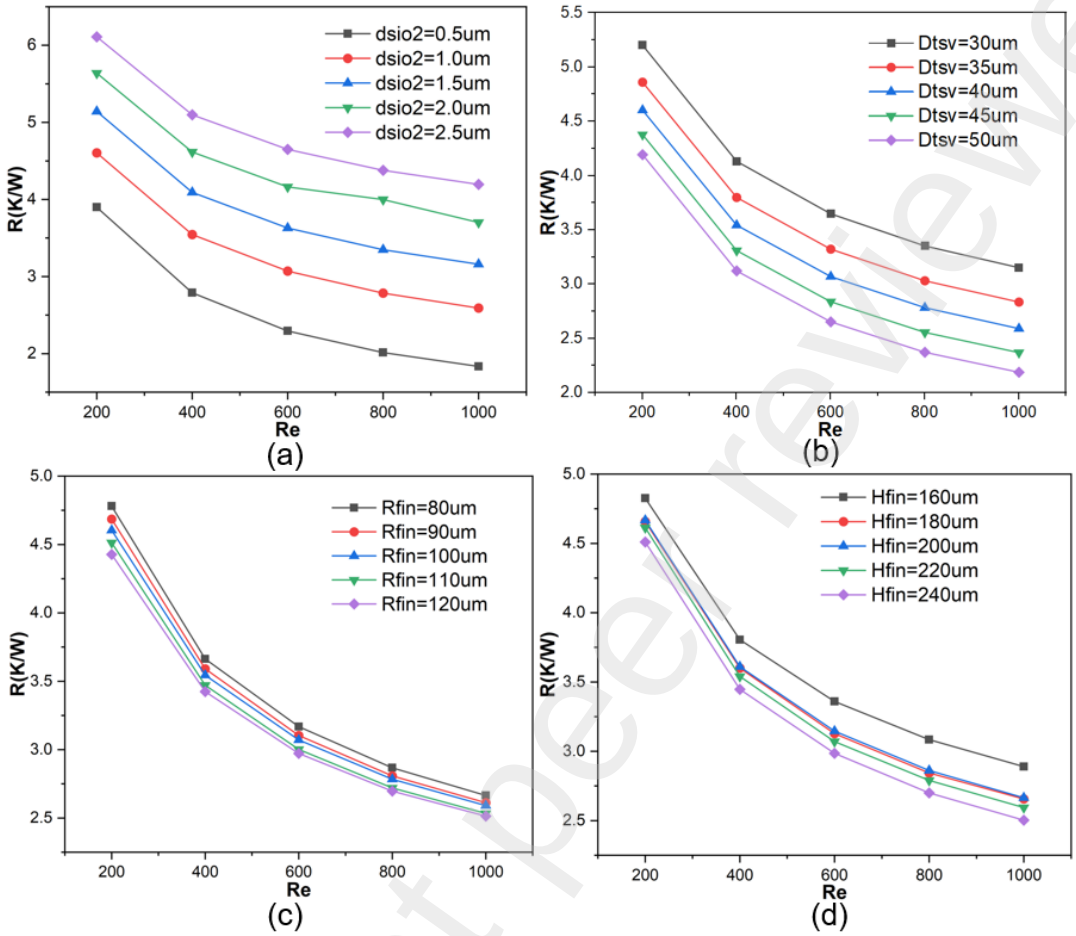

Fig.4 The effect of different structural parameters on thermal resistance with the change of Re(a) Influence of insulation thickness(b) Influence of TSV diameter (c) Influence of micro fin radius (d) Influence of micro fin height

3.2 Signal integrity analysis of TSV

In the high bandwidth signal transmission environment, the thermal management problem of 3D IC becomes more and more serious. Meanwhile, the research on the high-frequency characteristics of the chip also brings severe challenges. Furthermore, the introduction of microchannel structures can impact the high-frequency characteristics of 3D IC. Therefore, when studying thermal management issues, it is necessary to carry out signal integrity analysis of key interconnect components in the chip simultaneously as the signal integrity analysis in the chip is carried out for a standard network port. Thus, a pair of TSV signal transmission models are developed in this paper. As shown in Fig. 5, it is assumed that the upper and lower ports of TSV with on signal are connected to the load 50Ω, and the ground TSV is connected to the ground. The two groups of TSVs (G-S) form a signal transmission channel. The three-dimensional high-frequency electromagnetic simulation software HFSS is used to analyze the signal integrity of the model. Moreover, the length of the model is 1.5mm, and the width is 1mm. Other structural dimensions are consistent with the calculation model in Figure 1. As shown in Fig. 5 (b), the model

includes TSV, a silicon substrate, a BCB layer, and deionized water. For the electromagnetic simulation, the walls around the model are set to ideal magnetic conductor (PMC) boundary conditions, and the upper and lower ports of TSV are set as signal transmission and receiving ports through wave ports[17]. According to the equivalent circuit model, the difference from the conventional 3D IC is that microchannels replace some silicon substrates. When the microchannel is filled with deionized water, the parasitic electrical parameters in the silicon substrate change, and the total capacitance and electric conductance in the semiconductor material change, which affects the efficiency of signal transmission.

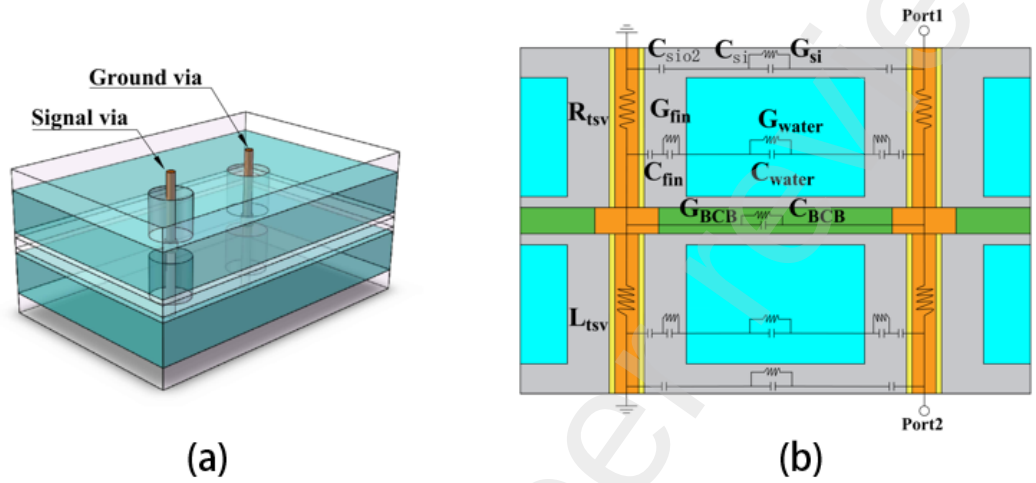

Fig.5 (a) Signal-ground TSV model in simulation (b) Equivalent circuit model

To investigate the influence of microchannel and TSV structure parameters on the signal integrity of key interconnect components of 3D IC. The effects of TSV diameter, oxide insulating layer thickness, micro fin height, and micro fin radius on the signal integrity of multilayer TSV signal transmission path in 3D IC were investigated. Furthermore, the signal transmission frequency is set from 1GHz to 20GHz. Furthermore, S21 (insertion loss) refers to the signal loss generated by the cable or element itself, which usually becomes the focus of researchers. Therefore, S21 is taken as the target value of this study, and the calculation results are shown in Figure 5. Fig. 5 (a) shows the influence of different TSV insulation layer thicknesses on S21 under different signal transmission frequencies. It can be seen from the figure that the insertion loss increases with the increase of signal transmission frequency, and the greater the thickness of the insulating layer, the smaller the insertion loss. That is because there is the parasitic capacitance between the insulating layers. When the thickness of the insulating layer increases, the capacitance also decreases, which reduces the charge leaked to the insulating layer during signal transmission. The reduction in parasitic capacitance of the silicon substrate facilitates signal transmission. Fig. 5 (b) shows the influence of different TSV diameters on S21 under different signal transmission frequencies. It can be seen from the figure that the insertion loss increases with the increase of signal transmission frequency. In addition, when the frequency is below 5GHz, the larger the TSV diameter, the greater the insertion loss. When the frequency is greater than 5GHz, the larger the TSV diameter, the smaller the insertion loss, and the greater the frequency, the greater the difference between different TSV diameters. That is because the increase of the TSV diameter compresses the transverse distance of the silicon fin, thereby increasing the parasitic capacitance in the fin. Therefore, the larger the TSV diameter, the greater the insertion loss. In addition, because there are micro bumps between chips. Moreover, the diameter of micro bumps is greater than the diameter of TSV. Therefore, the larger

the TSV diameter, the closer it is to the micro bump diameter, reducing the diameter jump in the signal transmission path and decreasing the insertion loss. Furthermore, when the signal transmission frequency is larger, the jump of diameter in the transmission path has a greater impact on the signal transmission efficiency. Fig. 5 (c) shows the influence of different micro fin radius on S21 under different signal transmission frequencies. It can be seen from the figure that the insertion loss increases with the increase of signal transmission frequency. In addition, with the increase of micro fin radius, the greater the insertion loss of signal transmission in TSV, This shows that the increase of the volume proportion of deionized water is conducive to the signal transmission in TSV, Fig. 5 (d) shows the influence of different Micro fin height on S21 under different signal transmission frequencies. It can be seen from the figure that the insertion loss increases with the increase of signal transmission frequency. In addition, at low frequencies, there is little difference in the effect of insertion loss for different micro-fin heights, and as the frequency increases, the difference in the effect of different micro-fin heights on the S21 value becomes greater, and the higher the micro fin height, the greater the insertion loss of signal transmission in TSV. That is because the length of TSV increases with the increase of micro fin height, and then the resistance value of TSV increases, resulting in the obstruction of signal transmission. At the same time, with the increase of micro fins, the capacity of silicon substrate also increases, resulting in the increase of parasitic capacitance and affecting signal transmission. It is clear from the analysis of the heat transfer characteristics and signals integrity of 3D ICs that the same structural parameters have different trends on the thermal resistance of the chip and the insertion loss values of the critical interconnect components. Therefore, it is vital to consider the signal integrity of the key interconnects components in the research of thermal management of 3D IC.

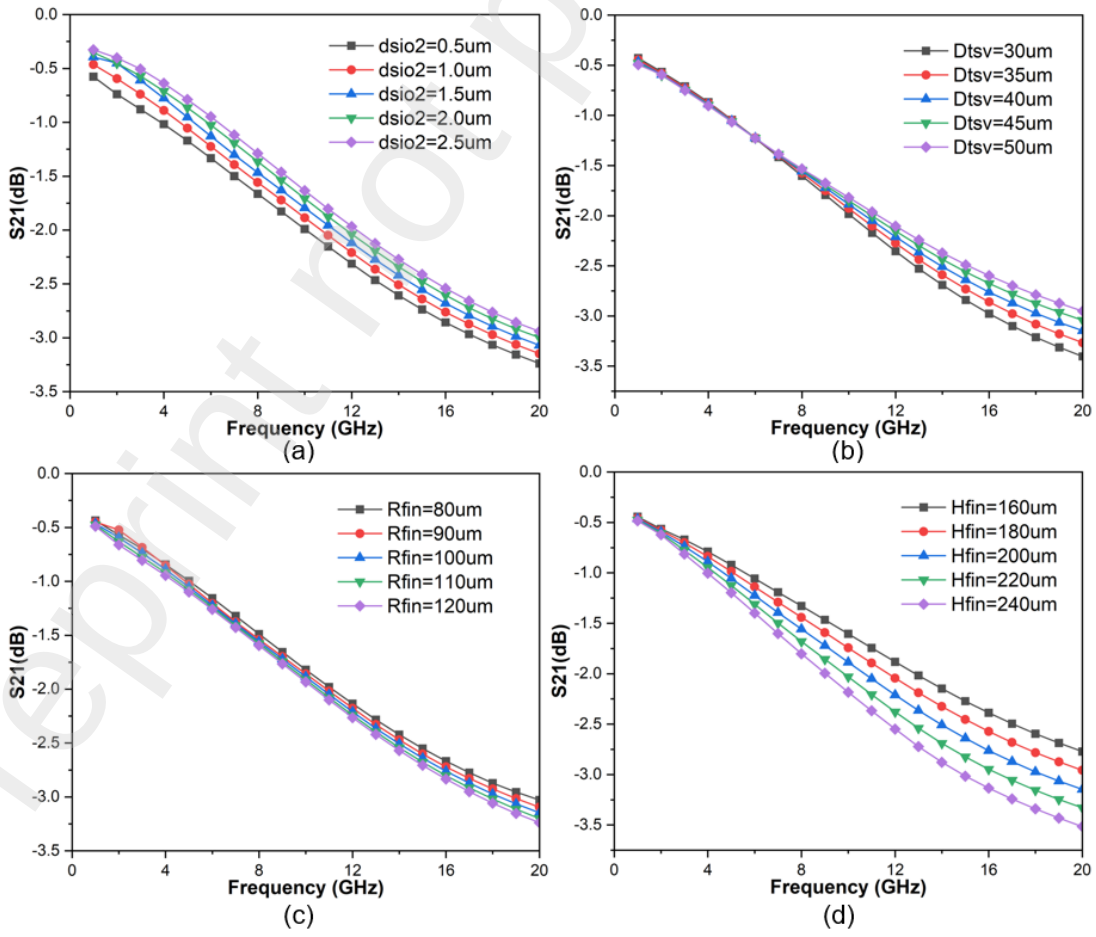

Fig.6 The effect of different structural parameters on S21 with the change of frequency (a) Influence of insulation thickness(b) Influence of TSV diameter (c) Influence of micro fin diameter (d) Influence of micro fin height

3.3 Multi-objective optimization design

Through the above analysis, the different structural parameters in a 3D integrated chip have different effects on thermal resistance and signal transmission and even have the opposite trend. Moreover, thermal management and signal integrity are essential performance parameters in chip design. To achieve better product design, multi-objective optimization of these two performance objectives is required. At present, for the multi-objective optimization analysis of microchannel thermal management, domestic and foreign scholars mainly analyze the thermal resistance and Pumping power consumption of the heat sink structure[24, 31–34]. However, multi-objective optimization of signal integrity of TSVs in chips and thermal resistance of chips has not yet been carried out. In this paper, multi-objective optimization of the performance of two objectives is performed to optimize both the heat transfer performance and the signal transmission quality of key interconnect components in a 3D integrated chip. The optimization process is shown in Figure 7. In this research work, the optimization objectives are the thermal resistance of three-dimensional integrated chip and the insertion loss(S21) of TSV in the chip, and the influencing factors are TSV diameter (D_{tsv}), insulation thickness (d_{sio2}), micro fin radius (R_{fin}) and micro fin height (H_{fin}). Secondly, the multi-factor experimental design is carried out by response surface analysis. The regression fitting equation for the target value and the impact factor was established. Then, the fitting equation is verified to judge the goodness of fit of the prediction equation. The fitted objective function is optimized and analyzed by the NSGA-2 optimization algorithm. After reaching the convergence requirement, Pareto optimal solutions are set. The optimal combination of solutions can be chosen according to the requirements, and finally, the optimal combination is verified.

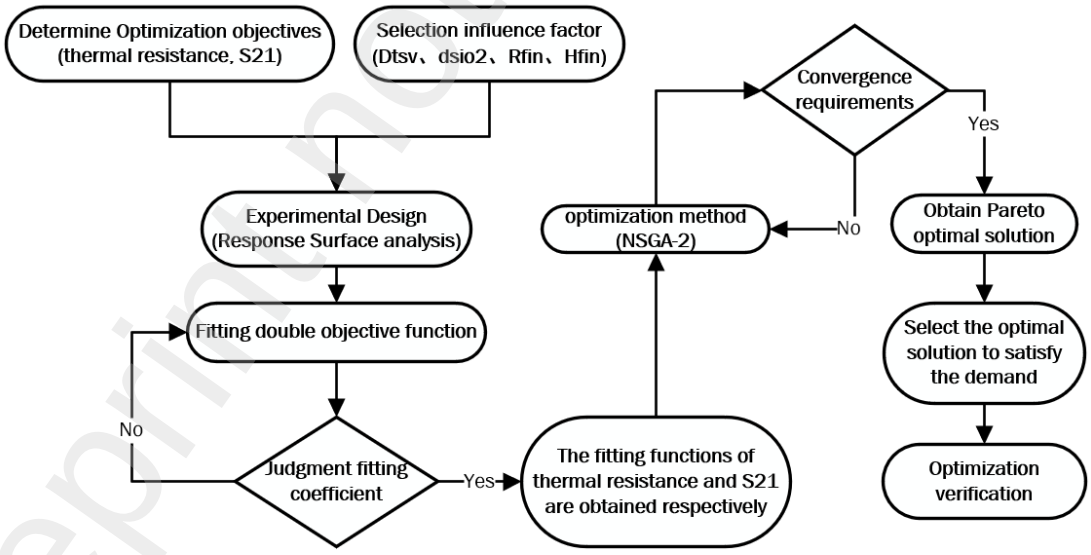

Fig.7 Multi-objective optimization process

3.3.1 Objective function analysis

In this paper, the experimental design was carried out by the response surface methodology, and a four-factor, five-level analysis was used in the experimental design. The four factors that have

a significant influence on the optimization objectives in 3D IC are TSV diameter (D_{tsv}), insulation thickness (d_{sio2}), micro fin radius (R_{fin}), and micro fin height (H_{fin}), and determine the range of values for each impact factor. Factor levels are shown in Table 3. The central combinatorial design approach based on response surface analysis allows accurate experimental results from a small number of experiments[32, 34]. The experimental design scheme is shown in Table 4. The calculation models of different structural parameter combinations are established, and the corresponding target values are obtained by electrothermal coupling heat transfer analysis and signal integrity analysis of key interconnection components. The results are shown in Table 4 for the thermal resistance and S21 values. Based on the calculated values in Table 4, the second-order regression models were developed, and the goodness-of-fit analysis was performed on the developed regression models. The fitted regression equations are (12), (13). In addition, when establishing the regression model, the model's error can be analyzed by the parameter R-square (R^2). The closer the value of R^2 is to 1, the closer the predicted model value is to the actual sample value[35]. Fig. 8 compares the actual value and the predicted value of the thermal resistance and the S21 parameter value. The R^2 values of thermal resistance and S21 are 0.9975 and 0.9993, respectively. Moreover, as shown from figure 8, the values on the diagonal dotted line in the figure represent the points where the predicted value is equal to the actual value. As can be seen from the graph, all samples fall almost diagonally, indicating that the optimisation objective's predicted value matches the actual value. The above results are consistent with the R^2 values, which proves the regression model's reliability.

$$\begin{aligned} Rt = {} & 4.3043 - 0.072037D_{tsv} + 3.57112d_{sio2} + 6.37812H_{fin} + 9.98542E-3R_{fin} + 2.7375E-4D_{tsv}^{\ 2} \\ & -0.26763d_{sio2}^{\ 2} - 2.16406E-5H_{fin}^{\ 2} - 7.65625E-5R_{fin}^{\ 2} - 0.031525D_{tsv}d_{sio2} \\ & +1.15625E-4D_{tsv}H_{fin} + 9.375E-5D_{tsv}R_{fin} - 2.08125E-3d_{sio2}H_{fin} \\ & -1.875E-4d_{sio2}R_{fin} - 3.78125E-5H_{fin}R_{fin} \end{aligned} \tag{15}$$

$$\begin{aligned} S21 = {} & -0.027865 + 0.010321D_{tsv} + 0.094125d_{sio2} - 0.011518E-3H_{fin} \\ & -7.52708E-3R_{fin} - 8.625E-5D_{tsv}^{\ 2} - 0.011625d_{sio2}^{\ 2} + 8.35938E-6H_{f}in^{2} \\ & +4.09375E-5R_{fin}^{\ 2} - 3.75E-4D_{tsv}d_{sio2} + 3.4375E-5D_{tsv}H_{fin} \\ & -1.625E-5D_{tsv}R_{fin} + 8.4375E-4d_{sio2}H_{fin} - 3.625E \\ & -4d_{sio2}R_{fin} - 1.21875E-5H_{fin}R_{fin} \end{aligned} \tag{16}$$

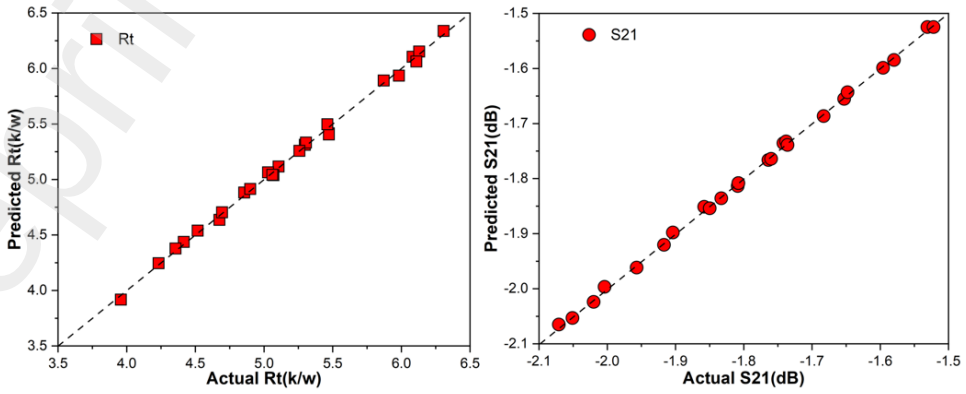

Fig.8 Comparison between predicted results and actual results

Table3 Factor level for RSM design

NO.	Factors	Level				
		-α	-1	0	+1	+α
1	D_{tsv}	30	35	40	45	50
2	d_{sio2}	0.5	1	1.5	2	2.5
3	R_{fin}	80	90	100	110	120
4	H_{fin}	160	180	200	220	240

Table4 RSM method design and response results

NO.	Parameters				Response Value	
	D_{tsv}(um)	d_{tsv}(um)	H_{fin}(um)	R_{fin}(um)	R(K/W)	S21(dB)
1	35	1	110	180	4.856	-1.809
2	45	1	90	180	4.517	-1.683
3	45	1	90	220	4.415	-1.957
4	50	1.5	100	200	4.675	-1.742
5	40	1.5	100	200	5.258	-1.808
6	40	1.5	80	200	5.472	-1.738
7	45	2	90	220	5.297	-1.764
8	45	2	110	220	5.106	-1.833
9	40	1.5	120	200	5.069	-1.858
10	35	2	90	180	6.307	-1.596
11	40	1.5	100	160	5.472	-1.531
12	40	1.5	100	200	5.258	-1.808
13	35	1	110	220	4.695	-2.108
14	35	1	90	180	5.029	-1.76
15	30	1.5	100	200	5.982	-1.904
16	40	1.5	100	200	5.258	-1.808
17	45	2	110	180	5.306	-1.58
18	35	2	90	220	6.082	-1.85
19	40	1.5	100	200	5.258	-1.808
20	40	1.5	100	200	5.258	-1.808
21	35	1	90	220	4.899	-2.051
22	45	1	110	220	4.233	-2.02
23	40	1.5	100	240	5.061	-2.071
24	35	2	110	220	5.871	-1.917
25	35	2	110	180	6.13	-1.653
26	45	2	90	180	5.462	-1.522
27	40	2.5	100	200	6.11	-1.648
28	40	0.5	100	200	3.957	-2.004
29	40	1.5	100	200	5.258	-1.808
30	45	1	110	180	4.356	-1.736

3.3.2 Genetic algorithm optimization design

The double objective regression model was obtained from the above research work. Then, the model was optimized using a genetic algorithm (NSGA-2), and the genetic algorithm is an adaptive

global optimization search algorithm that simulates the genetic and evolutionary process of organisms in the natural environment. With the help of genetics, individuals with higher adaptability are selected through the action mechanism of natural selection, heredity, and variation. NSGA-2 is an improved version of the genetic algorithm. The optimization algorithm introduces non-dominated sorting, congestion comparison, and elite strategy, making the optimization process more accurate[36]. This paper optimizes the total thermal resistance(Rt) and TSV insertion loss(S21) in 3D IC. Optimization aims to minimize the total thermal resistance and the insertion loss of interconnected components. However, when the total thermal resistance is improved, the signal transmission insertion loss of the interconnected components in the chip is worsened by the same structure in a three-dimensional integrated chip. The solution set obtained is Pareto optimal solution[36]. Therefore, the set of relative optimal solutions of two target values can be obtained after optimization by the genetic algorithm. In this research work, the genetic algorithm parameters are set as follows: The optimal individual coefficient is 0.3, the population size is 200, the maximum evolution algebra is 200, the stop algebra is 200, and the fitness deviation is 1E-100[37]. Furthermore, to select the optimal solution from the set of optimal solutions to match individual requirements, a multi-attribute decision-making method can be used to solve. In this case, the Technique for Order Preference by Similarity to Ideal Solution (TOPSIS) was used to decide on the set of optimal solutions. This method normalizes the optimal solutions and selects the best combination of optimizations by assigning weights. The Pareto solution set is sorted and selected by multi-attribute objectives [38]. After optimization, 100 sets of Pareto optimal solutions are obtained, as shown in Figure 9. To optimize the thermal resistance(Rt) of 3D IC and the insertion loss(S21) of key interconnect components, the two target weights W are determined to be 0.5. The best optimization point is obtained through calculation, as shown in Figure 9(a). The asterisk in the figure is the optimal solution. The thermal resistance of the optimal solution is 3.7549k/w, and the S21 value is -1.567dB. The structural parameter combinations corresponding to the optimal solution (D_{tsv}, d_{sio2}, H_{fin}, R_{fin}) are 49.993um、0.5168um、161.41um、81.22um, respectively. Moreover, when w is 0 and 1, the value is the head and tail port of the optimal solution. Figure 8(b)(c) shows the values of the different structural parameters corresponding to the Pareto optimal solution, the horizontal coordinates are the number of optimal solutions. It can be seen from figure 8(b), the TSV diameter distribution corresponding to the optimal solution is around 50um, and the oxide thickness distribution is between 0.5um and 2.5um. This indicates that the TSV diameter is beneficial for heat transfer and signal transmission at the maximum, while the oxide thickness affects the two target properties in different trends, so the optimal solution is more widely distributed. As can be seen from Figure 8(c), the optimal solution corresponds to a micro-fin height distribution at 162um and a micro-fin radius distribution at 82um, which indicates that a smaller micro-fin height and diameter can achieve better heat transfer and signal transmission quality. In this paper, the sorting method of approximate ideal solution is to obtain the weight of total thermal resistance Rt and insertion loss S21 in the chip by objectively analyzing the Pareto optimal solution set. In practical problems, we need to select the weight of the two optimization objectives according to the needs to get the best parameter combination.

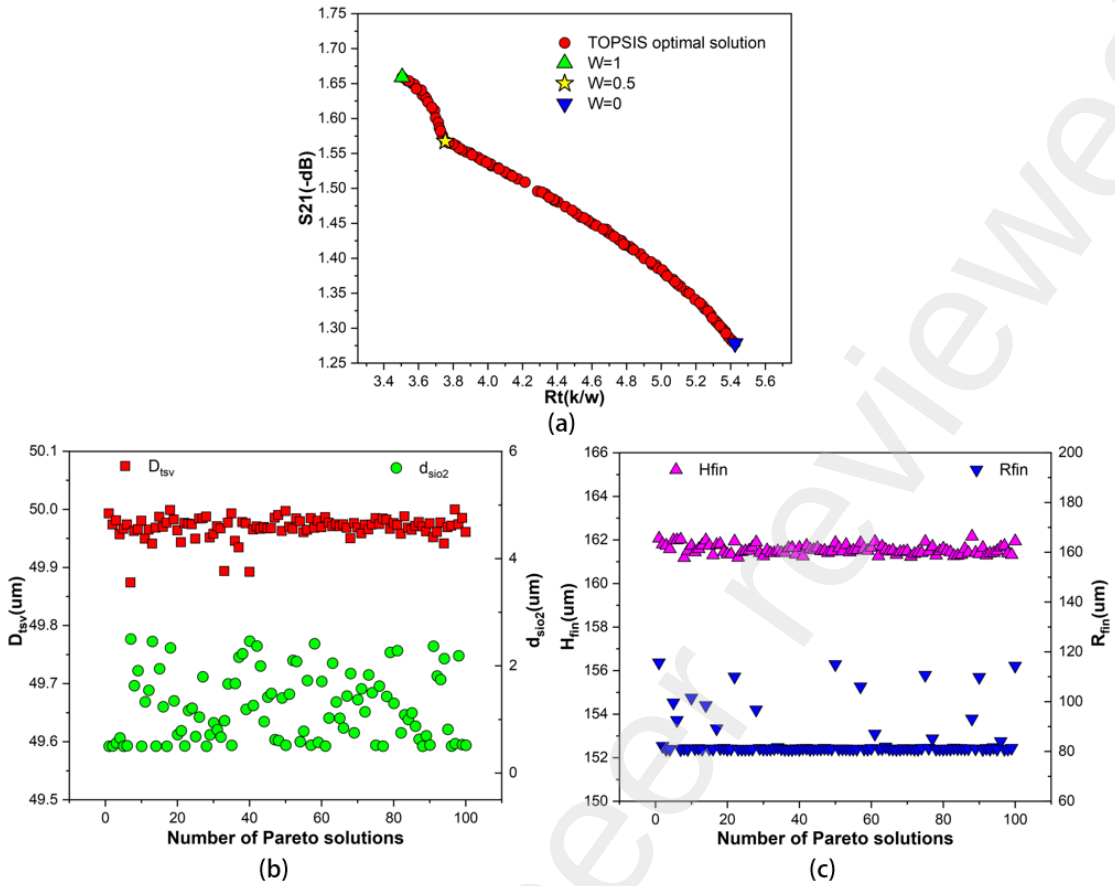

Fig.9 Pareto optimal solutions and corresponding variable parameters (a) Pareto optimal solution (b) TSV diameter and oxide layer thickness (c) Micro-fin height and radius

3.4 Validation of optimization results

The above research work filtered the optimal set of Pareto solutions by the TOPSIS decision method, and the optimal combination of solutions to satisfy individual requirements was obtained. In this paper, the Pareto solutions with different thermal resistance weights are selected to verify the reliability of the optimization results. As shown in Table 5, W represents the thermal resistance weight distribution ratio in the Pareto optimal solution set and the experimental design results in section 3.3.1, respectively. W is 1, which means that the thermal resistance of the three-dimensional integrated chip is the lowest in the actual design. The experimental design value corresponds to No. 9, W is 0, which means that the thermal resistance of the three-dimensional integrated chip is the lowest in the actual design. The experimental design value corresponds to No. 9. When W is 1, the primary consideration in the actual design is the optimal signal transmission efficiency of the 3D IC. The experimental design value corresponds to No. 29. Moreover, W is 0.5. The experimental design value corresponds to No. 4. The actual values in Table 5 represent the TOPSIS decision-making selection of the experimental results in Table 4. The actual values show the effectiveness of the TOPSIS decision-making method. In addition, the column of improvement rate represents the improvement efficiency relative to the actual value after optimization. It can be seen from the data in the table that the thermal resistance of 3D IC and the insertion loss of key interconnection components in the chip have been greatly improved after optimization. When the thermal resistance is taken as the maximum weight, the thermal resistance is increased by 11.4%. When the thermal

resistance weighting is minimal, the insertion loss of interconnected components in the chip is reduced by 16.01%. When the weight of thermal resistance and insertion loss is the same, the thermal resistance is reduced by 13.8%, and the insertion loss is reduced by 4.43%. Furthermore, the structural combinations corresponding to the above optimization solutions are simulated. The simulated thermal resistance(Rt) and insertion loss(S21) is compared with the optimized predicted values. The error column in Table 5 represents the error value between the verification result and the optimization prediction result under different thermal resistance weights. The error analysis shows little difference between the verification results and the optimization prediction results. The relative deviation of thermal resistance and insertion loss is less than 8.1%, especially the insertion loss deviation of chip signal transmission path is less than 0.7%. In this regard, this paper demonstrates the feasibility of the optimization method used to optimize the thermal resistance and signal transmission path insertion loss of 3D integrated chips. In addition, Figure 10 shows a cloud of temperature distributions for different thermal resistance weights in the set of optimized solutions. As can be seen from the figure, when the thermal resistance weight is the largest, the thermal resistance optimization value is the lowest, and the temperature peak in the chip is also the smallest. When the thermal resistance weight is 0, the thermal resistance is higher, and the temperature peak in the chip is the highest. That is because the TSV insulation is beneficial for signal transmission, but the low thermal conductivity of the insulation makes it difficult to conduct temperature. The validation of the optimization results illustrates the reliability of the optimization method. Moreover, the research work in this paper can provide reliable theoretical guidance for the thermal management of 3D IC and the compatible design of signal integrity of key interconnected components in chips.

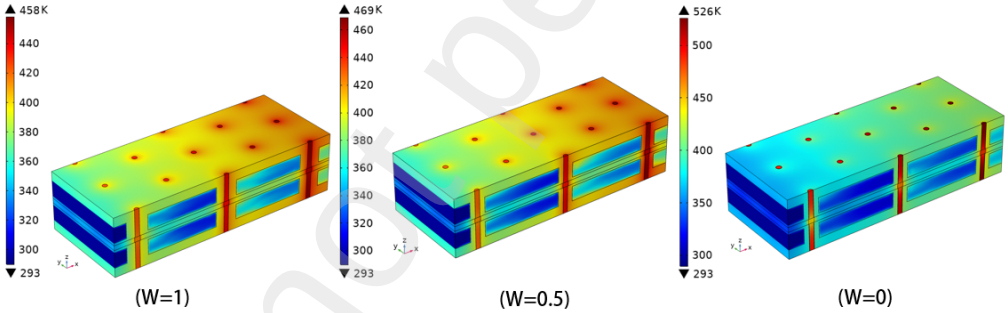

Fig.10 Temperature field distribution under different thermal resistance weights (W=0, W=0.5, W=1) in the optimization solution set

Table.5 Feasibility analysis of the optimization results

W (thermal resistance)		0	0.5	1
Optimized value	Rt(k/w)	5.2478	3.7024	3.4923
	S21(dB)	-1.4077	-1.7203	-1.8081
Actual value	Rt(k/w)	5.411	4.323	3.957
	S21(dB)	-1.593	1.817	-2.004
Validation value	Rt(k/w)	5.611	4.001	3.771
	S21(dB)	-1.398	-1.7299	-1.7988
Improvement rate	Rt(k/w)	3.02%	14.36%	11.74%
	S21(dB)	11.63%	5.32%	9.78%
Error	Rt(k/w)	6.92%	8.07%	7.98%
	S21(dB)	0.69%	0.56%	0.51%

4 Conclusions

This paper investigates the thermal performance of heat sinks and the signal integrity of key interconnect components in 3D IC. A 3D integrated chip electrothermal coupling simulation model with a micro-fine heat sink and a multilayer TSV electromagnetic simulation model is developed. The influence of different structural parameters on the total thermal resistance of the chip and the signal transmission efficiency of the interconnected components is revealed. A response surface-genetic algorithm optimization method is used to obtain both the best heat transfer performance and signal transmission efficiency of 3D IC. The main conclusions are as follows:

(1) The TSV diameter has the same tendency to influence the thermal resistance of the chip and the signal transmission quality of the interconnected components, while the oxide thickness, the height, and radius of the micro fins have the opposite tendency;

(2) The total thermal resistance of 3D ICs and the insertion loss of key interconnect components are optimized using a response surface-genetic algorithm, and 100 sets of Pareto optimal solutions are obtained after optimization;

(3) The optimal solution set is screened by the TOPSIS multi-attribute decision-making method. When the thermal resistance is chosen as the maximum weight, the total chip thermal resistance is reduced by 11.4%. With signal transmission as the maximum weight, the insertion loss is reduced by 16.01%. When the weight ratio of the two target values is the same, the total thermal resistance is reduced by 13.8%, and the insertion loss is reduced by 4.43%;

(4) The optimization results are verified, and the error is analyzed. The results show that the deviation between the optimized total thermal resistance and the actual results is less than 8.1%, and signal transmission quality is less than 0.7%. Therefore, the reliability and superiority of the optimization method are proved.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant NO. 52006102), the Natural Science Foundation of Jiangsu Province (No. BK20200489).

References

[1] R. K. Cavin, P. Lugli, and V. V. Zhirnov, "Science and engineering beyond Moore's law," *Proc. IEEE*, vol. 100, no. SPL CONTENT, pp. 1720–1749, 2012.

[2] S. H. Lee, K. N. Chen, and J. J. Q. Lu, "wafer-to-wafer alignment for three-dimensional integration: A review," *J. Microelectromechanical Syst.*, vol. 20, no. 4, pp. 885–898, 2011.

[3] S. Wang *et al.*, "Low-loss through Silicon Vias (TSVs) and transmission lines for 3D optoelectronic integration," *Microelectron. Eng.*, vol. 238, no. June 2020, p. 111509, 2021.

[4] C. R. King, D. Sekar, M. S. Bakir, B. Dang, J. Pikarsky, and J. D. Meindl, "3D stacking of chips with electrical and microfluidic I/O interconnects," in *Proceedings - Electronic Components and Technology Conference*, 2008, pp. 1–7.

[5] C. R. King, J. Zaveri, M. S. Bakir, and J. D. Meindl, "Electrical and fluidic C4 interconnections for inter-layer liquid cooling of 3D ICs," in *Proceedings - Electronic Components and Technology Conference*, 2010, pp. 1674–1681.

[6] R. van Erp, R. Soleimanzadeh, L. Nela, G. Kampitsis, and E. Mattioli, "Co-designing electronics with microfluidics for more sustainable cooling," *Nature*, vol. 585, no. 7824, pp. 211–216, 2020.

[7] B. Ding, Z. H. Zhang, L. Gong, C. Y. Zhu, and M. H. Xu, "Coupling management optimization of temperature and thermal stress inside 3D-IC with multi-cores and various power density," *Int. Commun. Heat Mass Transf.*, vol. 120, no. XXXX, p. 105021, 2021.

[8] B. Ding, Z. H. Zhang, L. Gong, M. H. Xu, and Z. Q. Huang, "A novel thermal management scheme for 3D-IC chips with multi-cores and high power density," *Appl. Therm. Eng.*, vol. 168, no. July 2019, p. 114832, 2020.

[9] S. Feng, Y. Yan, H. Li, Z. Yang, L. Li, and L. Zhang, "Theoretical and numerical investigation of embedded microfluidic thermal management using gradient distribution micro pin fin arrays," *Appl. Therm. Eng.*, vol. 153, no. November 2018, pp. 748–760, 2019.

[10] S. Feng, Y. Yan, H. Li, F. Xu, and L. Zhang, "Heat transfer characteristics investigations on liquid-cooled integrated micro pin-fin chip with gradient distribution arrays and double heating input for intra-chip micro-fluidic cooling," *Int. J. Heat Mass Transf.*, vol. 159, 2020.

[11] P. Srivastava, R. I. Patel, and A. Dewan, "A study on thermal characteristics of double-layered microchannel heat sink: Effects of bifurcation and flow configuration," *Int. J. Therm. Sci.*, vol. 162, no. January 2020, p. 106791, 2021.

[12] X. P. Wang, W. Y. Yin, and S. He, "Multi-physics characterization of transient electrothermal-mechanical responses of through-silicon vias applied with a periodic voltage pulse," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1382–1389, 2010.

[13] J. Y. Zhou, Z. Wang, C. Wei, J. Bin Fei, C. B. Ke, and X. P. Zhang, "Three-dimensional Simulation of Effects of Electro-Thermo-Mechanical Multi-physical Fields on Cu Protrusion and Performance of Micro-bump Joints in TSVs Based High Bandwidth Memory (HBM) Structures," *Proc. - Electron. Components Technol. Conf.*, vol. 2020-June, pp. 1659–1664, 2020.

[14] J. Chai, G. Dong, and Y. Yang, "Nonlinear electrothermal model for investigating transient temperature responses of a through-silicon via array applied with Gaussian pulses in 3-D IC," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 1032–1040, 2019.

[15] J. Chai, G. Dong, and Y. Yang, "An effective approach for thermal performance analysis of 3-d integrated circuits with through-silicon vias," *IEEE Trans. Components, Package. Manuf. Technol.*, vol. 9, no. 5, pp. 877–887, 2019.

[16] H. Oh, "Heterogeneous Integrated Microsystems With Nontraditional Through-Silicon Via Technologies," *IEEE Trans. Components, Package. Manuf. Technol.*, vol. 7, no. 4, pp. 1–9, 2017.

[17] H. Oh, M. Swaminathan, G. S. May, and M. S. Bakir, "Electrical Circuit Modeling and Validation of Through-Silicon Vias Embedded in a Silicon Microfluidic Pin-Fin Heat Sink Filled with Deionized Water," *IEEE Trans. Components, Package. Manuf. Technol.*, vol. 10, no. 8, pp. 1337–1347, 2020.

[18] H. Oh, X. Zhang, G. S. May, and M. S. Bakir, "High-Frequency Analysis of Embedded Microfluidic Cooling within 3-D ICs Using a TSV Testbed," in *Proceedings - Electronic Components and Technology Conference*, 2016, vol. 2016-August, pp. 68–73.

[19] C. Li, X. Wang, S. Song, and S. Liu, "21-Layer 3-D Chip Stacking Based on Cu-Sn Bump Bonding," *IEEE Trans. Components, Package. Manuf. Technol.*, vol. 5, no. 5, pp. 627–635,

2015.

[20] I. Comart, C. Cetintepe, E. Sagiroglu, S. Demir, and T. Akin, "Development and Modeling of a Wafer-Level BCB Packaging Method for Capacitive RF MEMS Switches," vol. 28, no. 4, pp. 724–731, 2019.

[21] Q. Chen, C. Huang, D. Wu, Z. Tan, and Z. Wang, "Ultralow-capacitance through-silicon vias with annular air-gap insulation layers," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1421–1426, 2013.

[22] Z. Wan and Y. Joshi, "Pressure drop and heat transfer characteristics of pin fin enhanced micro gaps in single-phase microfluidic cooling," *Int. J. Heat Mass Transf.*, vol. 115, pp. 115–126, 2017.

[23] D. Yang, Z. Jin, Y. Wang, G. Ding, and G. Wang, "Heat removal capacity of laminar coolant flow in a microchannel heat sink with different pin fins," *Int. J. Heat Mass Transf.*, vol. 113, pp. 366–372, 2017.

[24] M. Yang and B. Y. Cao, "Multi-objective optimization of a hybrid microchannel heat sink combining manifold concept with secondary channels," *Appl. Therm. Eng.*, vol. 181, no. February, p. 115592, 2020.

[25] T. Song, C. Liu, Y. Peng, and S. K. Lim, "Full-Chip Signal Integrity Analysis and Optimization of 3-D ICs," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 5, pp. 1636–1648, 2016.

[26] C. De Wang *et al.*, "ABF-based tSV arrays with improved signal integrity on 3-D IC/Interposers: Equivalent models and experiments," *IEEE Trans. Components, Package. Manuf. Technol.*, vol. 3, no. 10, pp. 1744–1753, 2013.

[27] N. K. Das, "A New Theory of the Characteristic Impedance of General Printed Transmission Lines Applicable when Power Leakage Exists," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 7 PART 1, pp. 1108–1117, 2000.

[28] Y. Zhai, G. Xia, Z. Li, and H. Wang, "Experimental investigation and empirical correlations of single and laminar convective heat transfer in microchannel heat sinks," *Exp. Therm. Fluid Sci.*, vol. 83, pp. 207–214, 2017.

[29] Z. Fakhreddine *et al.*, "Signal and Thermal Integrity Analysis of 3-D Stacked Resistive Random Access Memories," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 88–94, 2021.

[30] S. Chamoli, R. Lu, H. Chen, Y. Cheng, and P. Yu, "Numerical optimization of design parameters for a modified double-layer microchannel heat sink," *Int. J. Heat Mass Transf.*, vol. 138, pp. 373–389, 2019.

[31] T. H. Wang, H. C. Wu, J. H. Meng, and W. M. Yan, "Optimization of a double-layered microchannel heat sink with semi-porous-ribs by multi-objective genetic algorithm," *Int. J. Heat Mass Transf.*, vol. 149, 2020.

[32] W. Wang, Y. Zhang, Y. Li, H. Han, and B. Li, "Multi-objective optimization of turbulent heat transfer flow in novel outward helically corrugated tubes," *Appl. Therm. Eng.*, vol. 138, pp. 795–806, 2018.

[33] Z. He, Y. Yan, T. Zhao, L. Zhang, and Z. Zhang, "Multi-objective optimization and multi-factors analysis of the thermal/hydraulic performance of the bionic Y-shaped fractal heat sink," *Appl. Therm. Eng.*, vol. 195, no. May, p. 117157, 2021.

[34] W. Wang, Y. Zhang, K. S. Lee, and B. Li, "Optimal design of a double pipe heat exchanger based on the outward helically corrugated tube," *Int. J. Heat Mass Transf.*, vol. 135, pp. 706–

716, 2019.

[35] S. Chamoli, "ANN and RSM approach for modelling and optimization of designing parameters for a v down perforated baffle roughened rectangular channel," *Alexandria Eng. J.*, vol. 54, no. 3, pp. 429–446, 2015.

[36] K. Deb, A. Member, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multi-objective genetic algorithm: NSGAII," vol. 6, no. 2, pp. 182–197, 2002.

[37] Y. Fan, Z. Wang, and T. Fu, "Multi-objective optimization design of lithium-ion battery liquid cooling plate with double-layered dendritic channels," *Appl. Therm. Eng.*, vol. 199, no. May, p. 117541, 2021.

[38] A. Yusuf, N. Bayhan, H. Tiryaki, B. Hamawandi, M. S. Toprak, and S. Ballikaya, "Multi-objective optimization of concentrated Photovoltaic-Thermoelectric hybrid system via non-dominated sorting genetic algorithm (NSGA II)," *Energy Convers. Manag.*, vol. 236, p. 114065, 2021.