Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity

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Abstract

With the development of internet and the rise of artificial intelligence industry, the high performance semiconductor integrated circuits have become a hot product in the semiconductor industry. The 2.5D IC package with ultra-high density I/O is the first structure applied on high performance computing (HPC) like GPU. Applied on GPU or HPC, there is an ASIC die and multiple HBM dice on silicon interposer. Between ASIC die and HBM die, there are lots of high speed signal lines between them and over hundreds of thousands of small vias. But the productivity of silicon interposer is always issue to realize the ultra-high density I/O products. To consider the productivity and performance, TSV-less structure like FOCoS (Fan-Out Chip on Substrate) is proposed by few years ago [1] [2] [3] [4] [5].There are Chip First FOCoS and Chip Last FOCoS for different process and application [6].

In this paper, a real case with an ASIC die and 2 HBM dice is designed in 2.5D IC and Chip Last FOCoS structures. In this real case, the interposer design and Fan-Out RDL is utilized SiP-id (System in Package intelligent design) design platform to accelerate the ultra-high density I/O routings. In addition, the electrical performance including signal integrity (SI) and power integrity (PI) are compared between 2.5D IC and Chip Last FOCoS. From the analysis results, the dynamic power noise between the two structures is showed in this paper and the electrical performance of HBM2 and 28Gbps SerDes I/Os are displayed as well.

I. Introduction

The big data calculations were originally used in space science or meteorological simulation and analysis which were performed by supercomputers. With the advancement of information industry, internet and communication technology, the rise of the Internet of Things, big data analysis, artificial intelligence, industrial 4.0, autonomous driving and even the development of robotic development applications, the demand for huge amounts of data computing has been everywhere.

Previous supercomputers were usually built with many computers and a large number of CPUs, having the advantages of high speed, high bandwidth and huge computing capability, but volume of supercomputer is very large.

As semiconductor design and manufacturing capabilities continue to improve, today's computers can use smaller volumes to perform as much or as much computing power as ever. The 2.5D IC, as shown in Figure 1, is an innovation in IC packaging to meet the demand for huge amounts of computing in a small size.

II. Ultra High Density Packages

The main feature of the 2.5D IC is to use a Silicon Interposer to connect the homogenous dice or heterogeneous dice of a fine pitch footprint to expand computing capabilities or data bandwidth of a single IC package. Now many products have been successfully developed and mass produced with 2.5D IC packages.

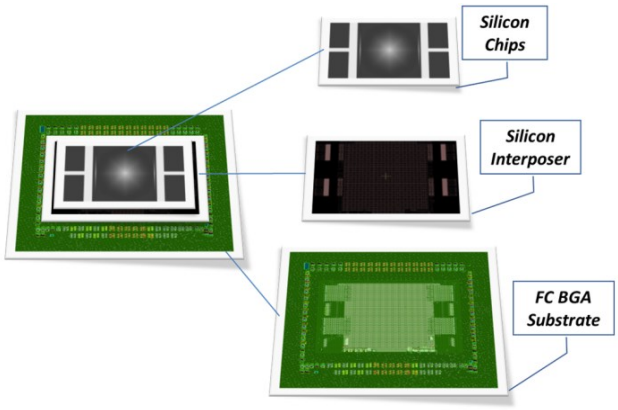

Fig. 1 2.5D IC Package Structure

Silicon interposer is manufactured using wafer fabrication process with Through-Silicon-Via (TSV), as shown in Figure 2. Therefore, the complexity of package manufacturing are always much higher than traditional packages. Because less than 1um RDL width and the diameter of via less can be designed on the silicon interposer [7] [8] [9], no other technology can completely replace the silicon interposer currently.

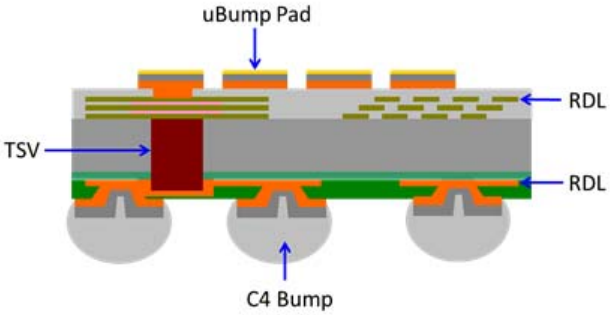

Fig. 2 TSV in 2.5D IC Interposer

The Bumping RDL process is another technology that can be used to design fine lines compared to conventional package

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substrates. Originally the bumping process is only applied to the wafer level package type, which is used as the routing layer for pins redistribution of the silicon IC, the width of the finest line is about 10um.

With the bumping technology is used in Fan-Out package type, and the development of Fan-Out PoP, Fan-Out SiP and integrated Fan-Out Chips on Substrate (FOCoS) packages, fine line requirements and technology development continues to improve, and the suitable applications for Fan-Out packages and the types of product designs are increasing.

For FOCoS which can be used to replace the homogenous integration IC package that can only be designed with 2.5D IC package, as shown in figure 3.

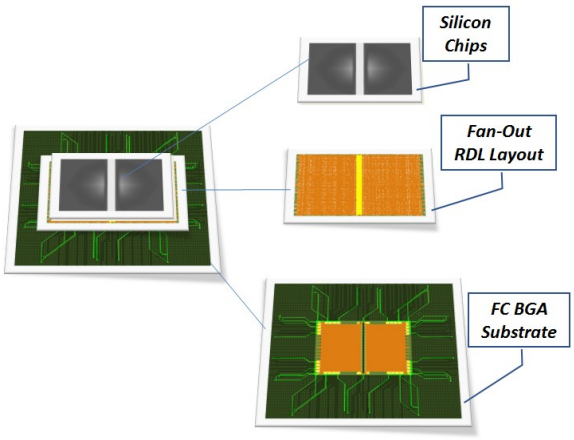


Fig. 3 Fan-Out Chip on Substrate

In this paper, FOCoS is used to design heterogeneous integration IC package which integrated ASIC and HBM (High Bandwidth Memory) dice. Chip Last FOCoS is suitable for ASIC integrated HBM chips IC package because Known-good RDL layer could be available. The spacing between I/O pins is getting smaller with the advancement of IC process technology and the increasing number of I/O pins for integrated multiple chips. The line width of the bumping technology RDL line is improved from the originally 10um to currently 2um. Table 1 is a comparison of the traditional FCBGA substrate, 2.5D IC interposer and the RDL layer design specification on FOCoS. According to the roadmap of the bumping technology, the line width of the RDL line will continue to shrink in the future.

Table 1. Design Rule Comparison

Design Rule	PKG Size	Cu Thickness	RDL L/S	Via Size	Hole Size
FC BGA Substrate	55 mm x 55 mm	15 um	15 um	50 um	150 um
Fan-Out RDL	30 mm x 30 mm	3 um	2 um	10 um	10 um
2.5D IC Interposer	30 mm x 30 mm	1 um	1 um	0.4 um	1 um

III. Design Tools and Flow

In addition to changes and improvements in ultra-high-density I/O package types and the corresponding process technology, the complete design flow and efficient design tools must be ready, as shown in figure 4. The traditional package design tools are difficult to design ultra high I/O package like Fan-Out RDL routings or 2.5D IC interposer routings including layout, design rule check (DRC) and layout versus netlist (LVS) tools. For example, each action of the layout tool becomes very slow even not work when the layout density becomes higher and higher; efficient design for manufacturing (DFM) check because the embedded DRC function in original package design tool doesn't support advanced design rule and new design drawing format; the complex signal interconnections cannot be compared with the original version of the customer's design document because the complete package design is much complexer than tranditional package design. Issue above are the challenges while the package design with ultra-high-density I/Os.

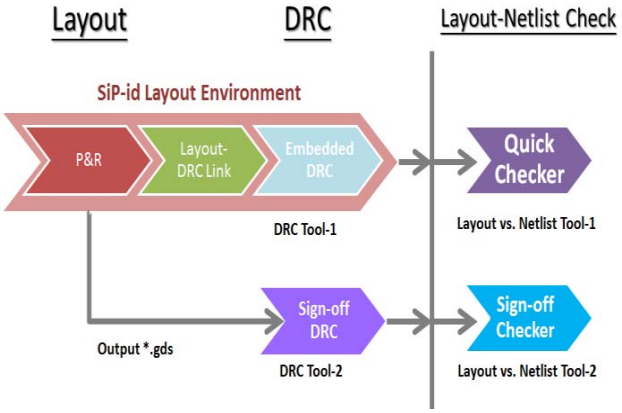


Fig. 4 SiP-id Package Design Environment

Addressing to problems above, the improvements for the design tool and the enhancement of the overall design process, as shown in figure 5, is to be planned and executed by the designer and EDA tool suppliers. Thus it results in a novel high-density I/O package design environment, as shown in figure 4. The novel high density I/O package design flow and tools include improved layout tool, new DRC tools and new LVS tools to make sure better design cycle time and design quality. Generally it takes about 3 months to finish a Fan-Out RDL layers design using the traditional package flow and tools for example. With new SiP-id design flow and tools, the design could be finished in 1 month design cycle time. It has about 3 times improvement.

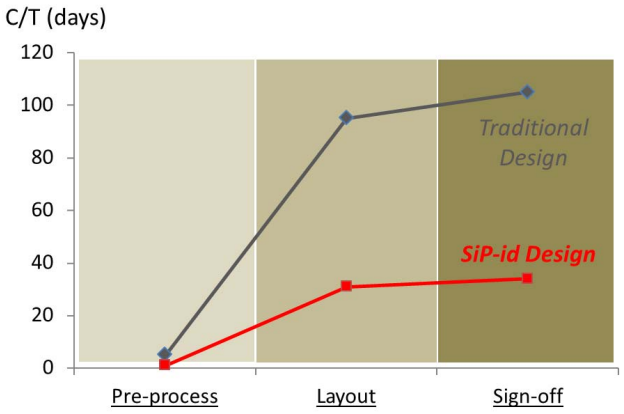


Fig. 5 Design Efficiency Improvement by SiP-id

IV. Design Requirement with HBM

HPC products incorporating High-Bandwidth-Memory (HBM) are common used for high-end GPUs, AI processors, high-end networking processors or state-of-the-art FPGA products. With 1 HBM, the bandwidth of the IC package could be higher than the PCB system with tens of traditional DRAM memory ICs, as well as shorter interconnections distance with better electrical performance between the processor and the memory. Figure 6 is for the JEDEC standard pinout. There are totally 1024 DQ signals and there are 48 DQ signals arranged repeatly in about 155um pitch. In other words, the 48 signals must to be faned-out in 155 um layout space. According to evaluation, it could utilize 2 RDL layers to Fan-Out all 48 signals, 24 signals in each RDL layer, if the RDL line width/space is 2um/2um with 16 um via size.

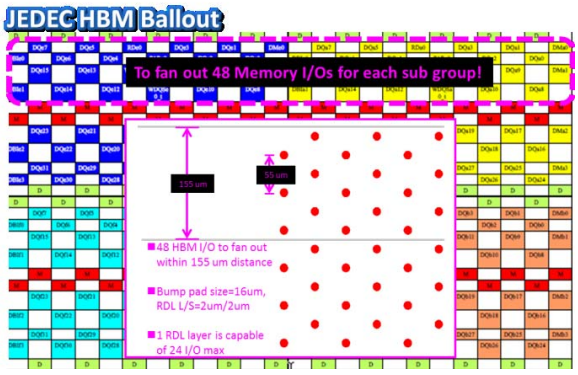


Fig. 6 Partial JEDEC HBM Footprint

Thus, the design strategy could be 2 RDL layers for die to die HBM I/O routings, 1 RDL layer as the ground layer between 2 HBM I/O routing RDL layers and 1 RDL layer for landing C4 pad, there are totally 4 RDL layers for the Fan-Out chip. Because RDL line width and space as well as via size are continuously to be reduced for Fan-Out technology, The design with processor integrated with HBM could be designed in FOCoS in more economical package, as shown in Figure 7.

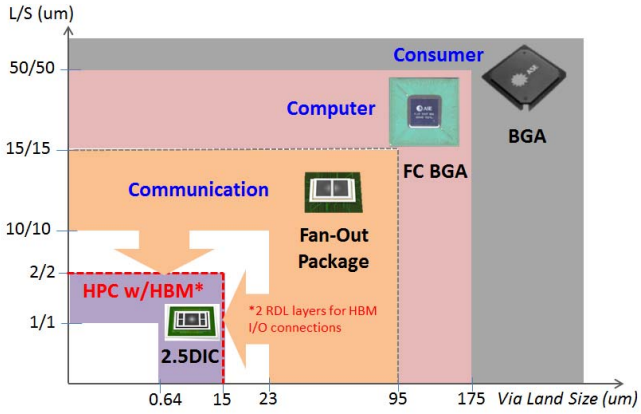
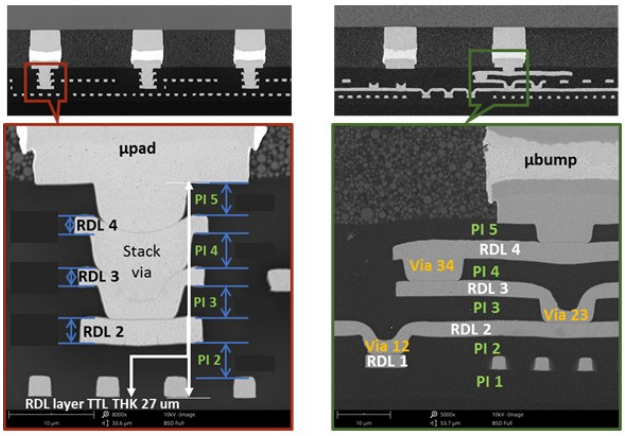


Fig. 7 Package Technology vs. Application

In addition, the process for FOCoS process can now achieve stack vias. The design with stacked vias can enable the package design engineers to have more design space and more design flexibility when designing high density packages. Figure 8 is for photographic images of the actual FOCoS product. In the pictures which shows both stacked vias and non-stacked vias structures.



(a) Stacked Vias (b) Non-stacked Vias

Fig. 8 SEM Images of FOCoS product

V. Electrical Characterization

From viewpoint of package structure and dimension, both 2.5D IC interposer and Fan-Out RDL layer can be designed to be much thinner than conventional BGA substrates. Since thin lines must be made with very thin copper thickness, the thickness is about 15 um for FC BGA substrate, while the thickness of the Fan-Out RDL copper is only 3~4 um, and the thickness of the 2.5D IC interposer is even smaller than 1um. So that the resistance value is very large for the line made by the thin line width plus the thin copper thickness. The resistance value of the FC BGA, Fan-Out RDL and 2.5D IC interposer per 1mm length is compared with table 2. For the resistance of Fan-Out RDL routing is about 70X of the

resistance of FC BGA substrate, and the resistance is about 4X of the resistance of Fan-Out RDL. The resistance is very high then traditional FC BGA substrate. Therefore, when designing high speed I/O on Fan-Out RDL and 2.5D IC interposer, try to shorten the connection distance to avoid high resistance. The major routings of the I/O traces could be designed on the traditional FC BGA substrate to connect especially for power or ground connections. The design should have vertical direct connection between the micron bump to the C4 bump by stacked vias, so that the high resistance value will not cause product design failure.

Table 2. Resistance of 1 mm Trace Routing

Resistance	wire bond BGA	FC BGA	FOCoS RDL	2.5D IC Interposer
@ DC (mΩ/mm)	19.4	64.4	4314.7	18966
@ 1GHz (mΩ/mm)	106.1	233.1	4552.5	19080

Generally the test pattern is designed at the edge of wafer which is next to the actual FOCoS design in order to verify the electrical performance of this new interface of Fan-Out RDL. The test pattern has a single-end transmission line and a differential pair transmission line to confirm that the electrical simulation tool can achieve accurate results when building the model of HBM I/O and SerDes I/O. Figure 9 and figure 10 are for the comparison of analysis between the measurement and the simulation of single-end and differential pair transmission lines individually. According to results, no matter signle –end transmission line or differential transmission line, the simulation results are very close to the measurement results. Therefore, electrical simulation tools can be used to perform complex electrical performance analysis.

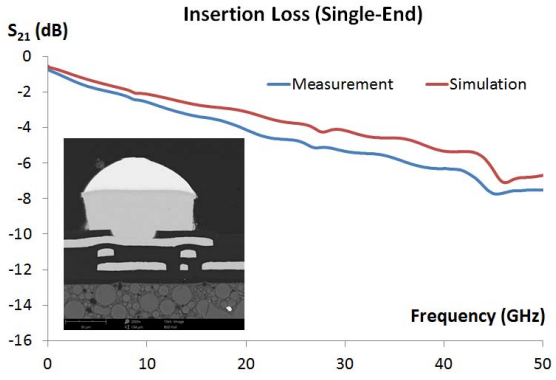


Fig. 9 Simulation vs. Measurement for Single-end TL in FOCoS

The design of a HPC product containing HBM, the most critical signals need to be carefully designed can be divided into HBM interconnection and SerDes signal of high-speed differential signal pair, as shown in Figure 11. Following sections will focus on signal integrity and power integrity analysis on these critical signals.

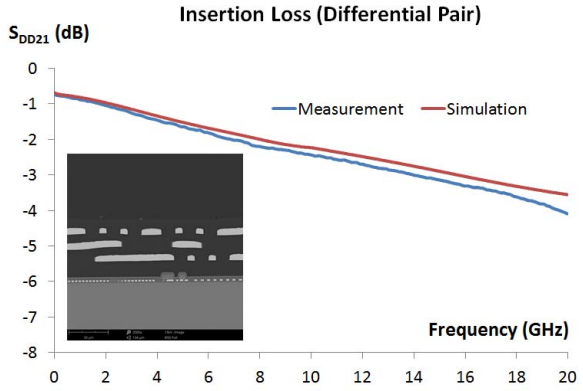


Fig. 10 Simulation vs. Measurement for Differential TL in FOCoS

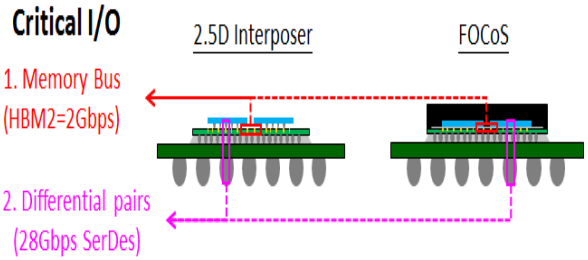


Fig. 11 Critical Signals in HPC Device

VI. Signal Integrity

Model extractions from electromagnetic solver and analysis on the eye diagram by system simulator to compare signal integrity performance of the HBM interconnection and high speed SerDes signal design [10]. The eye diagram analysis results for HBM signals is shown in figure 12. According to HBM eye diagram analysis results, it can be seen that the performance of the FOCoS design is the same as that of the 2.5D IC interposer for the analysis of HBM2 at 2Gbps speed. But at 3Gbps or 4Gbps speed, FOCoS performance is significantly better than 2.5D IC interposer because 2.5D IC interposer has large resistive transmission line loss than FOCoS package. Table 3 is the summary of eye height and eye widh for HBM eye diagram analysis.

Foe 28Gbps SerDes eye diagram simulation is shown as figure 13 and summary as table 4. Because the design from uBump of ASIC die side connected to C4 bump of substrae side is only stacked vias without resistive RDL routings, the eye diagram analysis results are good and almost equal for both 2.5D IC interposer and Chip Last FOCoS package design.

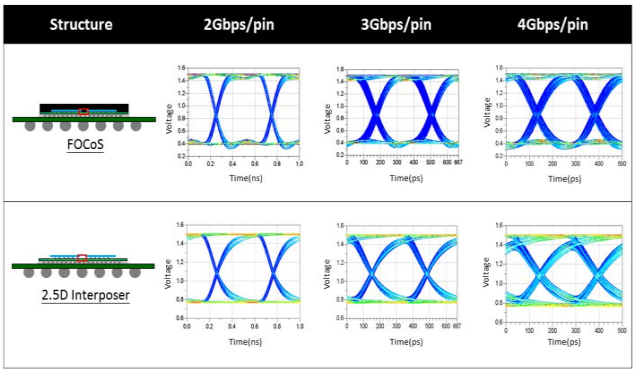


Fig. 12 Eye Diagram of HBM Interconnect

Table 3 Summary of HBM Eye Height and Eye Width

HBM Signal	Eye Height			Eye Width		
Package Design	2Gbps	3Gbps	4Gbps	2Gbps	3Gbps	4Gbps
2.5D IC Interposer	0.59 V	0.49 V	0.4 V	0.98 UI	0.94 UI	0.89 UI
FOCoS	0.97 V	0.99 V	0.95 V	0.98 UI	0.95 UI	0.94 UI

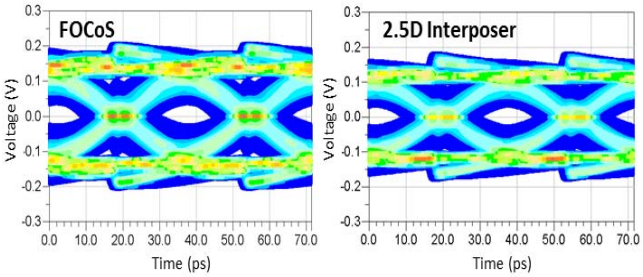


Fig. 13 Eye Diagram of 28Gbps SerDes Signals

Table 4 Summary of 28Gbps SerDes Eye Diagram

28Gbps SerDes	Eye Height	Eye Width
2.5D IC Interposer	0.072 V	0.47UI
FOCoS	0.082 V	0.48UI

VII. Power Integrity

Due to 1024 bits for HBM die, power noise is critical analysis item for HBM relative power system. Figure 14 shows the simulation results of HBM power/ground dynamic power noise including HBM core power VDDC and HBM I/O power VDDO network. Table 5 is the summary of VDDC and VDDO dynamic power noise analysis results. Both the 2.5D IC interposer and FOCoS designs have similar power integrity designs because they both have tens of thousands of u-bump, via and C4 bumps the design and they are vertically and directly connected. In this dynamic power noise analsys, the decoupling capacitors are not included in the analysis yet.

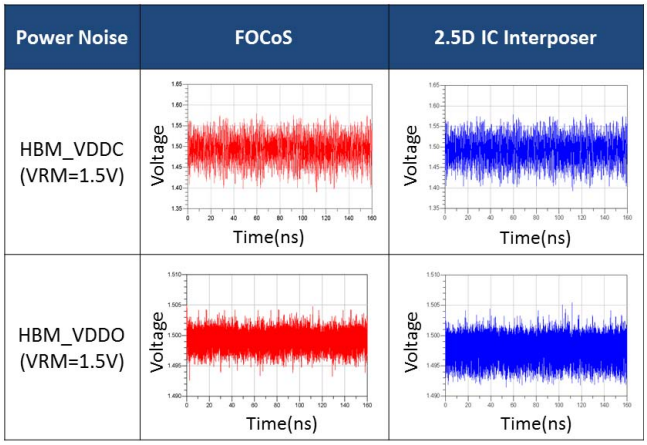


Fig. 14 Dynamic Power Noise Analysis

Table 5 Summary of Dynamic Power Noise

Power Net	Design	Noise_P2P (V)	Noise_P2P (%)
HBM_VDDC (VRM=1.5V)	2.5D IC Interposer	0.187	12.5
	FOCoS	0.189	12.6
HBM_VDDO (VRM=1.5V)	2.5D IC Interposer	0.014	0.9
	FOCoS	0.012	0.012

VIII. Conclusion

It could be expected that there will be more and more requirements for ultra high densisty package design including 2.5D IC interposer and chip last FOCoS design. Therefore the design tools for fast layout, design for manufacturing check including design rule check (DRC) and interconnections check for multi-chips are innovated and integrated. Through the novel design flow with innovated design tools, the design cycle time and quality are improved.

2.5D IC packaging is validated for ultra high density I/O device. FOCoS is an alternative package solution for ultra high density I/O device due to continously improvement of RDL trace width and space as well as the via size. In this paper, the package design for HPC application which includes ASIC die and HBM dice are implemented with SiP-id design platform and fabricated

by chip last FOCoS process. From viewpoint of electrical analysis, chip last FOCoS has similar even better electrical performance than 2.5D IC interposer no matter signal integrity or power integrity analysis.

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