Neural Network-Based 3D IC Interconnect Capacitance Extraction

Ryosuke Kasai[1], Koutaro Hachiya[2], Toshiki Kanamoto[1], Masashi Imai[1], and Atsushi Kurokawa[1*]
[1]Graduate School of Science and Technology, Hirosaki University
[2]Graduate Program in Environmental Information Science, Teikyo Heisei University
e-mail: *kurokawa@eit.hirosaki-u.ac.jp

***Abstract*—This paper presents a method to extract interconnect capacitance in three-dimensional integrated circuits (3D ICs) using a neural network (NN). The procedure is as follows: 1) create training datasets (by obtaining capacitance values from the complicated 3D interconnect structures using a 3D electromagnetic field solver), 2) build the trained models by inputting the training datasets to the NN, and 3) extract capacitance values by inputting structural parameters regarding the objective interconnect. The structures of general interconnects, interconnects surrounding a through-silicon via (TSV), and whole interconnects are examined. Experimental results show that the proposed NN-based extraction method can obtain reasonable accuracy and processing time. They also show that good trained models are obtained even if training datasets that integrate two structures into one are input to the NN.**

Keywords-interconnect; capacitance; extraction; neural network; 3D IC

I. INTRODUCTION

Layout parasitic extraction (LPE) has been widely studied since integrated circuits (ICs) surfaced in the world. Interconnect capacitance is one of the most important electrical parameters for designing ICs such as system-on-chip (SoC), system-in-package (SiP), and through-silicon via (TSV) based three-dimensional integrated circuits (3D ICs). The interconnect capacitances are used for delay calculation, power integrity (PI) analysis (e.g., IR-drop and power/ground noise), electro-magnetic interference (EMI) analysis, and signal integrity (SI) analysis (e.g., crosstalk noise) [1]. Although an objective interconnect has many coupling capacitances, the total capacitance is particularly important except for SI analysis.

Many studies have been published on interconnect capacitance extraction methodologies. They are classified into three approaches: numerical solutions, formulas (or analytical models), and table lookup models. Numerical approaches are based on solving potentials from electric fields, and include a finite element method (FEM) [2], a finite difference method (FDM) [3], a boundary element method (BEM) [3–4], and a floating random walk (FRW) method [5]. Numerical approaches can obtain capacitance values with very high accuracy, but they require an enormous amount of time. For very large scale integrated circuits (VLSIs), it is difficult to use the methods directly during the design stage.

Formula-based approaches are based on creating capacitance equations for various couplings by using regression analysis, etc. Many researchers have developed interconnect capacitance equations on a single chip [6–8], 3D IC TSV-to-TSV capacitance equations [9–10], and analytical models of 3D IC TSV-to-TSV capacitances by the inverse of inductance matrix [11–12]. However, there are limitations to create equations for most of the structures of LSI multi-layer interconnects. In another approach, table lookup models are obtained by saving discrete point data and interpolating between points during the design stage. However, saving mass data is not practical from the viewpoint of computer memory resources.

The most common current design flow method is as follows: 1) obtain capacitance values for various structures by using field solvers, 2) save the data simplified by using multivariate analysis such as regression analysis and principal component analysis (PCA) into interconnect libraries for each process technology, and 3) extract the objective interconnect capacitance by pattern matching during the design stage. With the method, however, it is necessary to divide LSI interconnects into a huge number of patterns, create approximate equations, and strive to ascertain a pattern with complete correspondence.

In this paper, we describe an interconnect capacitance extraction method we propose that uses a neural network (NN). We evaluate the approach using examples of general interconnects and interconnects surrounding a TSV. The NN finds an optimal solution by updating weights and biases, instead of optimizing the gradients and intercepts in multiple regression analysis to create formulas. A NN-based approach is advantageous in that any complicated structure can be handled by increasing the number of nodes (neurons).

The rest of the paper is organized as follows. In Section II, we describe the proposed interconnect capacitance extraction method. In Section III, the experimental results obtained with our method are shown. Finally, conclusions are drawn in Section IV.

II. NEURAL NETWORK BASED EXTRACTION METHOD

In this section, we present a NN-based interconnect capacitance extraction method with processing flows.

A. Overall Flow

Fig. 1 shows the overall flow of the proposed method. The procedure is as follows: 1) prepare training datasets, which include interconnect structural parameters and capacitance values, for the NN, 2) build trained models through the NN, and 3) extract capacitance values by inputting the structural parameters regarding the objective interconnect.

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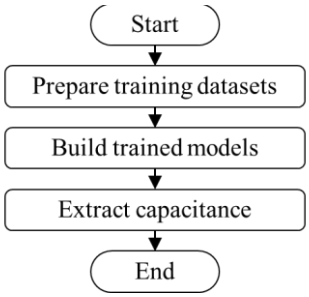

Figure 1. Overall flow of proposed NN-based extraction method.

B. *Preparing Training Datasets*

Fig. 2 shows a flow of creating training datasets used for NN learning. First, multi-layer interconnect structures are classified and then interconnect capacitance values are obtained by using 3D field solvers. Here, interconnect capacitance data with structural parameters become training datasets for the NN.

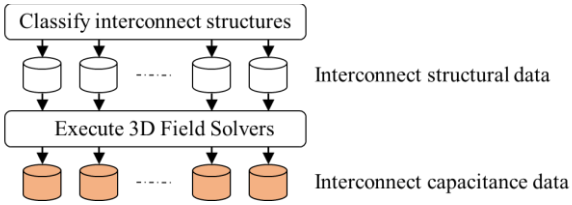

Figure 2. Flow of creating interconnect capacitance data.

C. *Building Trained Models*

Fig. 3 shows the NN model used in this study. The processing flow to build the trained models is as follows: 1) input training datasets, 2) train a NN, and 3) build the trained models. For training the NN, we used the backpropagation method. The procedure is to input the datasets into the NN, evaluate the error between the capacitance outputted from the NN and the original capacitance value of the training datasets, and update parameters (weights and biases) of the NN so that the error is minimized. To determine the parameters, we used Adam (adaptive moment estimation) [13] which is an optimization algorithm to train a NN. The mean squared error (MSE) was used to update the parameters, calculated for all output data, and expressed by

$$\mathrm{MSE} = \frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2, \qquad (1)$$

where y is the true capacitance value, $\hat{y}$ is the predicted capacitance value, and n is the number of examples.

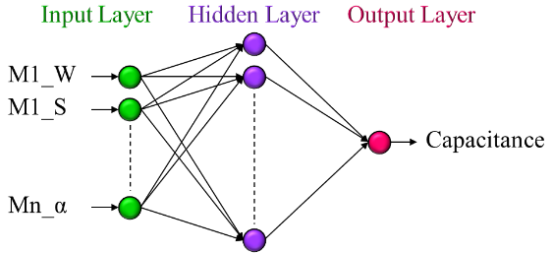

Figure 3. Neural network model used in this study.

D. *Extracting Capacitance*

Fig. 4 shows a flow of the NN-based interconnect capacitance extraction, which is executed during the design stage. We first obtain structural parameters regarding to the objective interconnect from the physical layout data. Next, we input the parameters as test data and obtain capacitance values of the objective interconnect through the NN.

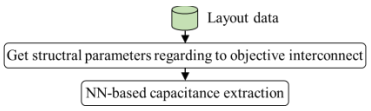

Figure 4. NN-based interconnect capacitance extraction flow.

III. Experimental Results

In this section, we present experimental results using typical examples of on-chip interconnect structures. The dimensions of the interconnect structures were based on the 2.1-nm technology node (which is the prediction for 2027) in IRDS 2017 [14]. The true capacitance values for creating the training data were obtained by using a Synopsys Raphael 3D field solver [3]. We used Chainer [15], which is a deep learning framework, for our implementations and experiments.

A. *Interconnect Structures*

For the 3D IC used in this study, we assumed that TSVs as vertical-electrical connections pierce the chip substrate layer and the metal (on-chip interconnect) layer, and that micro-bumps are used for the connections between chips. Arrangements of TSVs in the chip substrate and micro-bumps are relatively regular and simple compared to on-chip interconnects.

To examine the proposed method, we used two types of structures. One is a general on-chip interconnect structure without TSVs, as shown in Fig. 5. The illustration was drawn by a Murata software Femtet field solver [2]. The objective interconnect is the one in the center of the M1 interconnects. Table I lists parameters for examining the general interconnect structure. For example, there were eight M1 widths because the widths varied by 1 μm from 7 to 14 μm. There are 10,816 interconnect patterns for the general structure.

Another structure we used is one in which a TSV is surrounded by on-chip interconnects, as shown in Fig. 6. The objective interconnect is the inside one of the M1 interconnects. Table II lists parameters for examining the interconnect-surrounded TSV structure. The structure has 16,128 interconnect patterns and we used the field solvers to obtain the capacitance values for all of the patterns. The structural parameters and capacitance values become the training datasets. We also examined a structure that integrated the general structure and the interconnect-surrounded TSV structure into one. In this paper we call it the "whole interconnect structure" (see Fig. 7). In the experiments, we investigated and clarified the differences among three training datasets, one for a general interconnect structure, one for an interconnect-surrounded TSV structure, and one for the whole interconnect structure.

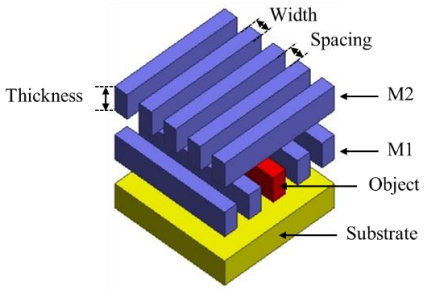

Figure 5. General interconnect structure.

TABLE I. PARAMETERS FOR EXAMINING GENERAL INTERCONNECT STRUCTURE

Parameter	Value (nm)
M1 Width	7 – 14 (1-nm step)
M1 Spacing	7 – 43 (3-nm step)
M1 Thickness	14
M2 Width	7 – 14 (1-nm step)
M2 Spacing	7 – 43 (3-nm step)
M2 Thickness	14
Dielectric Constant	3.9

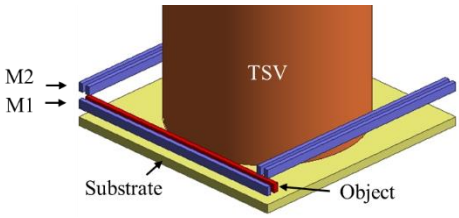

Figure 6. Interconnect-surrounded TSV structure.

TABLE II. PARAMETERS FOR EXAMINING INTERCONNECT-SURROUNDING TSV STRUCTURE

Parameter	Value (nm)
M1 Width	7 – 14 (1-nm step)
M1 Spacing	7 – 22 (3-nm step)
M1 Thickness	14
M2 Width	7 – 14 (1-nm step)
M2 Spacing	7 – 22 (3-nm step)
M2 Thickness	14
TSV Radius	150
TSV-Wire Spacing	20 – 50 (10-nm step)
Dielectric Constant	3.9

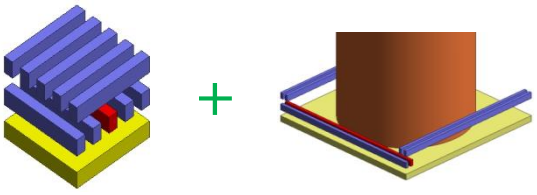

Figure 7. Whole interconnect structure.

B. Neural Network Model

The NN models for the general interconnect structure, the interconnect-surrounded TSV structure, and the whole interconnect structure had respectively 4, 5, and 9 neurons in the input layers. They had in common 100 neurons in the hidden layer and 1 neuron in the output layer.

The general structure, interconnect-surrounded TSV structure, and the whole structure had respectively 1,000, 1,000, and 2,000 data elements. Their test datasets were made by generating a random number for each parameter. Thus, the dimensions of the interconnect structures used for the training data are basically different.

C. Learning Time

The number of learning times for making training models is shown in Fig. 8. All experiments were run on the Intel Xeon CPU E31275 with a frequency of 3.4 GHz and RAM of 16 GB. The CPU time increased in proportion to the number of learning times. It increased in order for general interconnects, interconnects surrounding a TSV, and whole interconnects (for both the general interconnect and interconnect-surrounded TSV structures), because the general interconnect, interconnect-surrounded TSV, and whole interconnect structures had respectively 10,816, 16,128, and 26,944 learning patterns. Fig. 9 shows the MSE values in capacitance (fF) to the number of learning times.

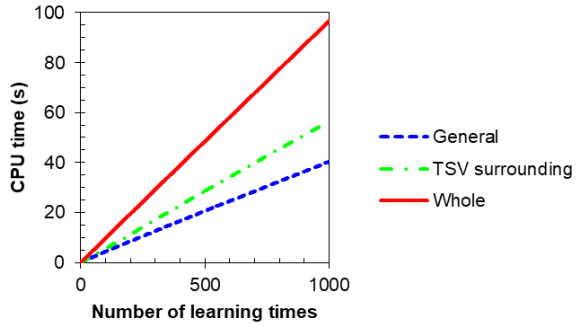

Figure 8. CPU time vs. the number of learning times for making training models.

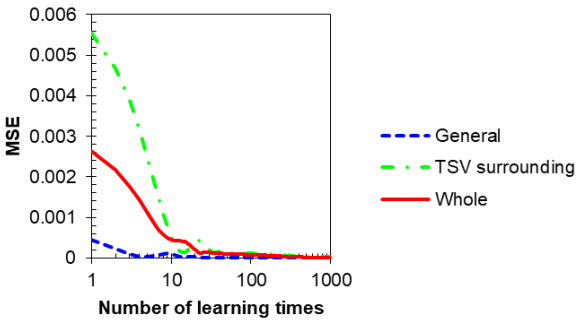

Figure 9. MSE vs. the number of learning times.

D. Extraction Time

Fig. 10 shows the CPU time required for extracting capacitance values from test data. The extraction times are almost the same regardless of the number of the training data. Therefore, it is predicted that the extraction time depends on the number of test data even if a huge number of training data are used.

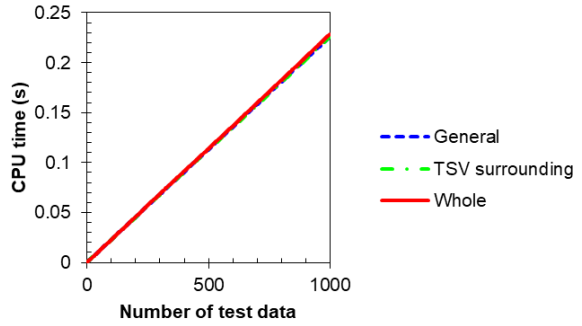

Figure 10. CPU time required for extraction.

E. Accuracy

The amount of coupling capacitance for objective interconnects is N-1, where N is the number of conductors. Here, we consider the total capacitance (C_{tot}), capacitance to a substrate (C_{sub}), and capacitance to a TSV (C_{TSV}). The histograms of relative errors (in percent) for the general, TSV surrounding, and whole structures for the total capacitance are shown in Figs. 11-13. Fig. 12 shows that the capacitance prediction for the interconnect-surrounded TSV structure is a little low in accuracy for a part of the test data. The errors are the relative errors of the results obtained by the proposed method to those obtained by a field solver in capacitance values.

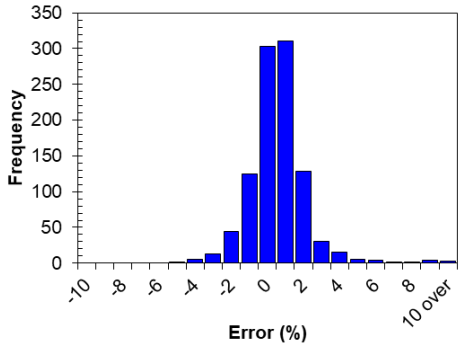

Figure 11. Histogram of extraction errors for total capacitance of general interconnect structure.

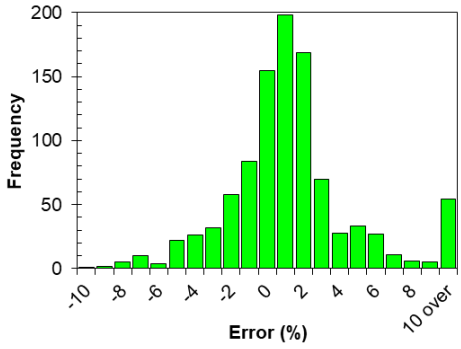

Figure 12. Histogram of extraction errors for total capacitance of interconnect-surrounding TSV structure.

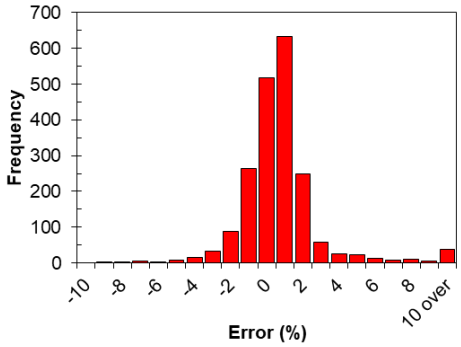

Figure 13. Histogram of extraction errors for total capacitance of whole interconnect structure.

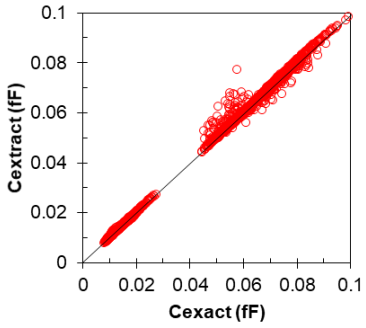

Figure 14. Capacitance comparison for total capacitance of whole interconnect structure.

TABLE III. ACCURACY OF PROPOSED EXTRACTION

Structure	Cap	MAE (%)	RMSE (%)
General	C_{tot}	1.1	1.7
TSV Surrounding	C_{tot}	2.7	4.5
Whole	C_{tot}	1.5	2.8
	C_{sub}	3.8	5.8
	C_{TSV}	4.6	7.3

Fig. 14 shows comparisons of the capacitance results obtained with the proposed method and those obtained by a field solver. It shows good fitting results were obtained. Table III lists the accuracy of the capacitance extraction. Comparing the three structures in terms of total capacitance, we found that both the mean absolute errors (MAEs) and the root mean square errors (RMSEs) showed good accuracy results. In other words, this means that we can make training models using datasets that integrated training datasets for a number of structures.

IV. CONCLUSIONS

We have presented a neural network-based interconnect capacitance extraction method that we propose for designing 3D ICs. We showed the results we obtained the total capacitance, capacitance to substrate, and capacitance to TSV by using general and TSV-surrounding structures. Our examination of the method showed that it provides suitable accuracy and runtime.

ACKNOWLEDGMENT

This work was supported by JSPS KAKENHI Grant Number JP17K00070. This work was also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc.

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