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Perspective

Cryo-CMOS device technology for quantum computers

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Cryogenic-CMOS (cryo-CMOS) technology has attracted considerable attention for realizing large-scale quantum computers. To develop cryo-CMOS circuits, a compact model that reproduces cryogenic MOSFET operations is required. Therefore, understanding the metal–oxide–semiconductor field-effect transistor (MOSFET) performance at cryogenic temperatures is critically important. However, the cryogenic operation of MOSFET is quite different from that at room temperature, and device physics is not fully understood. This study provides an overview of cryo-CMOS technology with a particular focus on device performance and presents future outlooks.

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1. Introduction

Quantum computers have been proven to be able to solve certain important problems such as material chemical calculations and combinatorial optimization problems at a faster speed than classical computers, and research and development have been actively promoted in recent years. The quantum bit (qubit) is the basic unit of information in the quantum computer, and it can be in a quantum superposition state of 0 and 1. To demonstrate its potential to the full extent, the realization of a gate-based quantum computer with over 1 million qubits is a future objective. The qubit is a quantum two-level system and it is physically implemented by various carriers such as photons, ions, electron spins, and others. Among them, solid-state qubits such as superconducting qubits and silicon qubits have an advantage in the large-scale integration (LSI) of qubits. This paper describes cryo-CMOS technology as the control method for these solid-state qubits.

Quantum computers consist of quantum circuits and their control unit comprising electronic instruments such as a microwave generator for qubit control. Solid-state qubits, such as superconducting qubits and silicon qubits, are placed at the bottom stage of a refrigerator for maintaining the quantum state at cryogenic temperatures. Currently, the control unit is placed outside the refrigerator, and the bulky control instruments and qubits are connected by massive numbers of electrical interconnects. This approach to controlling qubits is called the brute force method, and the number of interconnects increase exponentially as increasing qubits. Although this method can control a small number of qubits, it cannot be a realistic control method when the degree of integration increases. Even assuming a case in which two microwave interconnects are used per qubit, which is the minimum requirement for a superconducting qubit, the number of integrations eventually reaches the capacity limit of the refrigerator (several hundred interconnects). Power consumption due to the use of many instruments and heat inflow through interconnects are also concerns when using the current control system.

An approach to use the integrated circuits for the qubit control has been considered to solve these interconnect issues and pave the way for large-scale integrated quantum computers (Fig. 1). Such integrated circuits, called cryogenic-CMOS (cryo-CMOS) circuits, are placed near the qubit in the refrigerator and operate in cryogenic temperatures [1–3]. To develop cryo-CMOS circuits, a circuit compact model that reproduces cryogenic MOSFET operations is required. However, MOSFET performance at cryogenic temperatures of several Kelvin or less is quite different from that at room temperature and there is no guarantee that the existing model is applicable to cryogenic operation. Therefore, a physical understanding of cryogenic device performance is critically important to establish a compact model for cryo-CMOS.

In this study, the research status and trends of cryo-CMOS technology are described with a particular focus on device physics. Recent research results are also presented and the future outlook of cryo-CMOS technology is introduced.

2. Role of cryo-CMOS circuits in quantum computers

The role of cryo-CMOS circuits in quantum computers is to control the input/output signals of qubits. This means the initialization, manipulation, and readout of quantum states of a qubit by electrical measurements. Quantum states of superconducting qubits and silicon qubits are generally controlled by microwave signals with GHz frequency. Irradiating a qubit with a microwave pulse results in the creation of a quantum superposition state and the execution of an arbitrary quantum calculation. Therefore, precise microwave pulse generation is required for highly accurate qubit manipulation. Several methods exist for reading signals from qubits such as change of the resonator frequency in superconducting circuits [4] and charge sensing in silicon qubits [5]. Cryo-CMOS circuits are required to realize these control/readout functions with high accuracy.

The operating temperature of a qubit varies depending on the type of qubit. It is tens of mK in a superconducting qubit. In this case, superconducting qubits is placed in the mK temperature stage, which is the bottom stage of the refrigerator, and the cryo-CMOS circuits are placed in the 4 K stage having a high cooling capacity. With this control method, most of the control/readout functions are realized by integrated circuits in a refrigerator, so that the number of interconnects can be significantly reduced. The use of signal multiplexing is also being investigated, as crowded inter-

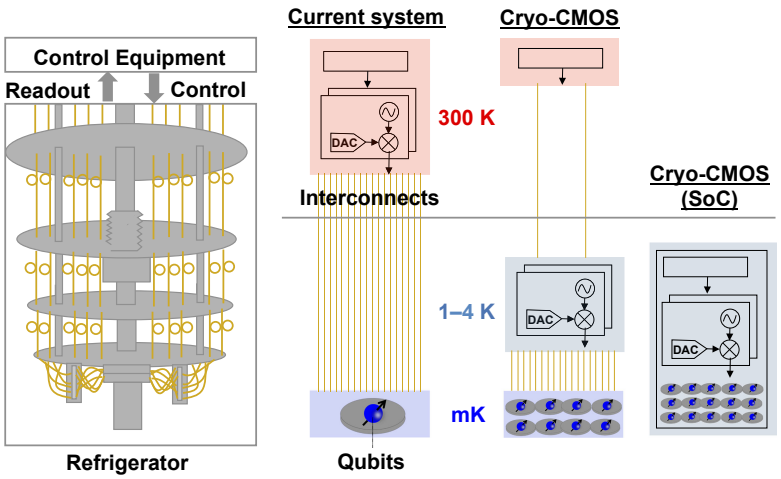

Fig. 1. Schematic illustration of qubit control by cryo-CMOS circuits. By using integrated circuits instead of bulky room temperature control instruments, the number of interconnects can be greatly reduced and paves the way for large-scale quantum computers.

connects between the mK and 4 K stages with increasing qubits. On the other hand, the final goal of qubit control for silicon qubits is assumed to be a system-on-a-chip (SoC) type that is attractive for large-scale integration. Silicon qubits and cryo-CMOS devices are both based on Si LSI technology, and thus integrating both quantum circuits and control/readout circuits on the same die would be possible. In this case, the limitation of the number of qubits can be overcome by the LSI multilevel interconnect. In addition, silicon qubits can operate at higher temperatures as compared with superconducting qubits [6], and thus realizing SoC-type Si quantum computer at the operating temperature of 1–4 K is assumed to be the final objective.

3. Research and development status of cryo-CMOS technology

A compact model applicable to cryogenic operation is required to develop cryo-CMOS circuits. However, the cryogenic performance of MOSFET differs greatly from that at room temperature, and whether the existing compact model can be applied remains unclear. A recent study of the cryogenic compact model from a group at the Swiss Federal Institute of Technology in Lausanne (EPFL) has worked on improving the Enz–Krummenacher–Vittoz (EKV) model, which is a charge-based compact model, and modeling MOSFET characteristics at 4.2 K [2,7]. Improving the temperature parameter of the BSIM model has also been investigated [8]. Since the research on modeling cryogenic MOSFET is in its early stages, a physical understanding of cryogenic device performance is quite important. Research on Si MOSFETs has a long history, and a vast amount of accumulated knowledge on the subject exists. However, as described in Sect. 5, various changes in device parameters that are unique to cryogenic operation cannot be explained only by the existing explanations.

Another problem with cryo-CMOS is that automated high-speed large-volume measurements are not easy at cryogenic temperatures. Modeling in conventional circuits is based on large-volume measurements, and optimizing device parameters is possible using extensive measurement results. However, in cryogenic measurements, the number of transistors that can be evaluated in one measurement cycle is quite limited, and a massive amount of time is required to obtain enough data for modeling. Accordingly, some technical developments for cryogenic large-volume measurements have been achieved. In 2019, the Finnish companies BlueFors and Afore developed an auto-prober for cryogenic 300-mm wafers that can achieve a measurement temperature of 2 K. Intel in the US and Leti in France have announced the introduction of their machines [9]. Cryogenic large-volume measurements are expected to become increasingly important in accelerating cryo-CMOS research.

Currently, although the optimal structure and degree of miniaturization for the cryo-CMOS devices are unclear, the actual development of cryo-CMOS circuits is underway. In 2019, Intel developed Horse Ridge, which is a control chip for qubits that operates at approximately 4 K [10], and one year later, Intel announced Horse Ridge II, which has extended functions [11]. This chip is said to be capable of controlling up to 16 qubits. In addition, Equal1 in the US announced the development of an SoC-type quantum processing unit (QPU), in which qubits and their control circuits are integrated on the same chip [12]. Although it is limited to small-scale qubit control at present, there are reports that cryo-CMOS circuits can achieve qubit control functions equivalent to conventional room temperature instruments [13] and development toward practical use is in progress.

4. Performance of cryo-CMOS devices

Many device parameters depend on temperature, and a decrease in operating temperature considerably alters MOSFET characteristics. Figure 2 shows the temperature dependence of the drain current–gate voltage characteristics of a bulk Si n-MOSFET. At cryogenic temperatures, several changes in MOSFET performance were observed such as on-current increase, off-leakage current decrease, steeper subthreshold swing (SS), and thermal noise decrease. These are the advantages of low-temperature operations and the reason why MOSFETs operating at liquid nitrogen temperature (77 K) have attracted attention as high-performance computing (HPC) technology in the past [14–16]. Since a decrease in intrinsic carrier density and substrate impurity freezeout also occur in cryogenic operation, these factors must also

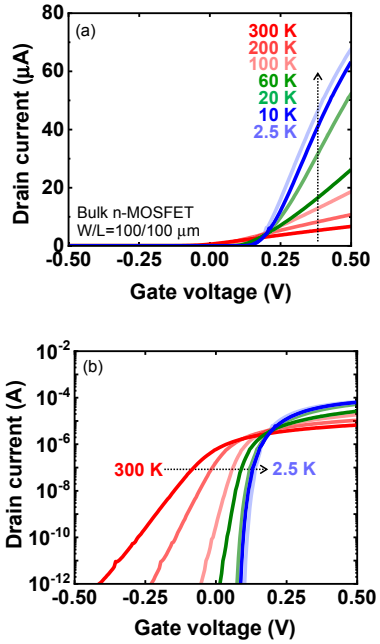

Fig. 2. (a) Linear plot and (b) log plot of drain current–gate voltage characteristics for Si n-MOSFET at the measurement temperatures from 300 K to 2.5 K. Increase in on-current, steeper SS, and shift of threshold voltage were observed as the temperature decreased.

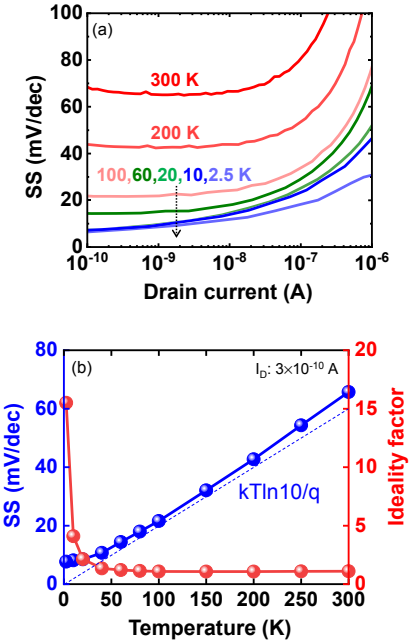

Fig. 3. (a) Drain current dependence of SS at different temperatures and (b) ideality factor as a function of temperature. Deviation of SS and increased ideality factor were observed at the temperature below 50 K [17].

be considered when predicting MOSFET performance. In addition, the device parameters at cryogenic temperatures are known to deviate from theoretical values, and thus the physical understanding of these aspects is urgently needed.

In the following subsections, the cryogenic characteristics of the major device parameters of SS, threshold voltage, carrier mobility, and noise are introduced based on our research results using bulk Si MOSFETs as subjects.

4.1 Subthreshold swing

SS is a parameter that indicates the steepness of on-current in the subthreshold region and is expressed as $SS = nkT\ln 10/q$, where n is the ideality factor, kT is thermal energy, and q is the elementary charge. The theoretical limit of SS at room temperature is approximately 60 mV/dec, and SS decreases monotonically with decreasing temperature. However, SS at cryogenic temperatures deviates from a theoretical value. Figure 3 shows the temperature dependence of SS and the ideality factor of bulk Si n-MOSFET [17]. The ideality factor is close to the ideal value of 1 at temperatures above 50 K, but it increases sharply at temperatures below that. The deterioration of SS at cryogenic temperatures has been observed not only in bulk MOSFET but also in other device structures such as gate-all-around and fully depleted Si-on-insulator (FDSOI) MOSFETs [18,19]. This deviation of SS cannot be explained by conventional physical understanding. Recent studies have pointed out that the interface states and band-tail states that are localized near the conduction band contribute to SS deterioration at cryogenic temperatures [20,21]. Our research also experimentally reported that bulk MOSFETs with high interface trap density exhibit large SS deterioration [17]. The modeling of cryogenic SS characteristics must incorporate these band-edge states, which do not need to be considered in the room temperature operation, and further investigation is required.

4.2 Threshold voltage

The threshold voltage is known to increase with decreasing temperature. The dominant factor that affects the shift of the threshold voltage with temperature is the change of the Fermi potential, which reflects the decrease in the intrinsic carrier density with decreasing temperature. For example, the intrinsic carrier density at 4.2 K is quite small at approximately 10^{-678} cm^{-3} [22]. However, it is also known that the threshold voltage is greatly influenced by interface states at cryogenic temperatures as well as SS. Figure 4 shows the temperature dependence of the threshold voltage of bulk Si n-MOSFETs fabricated on different substrate surface orientations. In this experiment, the influence of the interface states on the threshold voltage is evaluated by changing the surface orientation. It has been observed that the threshold voltage shift at cryogenic temperatures tends to increase in correlation with interface trap densities ((100) < (120) < (110)). A similar trend has been reproduced at cryogenic temperatures using a model incorporating the interface states term [23]. On the other hand, p- and n-MOSFETs have different trends in threshold voltage shift at cryogenic temperatures,

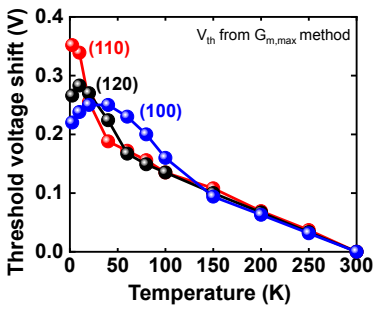

Fig. 4. Temperature dependence of threshold voltage shift for Si n-MOSFETs with different surface orientations. Threshold voltage at cryogenic temperature correlates with interface trap density.

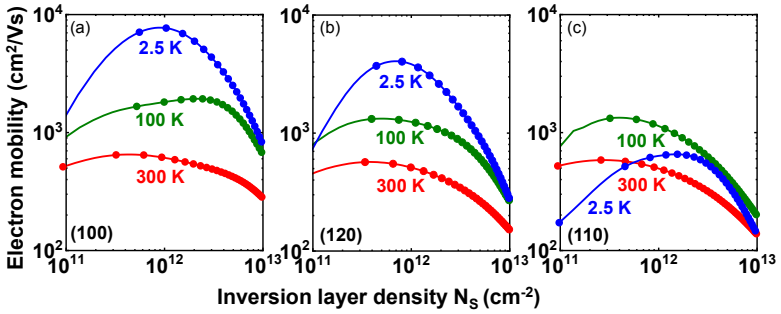

Fig. 5. Temperature dependence of electron mobility for (a) (100), (b) (120), and (c) (110) oriented Si n-MOSFETs. A significant difference was observed in the mobility curve between the orientations only at cryogenic temperatures [27].

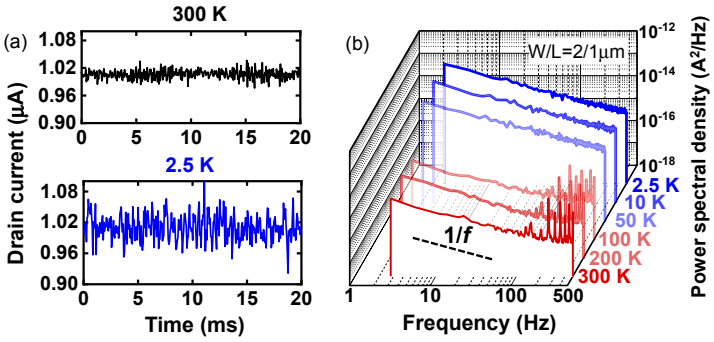

Fig. 6. (a) Drain current transient and (b) temperature dependence of $1/f$ noise in bulk Si n-MOSFETs. $1/f$ noise enhanced significantly at a temperature below 50 K [17].

and further verification is required for a systematic understanding.

4.3 Carrier mobility

The dominant carrier scattering mechanism that limits mobility changes with temperature. The influence of phonon scattering reduces with decreasing temperature, and thus Coulomb and surface roughness scattering determine the carrier mobility at cryogenic temperatures. Coulomb scattering determines maximum drive current and transconductance, which are important parameters for circuit design. Several Coulomb-limiting mobility models have been proposed to date [24–26], and the mobility curves above liquid nitrogen temperatures are reproduced relatively well. However, there are few examples of research at cryogenic temperatures. Figure 5 shows the temperature dependence of electron mobility in bulk Si n-MOSFETs [27]. We investigated the Coulomb scattering effect at cryogenic temperatures by utilizing different surface orientations exhibiting different interface state density. At room temperature, the mobility curves are similar regardless of the surface orientation. On the other hand, at cryogenic temperatures, a significant difference of nearly an order of magnitude was observed in peak mobility between the (100) and (110) orientations. This indicates that the Coulomb-limiting mobility decreases significantly at cryogenic temperatures depending on the interface trap density, where the quality of the MOS interface has a dominant effect on the cryogenic carrier mobility. Understanding the effects of other Coulomb scattering sources such as substrate impurities and also surface roughness scattering is essential for developing a cryogenic mobility model.

4.4 Noise

Cryo-CMOS circuits are classified as analog circuits for some of their functions. Therefore, accurate modeling of noise and also its reduction are particularly important. Thermal noise decreases as temperature decreases, and thus the effect on cryo-CMOS is thought to be minor. On the other hand, very few studies on $1/f$ noise characteristics below several Kelvin have been conducted [28,29], and its cryogenic behavior has been not fully understood. Against such a background, we began the investigation on $1/f$ noise at cryogenic temperatures. Our recent results revealed that $1/f$ noise in bulk Si n-MOSFETs has been shown to increase considerably at cryogenic temperatures (Fig. 6) [17]. In particular, significant increases in $1/f$ noise have been observed at temperatures below 50 K. We have also confirmed that the interface states are the dominant origin of cryogenic $1/f$ noise. These results suggest that $1/f$ noise becomes a major performance-limiting factor in cryo-CMOS devices, even if it does not affect room temperature operation. Therefore, MOS interface engineering including further reduction of interface states will be required.

As described in this section, the device parameters at cryogenic temperatures deviate considerably from conventional theoretical and empirical values, and establishing new or improved compact models based on an understanding of device physics is critical. In particular, recent studies by the authors points out that the difference in MOS interface quality, which is not a problem during operations at room temperature, has a large impact on each transistor characteristic. Reconsideration of the MOS structure, gate stack material, and fabrication process will be necessary to optimize cryo-CMOS devices.

5. Conclusion

In this paper, we reviewed the development trends of cryo-CMOS technology and described the status of research at the device level. MOSFET performance at cryogenic temperatures is quite different from those at room temperature, and research is being conducted to elucidate the physical origin of these characteristics. Cryo-CMOS device technology is a challenging research topic paving the way for large-scale quantum computers and offers new insight into the semiconductor device physics that is not well discussed even in the long history of Si MOSFET research. Further development is expected as more researchers participate in cryo-CMOS technology both in the device and the circuit aspects.

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Technical terms

Quantum two-level system
A two-level system is a system that consists of two energy levels. In the case of a spin qubit, the energy levels split when a magnetic field is applied to the qubit, forming a quantum two-level system.

Brute force method
This is a method of controlling qubits by preparing interconnects and bulky control instruments outside a refrigerator according to the number of qubits. As the degree of integration of qubits improves, the number of interconnects increases explosively, which means it is practically impossible to realize a large-scale quantum computer with this method.

Signal multiplexing technology
This is a technology that electrical signals are multiplexed on the same transmission path. Frequency multiplexing has been studied for controlling qubits.

SoC
A system-on-a-chip (SoC) is an integrated circuit with different processing functions on a single semiconductor chip. The SoC-type quantum computer integrates quantum circuits and their control circuits on the same chip.

BSIM model
The Berkeley short-channel IGFET model (BSIM) is a compact model for integrated circuit design developed at the University of California, Berkeley. BSIM3 and BSIM4 based on a threshold voltage-based model and the BSIM6 based on a charge-based model have been developed.

EKV model
The Enz–Krummenacher–Vittoz (EKV) model is one of the charge-based compact models. An improved model developed at the Swiss Federal Institute of Technology in Lausanne (EPFL) that can reproduce the cryogenic MOSFET performance at 4.2 K has recently been reported.

1/*f* noise
$1/f$ noise is the noise whose power spectral density is inversely proportional to frequency and is observed in the low-frequency region (also called flicker noise). This occurs in MOSFETs due to several factors such as interface traps.

Profile

Hiroshi Oka received the M.S. and Ph.D. degrees from Osaka University, Japan, in 2015 and 2018, respectively. He is currently with National Institute of Advanced Industrial Science and Technology (AIST), Japan.