LETTER

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A novel guard method of through-silicon-via (TSV)

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Abstract: An effective method of improving signal integrity of through-silicon-via (TSV) is proposed by adding a PN junction around conventional TSV. And the equivalent electrical model of the TSV with PN junction is proposed, based on which the S-parameters are obtained by ADS software and compared those of conventional TSV. It is shown that the TSV with PN junction offers more superior signal integrity than conventional TSV. Meanwhile, the S-parameters are validated by employing HFSS, and the results from ADS and HFSS show well agreements. Finally, a feasible fabrication process is given.

Keywords: through-silicon-via (TSV), guard method, PN junction, three-dimensional integrated circuit (3D IC)

Classification: Electron devices, circuits and modules

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1 Introduction

Three-dimensional integrated circuit (3D IC) offers exciting alternative to traditional scaling by stacking the semiconductor layers vertically, resulting in a continuous increase in functionality, performance, and integration density of the IC [1, 2]. Through-silicon-via (TSV) allows for implementing vertical electrical connections between active layers, becoming the most significant technology of 3D IC [3]. Therefore, TSV-based 3D IC provides a most promising platform to implement "more-than-Moore" technologies [4].

However, TSV is a major source of substrate noise that threatens the performance of neighboring devices [5], and the coupling crosstalk noise among TSVs severely impacts the signal integrity of TSV channel [6]. Guarding ring is a widely used method to shield the TSV-induced noise. The $p+$ guard ring [7, 8] and the $n+$/deep n-well guard ring [9] around TSV are respectively proposed as noise coupling suppression methods, but aim at reducing the coupling noise from TSV to devices, but cannot suppress the coupling noise among TSVs effectively. What is more, in order to be effective, the $p+$ guard ring and the $n+$/deep n-well guard ring must be biased.

This letter proposes a novel guard method, making a PN junction around TSV, which can shield the noise from adjacent TSV dramatically, thus improve the signal integrity of TSV effectively and eliminate the trouble of biasing.

2 Method

The schematics of the conventional TSV and TSV with PN junction proposed in this work are shown in Fig. 1. With an addition of an N-silicon region around the conventional TSV, the proposed TSV configuration can be obtained. The corresponding structure parameters are listed as follows. Radius of cylindrical TSV metal r_m is 2.5 µm. Thickness of oxide liner t_{ox} is 0.1 µm. TSV height h is 50 µm. Thickness of N-silicon t is 2 µm.

According to the theory of transmission lines, for the cases of conventional TSV and the proposed TSV configuration, another identical TSV is needed as the

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return-current path. Fig. 2 shows the schematic equivalent electrical models of conventional TSV and TSV with PN junction.

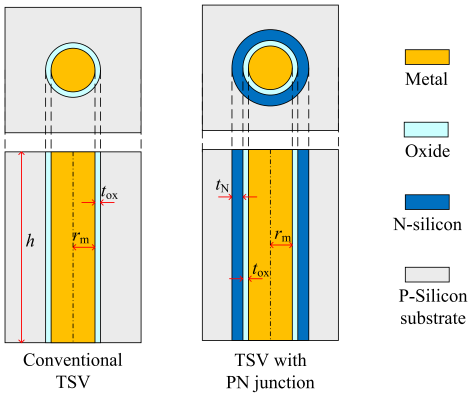

Fig. 1. Top and side views of cross-sectional schematics of different TSV configurations.

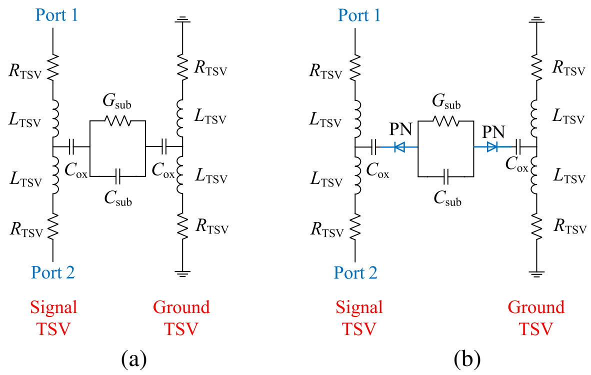

Fig. 2. Schematic equivalent electrical models of (a) conventional TSV and (b) TSV with PN junction.

Note that, N-silicon of the proposed TSV configuration need not be biased, for the reason that a reverse tubular PN junction is formed between the N-silicon and grounded silicon substrate. The junction capacitance can help reduce the total capacitance between signal TSVs and devices. As it is reverse-biased, PN junction can be approximated as barrier capacitor. Therefore, the inclusion of the PN junction is equivalent to an increase in the liner thickness. The junction capacitance can be evaluated as

$$C_{\mathrm{PN}} = \frac{2\pi\varepsilon_{\mathrm{si}}h}{\ln\left(\dfrac{r_{\mathrm{m}} + t_{\mathrm{ox}} + w}{r_{\mathrm{m}} + t_{\mathrm{ox}}}\right)} \tag{1}$$

where w is the width of the space-charge region, which is determined by

$$w = \sqrt{\frac{2\varepsilon_{\mathrm{si}}V_{\mathrm{bi}}}{q}\left(\frac{N_{\mathrm{a}} + N_{\mathrm{d}}}{N_{\mathrm{a}}N_{\mathrm{d}}}\right)} \tag{2}$$

where, $\varepsilon_{\mathrm{si}}$ is the permittivity of silicon; q is electronic charge; N_{a} and N_{d} are the doping concentration of P- and N-silicon, respectively; V_{bi} refers to the built-in potential barrier, which is obtained by

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$$V_{\mathrm{bi}} = \frac{kT}{q} \ln\left(\frac{N_{\mathrm{a}} N_{\mathrm{d}}}{n_{\mathrm{i}}^2}\right) \tag{3}$$

where K is Boltzmann's constant; T is absolute temperature; and n_{i} is intrinsic carrier concentration at room temperature.

The resistance of TSV, including the skin and proximity effects of high speed circuits, is given by [10]

$$R_{\mathrm{TSV}} = \sqrt{R_{\mathrm{TSV\_dc}}^2 + R_{\mathrm{TSV\_ac}}^2} \tag{4}$$

where $R_{\mathrm{TSV\_dc}}$ and $R_{\mathrm{TSV\_ac}}$ is the dc and ac resistance of the TSV

$$R_{\mathrm{TSV\_dc}} = \frac{h\rho_{\mathrm{TSV}}}{\pi r_{\mathrm{m}}^2} \tag{5}$$

$$R_{\mathrm{TSV\_ac}} = \frac{h\rho_{\mathrm{TSV}}}{2\pi r_{\mathrm{m}}\delta} \tag{6}$$

where r_{m}, h, and ρ_{TSV} are the radius, hight, and resistivity of the TSV, respectively; δ is the skin depth. The capacitance of oxide liner, C_{ox}, is modeled by

$$C_{\mathrm{ox}} = \frac{2\pi\varepsilon_{\mathrm{ox}} h}{\ln(r_{\mathrm{m}} + t_{\mathrm{ox}}/r_{\mathrm{m}})} \tag{7}$$

where $\varepsilon_{\mathrm{ox}}$ is the permittivity of oxide silicon. The capacitance and conductance of the silicon substrate between TSVs, C_{Si} and G_{Si} are modeled as

$$C_{\mathrm{Si}} = \frac{\pi\varepsilon_{\mathrm{Si}} h}{\ln[p/(r_{\mathrm{m}}) + \sqrt{(p/(r_{\mathrm{m}}))^2 - 1}]} \tag{8}$$

$$G_{\mathrm{Si}} = \frac{\sigma_{\mathrm{Si}}}{\varepsilon_{\mathrm{Si}}} C_{\mathrm{Si}} \tag{9}$$

where p is the TSV-to-TSV pitch; σ_{si} is the conductance of silicon.

3 Results and discussion

In order to compare the transmissions of signals in the conventional TSV and proposed TSV configuration, S-parameters are investigated. The S-parameters of the equivalent electrical model in Fig. 2 can be acquired by ADS [11]. In order to verify the results, HFSS [12] is employed as a 3D electromagnetism field solver, which is based on the finite element method (FEM). The physical parameters used in the simulations are listed as follows. Silicon substrate resistivity 10 Ω·cm. TSV-to-TSV pitch 20 µm. Doping concentration of N-silicon $1.25 \times 10^{15}\ \mathrm{cm}^{-3}$. Permittivity of oxide silicon 3.9. Permittivity of silicon 11.9.

Fig. 3 gives the simulation results of ADS and HFSS with frequency up to 5 GHz, which show well agreements. It can be summarized from Fig. 3 as well that, the reflection coefficient (S11) of TSV with PN junction is much less than that of conventional TSV. Especially at frequency of 0.3 GHz, the decrease of S11 reaches 13 dB. Compared with conventional TSV, TSV with PN junction provides much better transmission coefficient (S21). Especially at frequency of 1.5 GHz, S21 is improved as much as 0.09 dB. Therefore, the TSV with PN junction can offer superiors signal integrity.

The variation of S-parameter with doping concentration of N-silicon is shown in Fig. 4. It is shown that, with increasing doping concentration, the reflection

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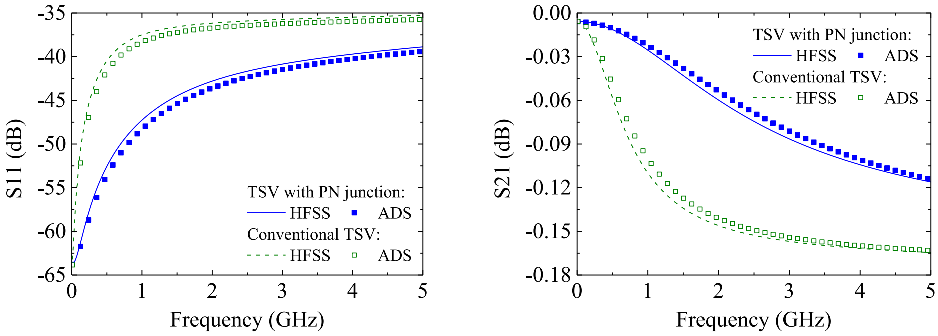
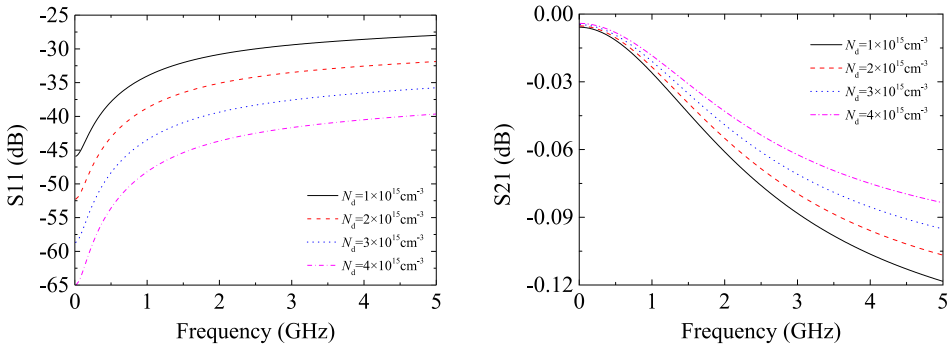
coefficient (S11) of TSV with PN junction becomes larger, while the transmission coefficient (S21) becomes worse. The variation of S-parameter with thickness of N-silicon is shown in Fig. 5. It is shown that, with increasing thickness, the reflection coefficient (S11) of TSV with PN junction gets smaller, while the transmission coefficient (S21) becomes better. Therefore, the TSV with PN junction with lower doping concentration and larger thickness of N-silicon can offer superiors signal integrity.



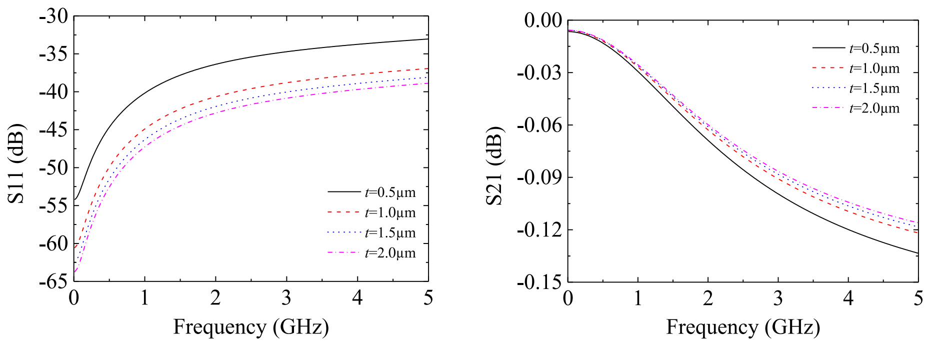
(a) (b)

Fig. 3. (a) S11 and (b) S21 of conventional TSV and TSV with PN junction obtained by HFSS and ADS.



(a) (b)

Fig. 4. (a) S11 and (b) S21 with doping concentration of N-silicon.



(a) (b)

Fig. 5. (a) S11 and (b) S21 with thickness of N-silicon.

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4 Feasible fabrication method

A feasible fabrication process for the proposed TSV configuration is given, as shown in Fig. 6, based on that of conventional coaxial TSV [13]. Formation of the proposed TSV configuration begins with reactive ion etching (RIE) the via. A layer of N-type poly-silicon is then deposited utilizing chemical vapor deposition (CVD). After that, a CVD oxide is deposited, and then the inner copper core is formed by depositing an ionized physical vapor deposition (IPVD) seed and electroplating a copper plug. Finally, a chemical-mechanical polish (CMP) is used to remove excess surface materials.

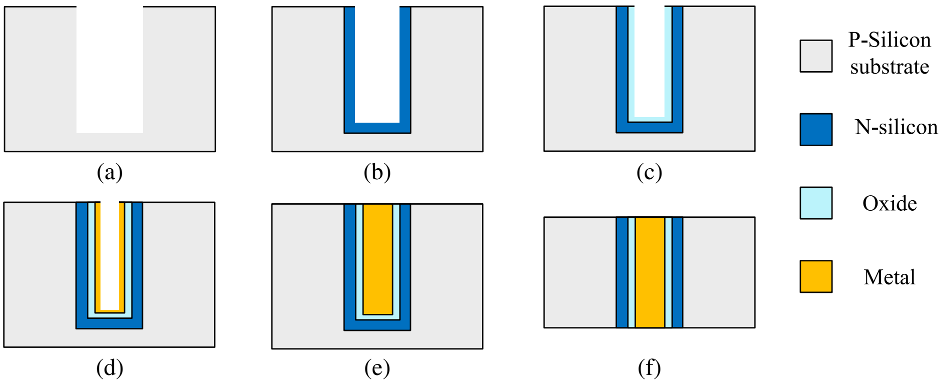

Fig. 6. Fabrication process for the proposed TSV configuration. (a) Etching via by RIE. (b) Depositing a layer of N-type poly-silicon by CVD. (c) Depositing oxide liner by CVD. (d) Depositing copper seed layer by IPVD. (e) Depositing copper plug by IPVD. (f) Remove excess surface materials by CMP.

5 Conclusion

In this letter, a novel effective method of improving the signal integrity of TSV is proposed by adding a tubular PN junction around conventional TSV. Based on the equivalent electrical models, S-parameters of the two configurations are acquired by ADS software, and are verified by employing HFSS, a FEM simulator. Therefore, the TSV with PN junction can offer superiors signal integrity. Finally, a feasible fabrication process for the proposed TSV configuration is given.

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