Analysis of Crosstalk Noise for Coupled Microstrip Interconnect Models in High-Speed PCB Design

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***Abstract*— In high-speed regime, as the PCBs (Printed Circuit Boards) are diminished, and the continuous increasing of the clock frequency in the state-of-the-art digital systems, at higher frequencies there is no more interconnects are transparent. The behavior of the electrical properties of traces (Transmission lines) plays a major role in determining the performance of the PCB board. As an enormous increase of frequencies and usage of data rates and decreasing of size, it's necessary to check the signal integrity issues on a PCBs to reduce failure products. In this paper, we design and analyzed the coupled transmission lines for a single-ended micro-strip model with 50Ω characteristic impedance and extracted RLC parameters. Estimated the Near End Crosstalk(NEXT) and Far End Crosstalk (FEXT) noise in ADS and validated with SPICE Tool on victim line and also, compared with an empirical equations values.**

Keywords— Crosstalk; FEXT; High-speed PCB; Interconnects; NEXT; RLC; Traces

I. INTRODUCTION

The rapid advances in technology have resulted in miniaturized feature size to sub-quarter microns and switching time in terms of Pico seconds or even less. As a result, the degradation of high-speed PCBs due to signal integrity(SI) issues such as impedance mismatching(ringing), coupling effects, clock feedthrough, crosstalk noise, and delay uncertainty noise[1]-[3]. The characteristic impedance and Crosstalk noise are the most effectively considered parameters in PCB design. Without performing the SI and Electromagnetic compatibility(EMC) test for an electronic product, it's may lead to failure of the product and delay in time to the market. These two are the crucial technologies for the electronic product design as continuous increasing of clock frequencies and high data bandwidth for PCB. To achieve such high data bandwidth will be one of the crucial for SI and EMC on PCBs[4]-[6]. As the PCBs (Printed Circuit Boards) are diminished, and the continuous increasing of the clock frequency in the state-of-the-art digital systems, the distortion of a signal and crosstalk between traces on PCB exploit relevant SI issues.

At higher frequencies, there is no more interconnects are transparent. The behavior of the electrical properties of traces plays a major role in determining the performance of the PCB board [7][8]. An wave will be established between two (or more) conductors when a signal propagates along an interconnect. When the spacing between neighboring traces are decreasing (close proximity), the electromagnetic fields from the signal will fringe and interact with adjacent conductors. The interaction of fields induces the coupling of energy from one trace to another when a stimulus is applied to PCB.

Since, In most digital systems use signaling interfaces in which large numbers of traces are routed in parallel through packages, connectors, and PCBs, crosstalk can play an important role in determining the performance of the system. Towards future decreasing of size and increasing of data rates will drive increased crosstalk noise resulting in two major impacts. First, crosstalk will affect signal integrity and timing by modifying the propagation characteristics of the lines (characteristic impedance and propagation velocity). Second, crosstalk coupled noise onto lines, which harms signal integrity and reduces noise margins[9].

Crosstalk is induced by mutual coupling of inductances and capacitances between conductors. As a consequence of mutual coupling, energy exchanges between traces via the magnetic and electric fields (due to mutual Inductance, L_M and capacitance C_M). C_M and L_M induces voltage noise and current from a driven line onto a quiet line by means of electromagnetic field[10].

A voltage noise on the victim in proportion to the rate of change of the current on the driven line according to $\Delta V_L = L_M \, di/dt$ and current is induced onto the victim line in proportion to the rate of change of voltage on the driven line: $\Delta i_C = C_M \, dv/dt$[9][11][12].

To determine the characteristic impedance of trace and crosstalk noise between traces (transmission lines) on PCB in general, there are different types of analysis we can use to calculate the characteristic impedance and crosstalk from the geometry[7][8]. An electromagnetic 2D field solver tool models the electromagnetic fields between transmission lines in a multi-conductor system, providing the basis for equivalent circuit models and the inputs to transmission-line simulators such as SPICE. Reduction of crosstalk noise in interconnect has become more important for high-speed digital applications

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[13][14]. In this paper, estimated the Far End Crosstalk (FEXT) and Near End Crosstalk (NEXT) noise of mutually connected interconnect models with simulations results in Advanced Design System(ADS) and validated with SPICE tool.

Further, the paper is organized as follows, the analytical model for coupled interconnects in II. In Section III, the design of Micro-strip Interconnect model and Extraction of RLC parameters. In section IV, discussion on results of design model and finally, this paper is concluded in Section V.

II. ANALYTICAL MODEL FOR COUPLED INTERCONNECTS

The coupled microstrip line in cross section and Equivalent lumped circuit model of one section of an n-section coupled transmission-line model shown in fig 1. Where C_S, L_S are self-capacitance and self-inductance per unit length, C_C and L_m are mutual capacitance and mutual inductance of lumped elements of transmission line.

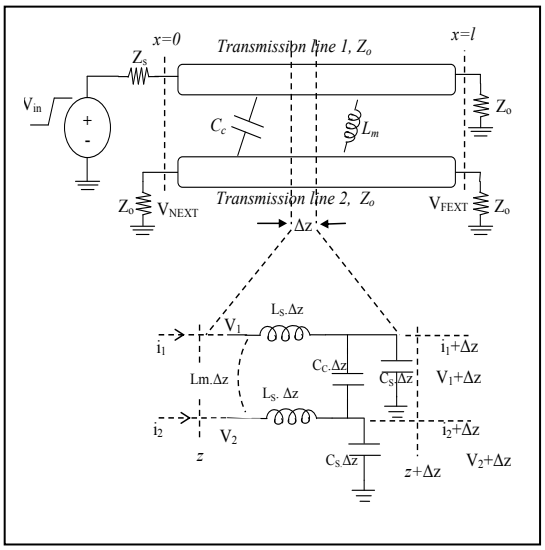

Fig. 1.Measurement of NEXT and FEXT noise of coupled microstrip lines and Lumped equivalent one-section coupled micro-strip line model.

The minimum number of sections are depending on the required bandwidth and the time delay, given by

$$\mathrm{n} = \frac{l}{\Delta z} = \frac{10\, l\sqrt{\epsilon_r}}{t_r . C}$$

Where n is the minimum number of lumped sections for an accurate model, t_r is rise (fall) time, l is a length of the transmission line and C is the velocity of light(3×10^8 m/s). Generalize equation for the lumped equivalent circuit of one-section of an n-section coupled microstrip transmission lines, the voltage change caused by the inductance and the current change by the capacitance of coupled lines one and two is given by

$$V_1(z) - V_1(z+\Delta z) = -j\omega L_S i_1(z).\Delta z - j\omega L_m i_2(z).\Delta z$$
$$= -j\omega[L_S i_1(z) + L_m i_2(z)].\Delta z \quad (1)$$
$$V_2(z) - V_2(z+\Delta z) = -j\omega[L_S i_2(z) + L_m i_1(z)].\Delta z \quad (2)$$
$$i_1(z) - i_1(z+\Delta z) = -j\omega(C_S + C_C)V_1(z)\Delta z + j\omega C_C V_2(z)\Delta z$$
$$= -j\omega[(C_S + C_C)V_1(z) - C_C V_2(z)]\Delta z \quad (3)$$
$$i_2(z) - i_2(z+\Delta z) = -j\omega[(C_S + C_C)V_2(z) - C_C V_1(z)]\Delta z \quad (4)$$

The voltage and current relation of the coupled lumped circuit described in matrix form from (1) & (2) as,

$$\frac{d}{dz}\begin{bmatrix} V_1(z) - V_1(z+\Delta z) \\ V_2(z) - V_2(z+\Delta z) \end{bmatrix} = -j\omega \begin{bmatrix} L_S & L_m \\ L_m & L_S \end{bmatrix} \begin{bmatrix} i_1(z) \\ i_2(z) \end{bmatrix} \quad (5)$$

Where, Indactancematrix, $L = \begin{bmatrix} L_S & L_m \\ L_m & L_S \end{bmatrix}$ H/m

And from equation (3)and (4) as,

$$\frac{d}{dz}\begin{bmatrix} i_1(z) - i_1(z+\Delta z) \\ i_2(z) - i_2(z+\Delta z) \end{bmatrix} = -j\omega \begin{bmatrix} C_T & -C_c \\ -C_c & C_T \end{bmatrix} \begin{bmatrix} V_1(z) \\ V_2(z) \end{bmatrix} \quad (6)$$

Where, Capacitance matrix, $C = \begin{bmatrix} C_T & -C_c \\ -C_c & C_T \end{bmatrix}$ F/m, $C_T = C_S + C_C$

To analyze multi-conductor transmission line, the effects of crosstalk noise induced impedance and velocity changes have on SI and timing issues by first order estimates of the impact. The effective Z_o and propagation velocity(V_P) is calculated by $z_o = \sqrt{\frac{L_S}{C_S + C_C}}$ and $V_P = 1/\sqrt{L_S(C_S + C_C)}$.

The mutual coupled inductance and capacitance causes Near End Crosstalk (NEXT) noise at near to the transmitter end and Far End Crosstalk (FEXT) noise at the receiver end on the victim line when source applied to an aggressor line. The noise signature will be different on the far end and near end on victim line adjacent to an aggressor line. The FEXT noise is related to the difference between the inductively and capacitively coupled currents. The NEXT noise is related to the sum of the inductively and capacitively coupled currents. Coupling effect is a short-range effect and which exists only between two adjacent signal lines[10]. Because of capacitive and inductively coupling sensitive with the coupling effects of the MOS drivers and the conducting elements adjacent to the original signal. The crosstalk noise at both end (NEXT and FEXT) on victim line can be calculated as,

$$V_{NEXT}(t) = \frac{1}{4}\left(\frac{C_C}{C_C + C_S} + \frac{L_m}{L_S}\right).\left[(V_{in}(t) - V_{in}\left(\frac{t-2l}{V_P}\right)\right] \quad (7)$$

$$V_{FEXT}(t) = \frac{1}{2}\left(\frac{C_C}{C_C + C_S} - \frac{L_m}{L_S}\right).\frac{l}{V_P}\frac{V}{t_r} \quad (8)$$

III. DESIGN OF MICROSTRIP INTERCONNECT MODEL AND RLC EXTRACTION

The key factors in determining the performance of microstrip transmission line models are the impedance, delays and losses. The parameters specification for simulation model are:

A. *Materials*

i. Dielectric constant $\varepsilon r = 4.6$ (FR-4)
ii. Loss tangent tan, TanD= 0.02

B. *Substrate*

i. Overall Height of the dielectric material, h =5 mil

ii. Length of the trace L= 3000 mil
iii. Trace width W = 8 mil
iv. Trace thickness T = 1.4 mil (Copper)

Spacing between coupled line, S= W

C. *Micro strip line Impedance(z_o)*

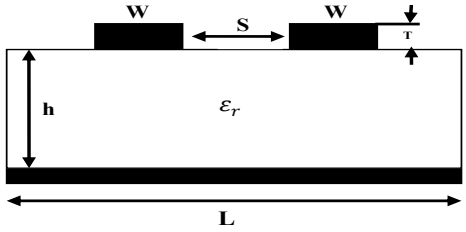

Fig. 2. Coupled micro-strip PCB traces

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98\ X\ h}{T + 0.8W)}\right)\ \text{Ohm}, \frac{W}{h} \leq 1 \qquad (9)$$

The characteristic Impedance is calculated by using (9) Where, Z_0, the characteristic impedance of microstrip model, h - the dielectric height between reference planes, T - copper thickness of the PCB trace, W - trace width, S - spacing between traces and $\boldsymbol{\epsilon_r}$ dielectric constant of the substrate.

TABLE I. THE VALID RANGES OF THE PARAMETER [15]

	Valid range
h	4 mil <h< 60mil
T	0.68mil<T<2.74mil
S/h	0.25<S/h<3.75
W/h	0.1<W/h<5
S/W	0.14<S/W<4

An electromagnetic 2D field solver gives, the inductance and capacitance matrices per unit length for providing properties of physical geometrics and it, model the electromagnetic fields between lines in a multi-conductor system. It provides the inputs to the simulators (SPICE) for the equivalent circuit models of the transmission line. And also, the empirical equations are given[15][16][17] in to calculate the parameters of an equivalent circuit of transmission line under physical geometries and material uses. In this paper, the model design at an operating bandwidth is 2.4GHz, clock frequency is 500MHz and rise time is 200ps, T_d is 500ps and the capacitance and inductance matrices of two-coupled transmission line for design model with 50Ω characteristic impedance are,

$$C = \begin{bmatrix} 3.124 & -0.2313 \\ -0.2313 & 3.124 \end{bmatrix} \text{pF/ Inch}$$

$$L = \begin{bmatrix} 7.70 & 1.1497 \\ 1.1497 & 7.70 \end{bmatrix} nH/\ Inch$$

$$R = \begin{bmatrix} 0.062 & 0 \\ 0 & 0.062 \end{bmatrix} ohms/Inch$$

By using above matrices and equation (7)(8) the FEXT and NEXT noise voltage calculated on victim line at both ends with respect to aggressor line.

IV. RESULTS AND DISCUSSION

The design micro-strip single-ended model for PCB using FR-4 substrate laminate and copper conductor with 50Ω impedance and analyzed at 500MHz clock frequency and 200ps rise time. In fig. 3 the simulation results shows, the output(V_{out}) response of design model when applied 1V input signal(V_{in}) with series resistance applied to aggressor line and the peak output response voltage is 0.904V. And also, analyzed the FEXT and NEXT noise on victim line for design model. From fig.4. the peak FEXT noise voltage is -78.0 mV and NEXT noise voltage is 49.0 mV.

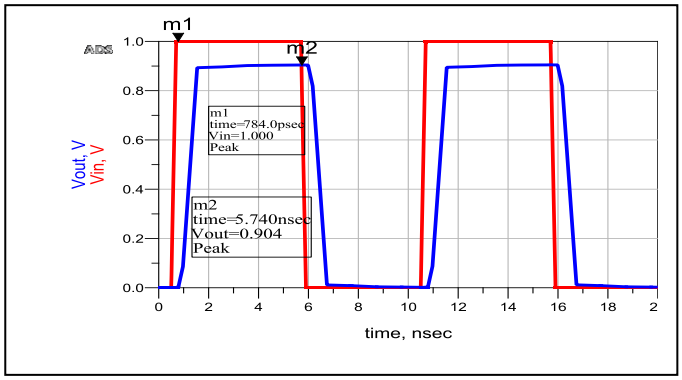

Fig. 3. An Input and Output of single-ended micro-strip line model with 50Ω Impedance in ADS

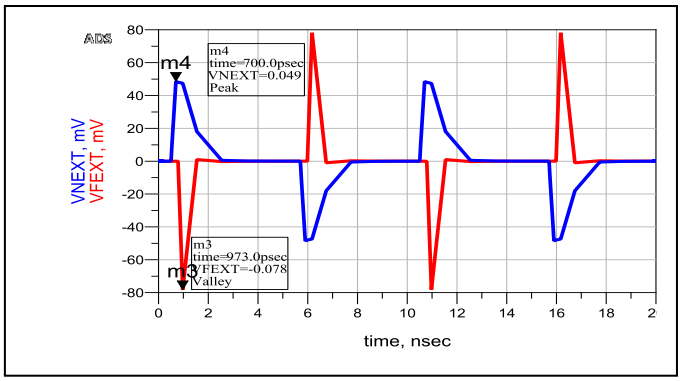

Fig. 4. FEXT and NEXT Noise of single-ended micro-strip line model with 50Ω Impedance in ADS.

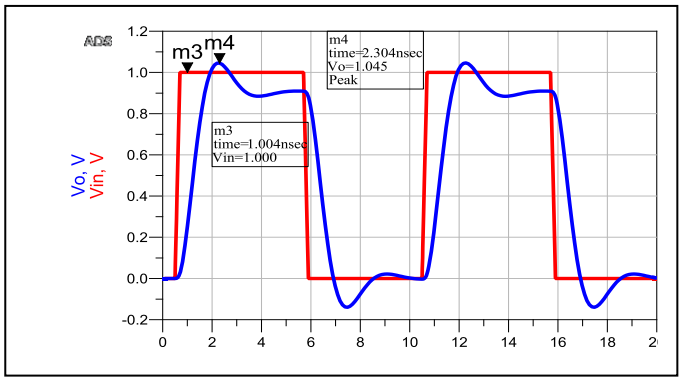

Fig. 5. An Input and output response of extracted RLC model in ADS

The RLC parameters are extracted for design micro-strip model using empirical equations and 2D field solver. In fig.5. shows the output (v_o) response of extracted RLC model when

applied the input stimulus as 1V with series resistance(V_{in}) on aggressor line and due to impedance mismatching, reflections are occurring in output signal and the peak voltage is 1.045 V

Fig. 6 and Fig. 7. the results shows, the FEXT and NEXT noise voltages on victim line and the peak voltages of FEXT noise is -70.0 mV at far end and NEXT noise is 132.0µV at near end on victim line.

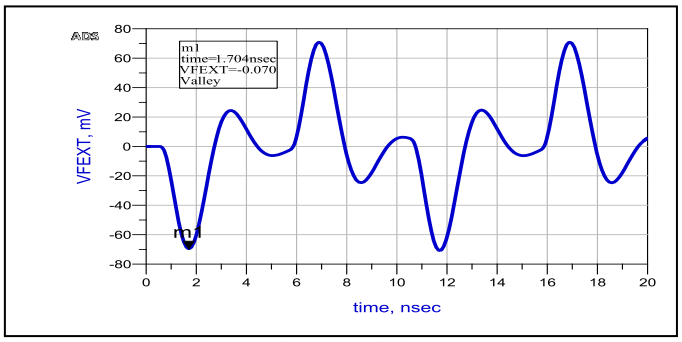

Fig. 6. FEXT Noise of extracted RLC model in ADS

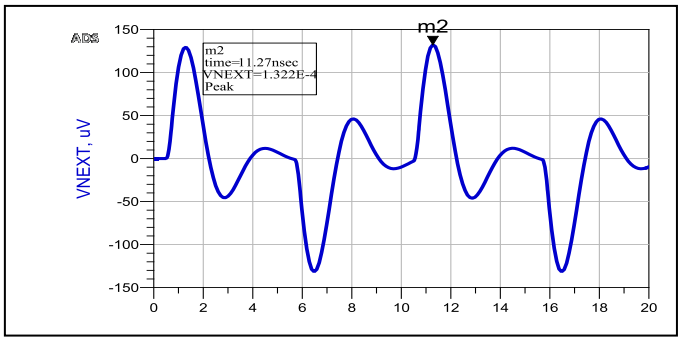

Fig. 7. NEXT Noise of extracted RLC model in ADS

In fig.8. the simulation results shows, an input, output response, FEXT and NEXT noise of the extracted RLC model in spice simulations. the peak output response voltage is 1.2 V when applied 1V input with series resistance. The FEXT noise voltage is -24 mV and NEXT noise voltage is 16 mV. In Table II given the comparison of FEXT and NEXT noise voltage with theoretical, ADS and SPICE tool.

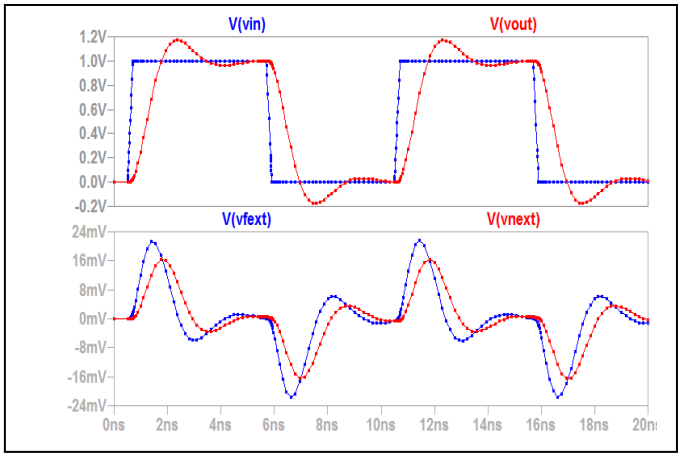

Fig. 8. An Input, Output, FEXT and NEXT Noise of extracted RLC model in SPICE Tool.

TABLE II. COMPARISON OF FEXT AND NEXT NOISE VOLTAGE

	Coupled RLC Interconnect model	
	V_{FEXT}	V_{NEXT}
Theoretical	-65mV	50mV
ADS	-70mV	132µV
SPICE	-24mV	16mV

V. CONCLUSION

In this paper, designed the single-ended micro-strip line model with 50Ω impedance at 500MHz clock frequency for high-speed PCB using copper conductor and FR-4 substrate laminate. An estimated and analyzed the FEXT and NEXT crosstalk noise on victim line at both ends. The obtained results simulated in Advance Design System(ADS) for high-speed PCB design and calculated theoretically. And also, validated with spice tool. The estimated FEXT noise is 7% , 2.4% and NEXT noise is 0.0132%, 01.6% on victim line at both ends in ADS and SPICE tool respectively.

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REFERENCES

[1] X.J.Zhang, W.Jiang, L.Gao, and H.li, “Impact of cross talk on signal integrity of high speed density ceramic package for IC”, IEEE international conference on electronic packaging technology, 2016. C. R. Paul, "Introduction to Electromagnetic Compatibility", New York, NY, USA: Wiley, 1992, (2nd ed., 2006).

[2] C. R. Paul, "Analysis of Multiconductor Transmission Lines. Hoboken, NJ: Wiley, 1994, (2nd ed., 2008).

[3] C. R. Paul, "Analysis of Multiconductor Transmission Lines. Hoboken, NJ: Wiley, 1994, (2nd ed., 2008).

[4] T. L.Wu, F. Buesink and F. Canavero, "Overview of Signal Integrity and EMC Design Technologies on PCB: Fundamentals and Latest Progress", IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 55, NO. 4, AUGUST 2013.

[5] V. Kumar, R. Sharma, E. Uzunlar, Li. Z., R. Bashirullah, P. Kohl, M. S. Bakir and A. Naeemi, " Airgap Interconnects: Modeling, Optimization, and Benchmarking for Backplane, PCB, and Interposer Applications", IEEE tran. on components, packaging and manufacturing technology, vol. 4, no. 8, august 2014.

[6] M. Nakhla and R. Achar, “Simulation of high-speed interconnects,” Proc. IEEE, vol. 89, no. 5, pp. 693–728, May 2001.

[7] Wei Jiang1, 2, Kevin Cai2 , Bidyut Sen2 , and Guoan Wang1, " Practical High Speed PCB Stackup Tool*Generation and Validation ", IEEE 68th Electronic Components and Technology Conference, 2018.

[8] Eric Bogatin, “Signal and Power Integrity-Simplified”, Second edition, Prentice Hall Modern Semiconductor Design Series.

[9] Stephen H. Hall Howard L. HECK, "Advanced Signal Integrity For High-Speed Digital Designs", a john wiley & sons, inc., publication, 2009.

[10] P. Hedari, S. Abbaspour and M. Pedram “Interconnect Energy in High Speed ULSI Circuits” Dept of EE and CS, University of California,Irvine, CA 92697.

[11] C. P. Yuan and T. N. Trick, “A simple formula for the estimation of the capacitance of two-dimensional interconnects in VLSI circuits,” IEEE Electron Device Lett., vol. EDL-3, pp. 391–393, 1982.

[12] N. Delorme, M. Belleville, and J. Chilo, “Inductance and capacitance analytic formulas for VLSI interconnection,” Electron. Lett., vol. 32, pp. 996–997, May 1996.

[13] Douglas Brooks, " *PCB Currents How They Flow,How They React",* Prentice Hall, 2013.

[14] Hall, S. H., Hall, G. W., and McCall J. A., “High-Speed Digital System Design.” John Wiley & Son.

[15] Y.S. Sohn, J.C. Lee, H. J. Park, and S.I. Cho, "Empirical Equations on Electrical Parameters of Coupled Microstrip Lines for Crosstalk Estimation in Printed Circuit Board", IEEE Tran. on advanced packaging, vol. 24, no. 4, november 2001.

[16] S.Kose, E. Salman, and E.G. Friedman,”Shielding methodologies in the presence of power/ground noise”, IEEE tran. On VLSI system vol.19, No.8.Aug.2011.

[17] S. C. Wong, G. Y. Lee, and D.-J. Ma, “Modeling of interconnect capacitance, delay, and crosstalk in VLSI,” IEEE Trans. Semicond. Manuf., vol. 13, no. 1, pp. 108–111, Feb. 2000.