

Signal integrity analysis and Peripheral Component Interconnect Express backplane link compliance assessment

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Abstract

This article presents research conducted on the backplane high-speed Peripheral Component Interconnect Express version 4 (PCIe gen4) link between central processor root complex and the end-point device in order to confirm its compliance. Signal integrity analysis was performed using a method that included channel segmentation, development of corner models for channel segments, full-wave electromagnetic simulation utilizing the finite element method (FEM) and the creation of cascaded channel models, as well as determination of the worst-case models for the channel. The results of this analysis were then used to modify the channel design in order to decrease insertion loss. Changes in the design included utilizing a very low loss dielectric for the backplane board, correcting the sizes of differential pairs and decreasing the via stubs. Frequency domain simulation of the modified channel design has shown a 25% decrease in insertion loss. The calculation of eye diagrams for the modified design has confirmed that the channel parameters meet the requirements for the PCIe gen4 standard.

KEYWORDS

channel segmentation, electromagnetic simulation, high-speed link, S-parameters, signal integrity

JEL CLASSIFICATION

Electrical and electronic engineering

1 | INTRODUCTION

Continuing advancements in big data analytics, artificial intelligence, cloud services, and the Internet of Things are driving the need for capacity to store more and more data. The International Data Corporation (IDC) is predicting that the total volume of data being stored will increase from 33 zettabytes (10^{21} bytes) in 2018 to 175 zettabytes by 2025.¹ The increasing demand for data is creating the need to design efficient and scalable high-performance data storage systems.

An essential part of any modern data storage system is a high-speed low-latency scalable data transfer bus that is energy efficient and cost-effective. Peripheral Component Interconnect Express (PCI-express or PCIe) is a high-speed serial full duplex data bus that has become today's industry standard used in modern data storage systems. The use of PCI-express enables storage systems utilizing multi-host architecture, high-speed data throughput, scalability, I/O virtualization, and

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hot-swap capability.² The bus uses a differential signaling scheme where transmitter (TX) and receiver (RX) differential pairs produce a full duplex data lane. PCI-express base specification allows 1, 2, 4, 8, 12, 16, and 32 lanes configuration to form a link with $\times 1$, $\times 2$, $\times 4$, $\times 8$, $\times 12$, $\times 16$, and $\times 32$ width respectively. More lanes in a link provide higher bandwidth but require additional space on PCB, more power and cost. Practically, $\times 32$ link width is not used in modern designs due to complexity. The PCI-express gen4 bus enables a serial channel data throughput of 16 Gbps with 8 GHz Nyquist frequency utilizing nonreturn to zero (NRZ) signal modulation.³

An essential part of the design flow for interconnects in modern printed circuit boards (PCB) is electromagnetic (EM) simulation using specialized CAD systems. During the design of a high-speed link, it is important for simulation to be performed both before topology design (for the evaluation and optimization of channel parameters within the required frequency range) and after (for design verification). There are three major classes of electromagnetic field solvers⁴: two-dimensional (2D) EM solvers used to calculate signal trace cross-sections, quasi three-dimensional (2.5D) solvers, integrating the calculated planar PCB layers and vias, as well as three-dimensional (3D) solvers essential to analyzing vias, pads for surface mount devices (SMDs), breakout regions for microchips and connectors and other complex structures of the PCB. In modern CAD systems, 2D and 3D EM solvers typically utilize the finite element method (FEM), while 2.5D solvers utilize the method of moments (MoM). EM solvers produce a numerical solution in a form of multi-port element described by a matrix of scattering parameters (S-parameters) for a certain frequency range and suitable for further circuit simulation. Additionally, circuit simulator is used to concatenate (or cascade) S-parameters of transmission line segments in frequency domain to obtain full channel S-parameters or to include to the channel circuit models of lumped components.

The most accurate results are obtained when a full-wave 3D EM simulation is performed for the channel region. The work⁵ reports that the full-wave 3D computing method is efficient and enables reaching a good consistency of the simulation and experiment for a 25 Gbps link. However, if the long channel is composed of several PCBs, this method proves less efficient due to the need for excessive computational resources. In such a situation, one of the acceptable actions to take is to use decomposition or to segment a channel region by individual parts (traces, vias, connectors, SMD-components, and integrated circuit packages) as independent numerical EM models. Then, an EM simulation is performed for each channel part to generate a list of S-parameters, which is then composed (cascaded) in the circuit simulator into an S-parameter model of the full channel. Using the channel segmentation method significantly reduces the computational resources required to calculate the channel while keeping acceptable accuracy compared to the full 3D method.^{6–8} Studies^{9,10} report that channel segmentation method can decrease simulation time by 50–90%, compared to full 3D simulation.

Typical methodology used to evaluate the channel compliance with the PCI-express standard using the segmentation method, 3D EM simulation is proposed in Reference 11. The author of work¹² shows the necessity of accounting for manufacturing tolerances in the PCB parameters when mass producing and using corner simulations to evaluate compliance. Moreover, works^{13,14} suggest a multi-dimensional methodology to evaluate frequency domain compliance using a genetic algorithm to identify channel boundary cases. An alternative to EM solvers simulation approach is based on equivalent circuit models developed in References 15–19, it provides good agreement with FEM simulations and experimental measurements.

This article is dedicated to signal integrity analysis and compliance testing of a PCI-express backplane link within the data-storage system being designed by YADRO. Section 2 of this article contains an overview of the link being simulated. Section 2 also describes a simulation method that includes channel segmentation, the generation and computation of segmented corner EM simulations, the generation of a set of cascaded channel models and identification of the worst case models. Section 3 contains simulation results in a frequency and time domains for the original and the modified link design. Simulation results for the compatibility of the modified link with PCI-express gen4 are also provided. Section 4 contains the conclusions on the performed work.

2 | SIMULATION METHODOLOGY

2.1 | SIGNAL LOSS FACTORS IN HIGH-SPEED LINKS

The PCI-express channels of modern backplane systems may be limited to several PCBs and may have a total length of a few dozen inches. A PCB channel is physically implemented as a complex of inner (striplines) and outer (microstrips) signal traces, and ground/power planes made of copper foil, separated with a dielectric and put together into a multilayer stack. Signal traces connect the channel components installed on the PCB using plated thru holes (PTH), or surface

mount technology (SMT). Signaling lines within different layers of the PCB are interconnected with vias, and connections between different PCBs are implemented using special connector components.

An information signal propagating through the channel is prone to degradation due to impedance discontinuity, conductor and dielectric loss, and crosstalk. Moreover, signal losses in the channel become greater as signal frequency increases, thereby leading to significant signal attenuation and distortion at high data rates.²⁰ Vias, breakout regions of the PCB components, nonuniformity of signal trace widths and gaps in the ground planes all create regions of impedance discontinuity in the channel, which leads to the reflection of high-frequency signal components back to the transmitter, thereby distorting the signal's waveform. Signal loss in the conductor is related to the skin effect, surface roughness and specific resistivity of the copper foil, while dielectric losses are determined by the polarization effect in the insulating material and are described as loss tangent (dissipation factor). Mutual inductance and capacitance between neighboring data lines generate crosstalk. In order to ensure compliance with the PCI-express gen4 standard, signal losses in the channel must be within the defined limits. The losses budget is drawn up at the stage of channel design; moreover, signal loss may be reduced by using signal equalization circuits on the transmitter and receiver side.

In order to minimize signal reflections at the design stage, it is recommended to minimize the length of via stubs, optimize the sizes of the via pads and antipads, perform cuts in ground planes under the pins of SMDs and edge sockets to decrease parasitic capacitance, as well as to refrain from placing signal traces above the gaps in the ground plane. In order to reduce channel crosstalk, it is recommended to route TX- and RX-lines on the different layers of the PCB, isolated from each other with ground planes, as well as to control the distance between differential pairs. Moreover, conductor loss reduction may be achieved by increasing transmission line width and thickness, thereby reducing the resistance of the surface layer, as well as by using foil with lower surface roughness. The value of dielectric losses may be decreased by using insulation material with a lower loss tangent.

In addition to the above design methods used for lowering channel signal loss, signal correction (equalization) circuits are used on the transmitter (TX) and receiver (RX) side. Since the channel impacts the signal as a low pass filter attenuating its high frequency components, leading to the degradation of signal rise time, bit time dispersion and the overlapping of its voltage on neighboring bits, which is called Inter Symbol Interference (ISI). In order to compensate for signal loss within the channel and decrease ISI, the PCI-express gen4 standard presumes the use of a 3-tap feed forward equalizer (FFE) on the transmitter's side, as well as the use of continuous time linear equalizer (CTLE) and decision-feedback equalizer (DFE) on the receiver's side. The FFE-equalizer amplifies high frequency signal components being transmitted relative to the low-frequency components, thereby lowering signal time dispersion at the channel output and reducing the ISI effect. The CTLE equalizer circuit acts as a high pass filter for the signal at the receiver input, thereby reducing low-frequency signal components relative to the high-frequency signal components and simplifying its detection at the receiver. Finally, the DFE equalizer is used for nonlinear correction of the signal at the output of the CTLE, which removes ISI by subtracting the voltage components of a time dispersed bit from the subsequent bits.

State of the art channel designs allow data-rate exceeding 112 Gbps with PAM4 modulation. To establish a reliable channel at such data-rate it is critical to account for signal degrading factors: crosstalk, common-mode conversion, unbalances, noise, and jitter. Mentioned signal degrading factors can be mitigated using equalizations at TX (pre-/de-emphasis) and at RX (CTLE, FFE, DFE). At high data-rate channel analysis can be made using statistical, channel operating margin (COM) or time-domain IBIS-AMI simulations.

2.2 | BACKPLANE LINK OVERVIEW

The link being researched in this work is part of a PCI-express gen4 interface for the data storage system being designed by YADRO. The link is comprised of three PCBs: a POWER9 base board,^{21,22} a passive backplane and an add-in card (AIC) with a PCI-express gen4 Broadcom switch. The base board and the add-in card are connected to the backplane PCB using a high-speed edge and corner vertical SMT connectors, respectively. The topology of the link being researched is shown in Figure 1, where red is used to indicate the channel between the POWER9 CPU and the switch (CPU-AIC channel), while the switch to the CPU channel is shown in blue (AIC-CPU channel).

The initial link design used in the simulation is based on a previous design, which utilized a PCI-express gen3 bus. The initial PCBs design parameters are listed in Table 1. Differential traces for the link have been designed to have 85 Ohm impedance for the base board and the backplane PCBs, and 100 Ohm impedance for the add-in card. In order to reduce crosstalk, CPU-AIC and AIC-CPU channels have been placed on different signal layers of the PCBs. The total channel length used in the simulation process equals 725 and 760 mm for the CPU-AIC and AIC-CPU channels, respectively.

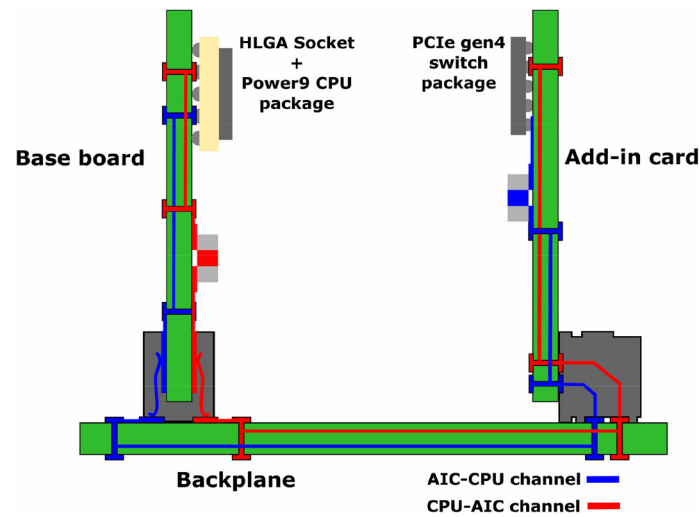


FIGURE 1 The topology of the PCIe link being simulated

TABLE 1 PCBs parameters for the simulated PCIe link

Parameter	Base board	Backplane	Add-in card
Differential impedance, Ohm	85	85	100
Trace width/distance between traces of a pair (for striplines), mil	4.1/4.9	6/6	6/9
Number of metallic layers (signal/polygon)	20 (8/12)	14 (8/6)	14 (8/6)
AIC-CPU total channel length, mm	155	460	145
CPU-AIC total channel length, mm	135	460	130
Dielectric constant ($F = 8$ GHz)	3.5	3.57	3.5
Loss tangent ($F = 8$ GHz)	0.008	0.004	0.008
PCB thickness, mm	2.4	2.2	2.7

2.3 | SIMULATION METHOD

In order to verify that the design for the developed link complies with the PCI-express gen4 standard requirements, the method shown in Figure 2 was used. This method is based on the channel segmentation methodology utilizing corner modeling,¹² and the recommendations for PCI-express channels simulation provided by IBM Corporation as part of its cooperation in the OpenPower consortium.²³ This method includes frequency and time domain simulation stages using the Cadence Sigrity software.²⁴

At the frequency domain simulation stage, channel regions of each PCB were split into individual EM models for numerical simulation. PCB traces were simulated with 2D cross-sections, while PTH vias, breakout regions and pads for SMD capacitors were simulated in 3D. In order to account for mass production effects for PCBs, in accordance with the simulation methodology explained in work,¹² a set of five EM corner models was generated for each channel segment. As a result of this numerical EM simulation, for each channel segment, a set of corner S-parameter models was generated. S-parameter corner models of channel segments were then cascaded into the set of the full channel models using a circuit simulator. This set was then used to simulate channel parameters in frequency and time domains and to define the two worst-case insertion loss (IL) and crosstalk (SXT) channel models. These two worst-case channel models, which nonetheless passed the test for compliance with the PCI-express gen4 standard in frequency domain, were used for time domain channel simulations and eye diagram calculations using AMI-IBIS models of the transmitter and the receiver. Vertical and horizontal eye diagram openings calculated for bit error rate (BER) of 10^{-12} were checked for compliance with the standard. If the sizes of the eye diagram of at least one worst-case channel model failed to satisfy the compatibility requirements of the PCI-express gen4 standard at all possible equalizer presets of AMI-IBIS models, then this channel

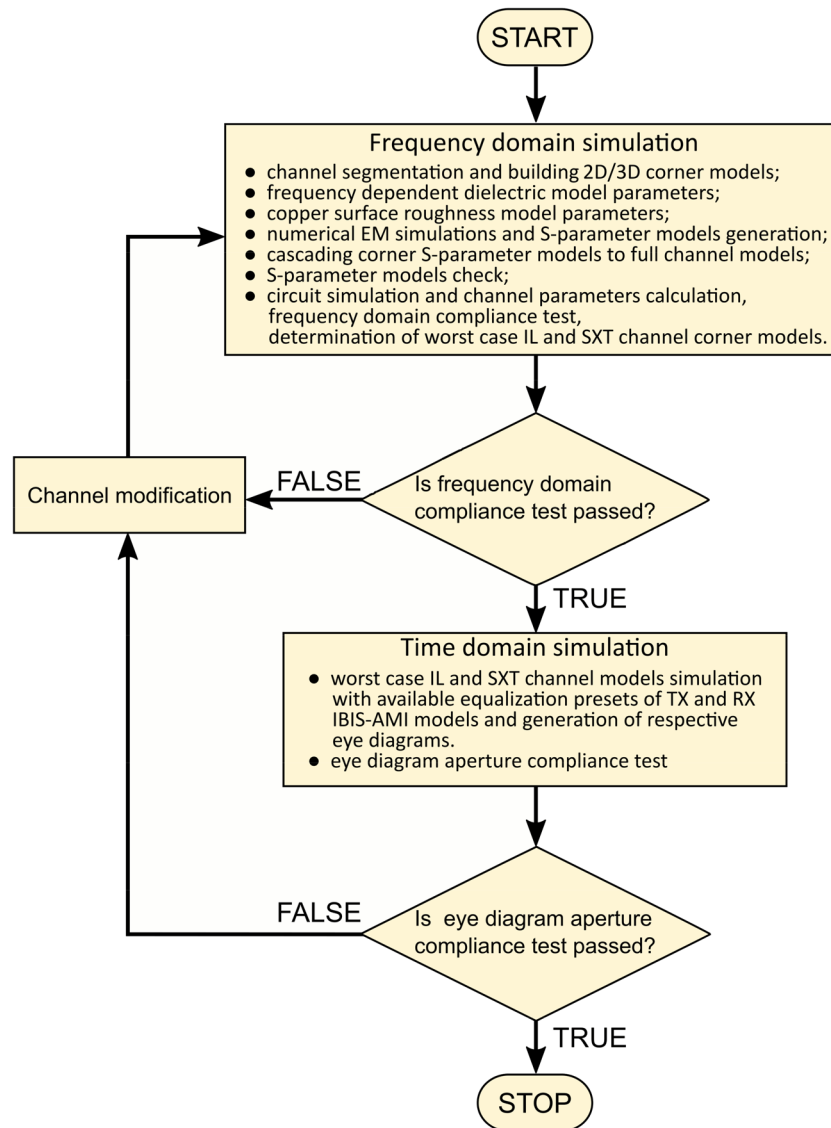


FIGURE 2 Channel design PCI-express gen4 compliance check method block diagram

design needed further work to lower the losses. If both worst-case channel models passed the compatibility test for at least one equalization preset, then the channel design was determined to be in compliance with PCI-express gen4.

2.4 | CHANNEL SEGMENTATION

The channel segmentation procedure was performed for all three PCBs (base board, backplane board, and the add-in card) for both AIC-CPU and CPU-AIC channels. Since the layout of both channels has been designed to be on different layers of the PCB, interchannel crosstalk has not been taken into account for EM simulations for the segmented channels. S-parameter models for the connectors and microchip packages of the IBM POWER9 CPU and the PCIe switch have been provided by their respective manufacturers. Diagram showing channel segmentation is shown in Figure 3, where AIC-CPU and CPU-AIC are shown in blue and green, respectively.

In order to account for crosstalk, each EM simulation of a channel segment contained eight aggressor pairs and one victim pair. The Djordjevic–Sarkar model was used to calculate frequency dependence of the dielectric constant and loss tangent in the insulator.²⁵ The Hammerstad–Jensen model was used to account for copper foil surface roughness.²⁶ Specifications for the dielectric materials and copper foil were provided by the PCB manufacturer.

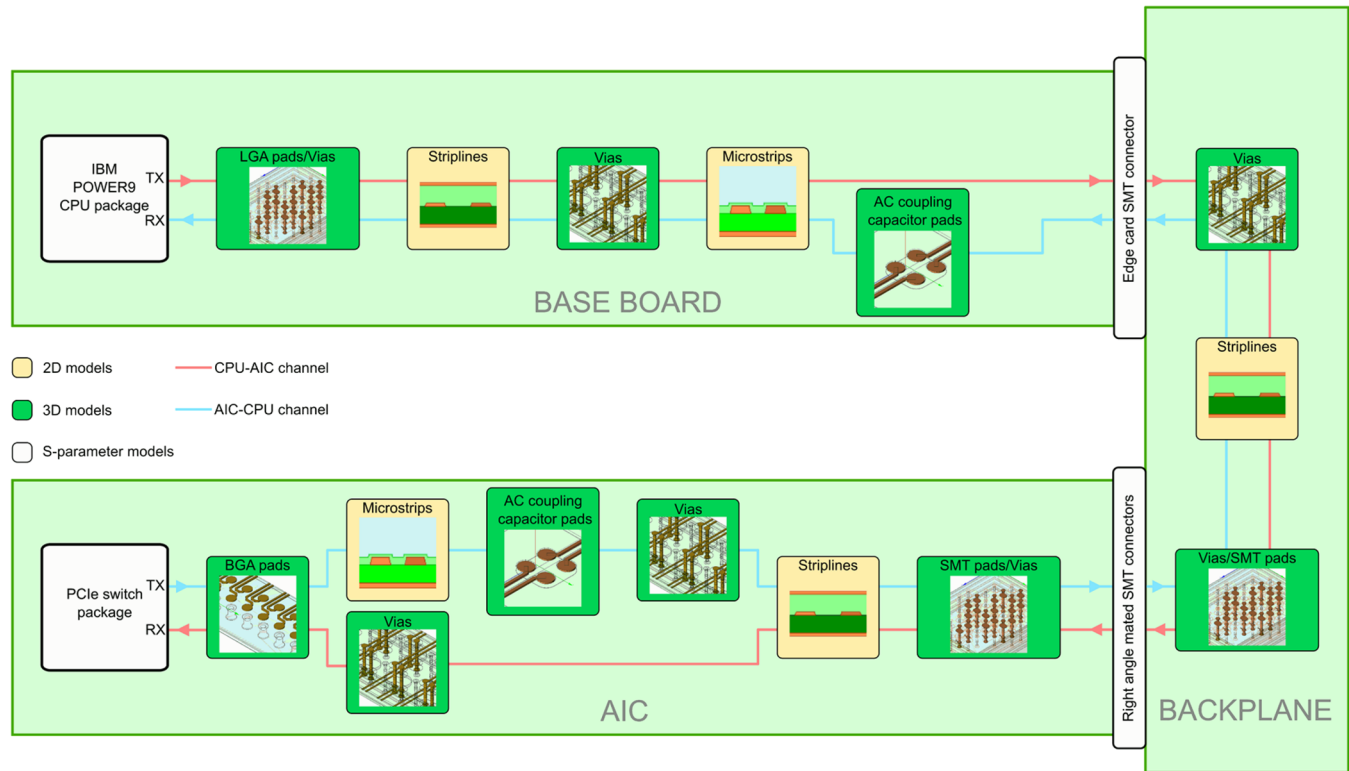


FIGURE 3 AIC-CPU (blue lines) and CPU-AIC (red lines) channels segmentation diagram

2.5 | CORNER MODELS

In order to account for the manufacturing tolerance of the channel parameters due to the effect of PCB mass production, a simulation methodology has been suggested as described in Reference 12. Each channel segment was simulated against a set of five EM corner models, represented within the attenuation-impedance coordinates system (α - Z_0). Attenuation and impedance of the signal within the channel are functions of numerically calculated specific parameters (per unit length) of the RLGC channel segment model – resistance (R), inductance (L), conductance (G), and capacitance (C). The dependencies of attenuation and impedance on RLGC parameters are reflected in Equations(1) and (2):

$$\alpha = \text{Re}[\sqrt{(R + j\omega L)(G + j\omega C)}], \quad (1)$$

$$Z_0 = \sqrt{(R + j\omega L)/(G + j\omega C)}, \quad (2)$$

where j is an imaginary unit, ω is the angular frequency (rad/s).

In order to describe boundary cases within the α - Z_0 coordinate system, a set of five EM corner models has been generated for each channel segment:

- Nominal impedance—nominal attenuation (NZNA);
- Low impedance—low attenuation (LZLA);
- Low impedance—high attenuation (LZHA);
- High impedance—low attenuation (HZLA);
- High impedance—high attenuation (HZHA).

PCB trace EM corner models have been generated using eight cross-section parameters as indicated in Figure 4. Value range for every parameter has been defined in the following Equation (3):

$$x_i = x_{i \text{ nom}} \pm k \cdot \Delta x_i, \quad (3)$$

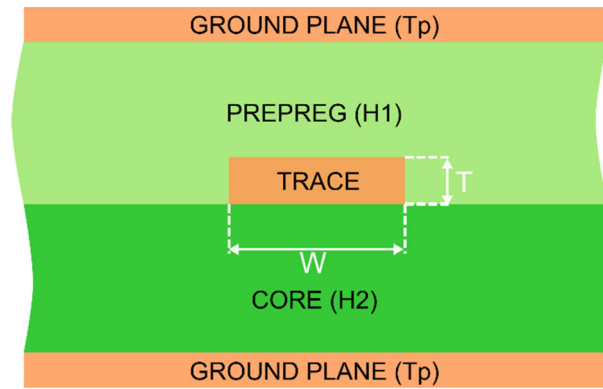


FIGURE 4 Stripline cross-section parameters used for the generation of a corner models set in accordance with work¹²

TABLE 2 EM corner model parameters

Parameter	Description	Difference in relation to nominal value ^a			
		LZLA	LZHA	HZLA	HZHA
W	Trace width, mil	+7.5%	+7.5%	−7.5%	−7.5%
T	Trace thickness, mil	+10%	+10%	−10%	−10%
H1	Prepreg layer thickness, mil	−5%	−5%	+5%	+5%
H2	Core layer thickness, mil	−5%	−5%	+5%	+5%
ϵ_r	Dielectric constant	+2.5%	+2.5%	−2.5%	−2.5%
$\tan\delta$	Dielectric loss tangent	−5%	+5%	−5%	+5%
Tp	Ground plane thickness, mil	+5%	−5%	+5%	−5%
ρ	Copper resistivity, Ohm m	+5%	−5%	+5%	−5%

^aNominal parameter values used for NZNA corner generation are shown in Table 3.

where x_i nom is the nominal value of the i th parameter, Δx_i is the tolerance value for the i th parameter, k is the scaling factor. In generating corner models, the scaling factor $k = 0.5$ was used, since the work¹¹ has demonstrated that this value realistically describes the distribution of the parameter values. The value in relation to the relative discrepancy (d_i) from the nominal value was calculated using the Equation (4). The list of EM corner model parameters and their values are listed in Table 2.

$$d_i = \left(\pm 0.5 \cdot \frac{\Delta x_i}{x_{i \text{ nom}}} \right) \cdot 100\%. \quad (4)$$

The NZNA EM corner models were generated using nominal parameter values for initial channel design for each board. Nominal parameter values are shown in Table 3.

As 3D EM corner models of the channel segments were being generated in accordance with the rules set out in Table 2, all dielectric and conductor layers were scaled in the PCB stack.

S-parameter corner model set for each channel segment on every PCB was calculated using EM field solvers. As a result, each channel segment is represented with five S-parameter corner models related to NZNA, LZLA, LZHA, HZLA, and HZHA cases.

2.6 | CHANNEL CASCADING

S-parameter corner models calculated during numerical EM simulations for channel segments were cascaded using circuit simulator into three sets of five corner models for each PCB. After that, S-parameter models for PCB, board

TABLE 3 Nominal parameter values for initial channel design

Parameter	Board		
	Base board	Backplane	AIC
W, mil	4.1	6	6
T, mil	0.65	0.65	0.65
H1, mil	3.5	3	4
H2, mil	4.16	12	10.3
ϵ_r	3.52	3.23	3.52
$\tan\delta$	0.0088	0.0049	0.0088
T_p , mil	0.65	1.3	0.65
ρ , Ohm cm	1.7×10^{-6}	1.7×10^{-6}	1.7×10^{-6}

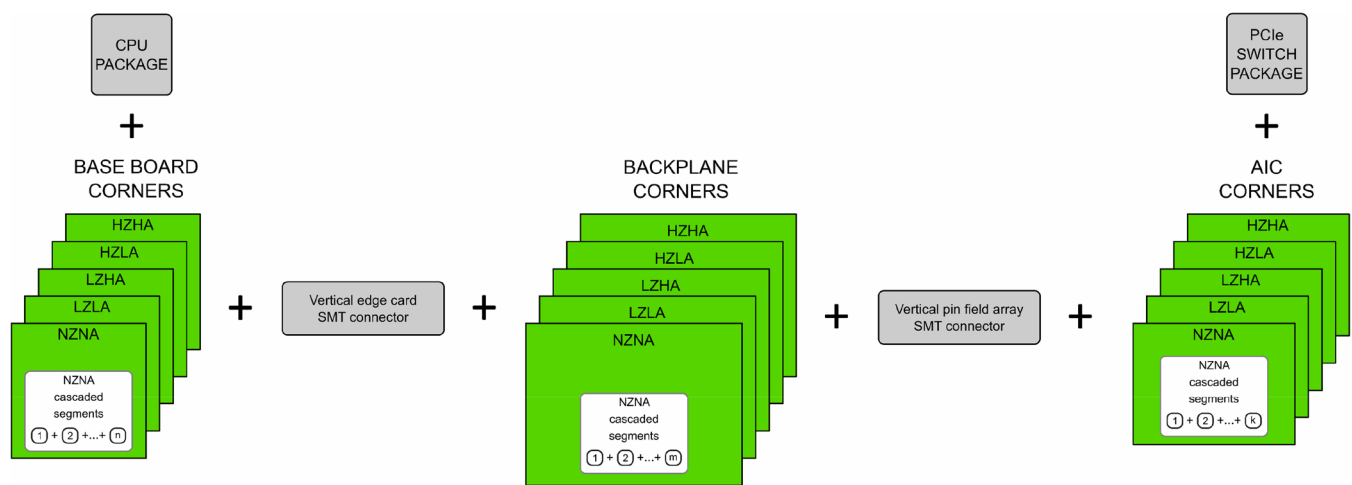


FIGURE 5 Block diagram of cascading segment S-parameter models into a full channel model

connectors, CPU and switch packages were used to generate 125 full channel models for AIC-CPU and CPU-AIC channels. Block diagram describing the channel cascading process is shown in Figure 5.

3 | RESULTS AND DISCUSSION

3.1 | LINK ANALYSIS IN FREQUENCY DOMAIN

Cascaded full channel models for AIC-CPU and CPU-AIC channels were used for frequency domain simulations and the calculation of insertion loss (IL), reflection loss (RL), power sum crosstalk (PSXT), and signal to crosstalk ratio (SXT) for the channel. All frequency domain characteristics of the channels were calculated for the victim pair in the differential mode of signal transmission. During the calculation, only the far-end crosstalk was taken into account: from input aggressor ports to the output of the victim port. The total influence of all aggressors on the victim pair was calculated as the power sum crosstalk (PSXT) using the Equation (5):

$$PSXT = 20 \log \left(\sqrt{\sum_{k=1}^N |S_{ik}|^2} \right), \quad (5)$$

where S_{ik} is the far-end crosstalk coefficient of k th aggressor port and i th victim port, while N is the number of aggressor ports in the channel.

The signal to crosstalk ratio was calculated using the Equation (6):

$$SXT = IL' - PSXT', \quad (6)$$

where IL' and $PSXT'$ are approximated frequency dependencies of insertion loss and the power sum crosstalk. IL and PSXT frequency dependencies were approximated to remove ripples by using the moving average smoothing function. Similarly to the IL averaging procedure of PCIe gen3 link used in Reference 13, sampling window size of 51 frequency points and 20 MHz step were used for moving average function.

Frequency characteristics IL' , $PSXT'$, and SXT were calculated for 125 cascaded models of each of the AIC-CPU and CPU-AIC channels. Worst-case IL and worst-case SXT models for each of the channels were defined as models with the greatest absolute IL' value and the smallest SXT value for 8 GHz Nyquist frequency. A comparison of simulated insertion loss for the worst-case channel models is shown in Figure 6. Worst-case values of insertion loss for the initial design of the link were determined to be -31.8 and -30 dB at 8 GHz signal frequency for the AIC-CPU and CPU-AIC channels, respectively. These values of insertion loss are far greater than the limit values defined for PCI-express gen4, that is, -28 dB³ (red horizontal line in Figure 6). Therefore, it was determined that in order to reduce signal loss, the initial design for the link needed modification.

Since the backplane PCB accounts for 60% of the total channel length, this PCB significantly contributes to the loss budget. In order to reduce dielectric loss in the backplane PCB, its dielectric material was replaced with a low loss material with the dielectric constant of $D_k = 3.2$ and loss tangent of $D_f = 0.0029$ at 8 GHz signal frequency. Moreover, in order to reduce conductor loss, the backplane and base board PCBs trace widths were increased. The trace widths and distance between traces in a pair of backplane PCB were set at 7 mil ($W = 7$ mil, $S = 7$ mil), while the trace width and distance between the traces of the base board were set at 6 mil ($W = 6$ mil, $S = 6$ mil). In addition, in order to reduce reflection in the channels, the maximum length of the via stubs was reduced from 22 to 10 mil.

The AIC-CPU and CPU-AIC channels with the modified design were simulated using the method described in Section 2.3 of this article. At the initial stage, the channels were segmented to create corner models for the segments for numerical EM simulation. Then, the calculated corner simulations of the channel segments were cascaded into full channel models using circuit simulator. Worst-case insertion loss and signal-to-crosstalk ratio models were determined for AIC-CPU and CPU-AIC channels.

A comparison of simulated curves for insertion loss for worst-case channel models is shown in Figure 7. As we can see, the figure demonstrates that the values of all insertion loss curves is above the limit defined in the PCI-express insertion loss limit of -28 dB at 8 GHz, which complies with the requirements.

Simulated return loss curves for worst-case models for the modified design are shown in Figure 8A,B. Figure 9 shows the simulated approximated insertion loss (IL) and power sum crosstalk (PSXT) for the worst-case models of the modified

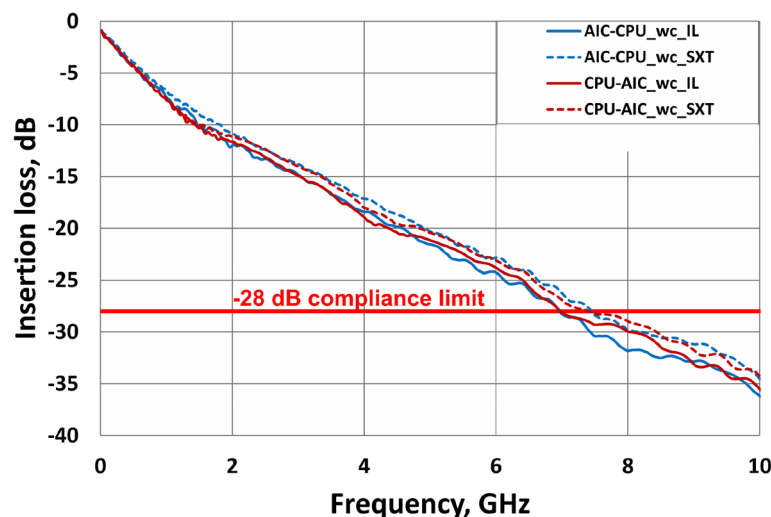


FIGURE 6 Comparison of simulated insertion loss curves for the worst case (wc_IL) and signal-to-crosstalk ratio (wc_SXT) models for the AIC-CPU and CPU-AIC channels

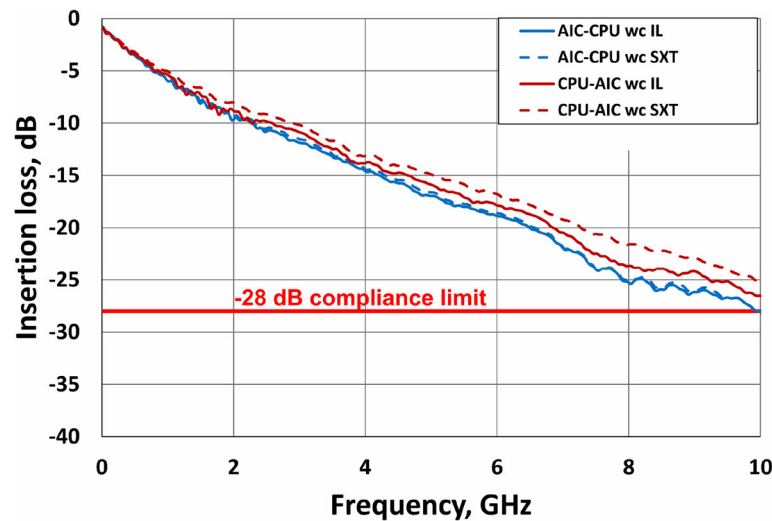


FIGURE 7 Comparison of simulated insertion loss curves for the worst case insertion loss (wc_IL) and signal-to-crosstalk ratio (wc_SXT) models of the modified AIC-CPU and CPU-AIC channels

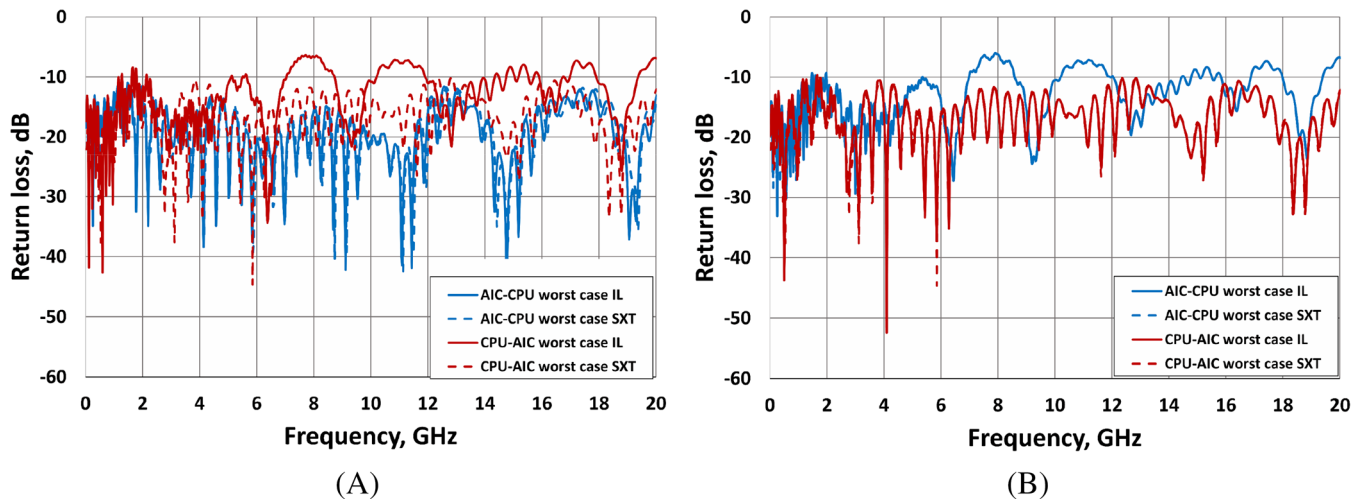


FIGURE 8 Simulated signal return losses for the modified design on the victim input port on the transmitter's side (A) and output port on the receiver's side (B) for worst-case IL- and SXT-channel models

design. Signal-to-crosstalk ratio (SXT) of the worst-case models for the AIC-CPU and CPU-AIC channels is computed from the Equation (6) using approximated IL and PSXT curves. It can be seen from the Figure 9 that SXT is positive in frequency range down to 20 GHz for all worst-case channel models of modified design. High positive SXT lowers the probability for crosstalk related errors in the channel. Frequency domain performance metrics IL, PSXT, and SXT for the 8 GHz Nyquist frequency are listed in Table 4 for all worst-case channel models.

From the insertion loss values shown in Table 4, we can see that the modifications in the channel design have lowered insertion loss by 25% compared to insertion loss in the initial design. From the simulation results, we can see that frequency domain channel characteristics for the modified design are in line with the requirements of the PCI-express gen4 standard. The set of worst-case models for modified design channels were used to produce time domain calculations.

3.2 | LINK ANALYSIS IN TIME DOMAIN

IBIS-AMI models²⁷ describing the performance of the transmitter and receiver of the POWER9 CPU were provided by IBM Corporation, while models for the transmitter and receiver of the PCI-express switch (end-point device) were provided

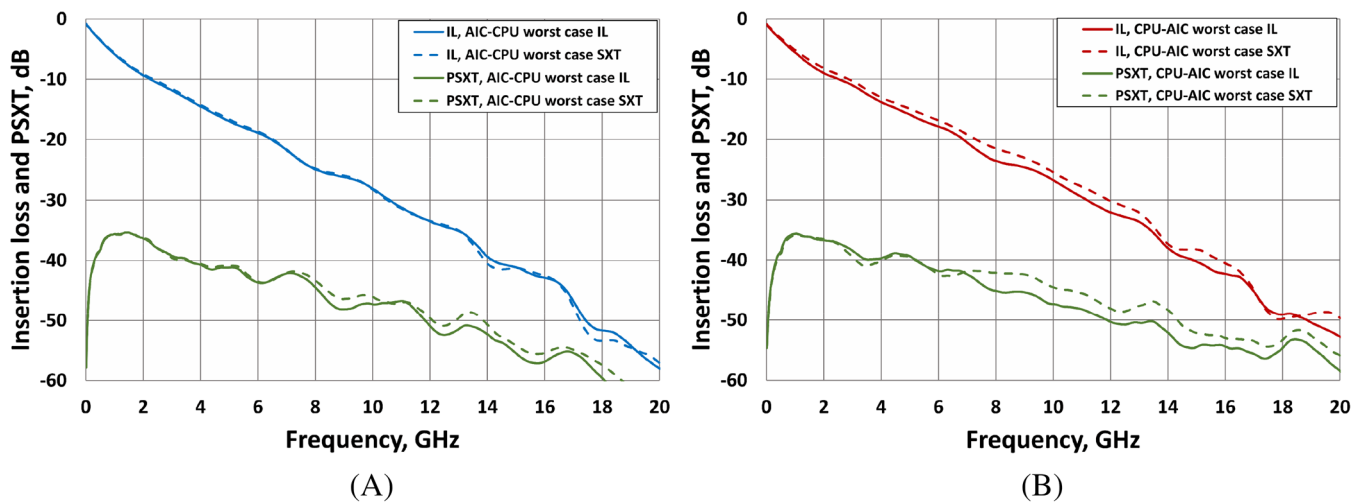


FIGURE 9 Simulated approximations of the IL and PSXT dependencies for worst-case models of the AIC-CPU (A) and CPU-AIC (B) channels of the modified design

TABLE 4 Values of approximated insertion loss (IL), power sum of crosstalk (PSXT) and signal-to-crosstalk ratio (SXT) at the Nyquist frequency of 8 GHz, calculated for the modified channel design

Parameter	AIC-CPU channel		CPU-AIC channel	
	Worst-case IL	Worst-case SXT	Worst-case IL	Worst-case SXT
IL, dB	-25.30	-25.25	-23.66	-21.61
PSXT, dB	-44.33	-43.36	-45.70	-42.09
SXT, dB	19.03	18.11	22.04	20.48

by Broadcom. Transmitter (TX) model of the POWER9 CPU included a 3-tap FFE with 10 presets. Receiver (RX) model of the POWER9 CPU included a CTLE equalizer with 40 presets, 12-tap DFE. Switch transmitter model also contained a 3-tap FFE with 10 presets, while the switch receiver model included a CTLE equalizer with 25 presets and 9-tap DFE.

A time domain simulation was performed for worst-case insertion loss and signal-to-crosstalk ratio models of the AIC-CPU and CPU-AIC channels of the modified design using SistemSI tool, which is part of the Cadence Sigrity package. In accordance with the PCI-express gen4 IBIS-AMI specifications, transmitter models were configured to transmit a signal using NRZ modulation, with a data rate of 16 Gbps. When calculating eye diagrams, the channel input was supplied with a pseudo-random binary sequence (PRBS) of 10^7 bits using a 128/130 b data encoding scheme. When calculating eye diagrams for the AIC-CPU channel, 400 equalization presets (10 FFE \times 40 CTLE) were available for AMI-IBIS models, while for the CPU-AIC channel, 250 presets were available (10 FFE \times 25 CTLE). DFE blocks were set to adaptive mode with equalization taps controlled by receiver IBIS-AMI model both for CPU-AIC and AIC-CPU channels. During the simulation, we used a circuit scheme with eight aggressors and one victim. In order to speed up the simulation of all available equalization presets, crosstalk was not taken into account. For each of the equalization presets, we calculated an eye diagram at the output of the receiver's victim pair. Dual Dirac extrapolation model^{28,29} were used to calculating eye width versus BER curve (bathtub curve). For each of the diagrams, at BER = 10^{-12} , vertical and horizontal openings were calculated (the height and the width of the "eye" of the diagram). The width of the eye was calculated in relative units (UI) as the ratio of eye width in seconds to the duration of the unit interval (62.5 picoseconds for PCI-express gen4). The height of the eye was calculated in millivolts. Once we had calculated eye diagrams for all preset values, for each worst-case model of the AIC-CPU and CPU-AIC channels we picked the five best equalization presets, which corresponded to the largest vertical and horizontal eye openings. Then, the eye diagrams were verified for the best equalization presets with the impact of eight aggressors. The heights and widths of eye diagrams simulated with the impact of the aggressors for the five best presets are shown in Figure 10. Figure 10 also shows dotted limiting lines, defining the minimum sizes of the diagram openings compliant with PCI-express gen4 standard. As you can see, for the POWER9 CPU receiver in

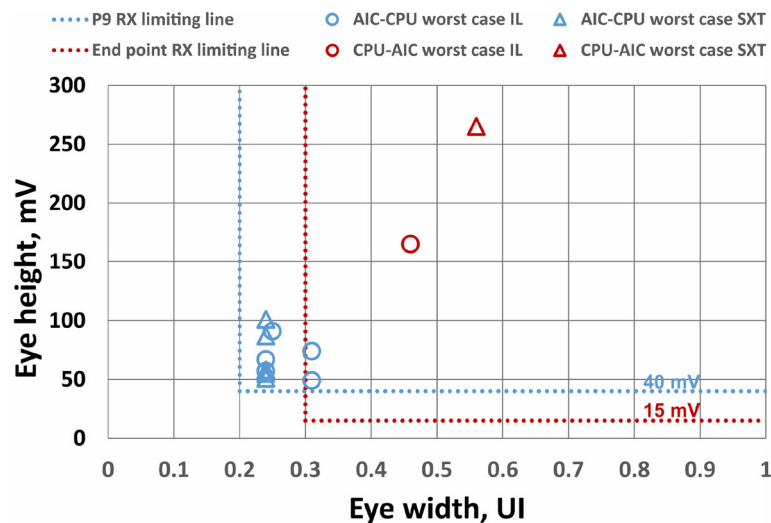


FIGURE 10 Simulated values for horizontal and vertical openings for the worst-case AIC-CPU channel models (blue symbols) and CPU-AIC (red symbols) for the five best presets of AMI-IBIS models of the modified design

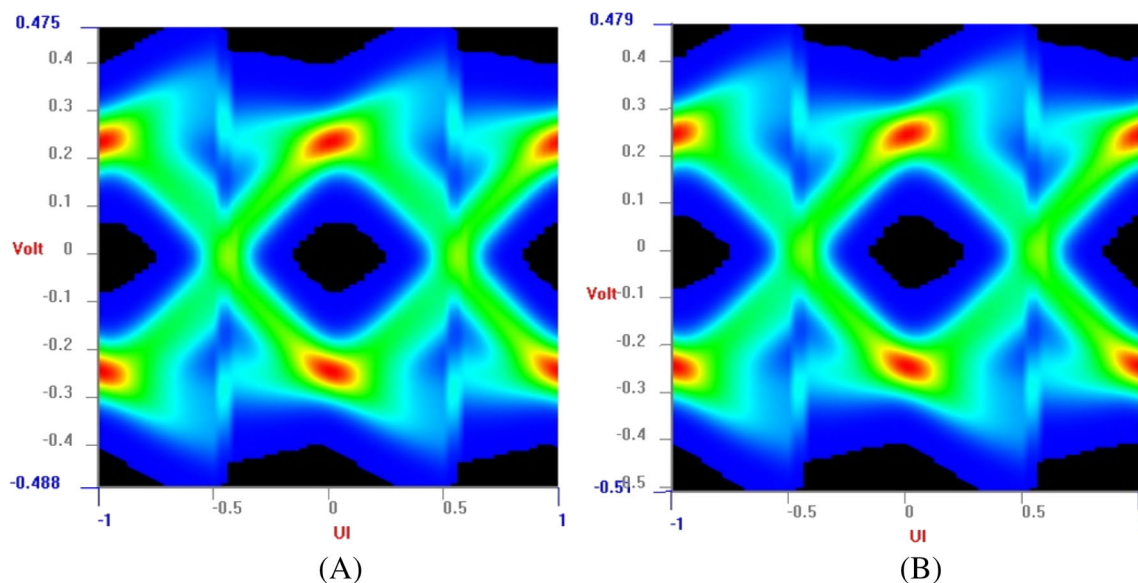


FIGURE 11 Simulated eye diagrams for worst-case IL (A) and SXT (B) models for AIC-CPU channel with modified design

the AIC-CPU channel, the minimum height and width of the eye must be 40 mV and 0.2 UI, respectively (blue dotted lines), while for the switch receiver in the CPU-AIC channel, the minimum height and width must be 15 mV and 0.3 UI, respectively (red dotted lines).

From the figure, we can see that the AIC-CPU and CPU-AIC channels of the modified design are compliant with the requirements of the PCI-express gen4 standard. Due to the lower signal loss, the eye diagram opening of the CPU-AIC channel is greater than in the AIC-CPU channel and does not depend on the equalizer presets set for the POWER9 CPU transmitter. The eye diagrams of the AIC-CPU channel also demonstrated significant jitter and noise. Nevertheless, the eye diagrams of both channels still satisfied PCI-express gen4 compliance requirements.

Simulated diagrams with the widest eye openings are presented in Figure 11 and Figure 12 for AIC-CPU and CPU-AIC modified design channels respectively. Additionally, calculated eye diagrams for the worst-case IL models with unmodified design are shown in Figure 13 for AIC-CPU (A) and CPU-AIC (B) channels. It is seen that eye diagrams are fully closed for both unmodified channels.

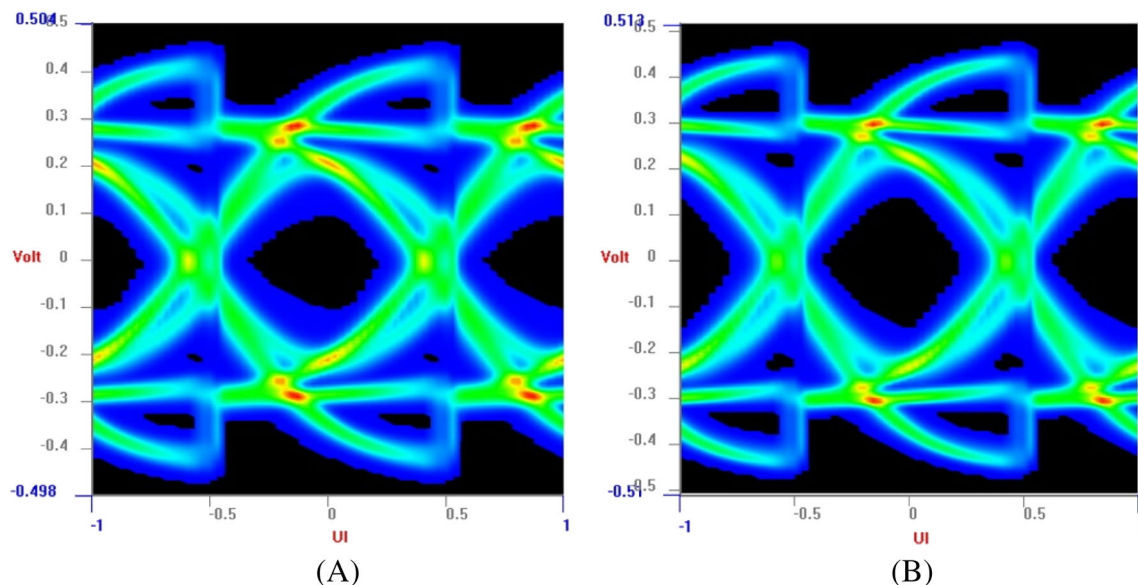


FIGURE 12 Simulated eye diagrams for worst-case IL (A) and SXT (B) models of modified design CPU-AIC channel

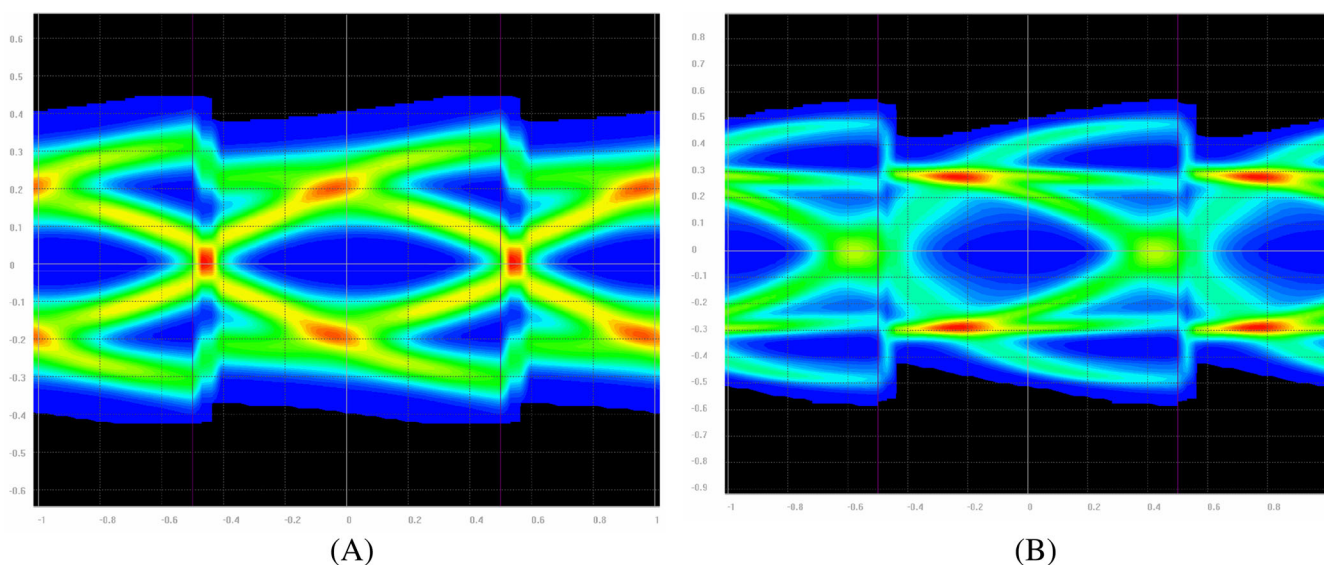


FIGURE 13 Simulated eye diagrams for worst-case IL for AIC-CPU channel (A) and for CPU-AIC channel (B) models without design modifications

4 | CONCLUSIONS

PCI-express gen4 signal integrity analysis of the backplane link connecting IBM POWER9 CPU and the switch was performed as part of this work. The link being analyzed was made of interconnects on the base board containing the CPU, passive backplane and add-in card containing the switch IC. PCBs were connected to form a link using high-speed connectors. During calculation of the link, we used a modeling method that included the stages of channel segmentation, corner modeling and numerical EM calculation, cascading of S-parameter corner models of channel segments into full-channel models, frequency domain simulations and the definition of worst-case channel models, as well as the stage involving time domain simulation of eye diagrams for the channels using IBIS-AMI models. At the stage of initial design channel simulation, significant insertion loss was detected; in order to decrease this insertion loss, the initial link design was modified. In order to reduce signal loss in the backplane, its dielectric was replaced with lower loss dielectric. The widths of

the signal traces were increased—both on the backplane and the base board; moreover, also the length of via stubs in the design was reduced. Further frequency simulations for the modified link showed a decrease in insertion loss of 25%. Time domain simulations the modified link confirmed its compliance with the requirements of the PCI-express gen4 standard.

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PEER REVIEW

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

CONFLICT OF INTEREST

The authors declare no conflicts of interests regarding the publication of this article.

AUTHOR CONTRIBUTIONS

Evgeny Orekhov: Methodology; simulation and analysis, writing original draft; writing review and editing. **Anton Smolenskiy:** Conceptualization (equal); project administration (lead); supervision (lead); writing review and editing (equal). **Boris Popov:** Conceptualization (equal); data curation (equal); formal analysis (equal); writing review and editing (equal).

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