The Signal Integrity of The High-speed IC Design

Kaer Huang, Wenyi Liu, Yan Zhang, Hongcheng Yan[*]
National Key Laboratory for Electronic Measurement Technology
North University of China
Taiyuan, Shanxi
* Corresponding author. E-mail: yanhc519@163.com

Abstract*—*With the continuous improvement of the Embedded Microprocessor's main frequency, the signal transmission and processing becoming faster and faster, the traditional method of circuit design and software will not be able to meet the requirements of high-speed circuit design. However, an increasing number of VLSI chips' work frequency has reached above 100MHz, the CPU with 450MHz will also be widely used. The edge of the signal is becoming steeper and steeper (has reached ps), which makes high-speed system design must face a variety of signal integrity issues. This paper presents a number of common signal integrity issues, and the corresponding improvement of the program. In addition, in the premise of that consider signal integrity in the process of high-speed circuit design, given the specific design, given out the solution for important issues of signal integrity that must to consider during the whole process from the schematic diagram design to PCB placement and routing.

Keywords-signal integrity; termination; high-speed circuit; perfect; routing

I. INTRODUCTION

The development of electronic technology in today is ever-changing. large-scale ultra-large-scale integrated circuits used in more and more common systems. At the same time, deep sub-micron technology used in IC design, makes the chip's integrated scale larger, nano-technology is also in the use. View the development of IC chip from package, chip size is getting smaller and smaller , pin count is getting more and more, speed is getting higher and higher. It can be seen that, the electronic system consisting of IC chips is developing rapidly to the direction of large-scale, small size, high-speed and the development pace is getting faster and faster. This caused a problem, that is, reduce the volume of electronic design led to the layout of the circuit wiring density become larger. At the same time the frequency of the signal is also increasing, making the question of how to deal with high-speed signal as a key factor for the success of design.

With the logic and system clock frequencies rapidly rising and signal edge continuously becoming steeper and steeper in electronic systems, the influence of printed circuit board wires interconnection and board layer characteristics for the electrical properties of the system is also increasingly important.

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II. SIGNAL INTEGRITY ANALYSIS

A. The Influence of Signal Integrity for High-speed Circuit

For low-frequency design, the impact of board wires interconnection and board layer can not be considered, when the frequencies above 50MHz, the distribution parameters, noise, signal impedance matching, signal edge changes of the transmission line, capacitance and inductance, as well as the board material's electrical parameters of the printed circuit board, such issues will have a very big impact on the stability of the system.

These are signal integrity problems, they usually occurred in the periodic signal, such as clock signal. Now, With the continuous improvement of the Embedded Microprocessor's main frequency, the signal transmission and processing speed becoming faster and faster, when the system clock frequency above 100 MHz, the traditional method of circuit design and software will not be able to meet the requirements of high-speed circuit design, However, an increasing number of VLSI chips' work frequency has reached above 100MHz, the CPU with 450MHz will also be widely used. The the signal edge is becoming steeper and steeper (has reached ps), which makes high-speed system design must confront a variety of signal integrity problems[1].

B. Signal Integrity Problems and Solutions

Signal integrity problems are not caused by a single factor, they are caused by many factors in the circuit board design process, the major signal integrity problems: Reflectrion, Ringing, Rounding, ground bombs, Crosstalk, synchronous switching noise(SSN) and electromagnetic compatibility (EMI), as well as non-continuous of transmission lines.

Ringing signal and rounding signal caused by the superabundant line inductance and capacitance, ringing is due to the damping state,while rounding is overdamped state. Ringing and Rounding are the same with the reflection caused by a variety of factors. the Ringing can be reduced through adding appropriate resistance at the source port and load port,but can not be completely eliminated.

Ground Bomb caused by a large surge of current in the circuit. Ringing and Ground Bomb both are the single signal line's (with in-plane loop) phenomenon of the issues of signal

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integrity. Crosstalk is caused by the two signal lines on PCB board and the horizon , it is also known as three-wire system. Crosstalk is the coupling between two signal lines, the noise of each line caused by mutual inductance and mutual capacitivity between signal lines. Capacitive coupling induced coupling current, and the inductance coupling induced coupling voltage[2].

Table 1 lists some common the signal integrity problems in high-speed circuit and some reasons that may damage the signal integrity, and given out some corresponding solutions.

TABLE I. NORMAL SIGNAL INTEGRITY (SI) PROBLEMS AND SOLUTIONS

problems	Possible reasons	solution	Alternative solution
Overshoot/undershoot	Termination resistances are not matching	End to end joint technology	Used the driver with a slow rise time
dc voltage level is not stable	Load on the line is too large	Replace dc load with ac load	Use the driving source with a greater drive current
Excessive crosstalk	Coupling between lines is too large	Use the main driver source with a long rise time	End-to-end joint in a passive receiver, re-wiring or checking the horizon
Propagation time is too long	transmission lines is too long, there is no switching action	Replace or re-wiring, check the serial termination	use the driver with matching impedance , change the routing strategy
Reflection	Source impedance and load impedance does not match	Make the source impedance and load impedance matching with the transmission line impedance	use the serial or parallel termination technique

Fig. 1 shows the wave that haven't been adjusted and the waves those been perfected by different methods.

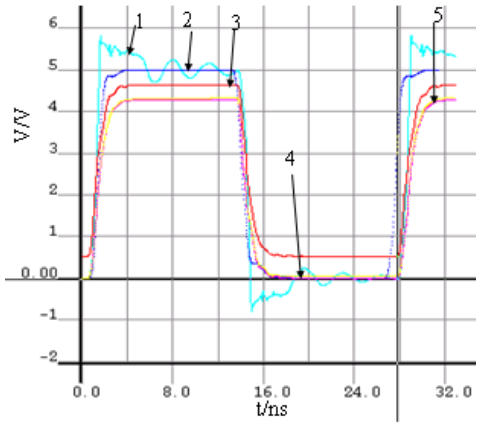

Figure 1. *Simulation result*

Wave "1" shows the signal that haven't been adjusted by jointing any component. Wave "2" shows the signal that adjusted by serial termination technology (head joint 50Ω resistor). Wave "3" shows the signal that adjusted by Thevenin termination (100Ω pull-up resistor, 100Ω pull-down resistor). Wave "4" shows the signal that adjusted by parallel termination (50Ωpull-down resistor). Wave "5" shows the signal that adjusted by parallel AC termination (50Ω pull-down resistor, 0.1uF capacitor). From the graph, the use of these types of termination impedance matching techniques inhibit the signal reflection in different degrees, and then reduces the ringing.

This indicate that using the termination technology in the circuit which there is a big reflection will receive good effect. Different termination technology impact the signal at different aspects,The Thevenin can effectively suppress overshoot and undershoot that makes the signal swing less and the system noise tolerance larger. From the waveform of "2" can be seen that the rising edge of signal is slowing down. And the waveform "3" low-level signals close to the low threshold. In fact, the signal in the actual circuit is not reliable[3].For the same circuit,all different termination technologies can achieve the effect that reducing the signal reflection.But the technology themselves will affect the signal too. We must according to the requirement of signal quality, comprehensively considered the impacts of termination, so that we can get the best signal that been perfected.

III. ACHIEVE THE HIGH-SPEED CIRCUIT DESIGN

The design command that perfecting the signal integrity makes high-speed circuit design more difficult. The board wire long, the key signal's impedance control, differential alignment lines' settings become very important in the design process.

A. The SDRAM Routing Design With Considering The Signal Integrity

There are so many signal integrity problems in the process of circuit design, then how to design effective high-speed IC based on perfecting the signal integrity? At present, SDRAM was used widely, this study used SDRAM as a example to introduce how to design high-speed circuit. In the embedded system uses SDRAM extended data storage area, choose SDRAM's working pattern, if it's maximum frequency up to 100MHz or above, then the SDRAM data lines, clock lines, chip select and other control signal lines are needed long match, the design specific need to follow the following points:

1) SDRAM clock signal: It's frequency is high, in order to avoid transmission line effect, in accordance with the principle that when operating frequency reached or exceeded 75MHz, the wiring length should be within 1000mil. And in order to avoid crosstalk with adjacent signals,the lines'length should be no more than 1000mil, line width 10mil, internal spacing 5mil, external Spacing 30mil, require differential routing, accurate matching differential pair routing, error allowed within 20mil[4].

2) Address, chip select and other control signals: Linewidth 8mil, external spacing 12mil, internal spacing 10mil, as far as possible use a daisy chain Topology, which can effectively control high-order harmonic interference, can longer than clock lines, but not shorter.

3) SDRAM data line: Linewidth 8mil, internal spacing 5mil, external Spacing 10mil, as far as possible wiring in the same layer, the length difference between data lines and clock lines should be controled in less than 50mil.

When the internal line width and line long failed to meet the design command, then we need to set internal constraint for the chip with the high-speed circuit design software.

B. Differential Line And Capacitance, Impedance Control To Improve Signal Interity

In order to Make circuit boards work more stable and get good EMC performance, we can route differential lines and control impedance to design multi-layer circuit boards. At least there is a power layer, a ground layer. Wiring, the bypass capacitor near the chips the more the better. It is best placed in the bottom of the chip on the bottom pcb. Terminal components and fiber-optic components can be placed on the bottom layer, reference resistor should be near RES pin, the other end of the resistance joint to the ground by a through-hole.

VSS joint the resistance's ground end,forming a shield. Differential transmission line route should be close (linewidth spacing 6-8mil), and keep their distance above two linewidth between this differential transmission line and other lines or components. TX and RX differential pair wiring should be away from each other, if necessary, can use the relative layer of pcb.

IV. CONCLUTIONS

Signal integrity is a ubiquitous problem, when we design system high-speed circuit and high-speed single board, we must combine the electrical features setting up and layout,wiring together. In the High-speed circuit design process, first of all, when design the schematic, it is necessary to consider perfecting signal integrity as a major factor that impact the system's function. Joint of its electrical characteristics, add corresponding resistance capacitance or other components to the appropriate place of the design.

For example: add pull-up resistor to the pin with OC door, add decoupling capacitor to the power supply pins of the chips, in most cases,capacitor can make the signals more stable. In the PCB design, when placet and route, we need to place the components in the most reasonable position according to the need of getting the best signal.Such as placed the matching download chip next to the FPGA, the firmware download chip on the best was placed next to the single-chip, a variety of other devices also follow the same rule.

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