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Signal Integrity Improvement on High-Speed Packaging Routing by Enhanced T Stub

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ABSTRACT

In this paper, T stub is adopted in the microstrip lines of the high-speed packaging to reduce the crosstalk. The impedance matching is also improved by using the enhanced core via with optimized surrounding ground vias. The simulation results show the lower far-end crosstalk and better impedance matching design are achieved. The signal integrity of the high-speed packaging has been improved and verified by the eye-diagram performance in the experiments.

I. INTRODUCTION

Signal interity (SI) degeneration on transmission lines occurs due to many factors, including crosstalk among transmission lines, and impedance mismatching, etc [1]. Crosstalk among signal transmission lines includes near-end crosstalk (NEXT) and far-end crosstalk (FEXT) where FEXT dominantly deteriorate SI [2]. The conventional method used for reducing the crosstalk is to adopt guard trace between signal traces [3], [4]. However, the guard traces occupy more layout space, which will decrease the available space for routing especially for compact 3C packaging devices. Moreover, noise might be induced accidentally by the open-stub lines of guard traces [5].

On the other hands, the shape-modified transmission lines or with stubs were proposed to suppress the crosstalk, such as serpentine signal trace [6], alternate stub [2], etc. In this flip-chip packaging design, T stub is adopted to decrease the crosstalk. In contrast to the guard traces, the T-stub microstrip lines enable a high routing density layout with low crosstalk.

Core vias also play a crucial role in the whole signal routing of the multilayer packaging. To improve the impedance mismatching issue, due to via-plate capacitance [7] from the core via and the surrounding ground vias (GND vias), the appropriate slot had been used on the via pad design with the optimized GND vias.

II. T-STUB TO SUPPRESS CROSSTALK

When two signal transmission lines are relatively close to each others, (i.e., the distance between two signal traces is relatively small), the transmission signal at aggressor trace will be coupled to the victim trace to become an interfering noise as shown in Fig. 1. The FEXT voltage and NEXT voltage [8] can be written as

$$V^{FE} = -\frac{TD}{2}\cdot\left(\frac{L_m}{L}-\frac{C_m}{C}\right)\cdot\frac{V_m}{T_r}, \quad (1)$$

$$V^{NE} = \frac{V_m}{4}\cdot\left(\frac{L_m}{L}+\frac{C_m}{C}\right), \quad (2)$$

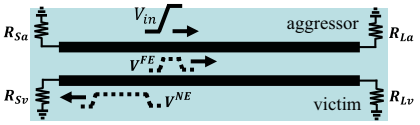

Fig. 1. Adjacent transmission lines with the coupled crosstalk.

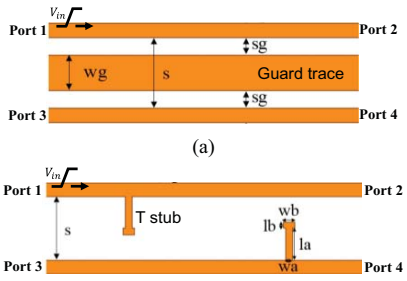

Fig. 2. Microstrip lines (1st layer of the packaging) with different crosstalk-suppression structures: (a) guard trace, (b) T stub.

TABLE I
PARAMETERS OF PACKAGING STRUCTURES

s	sg	wg	wa	wb	la	lb	t1	t2	t3	t4
200	50	100	20	24	100	20	25	30	15	800
All units are um.										

where C_m is the mutual capacitance per unit length of transmission lines, V_m is the maximum voltage applied at the aggressor line, TD is the delay time of a transmission line, L_m is the mutual inductanceper unit length, and T_r is the rising time, C is the self capacitance per unit length, L is the self inductance per unit length.

To decrease the dominant FEXT, the structure of traces can be modified to adjust these parameters in (1) to achieve smaller V^{FE}. In Fig. 2(a) both L_m and C_m can be decreased by adding the guard trace between the transmission lines. Fig. 2(b) shows T stubs are adopted into two adjacent signal traces periodically. The mutual capacitance C_m is dominantly determined by the parameters of T stub on the signal transmission lines. C_m becomes larger when larger la or wb of T stub is used. Then, the values of L_m/L and C_m/C are close to each others by appropriately designing of T stub.

In the packagings of this work, the solder mask has dielectric constant (DK) of 3.25 and dissipation factor (DF) of 0.023 with the thickness of 25 um. The substrate of 1st layer has DK of 3.2 and DF of 0.006 with the thickness of 30 um. The copper's thickness is 15 um. The length of transmission lines is 10 mm, and other parameters

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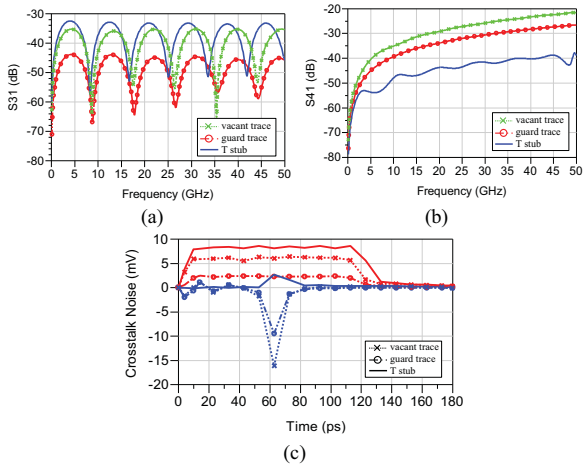

Fig. 3. Simulation results of microstrip lines with different crosstalk-suppression structures: (a) S_{31}, (b) S_{41}, (c) NEXT (red lines) and FEXT (blue lines).

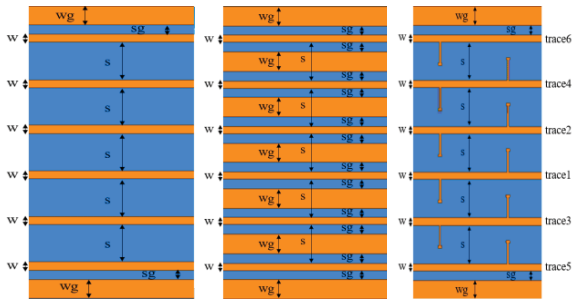

Fig. 4. Top view of 6-lines layout with different crosstalk-suppression structures: (a) vacant trace $w = 50\ um$), (b) guard trace $w = 42\ um$), (c) T stub ($w = 42\ um$).

of these packagings are listed in Table I. To be applied at the high-speed transmission, such as Graphic Double Data Rate 6 [9], the input digital signal has high voltage of 1.35 V, data rate of 16 Gbps, and rising time of 10 ps in the following simulations and experiments.

When the optimization of T stubs on microstrip lines is achieved in Fig. 2(a), the *SI* can be improved more than that with guard traces. As shown in Fig. 3, S_{31} of T-stub transmission lines is larger than that of guard-trace transmission lines due to less signal coupled to adjacent transmission lines. The coupled transmission coefficient S_{41} in Fig. 3(b) shows that T stub has larger suppresion of coupled interference than guard trace does.

The time-domain transients of FEXT (Fig. 3(c)) are in agreement with S parameters. However, NEXT will increase at the transmission lines with T stubs. Becase the growth of mutual capacitance in (2) increases NEXT as well.

III. Multiple I/O Lines

In practical applications, the layout of packaging technologies with different materials is restricted by its design rules, such as line width, line space, etc. Therefore, some methods for reducing crosstalk cannot be adopted in practical packaging, such as guard traces which is close to dies [5].

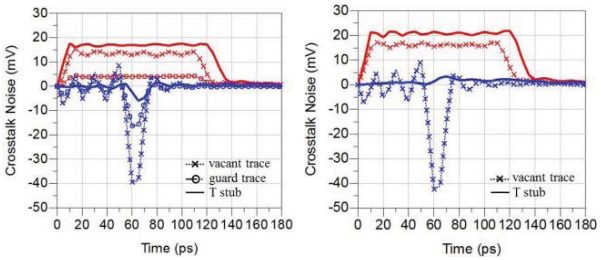

Fig. 5. NEXT (red lines) and FEXT (blue lines) on trace 2 of different crosstalk-suppression structures with different spaces: (a) 200 um, (b) 180 um.

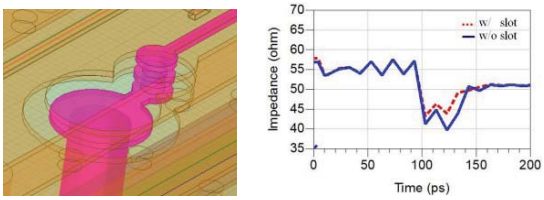

Fig. 6. (a) A slot, whose radius is 140 um, is above the signal core via pad, (b) TDR impedance of the single-ended signal trace from 1st layer to 6th layer through a core via with and without two upper slots of the via pad.

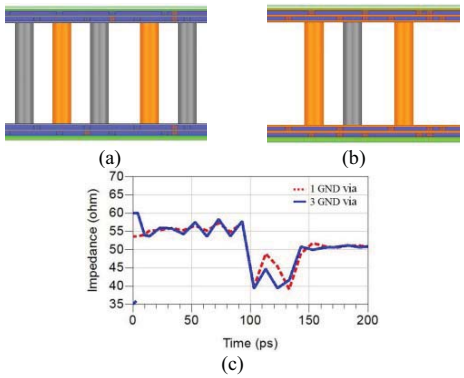

Fig. 7. Cross section of the six-layer routing (signal trace of orange colour) with adjacent GND via (gray colour): (a) three GND vias, (b) one GND via, and (c)TDR impedance with one or three GND vias.

Although the guard trace can reduce FEXT and NEXT simultaneously, this methodology is limited due to its size including a guard-trace line and ground vias. The design rules specify all allowable package parameters of manufacturing techniques. Therefore, the guard traces cannot be used in a smaller layout area full with signal transmission lines, i.e., space with higher line density, in the IC packaging.

There are three different types of signal-trace layout—vacant-trace (i.e., no cross-talk suppression structures), guard-trace and T-stub transmission lines, used for investigation on multiple lines (Fig. 4). When the line space is 200 um, FEXT can be improved by adopting guard trace and T stub (Fig. 5(a)). The value of crosstalk is obtained at trace 2 in Fig. 4 as feeding the step voltage of 1.35 V into its adjacent traces. However, the guard trace cannot be used among transmission lines when the line span is smaller than 200 um. T stub can still be used to improve the FEXT when the line space is 180 um (Fig. 5(b)). The T-stub mechanism can play a useful role to suppress the unwanted crosstalk coupling among transmission lines when the line space decreases, i.e. higher line density areas.

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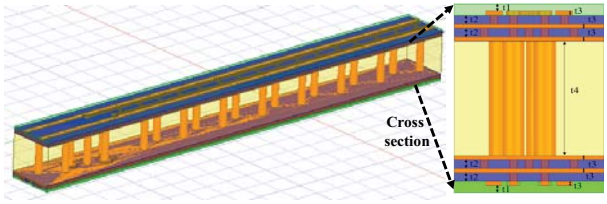
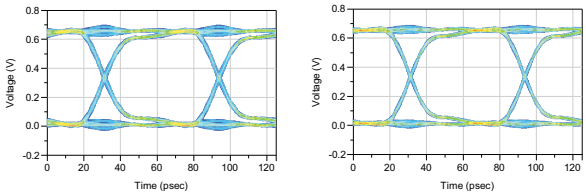


Fig. 8. Schematic of the experimental packaging.



(a) (b)

Fig. 9. Eye diagram of transmission lines with different crosstalk-suppression structures: (a) guard trace, (b) T stub.

IV. Core Vias

In order to enable the mechanical robustness of packaging, the thickness of core layer is generally larger than that of other layers. Consequently, the dimensions of core via are much larger than that of signal traces, and it further causes that the impedance of core via become smaller than 50 Ω. To improve the impedance mismatching issue between signal routing and core via (i.e., SI improvement), we adopted two slots above and below the core via pad in Fig. 6(a) where the T-stub single-ended microstrip lines are on the 1st layer of the packaging. These slots can decrease the parasitic capacitance of the via so that the via's equivalent impedance can be increased close to 50 Ω (Fig. 6(b)).

Moreover, the GND vias, which are generally positioned around the signal core vias, are relocated at the appropriate position for achieving better SI. Fig. 7(a) illustrates there are three GND vias close to these two signal core vias in common packaging, and one GND via is used in this packaging (Fig. 7(b)). Simulation result in Fig. 7(c) indicates the impedance of core via has been increased due to less parasitic capacitance from GND vias.

V. Experimental Results

In the experiments, the models of 6-layer package (Fig. 8) includes two main signal transmission lines with the adopted techniques which includes the T stub, the core pad slots and well-positioned GND vias.

The measurement results in Fig. 9 show the *SI* with these proposed mechanisms is better than that with the guard-trace counterpart. The eye height of the proposed mechanism is 0.55 V which has 2% improvement than that of the guard trace model. The eye width of the proposed mechanism is 60.8 ps which has 1% improvement than that of the guard trace model. The jitter of the proposed mechanism is 1.7 ps smaller than 2.4 ps of the guard trace model.

VI. Conclusion

When the rising time of the digital signal becomes smaller in the high-speed ICs, the crosstalk among signal traces is getting serious to rapidly deteriorate the *SI* of IC packaging. This paper presents T-stub mechanism into the signal traces to suppress crosstalk in contrast to the conventional method—guard trace. In the practical packaging design, the layout density is one of critical concerns. In this analytical study, T stub is beneficial to keep higher layout density than the guard trace does with similar *SI* performance. Furthermore, the impedance of core vias has been increased closer to the required characteristic impedance for overall design optimization.

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