

Parametric Approach for Routing Power Nets and Passive Transmission Lines as Part of Digital Cells

Sukanya Sagarika Meher , Chandan Kanungo, Ashish Shukla , and Amol Inamdar , Senior Member, IEEE

Abstract—In design and layout of rapid single flux quantum circuits, multiple independent biases are often desired to provide flexibility in timings of critical paths. In absence of automated power routing, power nets are often included as part of the layout cells. Multiple variants of each cell need to be manually created to support different biasing configurations. The parametric approach for routing power nets provides the flexibility to dynamically change biasing configurations, based on the same parametric cell. Multiple cells in a circuit block can be configured to be connected to a single power net or can be biased using several independent power nets. With the goal of minimizing the cell size, it is often difficult to maintain rotational symmetry for the power and passive transmission line (PTL) tracks. The parametric approach also enables rotating the cell while avoiding misalignment of the tracks. In addition, our implementation can dynamically add moat bridges to connect ground planes isolated by moats. This is especially useful to bridge very long moats that span two or more adjacent cells. Furthermore, this approach of dedicated tracks for power and PTL routing is also more amenable to design automation.

Index Terms—Design tools, integrated circuit interconnections, superconducting integrated circuits, bias routing, passive transmission routing, parametric cell, very large scale integration.

I. INTRODUCTION

CIRCUITS developed using superconductor logic families have proved energy efficient in the fields of communication, computing and signal processing [1]–[3]. The two logic families that we address here are rapid single flux quantum (RSFQ) and efficient rapid single flux quantum (ERSFQ), where the latter shares the same logic but uses lower power biasing [4]. We design these two logic families using a dual cell library approach with the same core logic sub-cells [5], but different bias sub-cells and subterranean sub-cells. Our ASIC design approach supports using standard cell library as well as custom cell library.

Design of superconducting integrated circuits in our layout methodology is carried out in the context of a particular multi-layer foundry process, such as the 8-Nb-layer planarized process

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S. Meher, A. Shukla, and A. Inamdar are with HYPRES, Elmsford, NY 10523 USA (e-mail: smeher@hypres.com).

C. Kanungo was with HYPRES and is now with the Teledyne Lecroy, Chestnut Ridge, NY 10977 USA (e-mail: Kanungo.chandan23@gmail.com).

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developed at MIT Lincoln Laboratory, known as SFQ5ee [6]. We are using the “M4” metal layer as the primary ground plane. The subterranean layers (M0 to M3 layers) are used for bias (power) lines and passive transmission lines (PTLs).

In our design approach, the bias and PTL tracks are interspersed. As subsequently explained in Section V, aligning the cell and block level tracks require creating four track variants of each cell. Furthermore, it is a common design practice for RSFQ circuits to use multiple independent biases to provide additional flexibility in controlling timing. To support different biasing schemes, multiple variants of each library cell need to be created. In addition, to support cell rotation with proper track alignment, cell variants for different rotation orientations need to be created for all possible track configurations. Thus, in absence of routing tools, hundreds of cell variants need to be created for the different track configurations, biasing schemes, and rotation orientation. We conceived a parametric routing approach that facilitates dynamic reconfiguration of the bias and PTL tracks within a cell, collapsing the multiple cell variants into a single parametric cell.

As this technology is scaled to larger-scale circuits, further development of superconducting electronic design tools [7] is essential. Our cell design approach with subterranean sub-cell facilitates easy adoption of power routing tools. In future, if the tools support power routing with multiple independent biases, we can eliminate the subterranean sub-cells causing no change to the core sub-cell of a library cell. The parametric approach is no longer required. If the power routing is not supported, our parametric approach can be used to quickly generate layout variants of the standard cell for different biasing schemes, track configurations and rotation orientation. The parametric approach of designing digital cells can be applicable for any fabrication technology.

In the following sections we address the cell library architecture and its methodology. Overcoming the disadvantages of the static subterranean sub-cells provides motivation for the development of the parametric approach.

II. LAYOUT ARCHITECTURE FOR DIGITAL CELLS

Various layout architectures are explored to design the cells from the metal stacks provided in the MIT-LL SFQ5ee fabrication process. Of these, comparison between two of the layout architectures are broadly discussed (see Fig. 1). In both the architectures, the upper stack of metal layers (M5–M7) are used to build active circuitry which consists of networks of Josephson

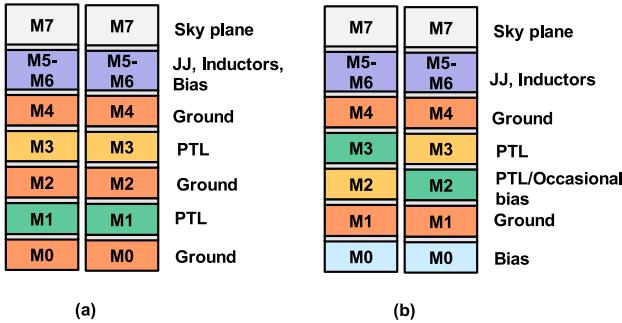


Fig. 1. Layout architectures for cell library. The arrangement of metal stack from MIT-LL SFQ5ee process for (a) first architecture where M5 layer is used for bias and (b) second architecture where M0 and M2 (optional) layers are used for bias purpose. Two metal stacks are shown for each architecture which highlights the difference in vertical and horizontal routing of PTLs.

junctions and inductors. The M4 metal layer is used as primary ground plane. The difference between two architectures is the selection of metal stacks for the bias network and PTL interconnects.

In the first architecture, the bottom metal stack (M0-M4) are used for PTLs and PTL ground planes [6]. Two independent PTL tracks can be laid out, the M1 PTL signal layer with M0 and M2 ground planes, and the M3 PTL signal layer with M2 and M4 ground planes as shown in Fig. 1(a). This architecture provides an advantage by maximizing isolation between the two PTLs. For biasing networks, the M5 metal layer is used. This arrangement leads to area overhead as dedicated space is required to route the bias lines while maintaining separation from active circuitry. Another demerit is it introduces coupling between bias lines and inductors which is a concern for designers [8], [9].

In the second architecture, the bottom stack of metal layers (M0-M4) are used for PTLs, PTL ground planes and bias lines. For PTL routing, the M2 and/or M3 metal layers are used for the PTL signal layer with M1 and M4 ground planes as shown in Fig. 1(b). This architecture introduces asymmetric PTL in the cell layout as opposed to symmetric PTL in the first architecture, while providing similar performance [3], [12]. Since both PTL tracks share same ground planes, coupling between PTL signals may be a concern. The M0 layer is used for the biasing network with the M2 layer as an occasional bias line. The choice of these metal layers for bias provides an advantage by eliminating area overhead as opposed to first architecture. Another merit is this architecture maximizes isolation between bias lines and active circuitry as they are in different metal layers [10], [11]. Both the architectures facilitate dense network of PTLs. Having analyzed the merits and demerits of both the architectures, the second architecture is chosen to build the layouts of digital cells.

III. CELL LIBRARY LAYOUT ARCHITECTURE

The cells are the basic building blocks in designing superconducting circuits [2]. For the cell library, we are building a dual RSFQ/ERSFQ library approach where, with a small incremental effort, we can have libraries for two logic families compared to building library for just one logic family [6]. In this architecture,

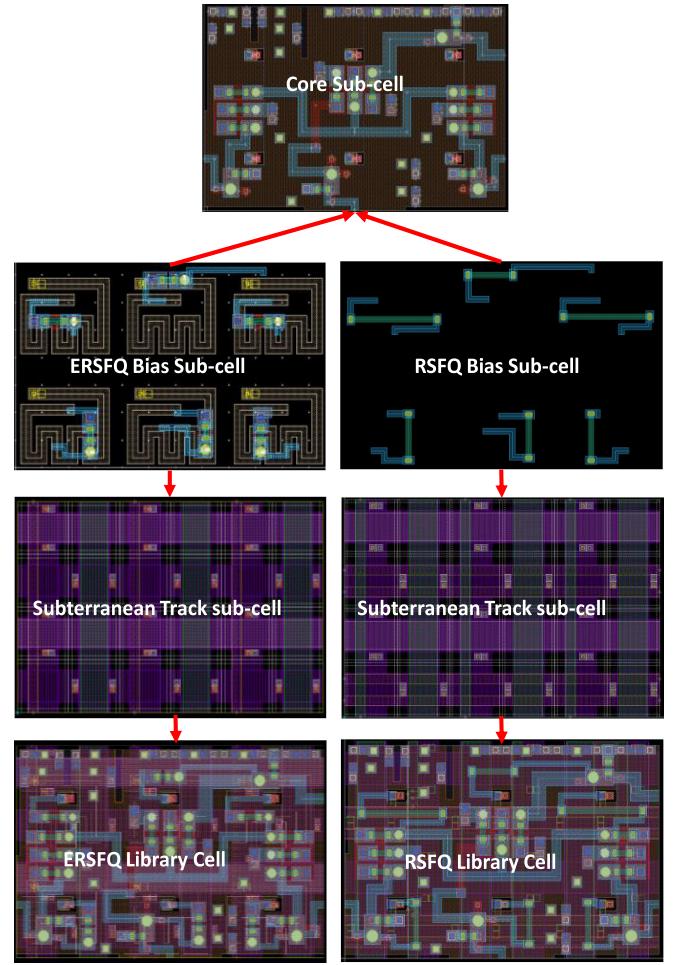


Fig. 2. Example of a $60\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$, XOR cell in dual cell library approach, designed for MIT-LL 10kA/cm². The logic circuit is implemented in core sub-cell and shared between RSFQ and ERSFQ logic families. The bias sub-cell has resistors for RSFQ and kinetic inductance with limiting junctions for ERSFQ families. The subterranean sub-cell supports the bias and PTLs network. The digital cell is laid out by instantiating core, bias and subterranean sub-cells.

M5 to M6 layers are used to build active logic circuitry (junctions, inductors) and incorporated in the core sub-cell. M4 is the main ground plane and M7 is the sky (top ground) plane. In the absence of place and route tools, the digital cells incorporate bias lines and PTL tracks in the form of subterranean sub-cells. The underground layers (M0 to M4) are used to build the bias lines and dedicated tracks for PTLs which are used to connect distant cells. The layout methodology involves designing a core sub-cell that is common between the RSFQ and ERSFQ logic families as shown in Fig. 2.

For RSFQ cells, the resistor biasing network is created in a separate RSFQ bias sub-cell. Similarly, for the ERSFQ cells the biasing network is created in high kinetic inductance (L0 metal layer) in series with a current limiting junction in the ERSFQ bias sub-cell. Thus, for creating the RSFQ and ERSFQ cells, only a small incremental effort is needed for creating different biasing cells [6]. The bias taps in the core sub-cell connects the bias lines to the resistor and bias junction network for RSFQ and ERSFQ cells respectively to bias the junctions. The RSFQ cell has multiple bias groups while ERSFQ cell has a single bias

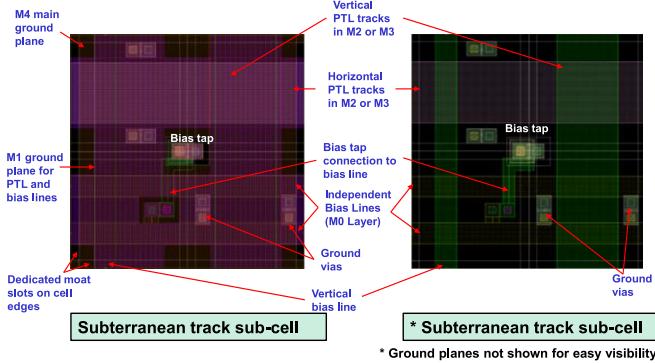


Fig. 3. Layout of a subterranean sub-cell of dimensions $20 \mu\text{m} \times 20 \mu\text{m}$. The left figure shows the different parts of subterranean sub-cell while the right figure shows the same parts; the ground planes are hidden for better visibility.

group. The core sub-cell, bias sub-cell and subterranean sub-cell are instantiated together to create the digital cell as shown in Fig. 2. This approach facilitates reuse of well characterized cells.

IV. SUBTERRANEAN SUB-CELL

The subterranean sub-cell provides biasing network and PTL tracks for the digital cells. As shown in Fig. 3, two horizontal bias lines in M0 layer every $20 \mu\text{m}$, form the primary bias lines. In addition, vertical bias lines in the M2 layer can be used. The bias lines are designed for linewidth of $1.8 \mu\text{m}$. Since the M2 layer is primarily used for PTL routing, the vertical bias lines in M2 restrict the PTL routing in the vertical direction as well. We envision using the M2 bias line sporadically, only when absolutely necessary. The bias lines can be configured into a single bias group for ERSFQ designs as well as multiple independent bias groups to support RSFQ designs. The bias current is provided to Josephson Junctions through bias taps which further connect to bias lines as shown in Fig. 3. For connecting distant cells, PTL tracks are routed in both horizontal and vertical directions within the subterranean sub-cell. Long connections of PTL tracks are established when the cells are abutted at chip level. The designer is given the flexibility to lay the PTLs either in M2 or M3. The PTLs are designed for a lower impedance of 8Ω with linewidth of $5.2 \mu\text{m}$ [12]. The PTL tracks and bias lines are shielded by using M1 and M4 ground planes. These ground planes are stitched at regular intervals of $20 \mu\text{m}$ by PTL ground vias to reduce the resonance of PTL signals [12].

V. CHALLENGES WITH STATIC SUBTERRANEAN SUB-CELL

A. Grid Configuration for Subterranean Sub-Cell

Each subterranean sub-cell has PTL tracks and bias lines that are interspersed at $20 \mu\text{m}$ pitch. Thus, the number of PTL tracks and bias lines in a cell is determined by the cell size. A cell incremented in $2x$ grid size at the block level provides a Bias-PTL pair for every $20 \mu\text{m}$; in this way bias lines and PTL tracks within the cell naturally align with chip tracks. The cell incrementation in $2x$ grid size facilitates the use of a single subterranean track configuration, but with an area penalty. As

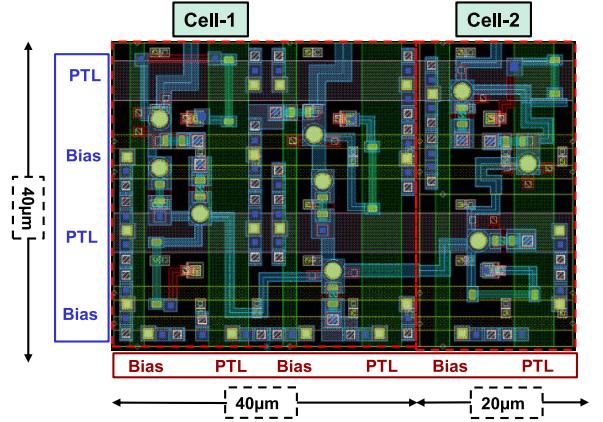


Fig. 4. Layout of block level where cell-1 and cell-2 are abutted. Maintaining $2x$ grid size enables uniform alignment of Bias-PTL track with chip tracks but with area penalty.

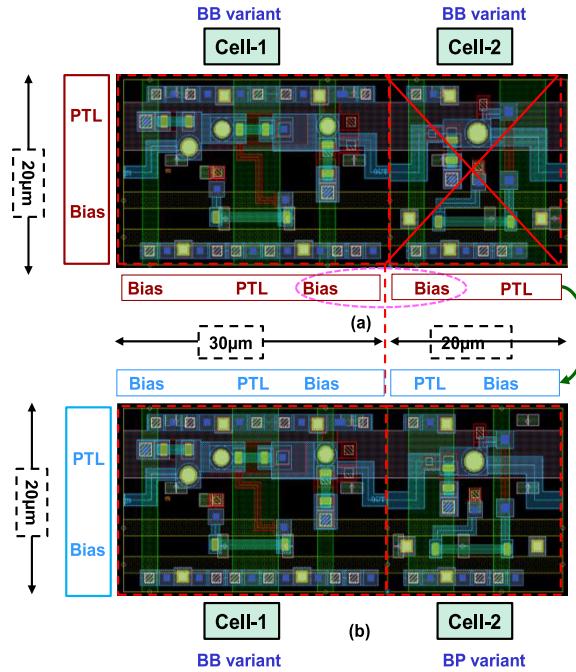


Fig. 5. Layout of block level where cell-1 and cell-2 are abutted. (a) The alignment of tracks is inconsistent when cells are incremented in grid size. (b) To maintain uniform alignment, the track configuration for cell-2 is changed to PTL-Bias and thus need to be re-designed.

shown in Fig. 4, the cell-1 and cell-2 with $2x$ grid size are abutted at block level. This arrangement provides a single uniform grid configuration of Bias-PTL.

In contrast, custom cell design facilitates area efficiency by allowing the cell incrementation in grid size at block level. This configuration provides either a bias line or a PTL track for every $10 \mu\text{m}$. The cell ending with bias line would require the adjacent cell to start with PTL track and vice versa. Thus, four different track configurations are required to maintain uniform alignment of PTL tracks and bias lines with block tracks. As shown in Fig. 5, when cell-2 is abutted with cell-1, it provides a bias-bias pair at the cell boundaries. To maintain uniformity, the grid configuration for cell-2 is changed and the bias line

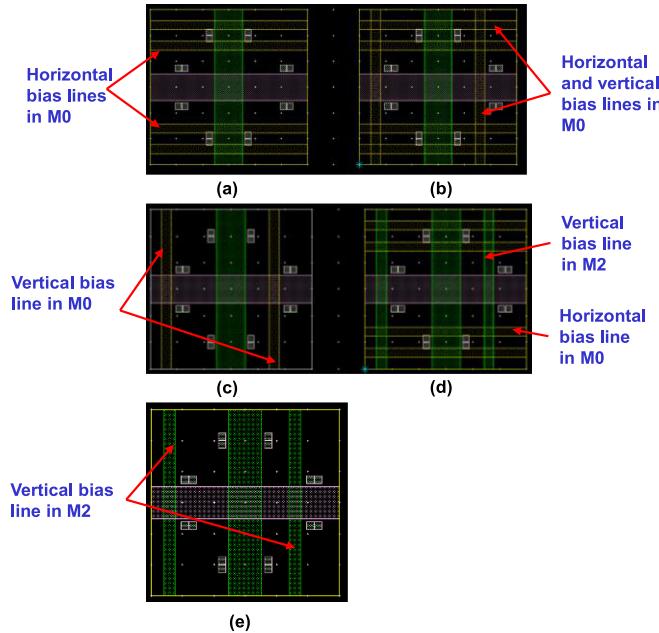


Fig. 6. Layout of subterranean sub-cell highlighting different biasing schemes. Horizontal bias lines drawn in M0 metal layer are primarily used for bias routing as shown in (a), (b) and (d). The vertical bias lines are used occasionally and drawn in M2 metal layer as shown in (d) and (e). Depending on the design requirement, vertical bias lines can also be drawn in M0 metal layer as shown in (b) and (c).

of the preceding cell is followed by a PTL track of the succeeding cell. In conclusion, a designer would need to create four variants of each custom cell in the cell library, which is a tedious task.

B. Bias Configuration for Subterranean Sub-Cell

The subterranean sub-cell provides bias lines which can be grouped into single and multiple bias groups for cells in ERSFQ and RSFQ logic families respectively. RSFQ circuit design requires multiple independent biases which facilitates controlling of critical paths as a function of applied bias voltage. Combining the bias requirements for both ERSFQ and RSFQ circuits, we have shown five different bias schemes as an example in Fig. 6. Multiple independent horizontal bias lines are laid out in the M0 layer which can be grouped into a single bias group as shown in Fig. 6(b) or used as independent biases as shown in Fig. 6(a). Similarly, Fig. 6(c) and 6(e) show multiple independent vertical bias lines in M0 and M2 respectively. Either of these configurations can be used to bias ERSFQ circuits. As shown in Fig. 6(d), the horizontal bias lines in M0 metal layer are primarily used for biasing while the vertical bias line in M2 metal layer is used occasionally for bias purpose.

As shown in Fig. 7, several bias variants are possible by shorting or disconnecting the bias lines. The D flip flop cell layout has two independent bias lines for clock and data paths. The data bias lines in horizontal direction are further shorted using the vertical bias line. Fig. 7 also shows that different bias taps need different connections to bias lines. So multiple variants of a digital cell are required to support multiple biasing schemes, and designing them manually would be tiresome. Having all the

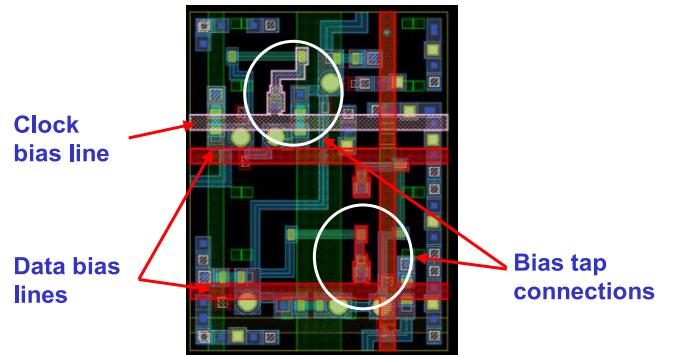


Fig. 7. Example of a D-flip flop cell with independent clock (pink colored) and data (red colored) biases. Bias taps are provided to tap the bias current for Josephson junctions. Different bias taps need different bias connection to the bias lines.

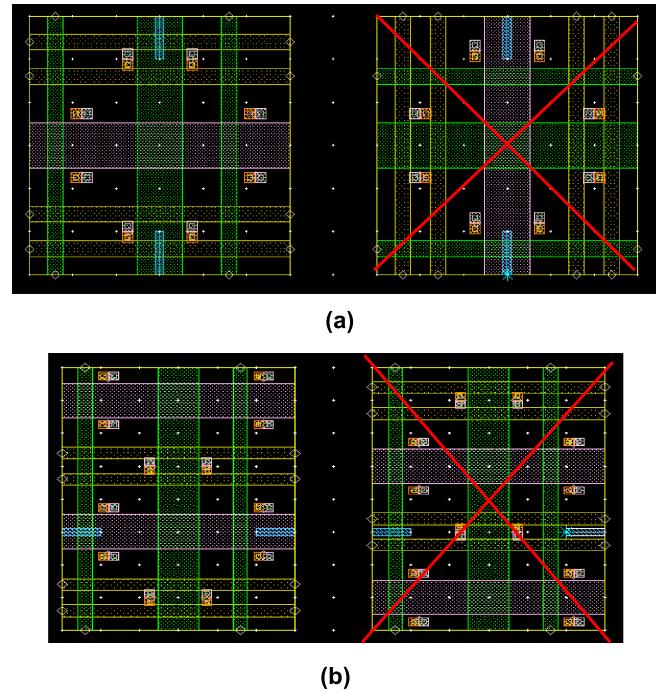


Fig. 8. Layout of subterranean sub-cell highlighting (a) rotation and (b) flipping is prohibited as they cause misalignment of bias lines and PTL tracks with block tracks.

features integrated in a single cell would result in effortless and robust design.

C. Rotation Feature for Subterranean Sub-Cell

The layout tools provide up to eight different rotation and flip options and have been widely used by the designers. For block level design, the cells are placed adjacent to each other. The cells are often rotated or flipped for proper orientation of input/output terminals. The cell designed by instantiating static subterranean sub-cell prohibits the rotation and flipping of cells. This is because along with the core sub-cell, the subterranean sub-cell is also rotated and flipped. This causes misalignment of bias lines and PTL tracks at the block level as shown in Fig. 8 and thus the subterranean sub-cell needs to be redesigned. In

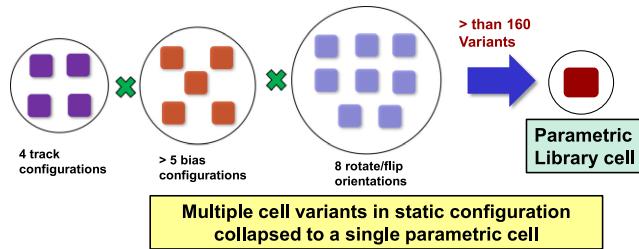


Fig. 9. Figure shows how multiple variants of a single cell can be collapsed to one variant by making the cell parametric.

conclusion, to support all the rotation and flipping orientations, eight variants of a cell must be manually designed.

VI. PARAMETRIC CELL DESIGN APPROACH

From the above discussion, it is evident that designing digital cells by instantiating static subterranean sub-cells dictates several layout flavors for each cell. Multiple variants of a cell are required to support different track configurations, biasing schemes and rotation orientations.

The parametric approach for a subterranean sub-cell provides several advantages as compared to its static version (see Fig. 9). It facilitates dynamic reconfiguration of bias lines. Different cells within a block can be connected to the same bias line or independent bias lines. It provides flexibility in creating horizontal and vertical power tracks in different metal layers when necessary. It facilitates rotating of the core sub-cell without rotating the subterranean sub-cell. This allows the bias lines and PTL tracks within a cell to align uniformly with the tracks at the block level. It enables parametric placement of PTL tracks and PTL ground vias. It allows for dynamic creation of moat bridges to connect ground patches within very long moats. At present, the parametric cell approach supports the creation of both library cells (fixed height) and custom cells (variable height).

VII. PARAMETRIC DIGITAL CELL

A. Parametric Configurations

The parametric cell enables creation of independent bias lines with stretch handles (see Fig. 10). These stretch handles are used to connect or disconnect the bias lines of abutted cells at block level design. It introduces parametric creation of bias connections from bias taps to bias lines. A default feature has been provided in the parametric cell to connect the bias taps to second horizontal bias line when it is created. The designer can modify it later as per the design requirements through the properties of parametric cell. The parametric cell also facilitates grouping of disconnected bias lines by parametrically creating a via to short the horizontal and vertical bias lines. The parametric features have been developed using Cadence Skill script.

Fig. 11 shows more features of parametric cell with the example of layout of a D flip flop cell. Figs. 11(a) and 11(b) show the two tracks variants of same cell namely BB and PP respectively. Fig. 11(a) starts with Bias-PTL along the x and y axis, while

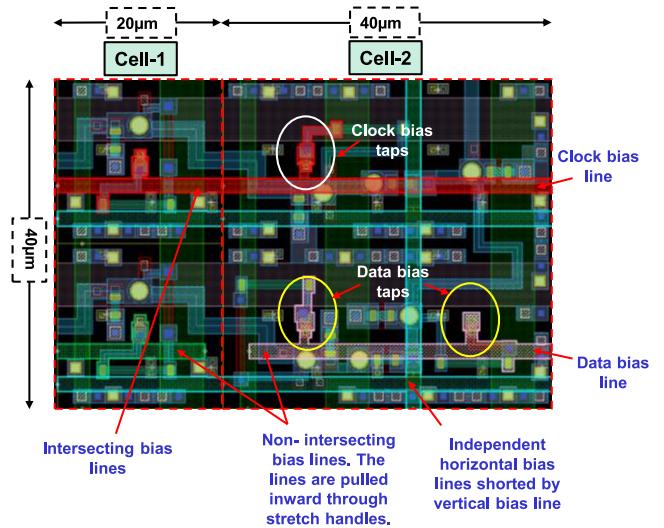


Fig. 10. Layout of block level where parametric cell-1 and parametric cell-2 are abutted. Parametric cell enables creation of multiple independent bias lines (clock and data) with stretch handles to connect or disconnect with abutted cells. The figure shows the bias connections from bias taps to clock and data bias lines, created parametrically.

Fig. 11(b) starts with PTL-Bias along both the axes. Fig. 11(c) shows the same cell track configuration as in Fig. 11(a) i.e., BB, however, the former is flipped along the y-axis (MY). Thus, the parametric cell approach allows the rotation or flipping of the core sub-cell keeping the subterranean sub-cell intact. Fig. 11(d) shows a single bias connection being shared among the data and clock paths. This is done by changing the bias configuration in the properties of parametric cell. Fig. 11(e) highlights the independent clock and data biases created as part of the cell, and creation of bias connection from bias tap to the bias lines parametrically. In conclusion, Fig. 11 shows a single cell of D flip flop with its five different variants, each showing different features. These features can be dynamically changed on the fly through the properties of the same parametric cell.

B. Parametric Creation of Moat Bridges

Moats are holes in the ground planes (M4 and M7 metal layers) and created during the design of core sub-cell. Sufficient moats are also provided along the edges of core sub-cell to minimize the impact of flux trapping. At the block level, when the cells are abutted, moats from multiple cells align together and creates long moat as shown in Fig. 12(a). The parametric cell facilitates adding moat bridges to bridge the ground planes isolated by long moats as shown in Fig. 12(b). This is achieved by selecting options in the properties of parametric cell. The moat bridges can be created in any or all the four edges of the cell.

C. Parametric Stretching of PTL Ground Vias

The subterranean sub-cell uses vias to connect the PTL ground planes in M1 and M4. The ground vias use i3 vias to connect M3 and M4 metal layers. These PTL ground vias

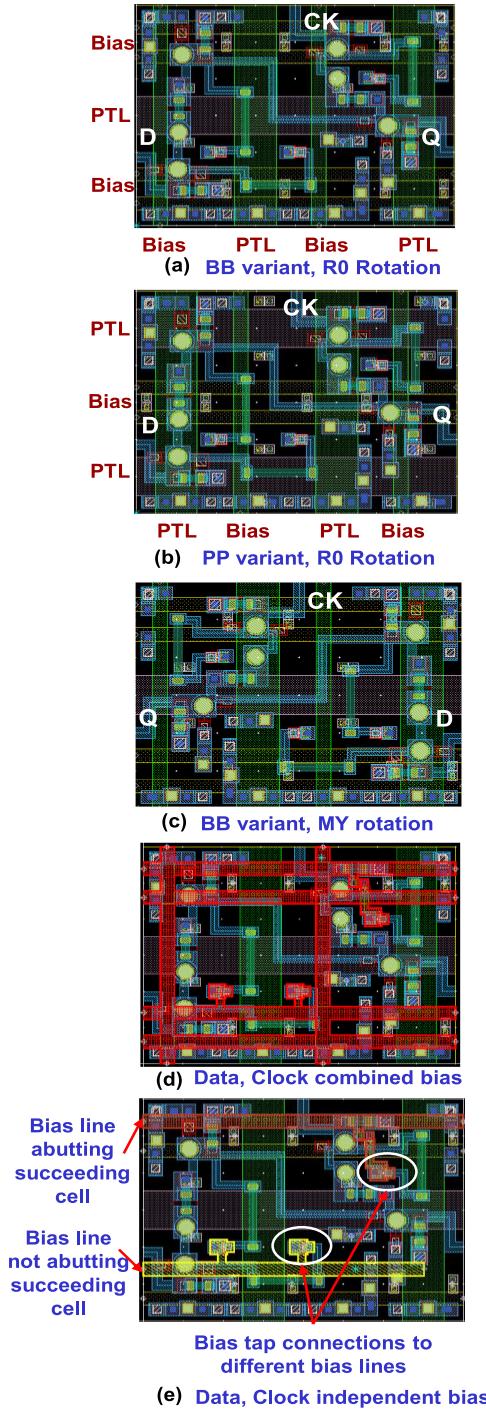


Fig. 11. Example of D-flip flop cell parametrically configured for different subterranean track, bias, and rotation configurations.

are placed at every $20 \mu\text{m}$ to avoid resonance of PTL signals. The core sub-cell uses i4-vias to connect the M5 metal layer to M4 ground, for example to ground the junctions. Sometimes, close proximity of i3 and i4 vias gives rise to DRC errors if the recommended minimum separation between i3 and i4 vias is not met. Parametric stretching of the PTL ground vias facilitates resolving such DRC errors. Different set of DRC errors may occur upon changing the rotation orientation of the cells, as shown in Fig. 13. Although this is not a robust technique, further

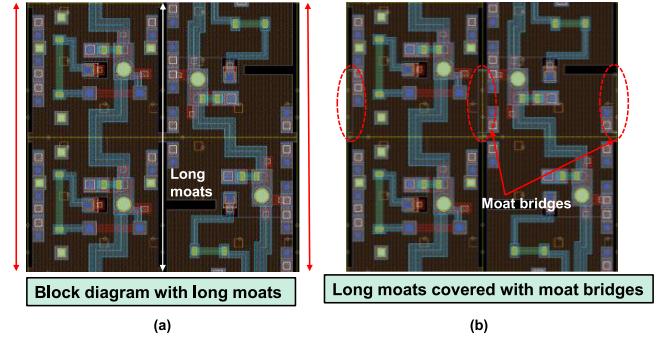


Fig. 12. (a) Layout of block level where abutting of cells creates long moats. (b) Layout of the same block level showing moat bridges created dynamically by the parametric cell.

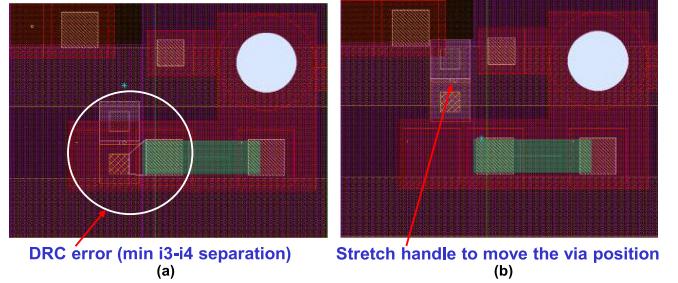


Fig. 13. (a) Layout of digital cell where the proximity of i3-i4 vias creates DRC error. (b) DRC error is removed by parametrically stretching PTL ground vias.

work needs to be carried out to explore improved approach to eliminate these DRC errors.

VIII. CONCLUSION

We have reported the dual cell library design approach for RSFQ and ERSFQ logic families, using the parametric approach. The small incremental effort involves designing the bias sub-cell for ERSFQ circuits while both of them share the same logic core sub-cell. The proposed layout methodology supports scaling of complex digital circuits and designing of both library and custom digital cells. Our design approach involves parametrically creating the digital cell by instantiating core, bias and subterranean sub-cells. The subterranean sub-cell supports a dense network of PTL interconnects and bias grids. It also enables easy adoption of placement and route (P&R) tools which automates the power routing and PTL tracks. If the power routing is not supported, our parametric approach can be used to quickly generate layout variants of the standard cell. The proposed parametric cell collapses multiple layout variants into a single cell. It enables parametric re-alignments of bias lines and PTL tracks with chip tracks and thus supports different track configurations and rotation orientations. It supports dynamic configuration of different biasing schemes as required by the designer. It facilitates parametric creation of moat bridges for moats extending over multiple cells. All of these enhance the flexibility and ease of use for designers of VLSI superconducting circuits.

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