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Signal integrity analysis of bundled carbon nanotubes as futuristic on-chip interconnects

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ABSTRACT

Rigorous technology scaling of integrated circuits to nanometer range aids to acquire prodigious operational speed and versatile functionality in system-on-chip. However, this leads to escalation in interconnect parasitics and non-ideal issues that have become primary bottleneck in the existing copper based on-chip interconnect system. Graphene based carbon nanotube bundle has emerged as prospective interconnect for high speed applications. This paper focuses on bundled carbon nanotubes and their different spatial arrangements viz. single wall CNTs (SWCNTs), multiwall CNTs (MWCNTs) and mixed CNT bundles (MCBs). Such bundle configurations boost the performance of system in terms of reducing system latency and power consumption in addition providing system reliability. The significant novel contribution of this paper lies in executing eye-diagram analysis of the futuristic bundled CNT structures as interconnects. Eye-diagram is an important tool for analysing signal integrity effects. The several performance analyses have been performed in SPICE and ADS EDA tools at 22 nm technology node.

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1. Introduction

Interminable upgradation in very large scale integration (VLSI) technology have paved way the development of highly dense integrated circuits that embed billions of transistors and interconnections. International technology roadmap for semiconductors (ITRS) highlighted limitations of copper interconnect at miniaturized technology nodes [1]. With shrinking of technology nodes, copper interconnect exhibits varying non-ideal effects such as thermal stress, electro-migration, surface and grain boundary scatterings. This in turn, increases resistivity of copper interconnects and augment reliability concerns in the interconnect system. Due to finite geometric dimensions of interconnects, there exist associated parasitic capacitance, resistance and inductance. The interconnect parasitics cause several concerning issues such as signal degradation, skin effect, crosstalk and propagation delay. The on-chip interconnects are crucial factor to determine speed, power consumption and operational frequencies of integrated systems. Hence, performance analysis of on-chip interconnects, exploration of advanced materials and methods to enforce better functionality have become meticulously significant.

To alleviate the non-ideal effects of copper interconnects, several researches have been performed [1–4]. It is investigated that graphene based carbon nanotubes (CNTs) is one of the promising materials for on-chip interconnects that can substantially perform better and deal with high-speed operation of futuristic VLSI designs. The prospective CNT interconnects are discussed next in this paper.

2. Carbon nanotube On-chip interconnect

Carbon nanotubes (CNTs) have emerged as magnificent nanoscale structural elements from which devices to interconnects can be constructed effectively. CNT can attribute incredible electrical, mechanical and thermal properties as that of metal or semiconductor depending on its chirality [5,6].

Carbon nanotubes can be categorized in varying forms. If CNT is containing single shell then it is referred as single-wall CNT (SWCNT). If multiple concentric CNT shells are present, then it is termed as multi-wall CNT (MWCNT). CNTs are often used in bundle form so as to reduce effective impedance. The bundled version of

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CNTs are further classified as SWCNT bundle (SWCNTB), MWCNT bundle (MWCNTB) and mixed CNT bundle (MCB). As the name suggests, SWCNTB comprises of only SWCNTs, alike MWCNTB contains only MWCNTs as shown in Fig. 1(a). These types of bundles are however not easily realizable as fabrication of bundle structures comprising of CNTs with all uniform diameters is difficult [3,4,7]. Hence, bundled CNTs are developed in mixed form that is composed of mixture of MWCNTs and SWCNTs as demonstrated in Fig. 1(b). Consequently, research in the present work is centered towards analysis of different versions of mixed CNT bundle and their comparison in order to get best suitable structure for on-chip interconnects.

The different properties in regards to conventional copper and futuristic CNT interconnect structures are enlisted and compared in Table 1. These parameters are dependent on diameters of CNTs, tube density, physical dimensions such as width (W) and height (H) of bundle structure and fabrication process variants. It can be observed from Table 1 that electrical properties of bundled CNTs are strikingly outstanding than copper and isolated SWCNT/MWCNT structures. Subsequently, MCB interconnect is motivation behind current research paper. Performance parameters such as propagation delay, power dissipation and crosstalk of MCB interconnect structures are evaluated. Along with this, signal integrity analysis with the aid of eye-diagram has been uniquely performed in the current work and discussed in the subsequent sections.

3. Modeling of on-chip interconnects

3.1. Electrical modeling of interconnects

For performance analysis of interconnect system, driver-interconnect-load (DIL) model is considered and is shown in Fig. 2. As figure demonstrates, the extracted parasitic elements of interconnect viz. lumped resistance (R_{lump}), equivalent single conductor (ESC) resistance (R_{ESC}), capacitance (C_{ESC}) and inductance (L_{ESC}) are modelled as distributed transmission line. The driver and load for transmission line are usually used as CMOS inverter [2–8]. The electrical parasitics of CNT bundle are technology dependent since width and height of bundle vary as per technology specifications. In a CNT bundle with given cross-sectional area, total number of CNTs is a key factor to evaluate interconnect parasitic parameters. Total number of CNTs (SWCNTs/MWCNTs) in a bundle structure is evaluated as [3–4,6,8].

$$N_{CNT}=\begin{cases} N_{W_{CNT}}N_{H_{CNT}}-\frac{N_{H_{CNT}}}{2}, & if\ N_{H_{CNT}}\ is\ even \\ N_{H_{CNT}}N_{H_{CNT}}-\frac{N_{H_{CNT}}-1}{2}, & if\ N_{H_{CNT}}\ is\ odd \end{cases} \quad \text{where,} \quad N_{W_{CNT}}=\left\lfloor\frac{W_{CNT}-D}{D+\delta}\right\rfloor+1 \text{ and } N_{H_{CNT}}=\left\lfloor\frac{H_{CNT}-D}{\frac{\sqrt{3}}{2}(D+\delta)}\right\rfloor+1 \tag{1}$$

where D represents diameter of CNT, δ is CNT-CNT spacing, N_{WCNT} and N_{HCNT} are number of CNTs along width and height of rectangular bundle cross section respectively. Mean free path of CNT bundle is a function of each of its diameter of CNT and is estimated as,

$$\lambda_{mfp}\approx 10^3 D_i \ \ and \ \ N_{total}=\sum_{i=1}^{N_{CNT}}N_{ch} \tag{2}$$

where N_{ch} is number of conduction channels for SWCNT or MWCNT and N_{total} is total number of conduction channels corresponding to whole CNT bundle. N_{ch} is obtained by cumulative sum of conduction channels of all shells in a CNT together with all CNTs in a bundle structure. N_{ch} is purely process dependent parameter that is derived as,

$$N_{ch}(D_i)=\begin{cases} K_1 T D_i + K_2, & when \quad D_i > d_t/T \\ \frac{2}{3}, & when \quad D_i < d_t/T \end{cases} \tag{3}$$

where $T = 300$ K, $K_1 = 3.87\times10^{-4}$ nm^{-1} K^{-1} and $K_2 = 0.2$. Lumped and distributed R_{ESC}, L_{ESC} and C_{ESC} parameters of CNT bundle as illustrated in Fig. 2 can be derived [2–8] using (4)–(6) as

$$R_{lump}=\left[\sum_{j=1}^{N_{CNT}}\left(\sum_{i=1}^{N_{shells}}\left(\frac{R_q}{N_i(D_i)}+R_{mc,i}\right)\right)^{-1}\right]^{-1} \text{ and } R_{ESC}=\left[\sum_{j=1}^{N_{CNT}}\left(\sum_{i=1}^{N_{shells}}\left(\frac{N_i(D_i).\lambda_{mfp,i}}{R_q}\right)\right)\right]^{-1} \tag{4}$$

where R_{mc} is contact resistance of SWCNT/MWCNT and typically considered as 3.5 KΩ. R_q is the quantum resistance and is calculated as $R_q=\frac{h}{4.e^2}\approx 6.45K\Omega$. The kinetic and magnetic inductances of CNT bundles are evaluated as,

$$L_{k,ESC}=\frac{L_{k_o}}{2.N_{total}}; L_{m,ESC}=\frac{1}{N_x}\left[\frac{\mu_o}{2\pi}ln\left(\frac{D_{shell}+2.h_t}{D_{shell}}\right)\right] \text{ and } L_{ESC}=L_{k,ESC}+L_{m,ESC} \tag{5}$$

The quantum and electrostatic capacitances are computed as,

$$C_{q,ESC}=2.C_{q_0}.N_{total}; C_{e,ESC}=\frac{2\pi\varepsilon_0\varepsilon_r}{cosh^{-1}\left(\frac{D_{shell}+2.h_t}{D_{shell}}\right)}\times N_x \text{ and } C_{ESC}=\frac{C_{q,ESC}\times C_{e,ESC}}{C_{q,ESC}+C_{e,ESC}} \tag{6}$$

where N_x are the number of CNTs along periphery of CNT bundle that are facing ground.

3.2. Spatial models of CNT bundle structure

Fig. 3 shows different versions of spatial arrangement of bundle structures comprising of SWCNT bundle, MWCNT bundle and mixed CNT bundle. For evaluating their performance as on-chip

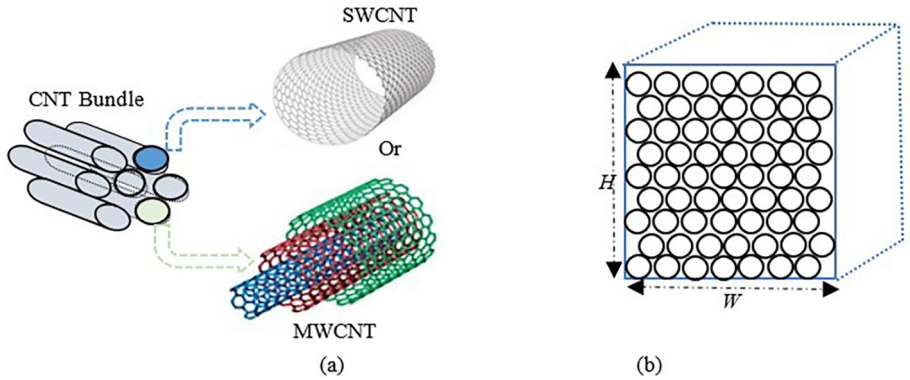

Fig. 1. (a) Carbon nanotube bundle structure containing SWCNTs/ MWCNTs (b) Cross sectional view of mixed CNT bundle containing SWCNTs and MWCNTs.

Table 1
Comparison among different properties of Carbon nanotube bundle structures and copper interconnect [1–5].

Parameters	Interconnect Materials			
	Copper	SWCNT	MWCNT	CNT Bundles
Mean free path at room temperature (nm)	40	>1000	$\approx 25 \times 10^3$	$>25 \times 10^3$
Thermal conductivity (W/m K)	390	1800–5800	$\approx$ 3000	> 3000
Current density (A/cm^2)	$\approx 10^7$	$>10^9$	$>10^9$	$>10^9$
Carrier mobility (cm^2/V.s)	5–9	$>10^5$	$>10^5$	$>10^5$

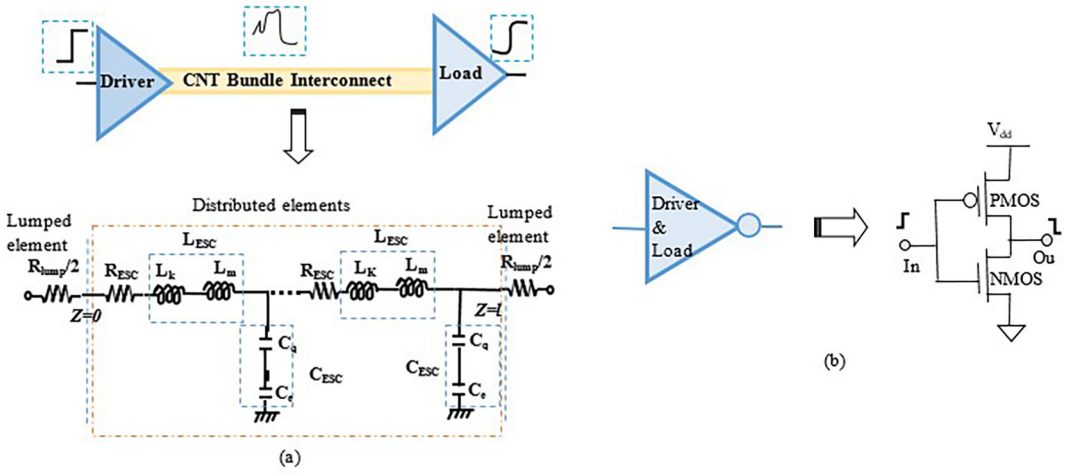

Fig. 2. (a) Driver-interconnect-load (DIL) model incorporating CNT bundle as interconnect (b) CMOS inverter as driver and load.

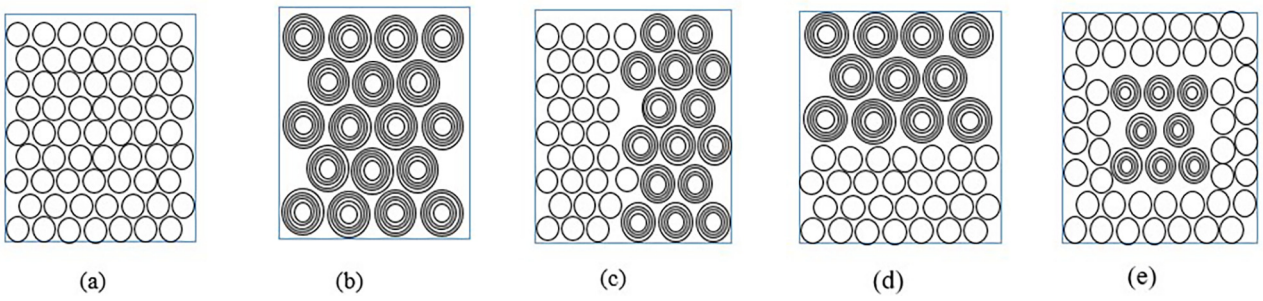

Fig. 3. Cross-sectional view of different CNT bundle structures nomenclature as (a) SWCNTB (b) MWCNTB (c) MCB –I (d) MCB-II (e) MCB-III [3,4].

interconnects, R_{ESC}, L_{ESC} and C_{ESC} parasitics of these bundles structures are extracted separately. The width (W) and height (H) of the rectangle in all the bundle structures of Fig. 3 are taken as 32 nm and 96 nm respectively for 22 nm technology node [1].

3.3. Models for crosstalk analysis

Most pivotal concern of interconnect system performance is coupling phenomenon and can be represented using crosstalk model as shown in Fig. 5(a). The figure shows crosstalk model for '*n*' number of parallel interconnect lines. These interconnect lines are capacitively and inductively coupled due to presence of dielectric between them. It leads to forced unwanted switching on victim lines. Two variants of crosstalk analysis have been performed in the current work. First is the functional crosstalk in which victim line is at quiescent and other lines (which are called as aggressor lines) are switching. In this case, switching activities at the victim line get either undershooted or overshooted. The other variant of analysis is dynamic crosstalk. Here both aggressor and victim lines are switched simultaneously. Signal over victim line may switch in-phase or out-of-phase with the signals over aggressor lines. This leads to added propagation delay at the victim line.

4. Results and analysis

All the analyses are performed at 22 nm technology node. As discussed, performance of the on-chip interconnect system is highly dependent on the material and length of interconnects. Thus, firstly performance of conventional copper interconnect is analysed and compared with the futuristic CNT bundle interconnects.

Fig. 4(a) and (b) show the propagation delay and power-dissipated variation with respect to interconnect length. The interconnect length is varied from 0.5 mm to 2 mm. From the figures, it can be seen that delay and power-dissipation in copper interconnects are highest amongst all other considered structures. It can be also inferred that incorporating copper as on-chip interconnects can be highly costlier in terms of lower speed as propagation delay increases tremendously with the length of interconnect. It is observed from the Fig. 4(a) and (b) that bundled CNTs are signifi-

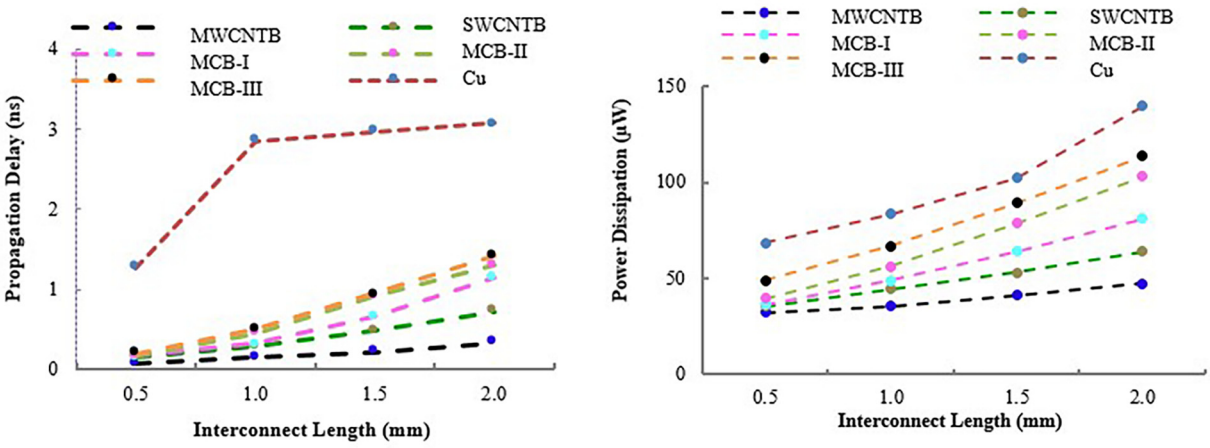

Fig. 4. (a) Propagation delay and (b) power-dissipation evaluation with varying interconnect length for copper and different CNT bundle structures.

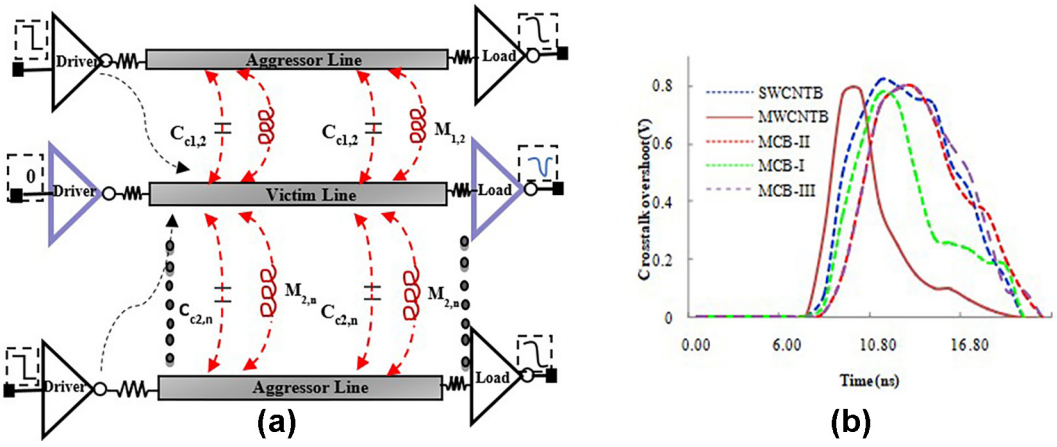

Fig. 5. (a) Capacitively and inductively coupled 'n' parallel interconnect lines (b) functional crosstalk induced noise in different bundle structure of interconnects.

cantly overcoming the issue of slowing down the system even at longer length of interconnects. Further, power dissipation of interconnect system is also reduced using prospective CNT bundles.

It is envisaged from the figure that amongst different CNT bundle structures, MWCNT bundle outperforms in case of system latency and power consumption. However, due to limitation with respect to fabrication of uniform diameter; mixed CNTs bundle configuration is considered in this paper. It is investigated that MCB-I arrangement of CNT bundle provides good performance and thus considered as optimal solution in the current work.

Further, crosstalk analysis is performed for different CNT bundle structures as interconnects. Analyses carried out in this work are functional and dynamic crosstalk. For the performance analysis, three-coupled line structure is considered. The middle interconnect line is considered as victim and other as aggressor. Fig. 5(b) shows the functional crosstalk effect i.e. noise at the victim line in coupled DIL model. It is seen that crosstalk noise is lowest for MCB-1 structure. Fig. 6 represents the results of dynamic crosstalk. It is analysed that with increase in spacing, crosstalk induced delay decreases. This is because as with increase in spacing, coupling between interconnects decreases. Lower coupling leads to lesser delay and faster system response. It is also seen that higher spacing marginally decreases power dissipation. Hence, by increasing spacing between the interconnects, crosstalk effects can be reduced. However this benefit comes at the cost of higher consumption of silicon area. Hence, for efficient system designing, optimum trade-off is required between the two.

Next signal integrity analysis that is prominent and effective measure for prediction of noise immunity and jitter issues in high-speed nano-interconnect is performed using eye-diagram technique. All the measurements of eye-diagram are performed at high-data rate of 1Gbps. The analyses are carried out for 1 mm of interconnect length in ADS tool.

An eye-diagram is a potential EDA aid for identifying signal discontinuities in the on-chip digital transmission line system, validating transmitter output compliance, unveiling the amplitude and time related abnormalities that degrade the performance of high performance SOCs [9,10]. By taking bandwidth samples of a high-speed digital signal, an eye diagram represents the sum of samples by superimposing high and low levels of the signal, and corresponding transition measurements. In the paper, eye-diagram analysis has been performed for proposed CNT bundle interconnect structures. The eye-diagram, rising jitter and falling jitter of signals propagated along transmission line of MCB-I interconnect structure are shown in Fig. 7(a), (b) and (c) respectively.

In Fig. 7(a), the value of eye opening factor should be unity that indicates no amplitude distortions are present in the signal at the receiver-end. While the values of eye-amplitude and eye-height should be equal to peak-to-peak value of transmitted signal. In this

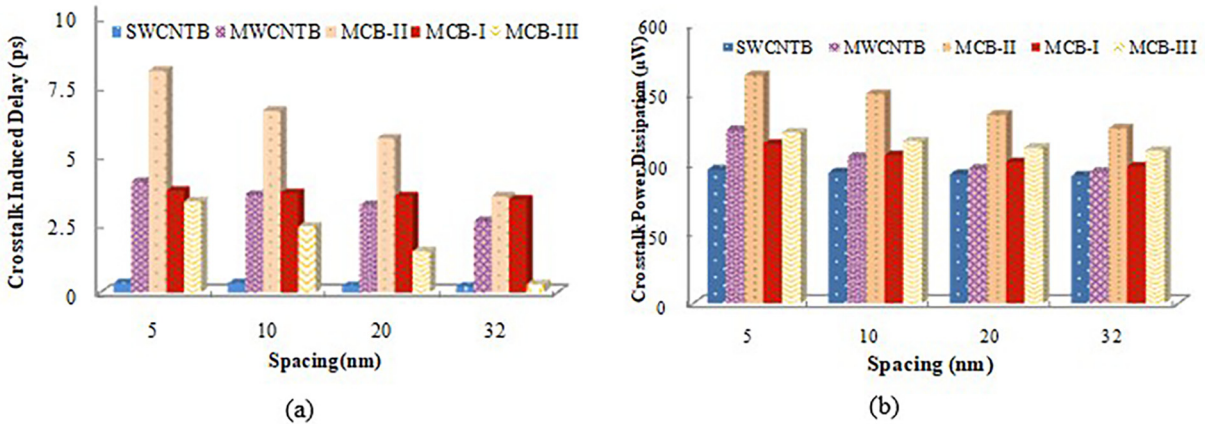

Fig. 6. (a) Dynamic crosstalk induced (a) delay and (b) power dissipation with varying spacing between interconnects for different CNT bundle structures.

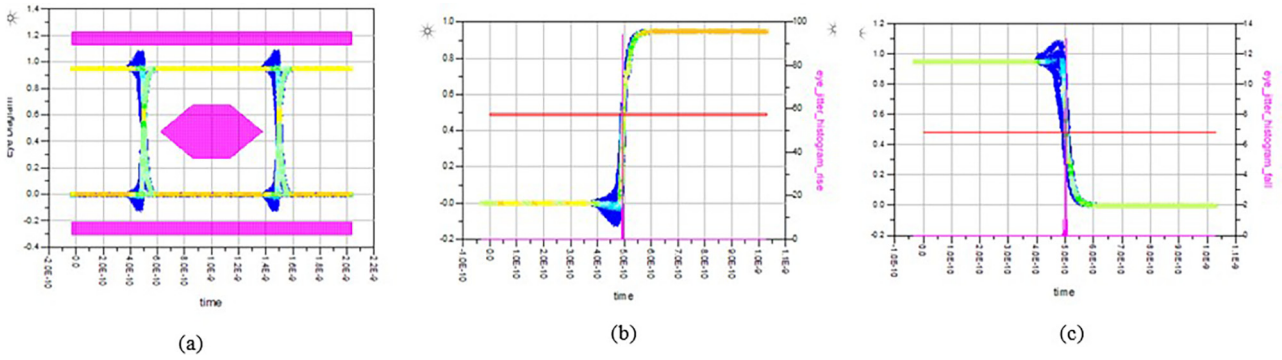

Fig. 7. (a) Eye-mask diagram (b) Rise edge jitter (c) Fall edge jitter of MCB-I at 1GBPS data rate.

case it is taken as 0.9 V. Eye-width and eye-jitter parameters are used to measure the time distortions present in the received signal. The signal-to-noise (SNR) of eye is the measure of the amplitude distortion and is evaluated as a ratio of the desired signal level to the level of noise present. Higher SNR values are desirable for good signal transmission.

SNR is defined as,

$$SNR = \frac{high\ \ level - low\ \ level}{\sigma \times high\ \ level + \sigma \times low\ \ level} \tag{7}$$

The values of all these different eye-diagram related parameters for different CNT structures are tabulated in Table 2. It is envisaged from the table that MCB-I interconnect structure exhibits superior performance than other bundle structures.

Timing distortions are measured in terms of jitter. To estimate jitter, time variances of the rising and falling edges of an eye-diagram at the crossing point are captured. These are shown in Fig. 7(b) and (c). It has been analyzed that MCB-I structure is lesser prone to jitter effects. From the several analyses performed in the paper, it is inferred that mixed CNT bundle with MCB-I structure is good and reliable for incorporating as futuristic on-chip interconnects in integrated circuit designs.

5. Conclusion

Prospective different spatial arrangements of CNT bundles are investigated and best suitable interconnect structure has been considered for high-speed integrated systems. It is observed from the primary analysis that copper interconnects performance is diminishing than CNT bundle interconnects at longer lengths in nano-scale technology node. Later, it is speculated that MCB possesses outstanding performance in terms of reduced system latency and power dissipation. But due to its fabrication limitations, different geometrical topologies of mixed CNT bundles are explored and

Table 2
Eye diagram measurements for different CNT Bundle structures at data rate of 1 GBPS.

Parameter	SWCNTB	MWCNTB	MCB		
			I	II	III
Eye Amplitude (V)	0.89	0.94	0.95	0.7	0.9
Eye height (V)	0.76	0.94	0.95	0.53	0.9
Eye width (ps)	940	942	983	867	992
Eye opening	0.89	1	1	0.87	0.94
Eye SNR	117.56	3.22E3	9.51E18	7.612	8E18
Eye jitter (RMS)	1.51E−10	5.49E−11	3.26E−11	4.39E−11	5.6E−10

analyzed. Amongst different mixed arrangements of CNTs in a bundle structure, it is analyzed that MCB-I structure provides better realization and exhibits approximately 30% reduction in delay and power compared to other bundle structures. MCB-I structure also outperforms as able to operate at higher speed with maximum SNR and minimum jitter amongst all other CNT bundle structures as interconnect. Hence, it is contemplated from the present work that graphene based CNT bundle structures are strong contender to existing copper based interconnects that can effectively replace copper in futuristic IC designs for high performance applications in nano-scale era.

CRediT authorship contribution statement

Takshashila Pathade: Writing - original draft, Conceptualization, Methodology, Software, Formal analysis, Investigation, Visualization, Validation. **Yash Agrawal:** Supervision, Visualization, Investigation, Resources, Writing - review & editing. **Rutu Parekh:** Supervision, Resources, Data curation. **Vinay Palaparthy:** Data curation, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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