Mitigation techniques for crosstalk in ICs

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Mitigation techniques for crosstalk in ICs

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Abstract. Crosstalk is a major concern among integrated circuit (IC) designers as it may contribute significantly to the amount of noise presented in a device. Hence, there is a need to mitigate the impact of crosstalk in order to preserve the signal integrity between interconnections. This paper will review several methods to mitigate crosstalk in high speed ICs. The methods include the usage of repeater, Schmitt trigger, shielding, skewing, space adjustment between signal wires and setting the coupling length of the signal wires. Although these methods are effective for crosstalk mitigation, the features might only be applicable due to certain constraints. Consequently, this paper will provide a sufficient review on each method as a guideline for crosstalk mitigation method selection in which the crosstalk is largely regulated in long interconnections.

1 Introduction

Nowadays, integrated circuits are designed in high densities and operated at high frequencies in the gigahertz region. The high densities feature corresponds to Moore's Law that states the number of transistors in an IC is doubled for every two years [1]. Technically, an IC is a set of electronic circuits which consist of thousands to billions of transistors on one small flat piece of semiconductor material that is normally silicon [2]. Figure 1 illustrates the evolution of total number of transistors in high speed ICs from 1971 until 2007. Based on the timeline, it can be seen that with the shrinkage of the process technology, more transistors can be integrated over the same die.

Continuous invention of advanced smart devices increases the need for high data rate transmission and support for large network capacity [3], [4-5]. The evolution of transceiver technology has allowed multiple wideband transmitter and receiver to be integrated on a single chip. Such integration of billions of transistors in single chip shall result reduction in terms of power consumption, chip size and weight without affecting the overall performance.

The next phase of mobile telecommunications is the fifth-generation (5G) technology. 5G is a system designed to fulfil the prerequisites of International Mobile Telecommunications (IMT-2020) set by the International Telecommunication Union Radio communication sector (ITU-R) Specification M.2083 [1-2].

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Research on the communication system 5G millimetre wave (mmWave) has begun in terms of system development in order to provide market-ready systems by 2020 [2]. In 2020, the communication system of 5G mmWave has a clear vision of getting user devices in the Internet of Things (IoT) and Big–Data setting [6-7]. Moreover, communications system 5G mmWave is capable in providing low latency high-speed data connections with gigabit speed for billions of consumers.

5G technology has to be established, developed, and deployed by a range of industry players. The upcoming service and implementation environment will involve associated applications such as smart city, multiple personal devices, wearable computing, education, and lifeline systems [6], [8-9]. Figure 2 shows the timeline of the third generation partnership project (3GPP) standardization towards 5G implementations in the industry.

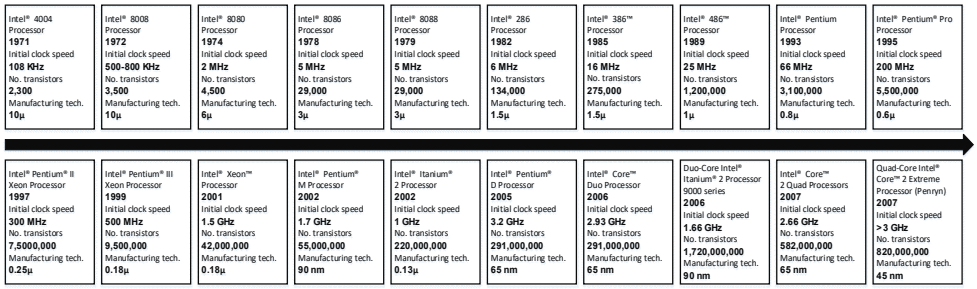

Fig. 1. 60 years of the transmissions: 1971-2007 [1].

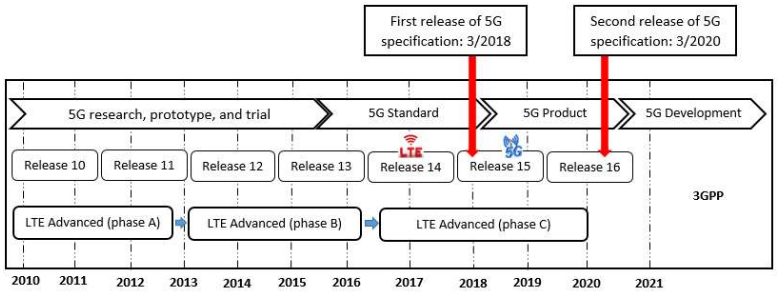

Fig. 2. The timeline of third generation partnership project (3GPP) standardization towards 5G implementations in the industry [10].

It is expected 5G technology will fundamentally change the way we see the role of telecommunications technology, which will have an impact through the pervasive digitalization of a hyper-connected society, as well as further economic growth. MmWave technology is just one of the techniques for the future 5G networks to be implemented. In mmWave technology, the spectrum band ranges from 30GHz-300GHz, in which the wavelength is between 10mm to 1mm [11]. Figure 3 shows the spectrum for both super high frequency (SHF) with a range of 3-30GHz and spectrum for extremely high frequency (EHF) is 30-300GHz.

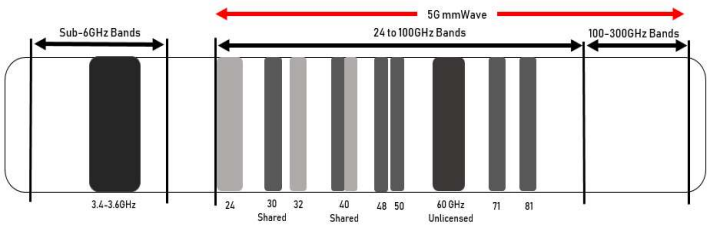

Fig. 3. The 5G mmWave spectrum.

Today, one of the most challenging issues faced by circuit designers is to design a system that is resilient to crosstalk. Generally, crosstalk is recognized as a hypercritical issue in high-speed IC design. Crosstalk refers to the interaction between signals on two parallel interconnects. An "aggressor" is the interconnect carrying the signal which creates the crosstalk, and a "victim" is the adjacent interconnect that suffers from the crosstalk [12]. Crosstalk appears when electromagnetic coupling occurs between the interconnects, which include mutual capacitance and mutual inductance. There are various crosstalk mitigation techniques that can be implemented in accordance to the IC design constraints.

The subsequent parts of this paper are organized as follows. Section 2 highlights the challenges in high-speed IC design for mmWave applications. Section 3 discusses the numerous techniques used to mitigate the impact of crosstalk. In section 4, the impact of crosstalk in IC will be discussed and finally, the concluding remarks terminate this paper.

2 Crosstalk issues in high speed integrated circuit design

ICs in nanoscale CMOS technology need to be designed in high densities and they operate at high frequencies, mainly in the gigahertz region. Based on these factors, it is essential to have circuits with smaller wire pitch that are capable to process data faster. Such requirements have caused ICs operating at mmWave frequencies to suffer from an electromagnetic phenomenon known as crosstalk. Crosstalk is a signal integrity (SI) issue where adjacent interconnect lines are susceptible to crosstalk when they are placed close enough for electromagnetic coupling to occur.

3 Crosstalk mitigation technique

There are numerous design techniques which can be implemented to reduce the effect of crosstalk in high-speed ICs. This section provides a brief review on the techniques which were agreed by researchers to reduce the impact of crosstalk.

3.1 Repeater insertion

As the size of complementary metal-oxide-semiconductor (CMOS) IC continues to shrink, interconnections became progressively vital. The interconnect delay will increase quadratically due to a linear increase in each interconnect resistance and capacitance with a linear increase in length [13-14]. Repeaters are traditionally used to linearize interconnect delay increases and improve signal transition times. Repeaters makes time delay linear with length by dividing the interconnection into smaller subsection [15].

To reduce interconnect delay, paper [16] suggest to implement a repeater. They used a linearized form of the Shichman-Hodges equations method [17]. At a particular operating point to determine the suitable repeater insertion locations. Meanwhile, paper [18] introduce

a parallel regeneration concept which added precharge circuitry to the repeaters to reduce the evaluation time. Though this method needs fewer repeaters, extra area is critical and a precharge signal is needed to operate correctly. They also consider optimal method for driving resistive interconnect in [19].

Although the repeater insertion function is to reduce the delay of the interconnects in a circuit, the increasing number of repeaters will increase the slew rate and the operating frequency but in the same time it will decrease the design performance in terms of area and power. Paper [20] proposed a method of the repeaters and improve the slew rate.

3.2 Schmitt trigger

With the help of buffer insertion, very large-scale integration (VLSI) circuit interconnect delay has always been addressed. Various buffer insertion methods have been suggested for single-line interconnections and tree structures. In [21], the impacts of inductance on propagation delay and repeater insertion in VLSI circuits were observed and shown. Paper [22], stated that interconnections are not always linear in shape and handling the delays in tree structure is also a problem. This is attributed to the effects of crosstalk due to the neighbouring branches.

Paper [22] proposed a novel method for buffer insertion which is based on Schmitt trigger. The Schmitt trigger can be intended to have a threshold voltage lower than $V_{dd}/2$ and therefore can be made to respond faster. For their analysis, a four transistors Schmitt trigger is used. The findings indicate that the proposed methods surpass current methods in terms reduce of delay, power and crosstalk noise. They also proved that the proposed method works even in nanometer designs.

Besides, in [12] stated that Schamitt trigger is intended to function at a greater frequency as a buffer. It is used to decrease energy and delay in interconnections. Compared to standard CMOS inverters as a buffer, the Schmitt trigger buffer switches faster, thus leading to decrease in delay. Coupling noise is decreased by concurrent sizing of the buffer and wire in order to propagate the signal with decreased noise and delay.

Furthermore, the author in [23] designed a Schmitt trigger as a buffer which operates at a frequency of 20GHz to minimize crosstalk noise and interconnection delay. They also state that buffer helps to reduce power and delay. They have noted that crosstalk noise is effectively reduce by 60% and the delay is reduced by 56%.

3.3 Shielding

Crosstalk generally happens due to magnetic or inductive coupling between an aggressor and victim trace. The best way to mitigate it is to increase the spacing between the high-speed traces; but that will end up eating premium board real estate. Another popular implementation is to add a guard trace in between adjacent traces which reduces the crosstalk [24].

The guard trace, also known as shield is used to decrease the shared inductance owing to which the present return path is formed by the shield between the two interconnecting lines. Shielding is one of the most efficient and popular ways to decrease uncertainty about crosstalk and signal delay [12]. The author stated that shielding is nothing but a wire that is straight attached to V_{dd} or ground. One of the efficient shielding methods is to place ground or power lines between two cables to reduce noise. Different parameters that can be considered when shielding are the shield length, shield width, and the separation between shield and signal.

Some research has stated that two entire layers of metal are dedicated to shielding even in a 600MHz Alpha microprocessor [25-26]. Some research has also been conducted on integrated shielding and net ordering in paper [27-28]. Besides that, impact of different

structures of shielding under separate standardized energy pitches as well as under restricted power grid disturbances were investigated in [28]. Furthermore, integrated shielding and signal net ordering algorithms without addressing any power grid design issues were studied in [27].

On the other hand, the authors in [24] proposed "Elevated guard trace technique" that is capable to reduce more crosstalk and electromagnetic interference in order to increase overall system performance. They vary the guard trace thickness to enhance the protection between the traces to further decrease the crosstalk compared to standard guard trace application.

3.4 Skewing

Repeater insertion methods are commonly used to decrease the capacity and strength of lengthy interconnections in order to reduce the wire delay and to decrease crosstalk [29]. Nevertheless, since simultaneous transition at opposite directions still occur; crosstalk increases the worst-case bus delay. The authors in [30] proposed a delay reduction technique to prevent simultaneous opposite transition by skewing signal transition timing of adjacent wires.

Skewing is a time-consuming technique that can be implemented to reduce crosstalk [12]. Time or timing skew has been previously used in buses where the delay of a coupled bus was decreased by skewing the timing of adjacent wires or interconnections. Besides, skewing was used to decrease the energy dissipation, delay of a coupled bus, and decrease the peak power.

However, skewing is nothing but a static delay in signal propagation [26]. Thus, driver skewing triggered the time decrease in driver switching, thereby decrease the crosstalk. Also, skewing is known as the spatial variation in the arrival time of the signal edge [31]. With the increasing skew of the victim line with regard to aggressor lines, the window for the overlapping part of the signals decreases. The overlapping window minimizes with the increased skew, resulting in weaker inductive coupling into the victim wire and also resulting in lower voltage overshooting [32]. The authors in [32] also stated that skewing the victim line (when the aggressors switch in the opposite direction) significantly improves voltage shooting and propagation delay to some degree.

Skewing was implemented to decrease a coupled bus energy dissipation where it was used to decrease bus peak power [33-34]. It should be noted that deliberate skewing has previously been used to reduce crosstalk effect such as crosstalk delay and crosstalk energy dissipation in buses [30], [33]. Paper [35] proposed reducing crosstalk voltage by induced on quite victim wires.

3.5 Space between signal wires and coupling length of the signal wires

Crosstalk refers to the unintended coupling of adjacent transmission wires. It is an electromagnetic phenomenon caused by the inductive and capacitive coupling between the adjacent wires [36]. Therefore, suppressing the crosstalk to an acceptable margin is crucial. To attain that goal, designers increasing increase the separating distance between the aggressor and victim wires. In addition, increasing the physical distance between the wires of the aggressor and the victim can reduce the mutual inductance and mutual capacitance between two adjacent lines [12][36].

It is stated that to minimize the crosstalk coupling between the two wires, the distance between the separation wires must be maximized [37]. [37]. As this increases the wire pitch, it is required to balance out between crosstalk and the wire pitch. Researchers also agreed that the distance separation between traces must be three times the width of a single trace

measured from centreline to centreline, or the distance separation between two traces, edge-to-edge, must be greater than two times the trace width [37-38].

The authors in [39] investigated the effect of crosstalk on channel performance based on the IC package and the motherboard breakout routing by varying the differential pair spacing and coupling length. From these models, the differential pair spacing affects the crosstalk reading from the frequency and time domain.

4 Discussion

With the advancement of technology, IC designers were facing a challenge to design ICs with smaller form factor that are capable to operate at high operating frequencies. This is caused by one of the SI issues known as crosstalk. This section will discuss on the impact of crosstalk in IC.

Based on the articles reviewed, there are an abundance of researches on methods to mitigate crosstalk and the impact of crosstalk in IC. Crosstalk is a major issue because it can contribute significantly to the amount of jitter present in a device. Briefly, jitter is an edge deviation from its expected location. A large amount of jitter in a coupling wires can trigger bit errors in the victim line. It can cause a failure in the timing budget. These impacts have decreased the interactions between signals and reduce the noise immunity of digital CMOS circuits.

Furthermore, crosstalk may trigger undesirable impacts including excessive overshooting, extra signal delay, even a decrease in signal delay and undershooting. Crosstalk will cause noise on other lines, which may further degrade the integrity of the signal and increase noise margins.

Crosstalk can cause a signal to assume inaccurate value. This is particularly critical when the signal is about to be latched, as an inaccurate value can be loaded into a storage component and crosstalk may delay signal settling to the accurate value. This is often called “noise-on-delay”.

However, there are inadequate investigations done on crosstalk in IC for mmWave applications. There is a need to carefully investigate the behaviour and characterize the crosstalk to prevent further iterations caused by failing to address the crosstalk issue during the IC design stage. Other than that, the impact of crosstalk from the IC for mmWave applications is also inadequate.

5 Conclusion

In conclusion, there are several techniques that can be used to minimize the impacts of crosstalk. However, crosstalk cannot be minimized totally. Further research on crosstalk mitigation techniques for designers to overcome the limitations on millimetre wave applications is inevitable. In the future, the finding of this study is expected to enable aggressive high-speed signal density for premium packages and client platforms.

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