

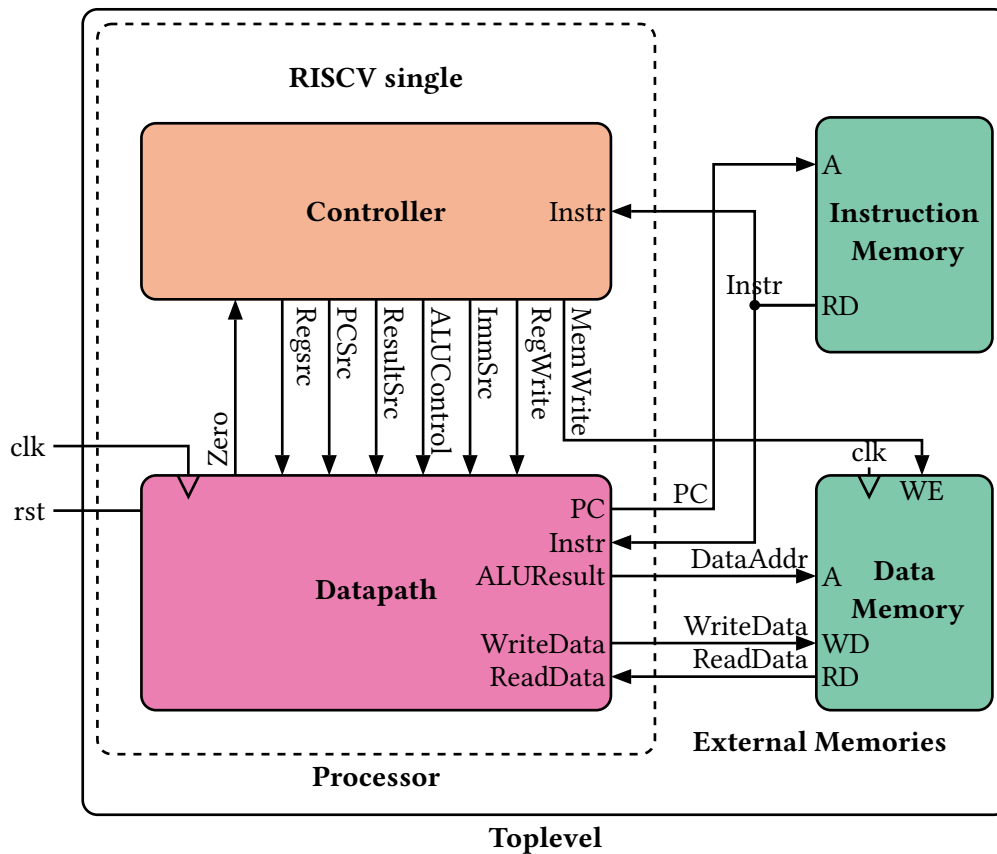
Revision History

Contents

Revision History	1
1 Terminology	1
2 Overview	1
3 Parameters	2
4 Interface	2
5 Microarchitecture	2
5.1 RenameUnit	2
5.2 DispatchUnit	2
5.3 IssueUnit	2
5.4 ExcUnit	3

1 Terminology

2 Overview



3 Parameters

4 Interface

5 Microarchitecture

5.1 RenameUnit

重命名单元将逻辑寄存器地址映射成实际寄存器。逻辑寄存器指的是 ISA 定义的 x0-x31，而实际寄存器数量多于 32 个，一般可达 128 个。主要解决 WAW，WAR 等问题。

RenameUnit 的构造参数如下：

Name	Type	Description
test	Int	

IO 端口定义如下：

Name	Type	Description
in	<code>Input(Vec(p.RENAME_WIDTH, DecodedInstr))</code>	输入
out	<code>Output(Vec(p.RENAME_WIDTH, RenamedInstr))</code>	soaeuaoeu

```
1
2  val io = IO(new Bundle {
3    val in = Input(Vec(p.RENAME_WIDTH, DecodedInstr)) /* 输入 */
4    val out = Output(Vec(p.RENAME_WIDTH, RenamedInstr)) //soaeuaoeu
5  })
```

scala

5.2 DispatchUnit

oeusnth

IO 端口定义如下：

Name	Type	Description
in	<code>Input(Vec(p.RENAME_WIDTH, RenamedInstr))</code>	
out	<code>Output(Vec(p.DISPATCH_WIDTH, DispatchedInstr))</code>	

```
1
2  val io = IO(new Bundle {
3    val in = Input(Vec(p.RENAME_WIDTH, RenamedInstr))
4    val out = Output(Vec(p.DISPATCH_WIDTH, DispatchedInstr))
5  })
```

scala

5.3 IssueUnit

IO 端口定义如下：

Name	Type	Description
------	------	-------------

in	<code>Input(Vec(p.DISPATCH_WIDTH, DispatchedInsr))</code>	
out	<code>Output(Vec(p.ISSUE_WIDTH, IssuedInsr))</code>	

1scala

2 `val io = IO(new Bundle {`

3 `val in = Input(Vec(p.DISPATCH_WIDTH, DispatchedInsr))`

4 `val out = Output(Vec(p.ISSUE_WIDTH, IssuedInsr))`

5 `})`

5.4 ExcUnit

IO 端口定义如下：

Name	Type	Description
in	<code>Input(Vec(p.ISSUE_WIDTH, IssuedInsr))</code>	

1scala

2 `val io = IO(new Bundle {`

3 `val in = Input(Vec(p.ISSUE_WIDTH, IssuedInsr))`

4 `})`