

STM32F437VIT6 U1001A

PA0 23 FMU-UART4_TX
 PA1 24 FMU-UART4_RX
 PA2 25 BATT_VOLTAGE_SENS
 PA3 26 BATT_CURRENT_SENS
 PA4 29 VDD_5V_SENS
 PA5 30 SPI_INT_SCK
 PA6 31 SPI_INT_MISO
 PA7 32 SPI_INT_MOSI

STM32F437VIT6 U1001B

PA8 67 VDD_5V_PERIPH_EN
 PA9 68 VBUS
 PA10 69 311-470LRCT-ND
 PA11 70 DTG_FS_N
 PA12 71 DTG_FS_P
 PA13 72 FMU-SWDIO
 PA14 76 FMU-SWCLK
 PA15 77 ALARM

STM32F437VIT6 U1001C

PB0 35 EXTERN_DRDY
 PB1 36 EXTERN_CS
 PB2 37 PB2-BOOT1
 PB3 89 FMU-SWO
 PB4 90 Future Use
 PB5 91 VDD_BRICK_VALID
 PB6 92 CAN2_TX
 PB7 93 VDD_BACKUP_VALID

STM32F437VIT6 U1001D

PB8 95 FMU-I2C1_SCL
 PB9 96 FMU-I2C1_SDA
 PB10 47 FMU-I2C2_SCL
 PB11 48 FMU-I2C2_SDA
 PB12 51 CAN2_RX
 PB13 52 FRAM_SCK
 PB14 53 FRAM_MISO
 PB15 54 FRAM_MOSI

Timer allocation:
 PE9: TIM1_CH1: FMU-CH4
 PE11: TIM1_CH2: FMU-CH3
 PE13: TIM1_CH3: FMU-CH2
 PE14: TIM1_CH4: FMU-CH1
 PA15: TIM2_CH1: ALARM
 PB0: TIM3_CH3: GYRO1_DRDY
 PB1: TIM3_CH4: GYRO2_DRDY
 PB4: TIM3_CH1: ACCEL_DRDY
 PB5: TIM3_CH2: MAG_DRDY
 PD13: TIM4_CH2: FMU-CH5
 PD14: TIM4_CH3: FMU-CH6
 PD15: TIM4_CH4: spare

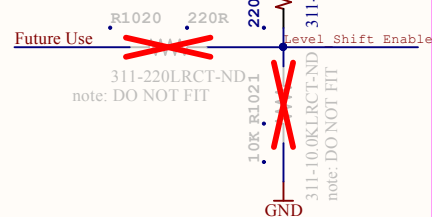
Note: MAG/ACCEL/GYRO_DRDY pins chosen
 for both timer capture and separate
 EXTI operation.

EXTI0 - TIM3_CH3 - GYRO1
 EXTI1 - <free>
 EXTI2 - <free>
 EXTI3 - <free>
 EXTI4 - TIM3_CH1 - ACCEL
 EXTI5-9 - TIM3_CH2 - MAG

Serial Level shifter protection

option 1: R1022 fitted

option 2: R1020 and 1021 fitted
 DO NOT USE

**STM32F437VIT6 U1001E**

PC0 15 VBUS_VALID
 PC1 16 SPI_INT_MAG_ICS
 PC2 17 MPU_CS
 PC3 18 FMU_AUX_POWER_ADC1
 PC4 33 FMU_AUX_ADC2
 PC5 34 PRESSURE_SENS
 PC6 63 SERIAL_FMU_TO_IO
 PC7 64 SERIAL_IO_TO_FMU

STM32F437VIT6 U1001F

PC8 65 SDIO_D0
 PC9 66 SDIO_D1
 PC10 78 SDIO_D2
 PC11 79 SDIO_D3
 PC12 80 SDIO_CLK
 PC13 7 GYRO_EXT_CS
 PC14 8 BARO_EXT_CS
 PC15 9 ACCEL_MAG_EXT_CS

STM32F437VIT6 U1001G

PD0 81 CAN1_RX
 PD1 82 CAN1_TX
 PD2 83 SDIO_CMD
 PD3 84 FMU-USART2_CTS
 PD4 85 FMU-USART2_RTS
 PD5 86 FMU-USART2_TX
 PD6 87 FMU-USART2_RX
 PD7 88 BARO_CS

STM32F437VIT6 U1001H

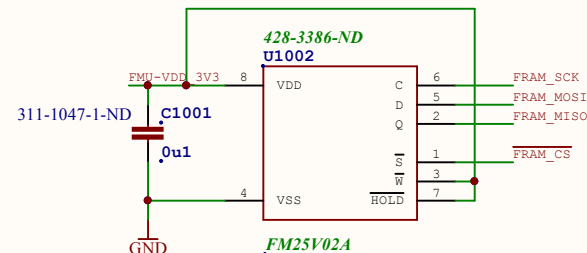
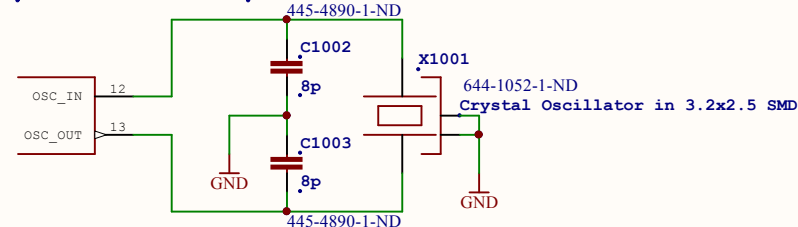
PD8 55 FMU-USART3_TX
 PD9 56 FMU-USART3_RX
 PD10 57 FRAM_CS
 PD11 58 FMU-USART3_CTS
 PD12 59 FMU-USART3_RTS
 PD13 60 FMU-CH5
 PD14 61 FMU-CH6
 PD15 62 MPU_DRDY

STM32F437VIT6 U1001I

PE0 97 FMU-UART8_RX
 PE1 98 FMU-UART8_TX
 PE2 1 SPI_EXT_SCK
 PE3 2 VDD_3V3_SENSORS_EN
 PE4 3 MPU_EXT_CS
 PE5 4 SPI_EXT_MISO
 PE6 5 SPI_EXT_MOSI
 PE7 38 FMU-UART7_RX

STM32F437VIT6 U1001J

PE8 39 FMU-UART7_TX
 PE9 40 FMU-CH4
 PE10 41 VDD_5V_HIPPOWER_OC
 PE11 42 FMU-CH3
 PE12 43 FMU-LED_AMBER
 PE13 44 FMU-CH2
 PE14 45 FMU-CH1
 PE15 46 VDD_5V_PERIPH_OC

STM32F437VIT6 U1001K

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PCB005

PCB005

Title: FMU FMU3 REV G.SchDoc

Date: 9/09/2015

Time: 4:09:31 PM

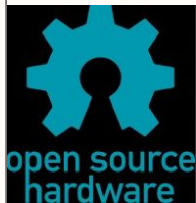
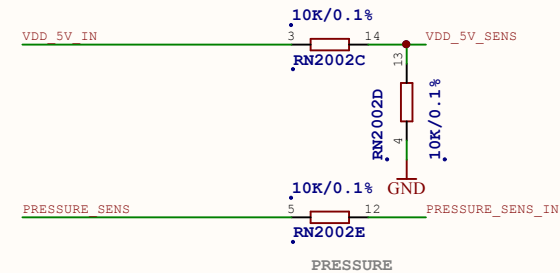
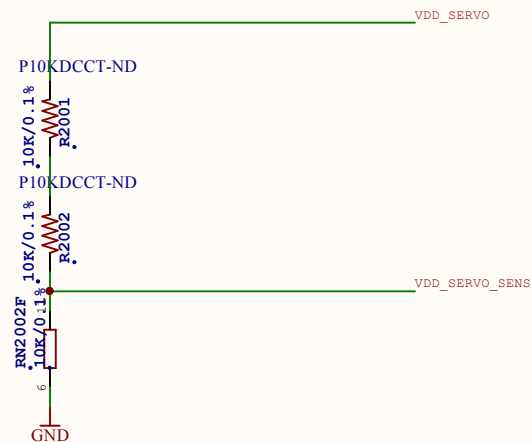
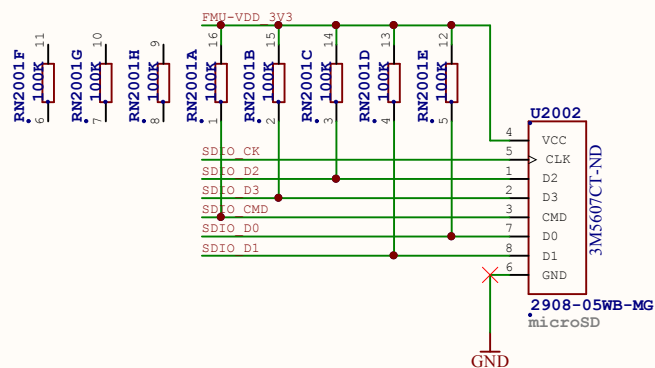
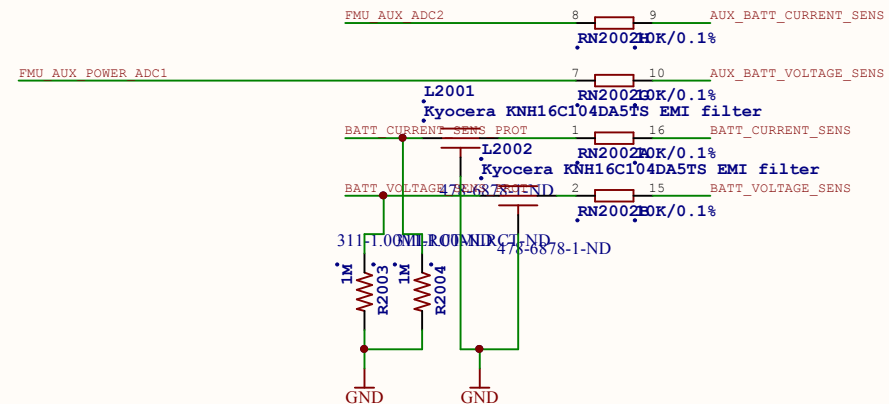
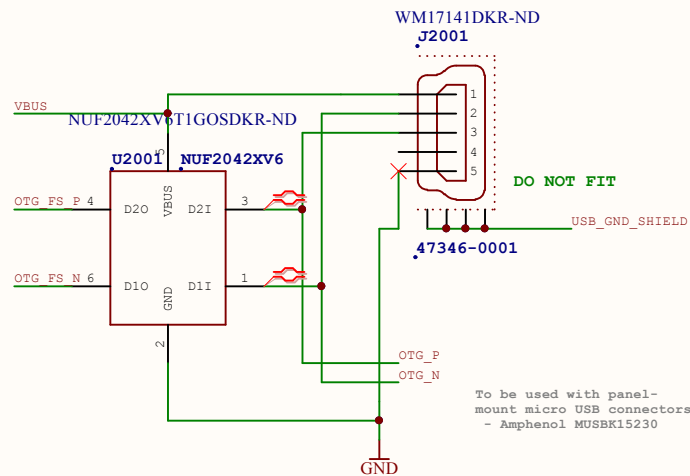
Sheet:1 of: 10

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Approved: *

Checked By: *

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Title: SD USB FMU3 REV G.SchDoc

Date: 9/09/2015

Time: 4:09:31 PM

Sheet:2 of: 10

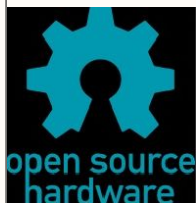
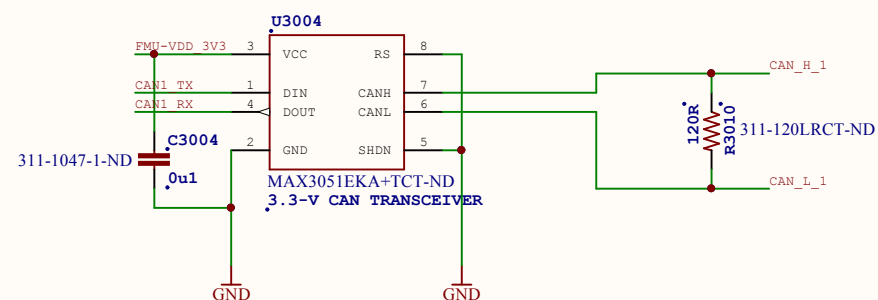
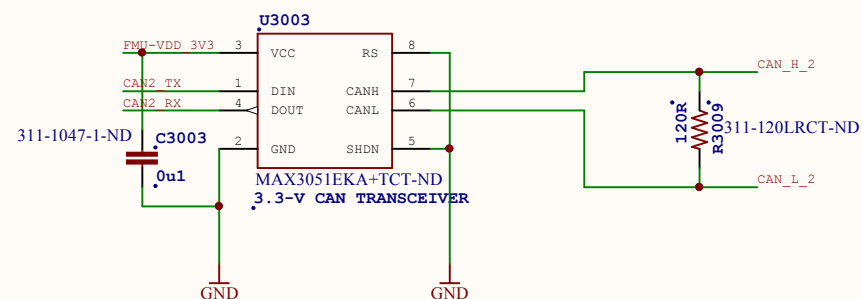
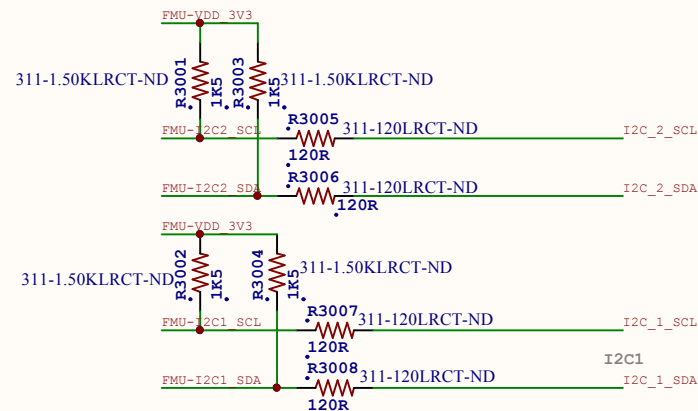
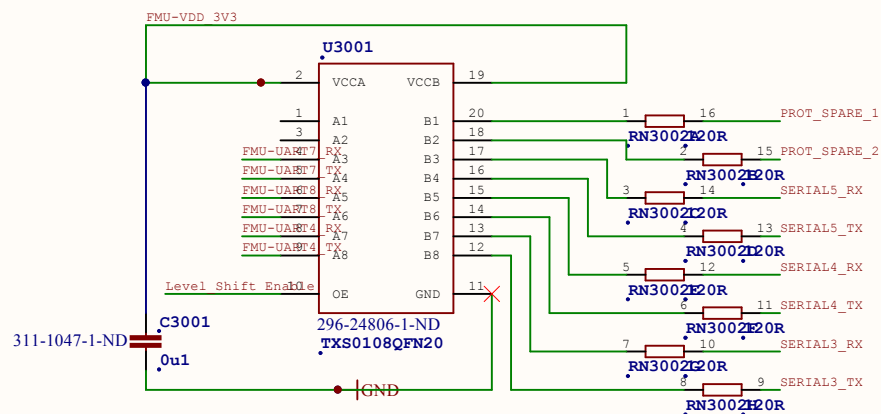
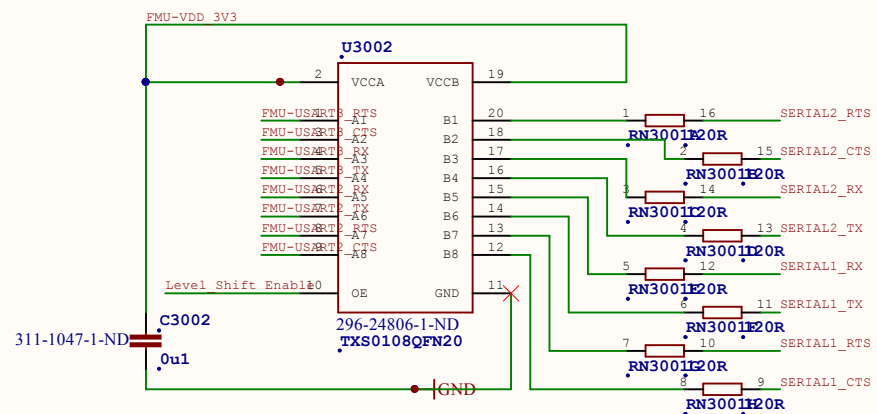
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Title: SERIAL FMU3 REV G.SchDoc

Date: 9/09/2015

Time: 4:09:32 PM

Sheet:3 of: 10

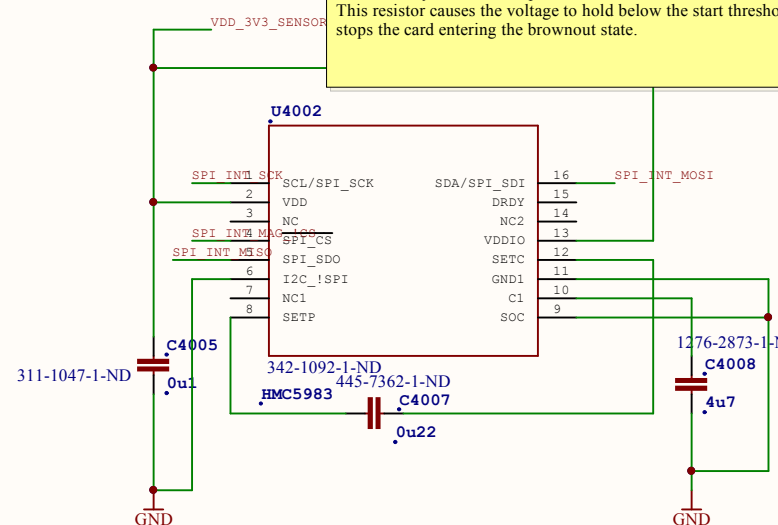
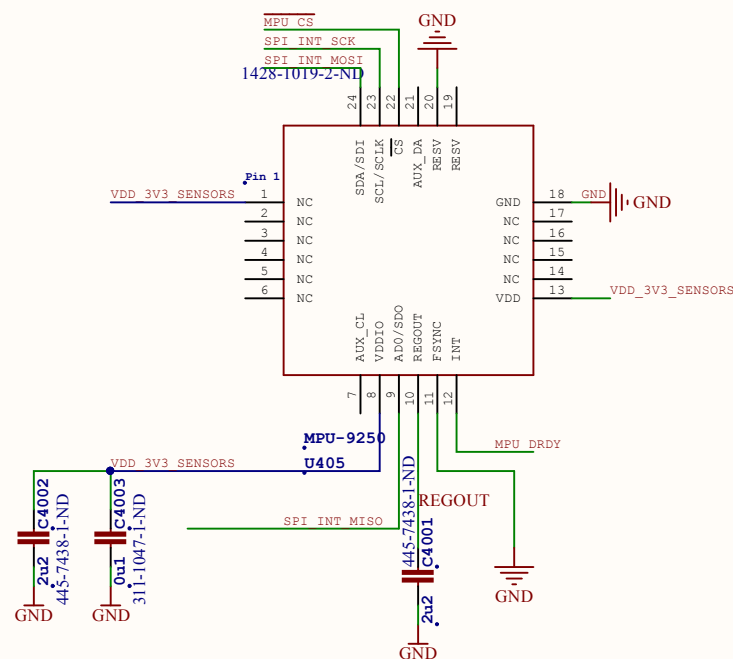
Drawn By: Philip Rowse

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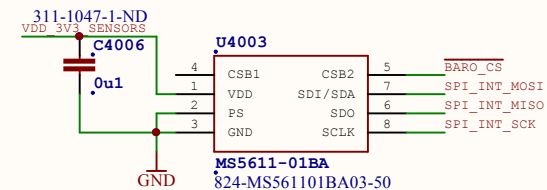
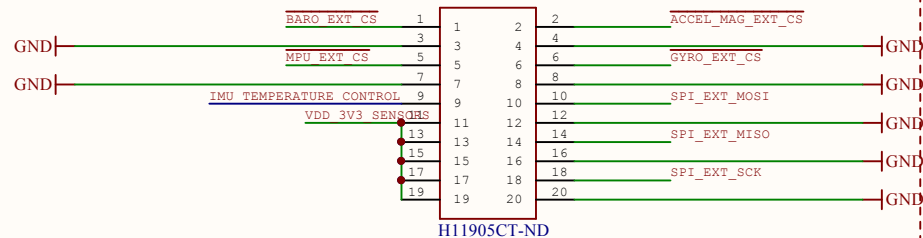
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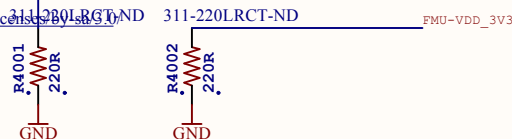


due to the serial lines being able to back power the cpu, The SD card can end up in a state where it's CPU does not shut down correctly, and it goes into a brownout state. This can cause the SD card to fail on startup. This is characterised by an SOS tone from the buzzer, every second startup. This resistor causes the voltage to hold below the start threshold of the SD card, and therefore stops the card entering the brownout state.



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Title: SENSORS FMU3 REV G.SchDoc

Date: 9/09/2015

Time: 4:09:32 PM

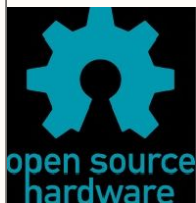
Sheet:4 of: 10

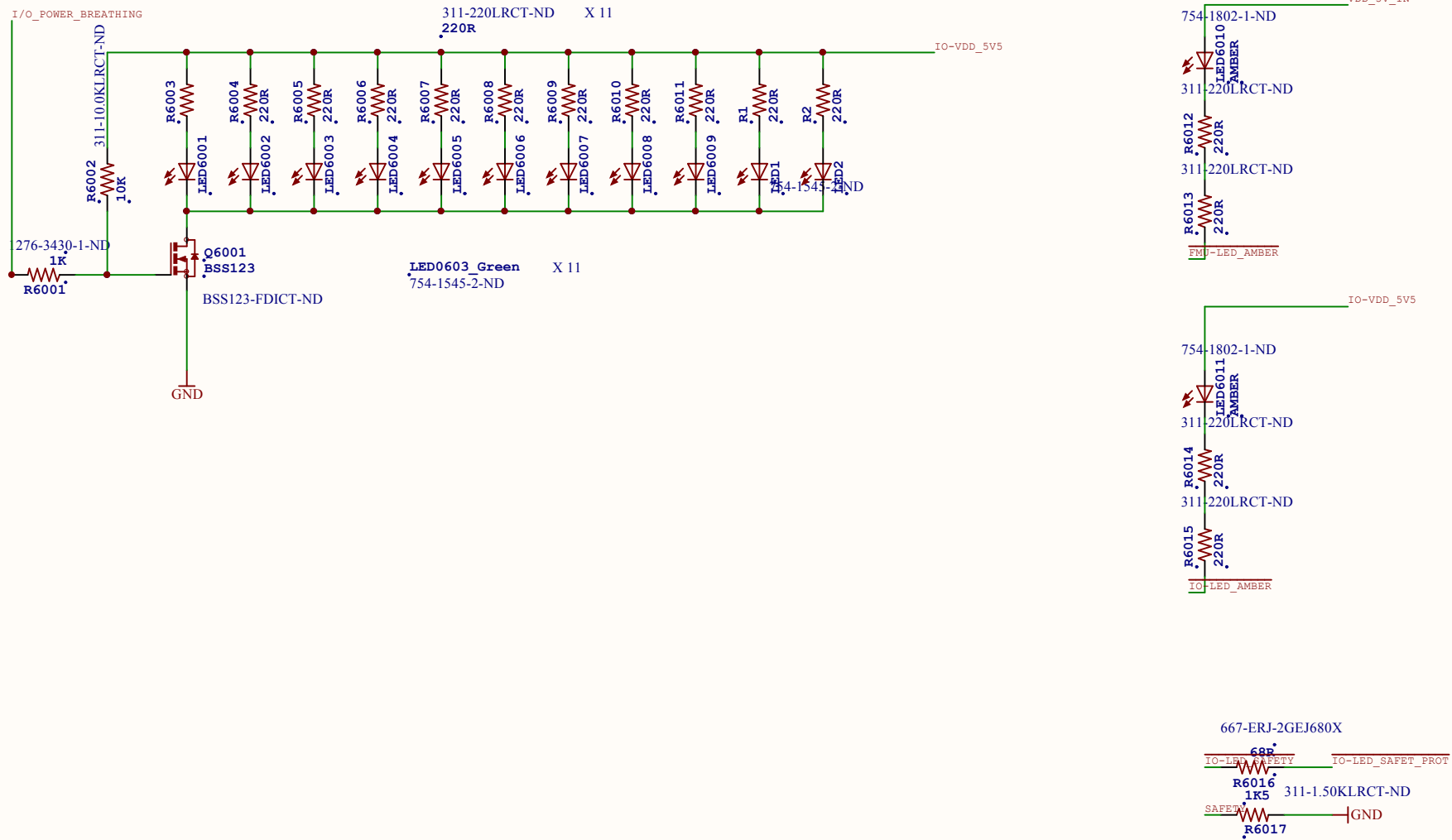
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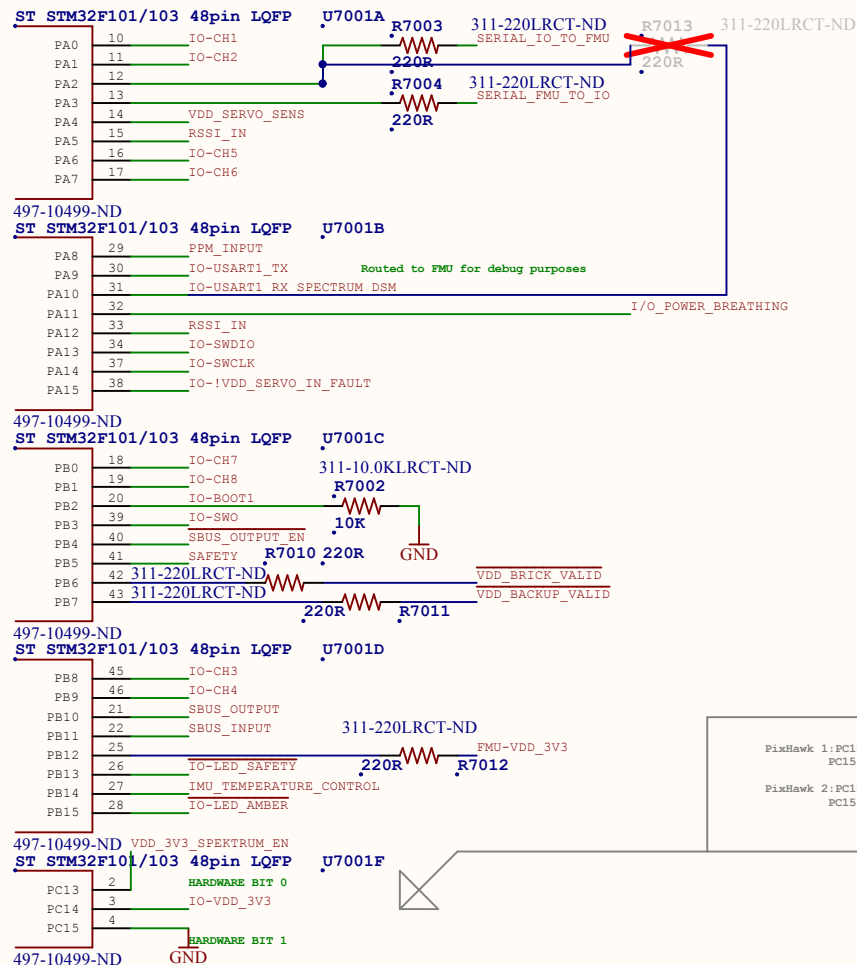
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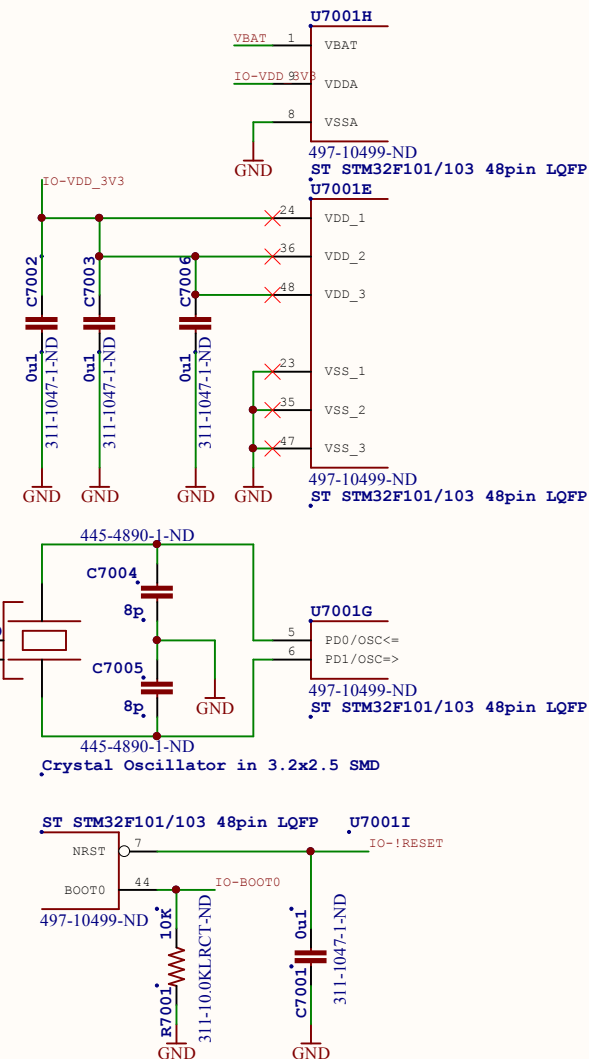


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|-------------------------------|------------------------|---|
| Title: LEDs FMU3 REV G.SchDoc | |  |
| Date: 9/09/2015 | Time: 4:09:32 PM | |
| Sheet:6 of: 10 | Drawn By: Philip Rowse | |
| Approved: * | Checked By: * | |
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Timer allocation:
PA0: TIM2 CH1: IO-CH1
PA1: TIM2 CH2: IO-CH2
PB8: TIM4 CH3: IO-CH3
PB9: TIM4 CH4: IO-CH4
PA6: TIM3 CH1: IO-CH5
PA7: TIM3 CH2: IO-CH6
PB0: TIM3 CH3: IO-CH7
PB1: TIM3 CH4: IO-CH8
PA8: TIM1 CH1: PPM_IN
PA11: TIM1 CH4: RSSI_IN



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Title: IO FMU3 REV G.SchDoc

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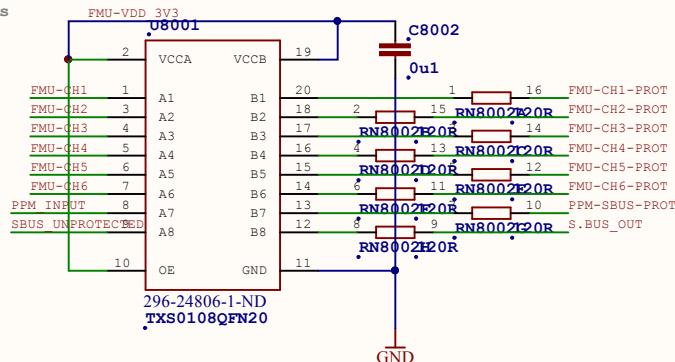
Approved: *

Checked By: *

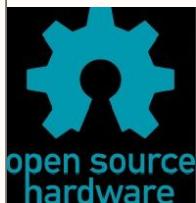
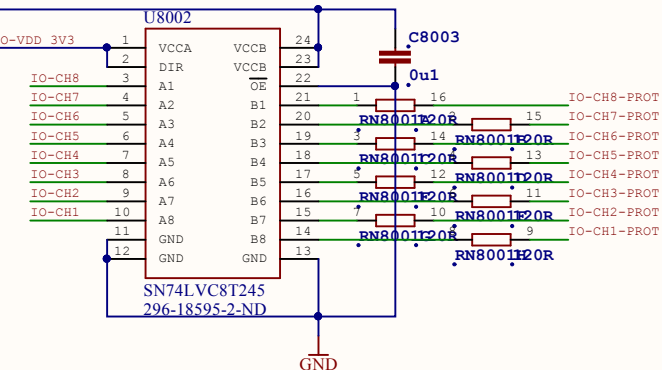
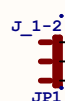
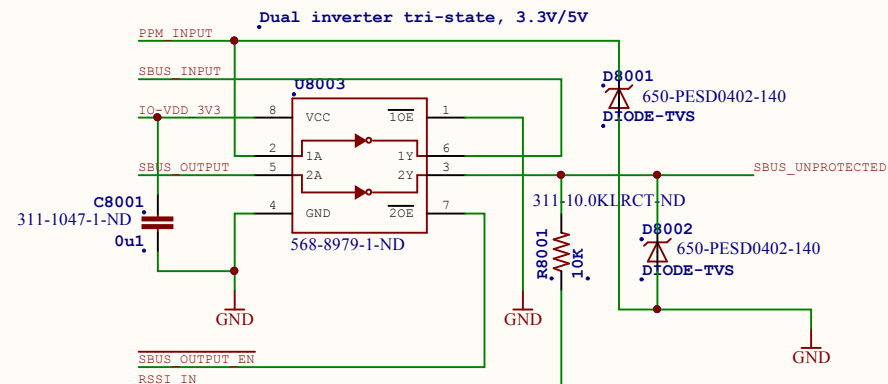


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Servo outputs



S.Bus in/out



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Title: PWM PPM FMU3 REV G.SchDoc

Date: 9/09/2015

Time: 4:09:32 PM

Sheet:8 of: 10

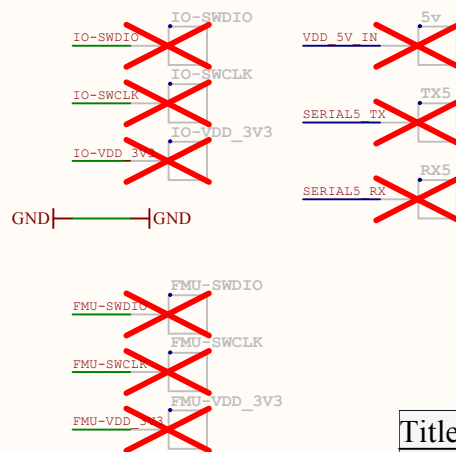
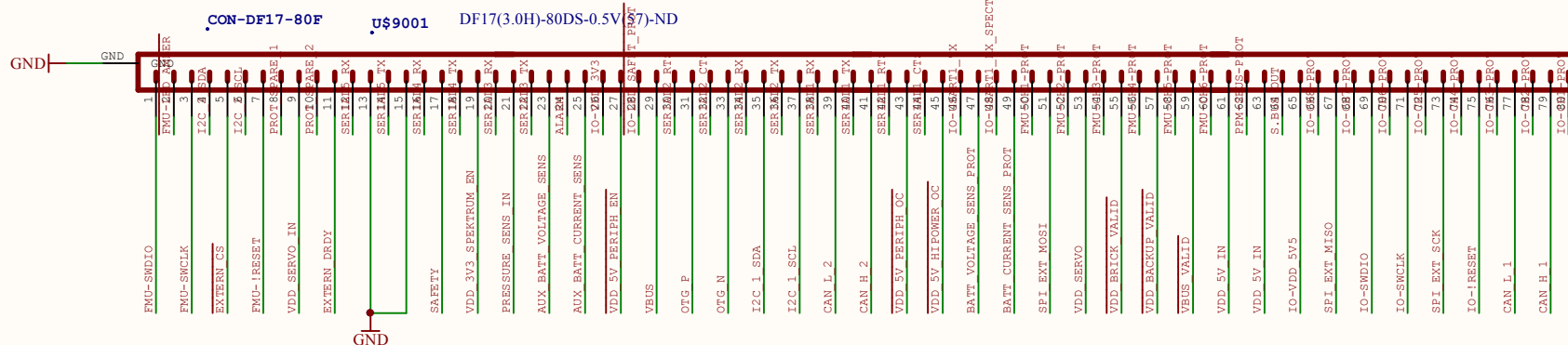
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Title: 80PIN FMU3 REV G.SchDoc

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Time: 4:09:33 PM

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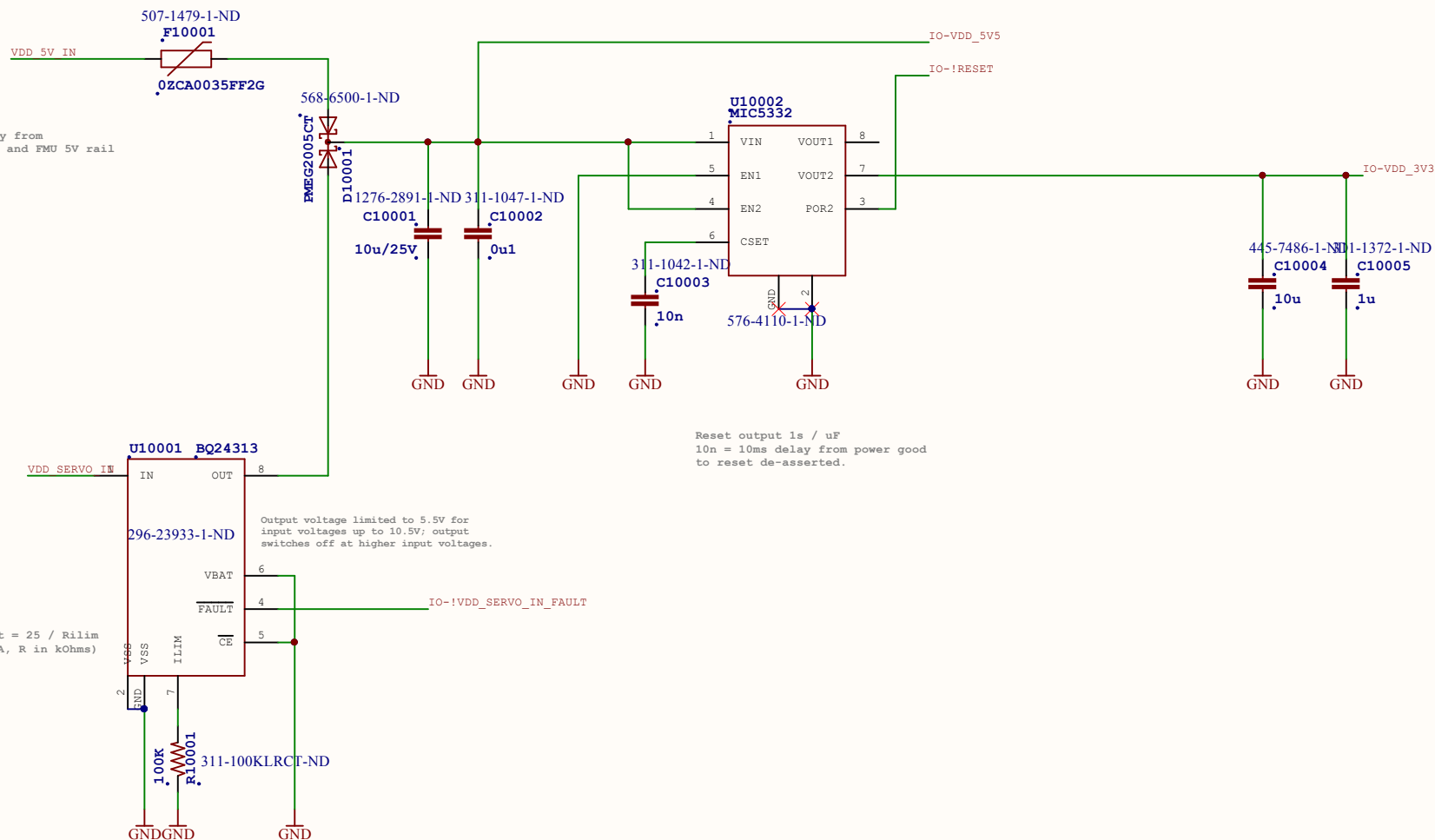
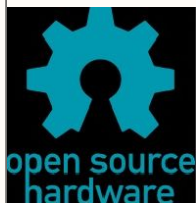
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Title: IO PWR FMU3 REV G.SchDoc

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Time: 4:09:33 PM

Sheet:10 of: 10

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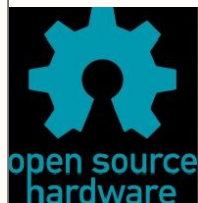
4

1. What
 - a.new revision of the FMU
2. Why
 - a.To increase drive capability of I/O PWM 1-8
3. Who
 - a.Production
4. When
 - a. URGENT
5. Milestones.
 - a.
6. Budget
 - a.
7. Testing and programming plan
 - a.Testing as per existing FMU
8. Field upgrade plan
 - a.Bootloadable, No Change
9. Compliance
 - a.No Compliance changes
10. Accountability
 - a.Review to be signed off by David. W, and Lorenz

Changes for Rev E

Changed Drive chip on I/O out 1-8 to be SN74LVC8T245

This is to allow the PWM pins to drive up to 10mA each (hard limit is 100 mA for all 8 or aprox 12.5mA each)



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Title: CHANGE FMU3 REV G.SchDoc

Date: 9/09/2015

Time: 4:09:33 PM

Sheet:10 of: 10

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