Experience in Using the OpenROAD Flow Scripts tool with ASAP7 Technology by designing the RISC V Processor Design

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***Abstract*— We will develop the RISC-V core processor and discuss our usage of the OpenROAD Flow Scripts tool in this work. It is also known as the ORFS tool, to put it briefly. In essence, OpenROAD Flow Scripts is an open-source tool for producing RTL to GDS Flow of any particular digital design.**

This paper mainly focuses on the design RISC V Core Processor which we are going to implement using Openroad And OPENROAD FLOW SCRIPT using ASAP7 Technology and also focuses on its area and power performance improvement.

Keywords—- ***RTL-to-GDSII flow, Open ROAD Flow Scripts,open-source tools, automated design, Verilog code.***

I. Introduction

For any digital circuit design, the OpenROAD Flow Scripts tool is used to create the RTL to GDS. This tool uses an automated flow that does not include any humans at any point. We will discuss the OpenROAD Flow Scripts on a RISC V core processor design in this work, as well as the advantages and disadvantages of various implementation-related difficulties. High-Performance Computing systems are able to jointly solve issues that are beyond the capabilities of standalone computing architectures when paired with conventional desktop computer CPUs, specialized storage & connection resources, and huge computing clusters or grids.

The experience of using the ORFS tool is quietly great as it is automated flow which does need any in human in between the generation of flow also, it's cost effective and it can be designed for any digital design . This tool has the quality for improving the performance for higher digital designs andis also used for optimizing the design . Hence, the tool is quietly great, but it is dependent on other opensource tool such as OpenROAD which has it's down dependemcies, installations for a particular design. So, the tool need to be analyzed carefullt first.

II. Experience and Working

The ORFS experience is absolutely outstanding as it is an automated flow, requires no human intervention between flow generation, is inexpensive and can be customized for any digital project. This tool has a performance-enhancing quality for higher-value projects and is also used for design optimization. So the tool is still great, but it depends on another open source tool like OpenROAD, which has its own dependencies, installations for a specific project. Therefore, the tool should be checked carefully first. Also, If I compare this ORFS tool with openlane then, this tool integrates multiple tool like EDA, Yosys,klayout, OpenROAD.This tool is highly customizable as it meets the specific design requirement params while openlane is much more rigid and customization focus is not there. So, ORFS is great tool for designing any digital design .

So, in this paper, we are going to implement the Riscv design using OpenROAD and OPENROAD FLOW SCRIPT Tool With ASAP7 Technology which is basically the 7nm technology.

Here, given the glimpses of some of the information and working of the RISC-V CPU Core (RV32IM):-

• Such as SoC level drivers, monitors, reference models, functional coverage, top-level test benches, scoreboards/checkers, and assertions are common verification components.

• The configuration of the entire SoC or its submodules utilizing the processor to drive SoC level stimuli is known as a processor-based SoC.

• Integration of fast interface subsystems. Enabling SoC level debuggability via the CPU architecture's Trace interface is a possibility. Power-conscious CPU architectures that allow the Cores or Clusters to be turned off when not in use

III. Circuit Design

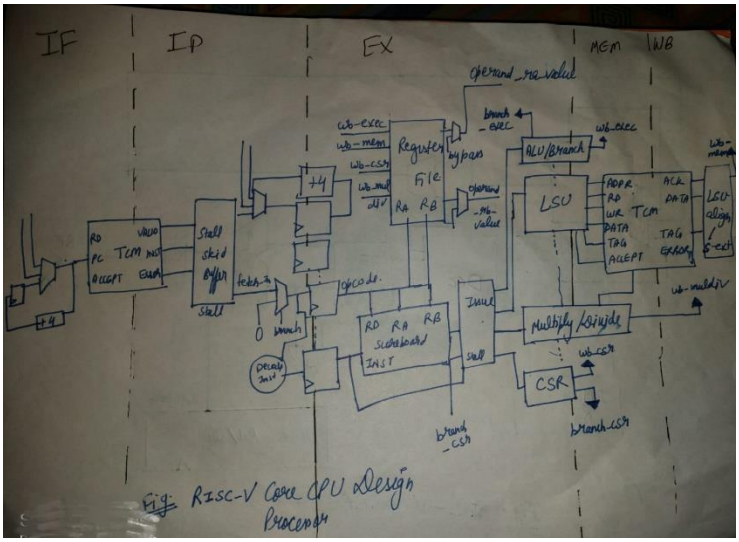

Fig. This above block diagram is of RISC-V Core CPU Processor as it is going to be implemented in the tool.

IV. Conclusion

High-Performance Computing systems are able to jointly solve issues that are beyond the capabilities of standalone computing architectures when paired with conventional desktop computer CPUs, specialized storage & connection resources, and huge computing clusters or grids. So, here also we are going to design the RISC-V CPU Core which can be used in computers and this paper describes the design which we are going to implement this design using Openroad And OPENROAD FLOW SCRIPT using ASAP7 Technology and also focuses on its area and power performance improvement.

V. References

[1] AE-AVI Encoder implementation: Using OpenROAD to achieve Real-time Throughput. By Tulio Pereira Bitencourt https://theopenroadproject.org/ae-av1-encoder-implementation-using-openroad-to-achieve-real-time-throughput/

[2] RISC-V CPU Core by ultraembedded https://github.com/ultraembedded/riscv

[3] OPENROAD FLOW SCRIPTS https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts

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