OpenROAD Improvement in Area and performance for IBEX Core Processor implemented using ASAP7 Technology

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***Abstract*— OpenROAD and OpenROAD Flow Scripts are combinely and separately both are an open-source tool that is used for generating the RTL to GDS Flow without any inhuman involvement in between the flow. This paper describes the suggested different solutions by reducing the runtime, improving area or power performance, and also, trying for making the docs for the IBEX Core processor which is already implemented using ASAP7 using OpenROAD Flow Scripts and OpenROAD.**

Keywords*— *OpenROAD Flow Scripts, RTL-to-GDSII flow, open-source tools, automated design, no-human-in-the-loop, Verilog file, ASAP7,etc..

I. INTRODUCTION

. OpenROAD is an efficient open-source tool that is used for generating the RTL-to-GDSII flow which provides an implementation of the layout for any digital system design.

So, here I have taken the IBEX Core processor in which I am going to improve its area basically optimizing the area, and frequency and also going to reduce the running time of the whole circuit for getting the fastest run time . Also, try to improve or optimize its power performance and also try to improve the documentation of OpenROAD documentation.

II. IMPROVEMENT

The suggested improvement in the IBEX Core will be going to do changes when trying the solution in reducing the timing parameters, run time improvement, its die area and area, by doing changes in it's configuration file of the already existing IBEX Core processor and if possible then will also try to improve the power performance by doing some changes in its scripts and also in it's python file and make file.

The configuration file of IBEX Core is shown below and the marking of blue line shows where I am going to do changes for area improvement of IBEX Core Processor:

```
export PLATFORM               = asap7

export DESIGN_NICKNAME        = ibex
export DESIGN_NAME            = ibex_core

export VERILOG_FILES          = $(sort $(wildcard ./designs/src/$(DESIGN_NICKNAME)/*.v))
export SDC_FILE               = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION       =  40
export CORE_ASPECT_RATIO      = 1
export CORE_MARGIN            = 2
export PLACE_DENSITY_LB_ADDON  = 0.20

export ENABLE_DPO = 0

export DFF_LIB_FILE           = $(CORNER)_DFF_LIB_FILE
```

III. CONCLUSIONS AND RECOMMENDATIONS

The conclusion of this is that we are going to reduce the area and power performance and also try to reduce the run time and power of the IBEX Core processor which is already implemented in the OpenROAD Flow Scripts using ASAP7 technology. So, the main focus of this paper is that going to improve power performance and reduce the Area. And, if possible in the end, then, we are going to also improve the runtime and the docs of the OpenROAD Flow Script tool.

IV. REFERENCES

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