AXP203 Datasheet

Enhanced single Cell Li-Battery and Power System Management IC

Version: 1.0

Release Data: Apr 03,2015

Revision History

Revision	Date	Description
V1.0	Apr.03,2015	Initial Release Version

Declaration

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Catalog

1.Introduction

AXP203 is a highly integrated power management IC that provides easy and flexible power solution for applications that powered by single cell Li-battery (Li-ion or Li-polymer) and require multi-power outputs as well. It has fully met the increasingly complex needs of application processors on accurate power control.

AXP203 integrates an adaptive and USB-compatible PWM charger, two step-down converters (Buck DC-DC converter), five LDO regulators, multiple voltage/current/temperature 12-bit ADCs, and four configurable GPIOs. It also features protection circuitry such as over/under-voltage protection(OVP/UVP), over-temperature protection (OTP), and over-current protection (OCP) to guarantee the power system security and stability.

The Intelligent Power Select of AXP203 (Intelligent Power Select, IPS™) can allocate power safely and transparently among USB, external AC adapter, Li-battery, and application loads. It also enables applications to work normally with only external input power but no batteries (or battery deeply discharged/damage).

AXP203 is capable of three input methods: external adaptor input, USB input and battery input. It also supports rechargeable backup batteries.

In addition, AXP203 comes with a Two Wire Serial Interfaces (TWSI), through which the application processor is capable of enabling/disabling some power outputs, programming the voltage, and visiting internal registers and measurement data (including Fuel Gauge). High accuracy (1%, depending on the 1% accuracy of BIAS resistors) of power measurement enables consumers to know more clearly the real-time power consumption, and provides them with unprecedented experience of power management.

Applications:

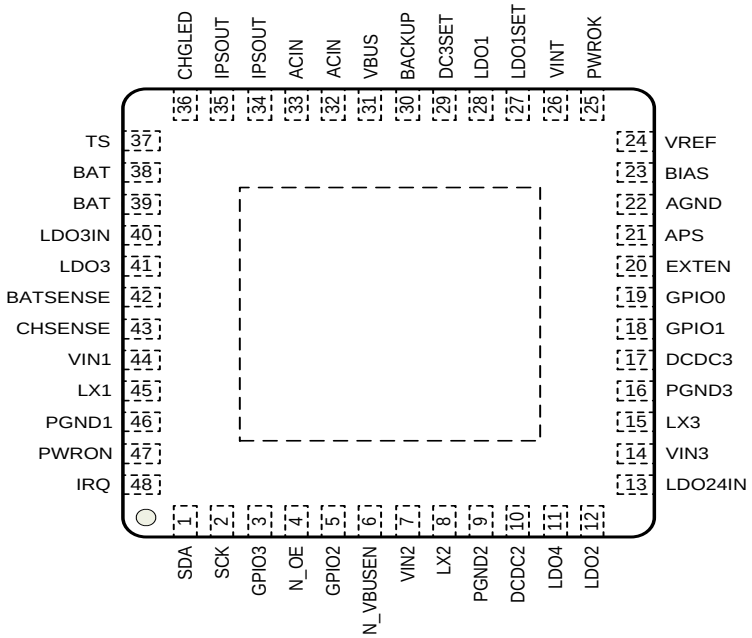
- Portable Devices: Smart Phone, PMP/MP4, Digital Camera, Camcorder, PND, PDA, PTV
- Mobile Internet Devices xPad, MID
- Digital Photo Frame, Portable DVD Player, Ultra-Mobile PC(UMPC) and UMPC-like, Entertaining and Education Machine
- Application Processor Systems
- Other battery and multi-power application system

2.Features

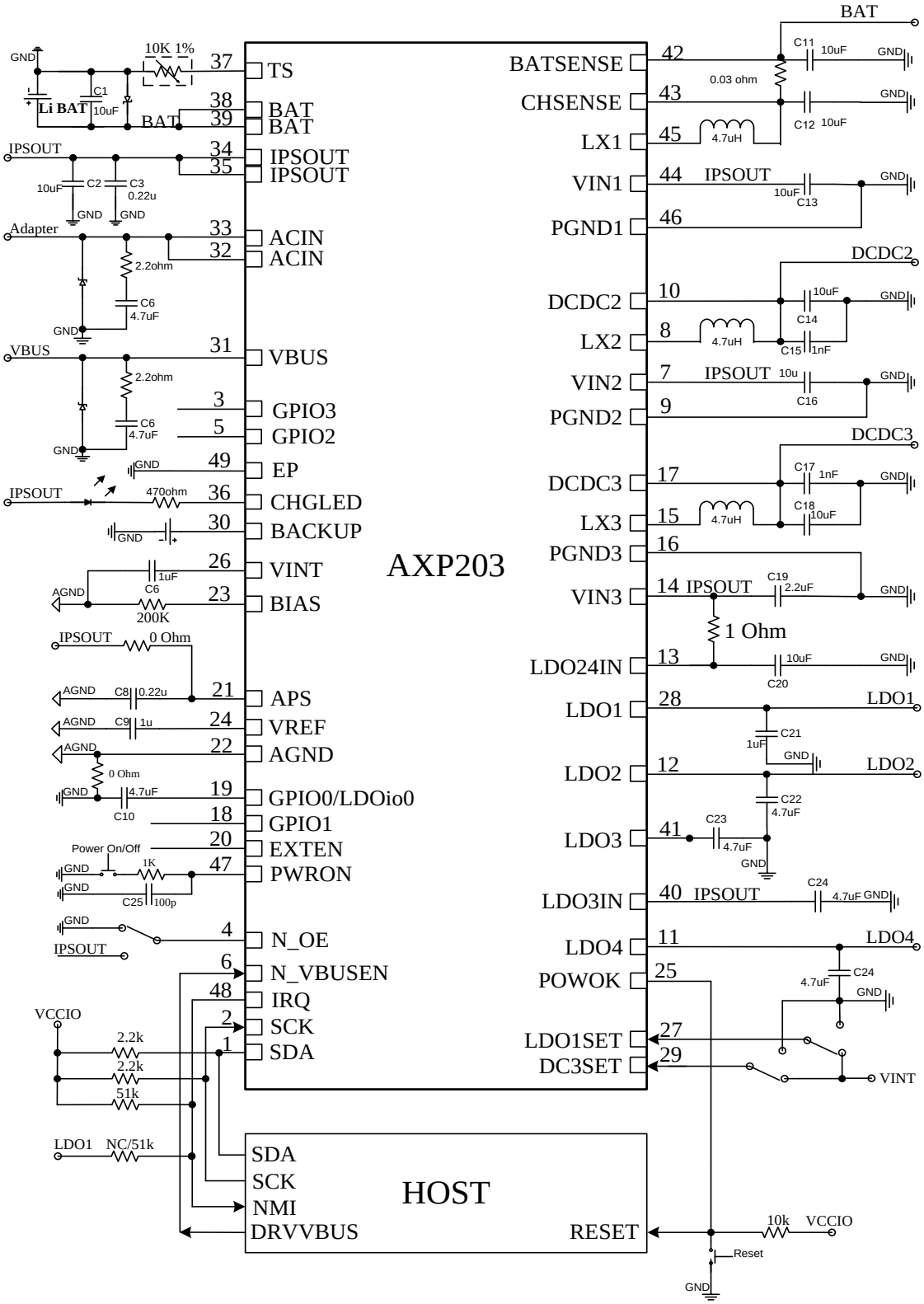
- Power Management IPS
  - ✧ Wide range of voltage input: 2.9V~6.3V (AMR：-0.3V~11V)
  - ✧ Configurable IPS™ system
  - ✧ Adaptive USB (supporting USB3.0) or AC adaptor Voltage/current limit (4.4V/900mA/500mA/100mA)
  - ✧ Equivalent internal resistance of battery below 75mΩ.
- Fully Integrated PWM Charger
  - ✧ Maximum charge current up to 1.8A.
  - ✧ Support battery temperature monitoring
  - ✧ Fully support USB charging (including 3.0) complied with regulation
  - ✧ High charge accuracy, with error less than 0.5%
  - ✧ Support batteries of 4.1V/4.15V/4.2V/4.36V
  - ✧ Automatic charge process control
  - ✧ Directly drive LED to indicate charge status
  - ✧ Automatic scaling of charge current according to system load
- Backup Battery
  - ✧ Backup battery input for RTC
  - ✧ Support backup battery charging with configurable charge current
- 2 Synchronous Buck Converters (DC-DC)
  - ✧ DC-DC2: 0.7-2.275V adjustable, 25mV/step, driving ability 1.6A, support VRC (Voltage Ramp Control)
  - ✧ DC-DC3: 0.7-3.5V adjustable, 25mV/step, driving ability 1.2A
- 5 LDOs
  - ✧ LDO1: 30mA, always on
  - ✧ LDO2: low noise LDO, 1.8V~3.3V adjustable, 100mV/step, driving ability 200mA
  - ✧ LDO3:0.7-3.5V adjustable, 25mV/step, driving ability 200mA
  - ✧ LDO4: low noise LDO, 1.8V~3.3V adjustable, 100mV/step, driving ability 200mA
  - ✧ LDO5: low noise LDO, 1.8V~3.3V adjustable, 100mV/step, driving ability 50mA
- Timer
  - ✧ 7-bit timer with 1~127 minutes timing range
  - ✧ Timer interrupt output
- Signal Capture System
  - ✧ Built-in twelve 12-bit ADCs
  - ✧ Two external signal inputs
  - ✧ Provide the voltage/current data of batteries and external input powers
  - ✧ Built-in highly accurate Coulomb Counter and Fuel gauge system
  - ✧ Provide rich power management information, such as instantaneous power consumption (mA or mW), remaining battery power (% or mA), charging status (%), remaining power life or charging time, etc.
  - ✧ Two-level low power warning and protection
  - ✧ Provide die temperature data
- Host Interface

- ✧ Data exchange through TWSI interface.
- ✧ Flexible interrupt and sleep management configuration
- ✧ Flexible pin configuration: multiple GPIOs set as IO or ADC.etc.
- ✧ Built-in configurable timer
- ✧ Provide twelve registers for data storage during system shutdown

- System Management
  - ✧ Support soft reset and hard reset
  - ✧ Support soft shutdown and hard shutdown
  - ✧ Support external wakeup triggers
  - ✧ Support output voltage monitoring and self-diagnostic function
  - ✧ Output PWROK for system reset or shutdown indication
  - ✧ External power detection (insert/remove/drive capability deficiency)
  - ✧ Support soft booting.
  - ✧ Over/under-voltage protection (OVP/UVP)
  - ✧ Over-current protection (OCP)
  - ✧ Over-temperature protection (OTP)
  - ✧ Support OTG VBUS power status setting/monitoring
- Full Integration
  - ✧ Internally produced reference voltage of high accuracy (0.5%).
  - ✧ Built-in MOSFET
  - ✧ Programmable timing and output voltage
- Decryption Module
  - ✧ 128-bit OTP code storage
  - ✧ Dynamic real-time decryption algorithm
- AXP203 is available in 6mm x 6mm 48-pin QFN package



3.Typical Application



4.Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
ACIN	Input Voltage	-0.3	11	V
VBUS	Input Voltage	-0.3	11	V
T_J	Operating Temperature Range	-40	130	℃
Ts	Storage Temperature Range	-40	150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)	-	300	℃
V_{ESD}	Maximum ESD stress voltage，Human Body Model	-	>4000	V
P_D	Internal Power Dissipation	-	2100	mW

5.Electrical Characteristics

V_{IN} =5V， BAT=3.8V， T_A= 25℃

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
ACIN						
V_{IN}	ACIN Input Voltage		3.8		6.3	V
I_{OUT}	V_{OUT} Current Available Before Loading BAT	500mV Voltage Drop		2500		mA
V_{UVLO}	ACIN Under Voltage Lockout			3.8		V
V_{OUT}	IPS Output Voltage		2.9		5.0	V
R_{ACIN}	Internal Ideal Diode On Resistance	PIN to PIN, ACIN to IPSOUT			170	mΩ
VBUS						
V_{IN}	VBUS Input Voltage		3.8		6.3	V
I_{OUT}	V_{OUT} Current Available Before Loading BAT			500	900	mA
V_{UVLO}	VBUS Under Voltage Lockout			3.8		V
V_{OUT}	IPS Output Voltage		2.9		5.0	V
R_{VBUS}	Internal Ideal Diode On Resistance	PIN to PIN, VBUS to IPSOUT			300	mΩ
Battery Charger						
V_{TRGT}	BAT Charge Target Voltage		-0.5%	4.2	+0.5%	V
I_{CHRG}	Charge Current			1200	1800	mA
I_{TRKL}	Trickle Charge Current			10%		I_{CHRG} mA
V_{TRKL}	Trickle Charge Threshold Voltage			3.0		V
ΔV_{RECHG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{TARGET}		-100		mV
T_{TIMER1}	Charger Safety Timer Termination Time	Trickle Mode		40		Min
T_{TIMER2}	Charger Safety Timer Termination Time	CC Mode		480		Min
I_{END}	End of Charge Indication Current Ratio	CV Mode		10%	15%	I_{CHRG} mA
Backup Battery						
V_{TRGT}	Backup Battery Charge Target Voltage		2.5	3.0	3.1	V
I_{CHRG}	Backup Battery Charge Current		50	200	400	uA
I_{Backup}	Current when use Backup Battery			10	15	uA
NTC						
V_{TL}	Cold Temperature Fault Threshold Voltage	Charge	0	2.112	3.264	V
		Discharge		3.226		

V_{TH}	Hot Temperature Fault Threshold Voltage	Charge	0	0.397	3.264	V
		Discharge		0.282		
V_{TE}	NTC Disable Threshold Voltage	Falling Threshold Hysteresis		0.2		V
Ideal Diode						
$R_{ds(on)}$	On Resistance(BAT to IPSOUT)				75	mΩ

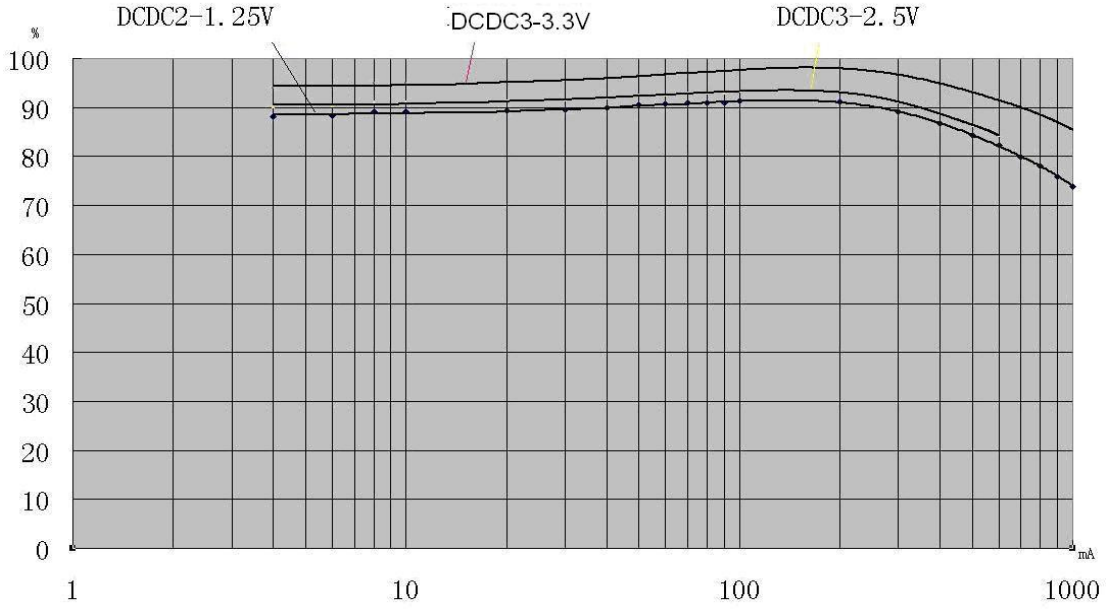
SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Off Mode Current						
I_{BATOFF}	OFF Mode Current	BAT=3.8V		27		μA
$I_{SUSPEND}$	USB VBUS suspend Mode current	BAT=3.8V，VBUS=5V，N_VBUSEN=1		86		μA
Logic						
V_{IL}	Logic Low Input Voltage			0.3		V
V_{IH}	Logic High Input Voltage			2		V
TWSI						
V_{CC}	Input Supply Voltage			3.3		V
ADDRESS	TWSI Address			0x68		
f_{SCK}	Clock Operating Frequency			400	1200	kHZ
t_f	Clock Data Fall Time	2.2Kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2Kohm Pull High		100		ns
DCDC						
f_{OSC}	Oscillator Frequency	Default		1.5		MHz
DCDC2						
I_{LIM2}	PMOS Switch Current Limit	PWM Mode		2300		mA
I_{DC2OUT}	Available Output Current	PWM Mode			1800	mA
V_{DC2OUT}	Output Voltage Range		0.7		2.275	V
DCDC3						
I_{LIM3}	PMOS Switch Current Limit	PWM Mode		1400		mA
I_{DC3OUT}	Available Output Current	PWM Mode			1000	mA
V_{DC3OUT}	Output Voltage Range		0.7		3.5	V

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
LDO1						
V_{LDO1}	Output Voltage	I_{LDO1}=1mA	-1%	1.3 3.3	1%	V
I_{LDO1}	Output Current			30		mA
LDO2						
V_{LDO2}	Output Voltage	I_{LDO2}=1mA	1.8		3.3	V
I_{LDO2}	Output Current			200		mA
PSRR	Power Supply Rejection Ratio	I_{LDO2}=60mA，1KHz		TBD		dB
e_N	Output Noise,20-80KHz	Vo=3V , Io=150mA		28		μV_{RMS}

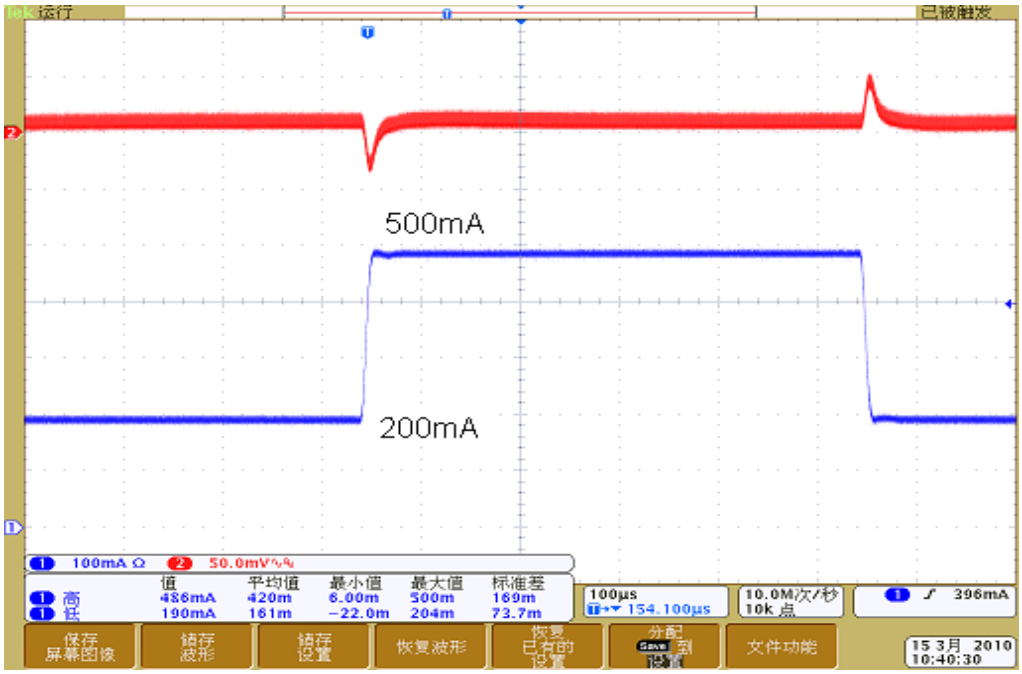
LDO3						
V_{LDO3}	Output Voltage	I_{LDO3}=1mA	0.7		3.5	V
I_{LDO3}	Output Current			200		mA
PSRR	Power Supply Rejection Ratio	I_{LDO3}=10mA， 1KHz		TBD		dB
e_N	Output Noise,20-80KHz	Vo=1.8V , Io=150mA		TBD		μV_{RMS}
LDO4						
V_{LDO3}	Output Voltage	I_{LDO3}=1mA	1.8		3.3	V
I_{LDO3}	Output Current			200		mA
PSRR	Power Supply Rejection Ratio	I_{LDO3}=10mA， 1KHz		TBD		dB
e_N	Output Noise,20-80KHz	Vo=1.8V , Io=150mA		18		μV_{RMS}
LDO5						
V_{LDO5}	Output Voltage	I_{LDO5}=1mA	1.5		3.3	V
I_{LDO5}	Output Current			50		mA
PSRR	Power Supply Rejection Ratio	I_{LDO5}=10mA，1KHz		TBD		dB
e_N	Output Noise,20-80KHz	Vo=1.8V, Io=30mA		18		μV_{RMS}

6.Typical Characteristics

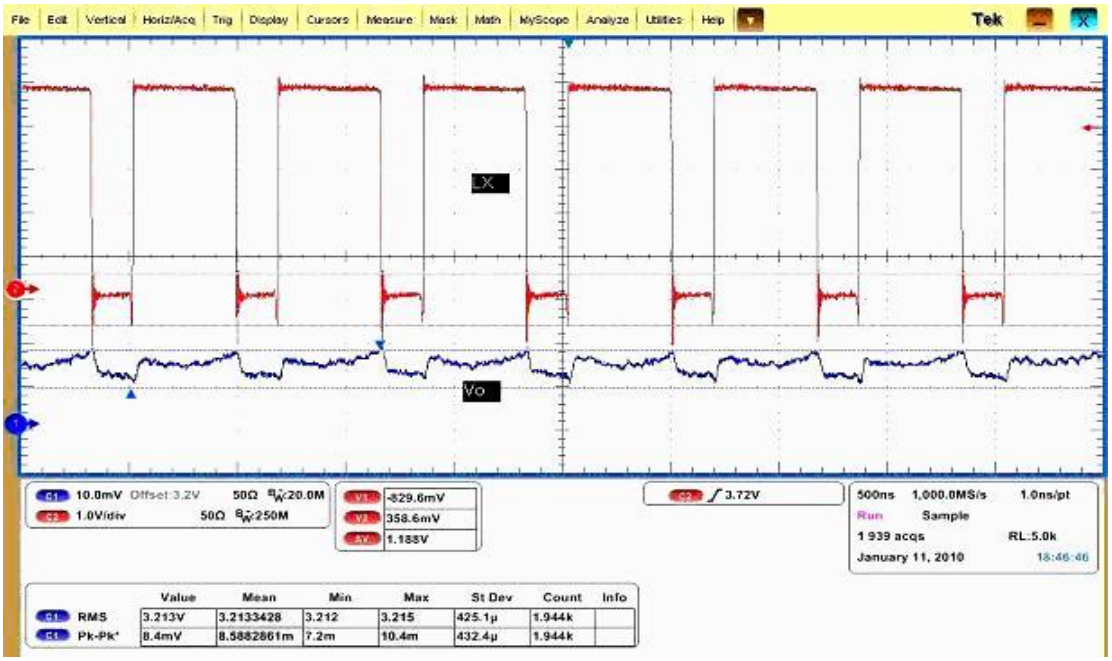
DC-DC Efficiency vs. Load(3.8Vin)



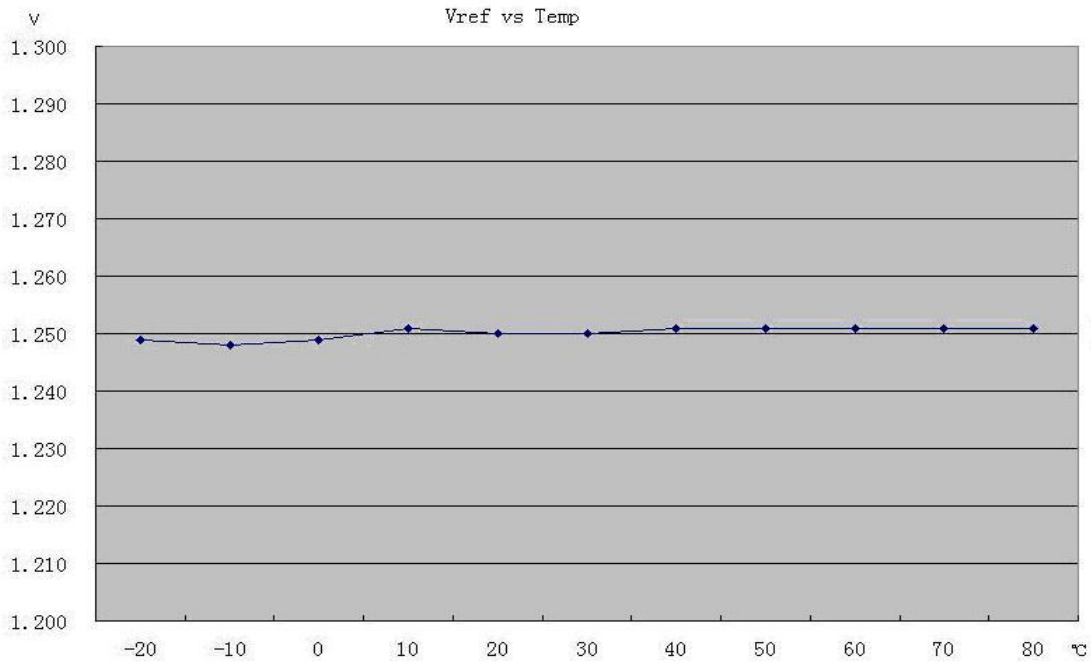
DC-DC Load Transient(Typical)



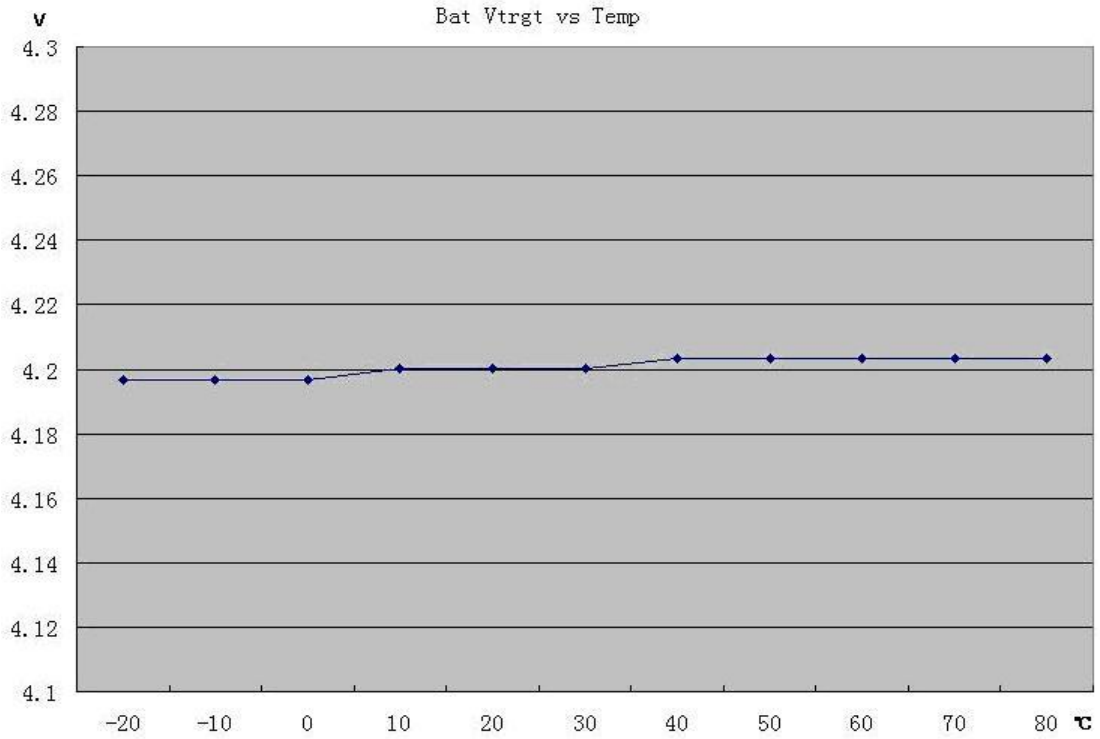
DC-DC Ripple



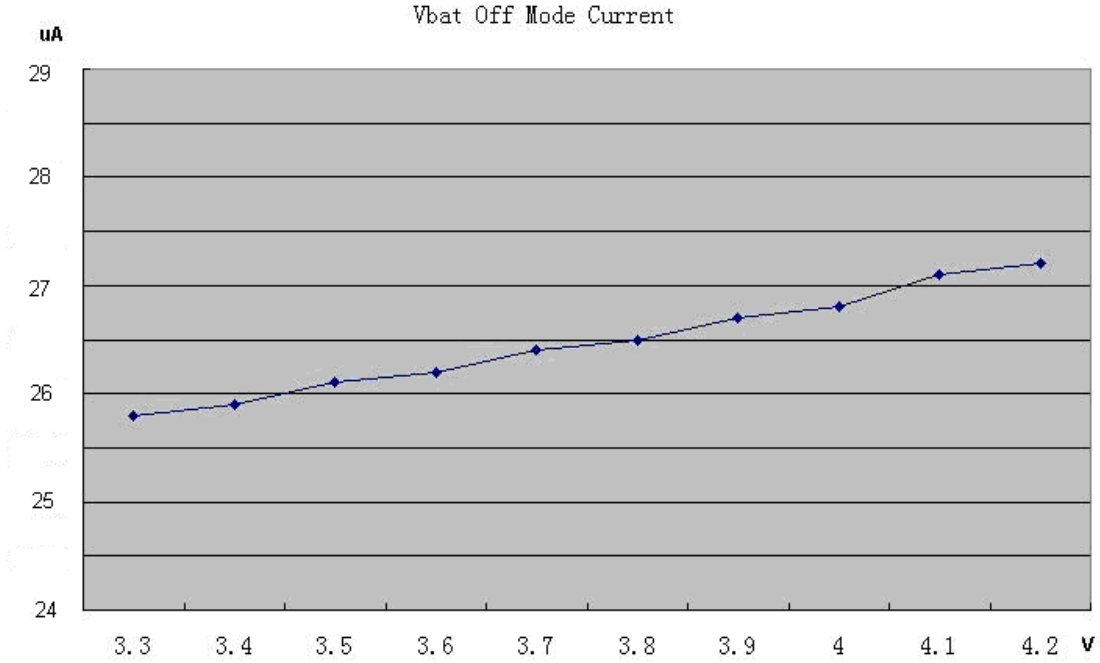
V_{REF} vs. Temperature



V_{TRGT} vs Temperature



Off Mode Current vs V_{BAT}

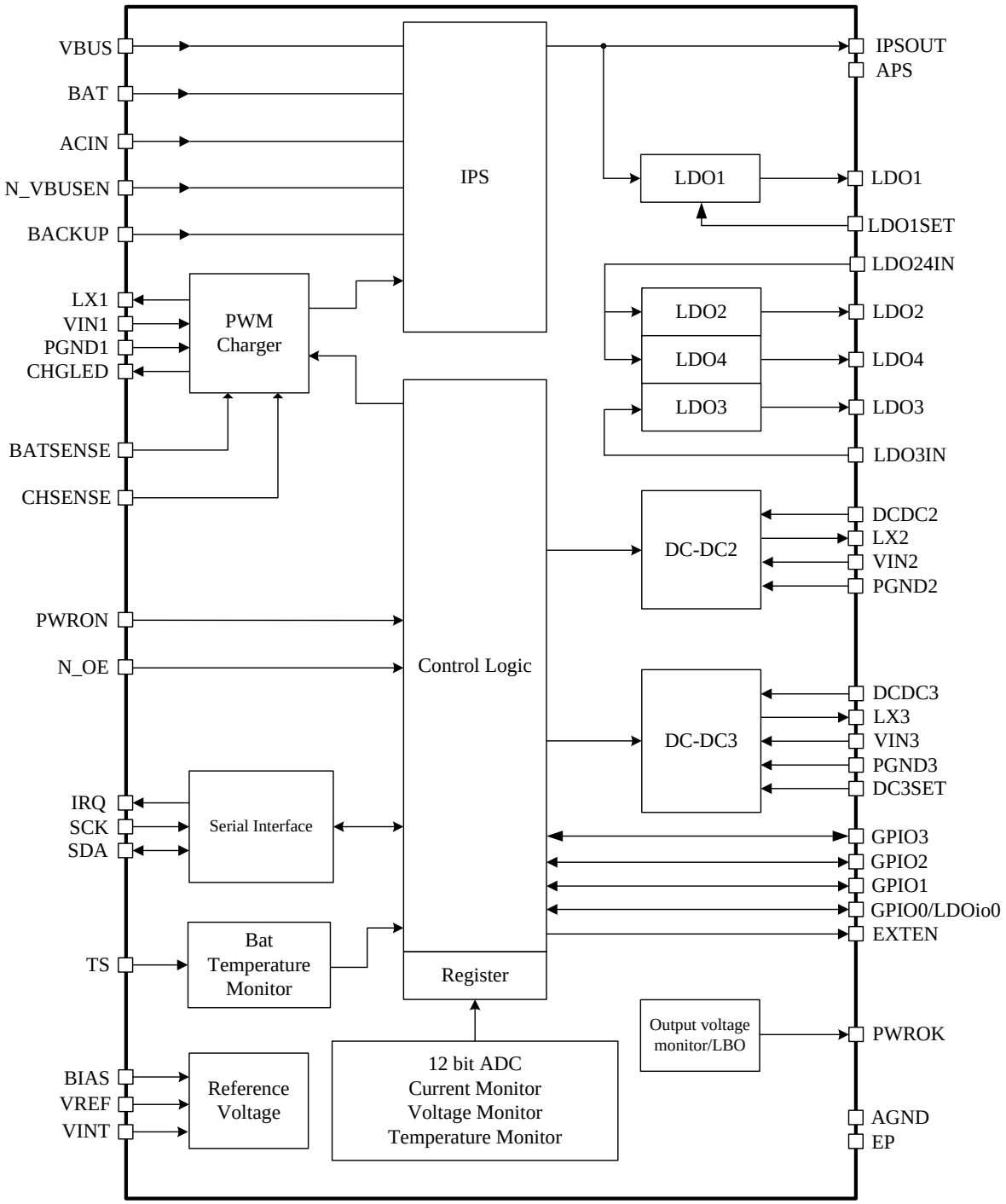


7.Pin Description

Num	Name	Type	Condition	Function Description
1	SDA	IO		Data pin for serial interface, normally it connects a 2.2K resistor to 3.3V I/O power
2	SCK	I		Clock pin for serial interface, normally its connect a 2.2K resistor to 3.3V I/O power
3	GPIO3	IO	REG9EH[7]	GPIO 3
4	N_OE	I		Power output on/off switch GND: on； IPSOUT: off
5	GPIO2	IO	REG92H[2:0]	GPIO 2
6	N_VBUSEN	I		VBUS to IPSOUT Selection GND:IPSOUT select VBUS High: IPSOUT not select VBUS
7	VIN2	PI		DCDC2 input source
8	LX2	IO		Inductor Pin for DCDC2
9	PGND2	G		NMOS Ground for DCDC2
10	DCDC2	I		DC-DC2 feedback pin
11	LDO4	O		Output Pin of LDO4
12	LDO2	O		Output Pin of LDO2
13	LDO24IN	PI		Input to LDO2 and LDO4
14	VIN3	PI		DCDC3 input source
15	LX3	IO		Inductor Pin for DCDC3
16	PGND3	G		NMOS GND for DCDC3
17	DCDC3	I		Feedback to DCDC3
18	GPIO1	IO	REG93H[2:0]	GPIO 1
				ADC Input
19	GPIO0	IO	REG90H[2:0]	GPIO 0
				Low noise LDO/Switch
				ADC Input
20	EXTEN	O		External Power Enable
21	APS	PI		Internal Power Input
22	AGND	G		Analog Ground
23	BIAS	IO		External 200Kohm 1% resistor
24	VREF	O		Internal reference voltage
25	PWROK	O		Power Good Indication Output
26	VINT	PO		Internal logic power, 2.5V
27	LDO1SET	I		It sets the LDO1 default voltage.
28	LDO1	O		LDO1 output，for Host RTC block
29	DC3SET	I		It sets the DCDC3 default voltage

30	BACKUP	IO		Backup battery pin
31	VBUS	PI		USB VBUS input
32，33	ACIN	PI		Adapter input
34，35	IPSOUT	IO		Main Battery
36	CHGLED	O		charger status indication
37	TS	I		Battery Temperature sensor input or an external ADC input
38，39	BAT	PO		System power source
40	LDO3IN	O		LDO3 input source
41	LDO3	I		Output Pin of LDO3
42	BATSENSE	I		Current sense port1
43	CHSENSE	O		Current sense port2
44	VIN1	PI		DCDC1 input source
45	LX1	IO		Inductor Pin for DCDC1
46	PGND1	G		NMOS Ground for DCDC1
47	PWRON	I		Power On-Off key input， Internal 100k pull high to APS
48	IRQ/ WAKEUP	IO		IRQ output or wakeup
49	EP	G		Exposed Pad, need to be connected to system ground

8. Functional Block Diagram



9.Control and Operation

When AXP203 works, SCK/SDA pin of TWSI interface are pulled up to the system IO power, so Host can conduct flexible monitoring and adjustment for AXP203 operation via this interface.

NOTE:

- ✧ The " host " refers to the main processor of application system.
- ✧ The following " external power " includes ACIN and VBUS inputs.

9.1. Power On/Off and Reset

Power Enable Key (PEK)

A key can be connected between the PWRON pin of AXP203 and the GND to be an independent Power Enable Key (PEK) or Sleep/Wakeup Key. AXP203 can automatically identify the " long-press " and " short-press " of the key and then act accordingly.

Several Startup Sources

1. ACIN, BUS, and battery input
2. N_OE from high to low
3. PEK

Power On

The system can be started up in three ways:

When N_OE is low, AXP203 will be automatically powered on if satisfactory main power (ACIN or VBUS exceeds 3.8V, or the battery voltage is higher than shutdown voltage) is plugged in. (Whether or not AXP203 will automatically startup in external power presence can be modified accordingly.)

However, when N_OE is low and the system is shutdown, startup should be conducted through PEK. AXP203 can be powered on through PEK (the press time is longer than " ONLEVEL "). In practice, the alarm output signal of Host can be connected to PWRON as well—when parallel connected to PEK, valid Alarm signal (low level) can achieve the same result of pressing PEK and enables AXP203 startup,.

When external powers or batteries are available, N_OE changing from high to low can also bring about AXP203 startup.

After startup, DC-DC and LDO will be soft boot in preset timing sequence. After the boot, related power will be enabled / disabled via TWSI by Host.

Power Off

When the PEK long-press time is longer than IRQLEVEL, Host can write " 1 " to REG32H[7] register in PEK

interrupt service routine to inform AXP203 to shutdown, in which case all other power inputs except LDO1are disabled.

AXP203 will automatically shutdown in following cases:

(1) Under-voltage protection for low input voltage;
(2) overload protection for low voltage output due to overload;
(3) overvoltage protection for high voltage input (See the “Power Path Management” section for details);
(4) When N_OE changes from low to high, and the waiting time exceeds the preset time (2S by default);
(5) When the press time of PEK is longer than OFFLEVEL (6S by default), system will automatically disable all other output except LDO1(Reset key can be omitted).

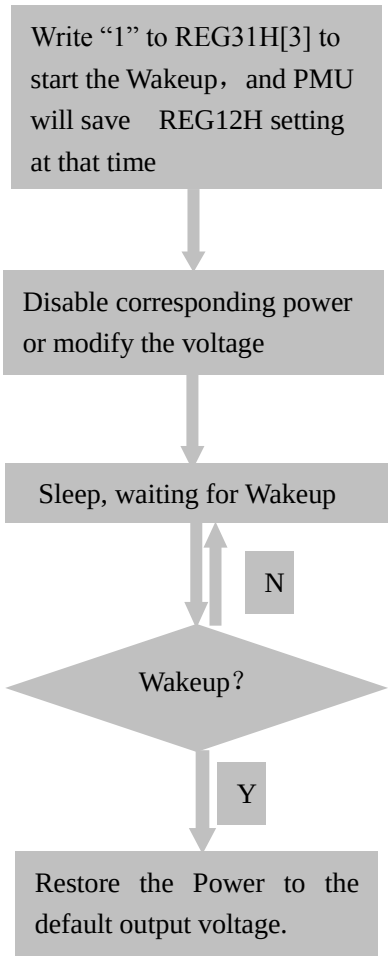
The automatic protection mechanism of AXP203 can protect the whole system by preventing irreversible damage to the power-supplied devices due to application system abnormality.

Sleep and Wakeup

When the running system needs to enter Sleep mode, one or more power outputs are disabled or have voltage modified, in that case, REG31H[3] can be used to decide whether to have the Wakeup triggered by PEK key signal, or the rising and/or falling edge of GPIO0、GPIO1、GPIO2、GPIO3 (To be the rising or falling edge, or both can be programmed by REG90H[7:6]、REG92H[7:6]、REG93H[7:6] and REG95H[7:6]), so that the output voltage can be restored to the default state by PMU and all disabled or modified power can be enabled in regulated sequence.

NOTE: PEK IRQ（REG42H[1]）、GPIO0 INPUT Edge IRQ（REG44H[0]）、GPIO1 INPUT Edge IRQ（REG44H[1]）、GPIO2 INPUT Edge IRQ（REG44H[2]）、GPIO3 INPUT Edge IR（REG44H[3]）should be “Enable” to notify the processor to exit Sleep Mode via IRQ PIN.

The control process in Sleep and Wakeup Modes is shown below.



System Reset and Output Monitoring (PWROK)

The PWROK in AXP203 can be used as reset signal of application system. During AXP203 startup, PWROK outputs low level, which will then be pulled high to startup and reset the system after each output voltage reaches the regulated value.

When application system works normally, AXP203 will be always monitoring the voltage and load status. If overload or under-voltage occurs, the PWROK will instantly output low level to reset the system and prevent malfunction or data errors.

9.2. Power Path Management (IPS)

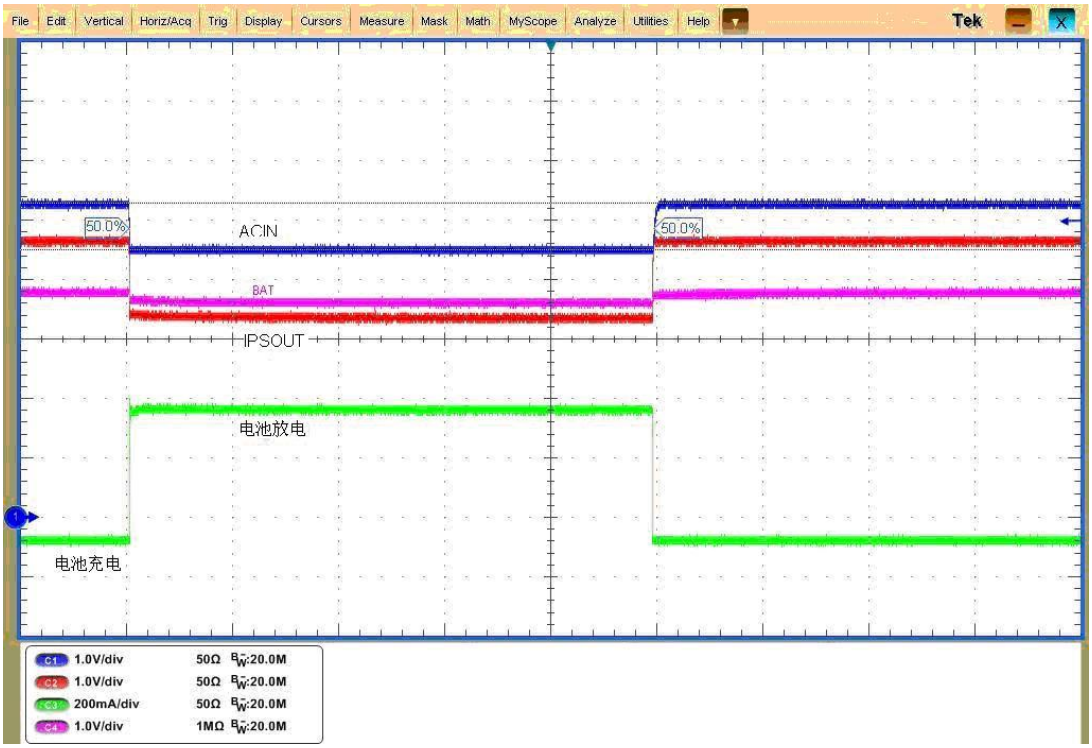
Power input of AXP203 may come from Li-battery, USB VBUS input, external power ACIN (such as AC adapter). IPS can select proper power allotting method according to external power and Li-battery status.

- ✧ If only Li-battery is available, and no external power input, Li-battery is used for power input;
- ✧ If external power is available (VBUS or ACIN), it is preferred in power supply;
- ✧ If Li-battery is available, it is instantly selected for power supply as soon as external power is removed;
- ✧ When both VBUS and ACIN are available, ACIN is preferred, and Li-battery is charging;
- ✧ And if in the above case, ACIN cannot provide enough drive ability, VBUS should be enabled properly to

achieve ACIN/VBUS common power supply;

✧ And if the drive capacity is still insufficient, charge current will be reduced to zero, and batteries are used for power supply;

Therefore, compatibility of the system with external powers of different drive ability can be dramatically improved, and no special customized adapters are required to be provided on the part of manufacturers.
Please refer to the following diagram.



As shown above, when ACIN provides insufficient load ability, IPSOUT voltage will fall, and BAT will change from charge to discharge to supply load current together with ACIN.
Host can set IPS parameters and read the feedback by visiting internal registers in AXP203 via TWIS.

Voltage-Limit/ Current-Limit Mode and Direct Mode

In order not to affect the USB communication, VBUS is always working in VBUS Voltage-Limit mode by default. In this mode, VBUS voltage remains above a configurable reference voltage VHOLD to meet the USB specification. The default VHOLD is 4.4V, adjustable in Reg30 H [5:3] register.

If the system has limit on current obtained from USB VBUS, a current-limit mode is provided (See REG30H [1] register), with 900mA/500mA/100mA (Reg30H [0]) selectable.

If the system just utilizes the USB for power supply rather than communication, or the USB power adapter is utilized, AXP203 can be set to “VBUS Direct Mode” by modifying register REG30H[6], and then AXP203 will give priority to the application power demand. When the drive ability of USB Host is insufficient or system power consumption is huge so that the VBUS voltage is lower than VHOLD, AXP203 will release IRQ to indicate the weak power supply ability of Host VBUS, which may affect USB communication, and then Host software will follow up.

AXP203’s Reaction to External Power Source Enabling

When external power is inserted, AXP203 can automatically detect it, judge whether the power is usable or not,

set the result in corresponding registers, and release IRQ to inform the Host at the same time.

The following table has listed the status bits and meanings of external power registers.

Register Status Bits	Description
REG00H[7]	Indicating the presence of external ACIN
REG00H[6]	Indicating whether the external ACIN is usable or not
REG00H[5]	Indicating the presence of external VBUS
REG00H[4]	Indicating whether the external VBUS is usable or not
REG00H[3]	Indicating whether the VBUS voltage is above V_{HOLD} when used
REG00H[1]	Indicating whether ACIN/VBUS short circuits on PCB or not
REG00H[0]	Indicating whether the system is triggered to startup by ACIN/VBUS or not

The status bit of "indicating whether the VBUS voltage is above V_{HOLD} or not when used" enables the Host to judge when it receives IRQ7(indicating weak supply ability)whether VBUS is pulled low by system load input or the external power itself is below V_{HOLD}, which may facilitate Host software to decide either to keep on working in Voltage-Limit mode or switch to Direct mode.

When to Select VBUS as Input Power

When to select VBUS as the input power is determined by N_VBUSEN and register REG30H[7]:

N_VBUSEN	REG30H[7]	Input Power	Description
Low	0	VBUS	Select if VBUS is valid and no ACIN is available
Low	1	VBUS	Select if VBUS is valid
High	1	VBUS	
High	0	ACIN/BAT	Not select VBUS

Under-Power Warning and Under-Power Protection (Automatic Shutdown)

AXP203 can set under-power warning voltage $V_{WARNING}$ and automatic shutdown voltage V_{OFF}, and then compare them with the system power. If the system power is found to be lower than $V_{WARNING,}$ IRQ19/IRQ20 will be released. If APS is lower than $V_{OFF,}$ AXP203 will automatically enter Shutdown Mode, and disable all other outputs except LDO1.

$V_{WARNING}$ has two set levels: LEVEL 1 and LEVEL 2, which have different indications in application. For example, LEVEL1 is used to indicate insufficient power while LEVEL 2 is used to indicate the oncoming shutdown.

The default values of $V_{WARNING}$ and V_{OFF} can be respectively set in registers REG3AH、REG3BH and REG31H[2:0].

Over-Voltage Protection

When the external power voltage exceeds 6.3V, AXP203 will release IRQ1⁄4 for indication. When the external power voltage exceeds 7V, AXP203 will automatically shutdown.

9.3. Adaptive PWM Charger

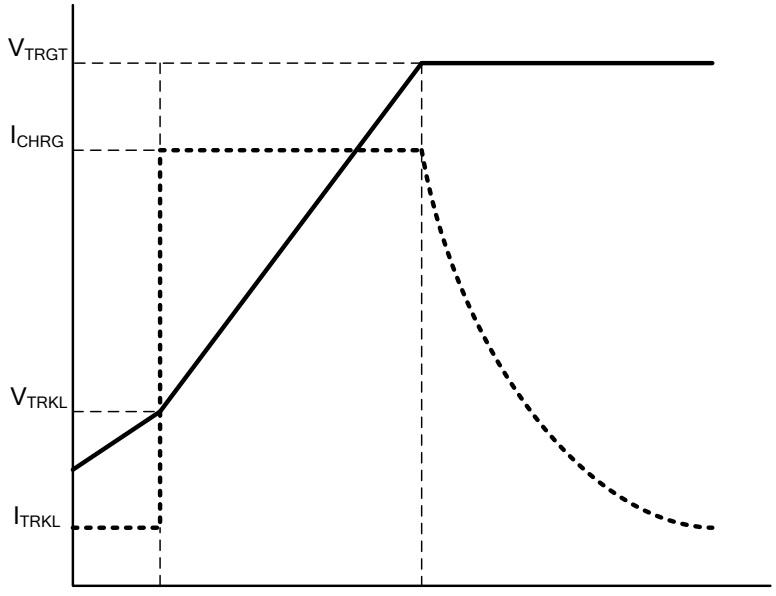
AXP203 integrates a constant current/voltage PWM charger to automatically control the charge cycle, with a built-in safety clock capable of automatic charge termination without processor intervention. This charger features automatic charge current scaling in accordance with the system power consumption, as well as battery detection, trickle charge and activation. In addition, the built-in temperature detection circuit can automatically decrease the charge current when the temperature is too high or too low.

Compared with traditional linear charge module, this PWM charger features dramatic efficiency increase and power consumption decrease in systems that require large power consumption and fast battery charging, and thus greatly improve the system temperature performance.

Adaptive Charge Startup

The default state of the charger is “Enable”. (It can be programmed via registers. Refer to register REG33H.) When external power is enabled, AXP203 will firstly judge whether it is chargeable. If the charger is suitable for the power, and the charge function is usable, AXP203 will automatically start the charge, and send IRQ to Host for indication. At the same time, GHGLED pin will output low level to drive external LED to indicate the charging state.

Charge Voltage/Current:



Two Symbolic Voltages

V_{TRGT}, charge target voltage. The V_{TRGT} is 4.2V by default, which can be set by register (Refer to“REG33H[6:5]”) . At the same time, AXP203 will automatically adjust the charge target voltage when external power voltage is low.

V_{RCH}， automatic recharge voltage. V_{RCH}=V_{TRGT}-0.1V。

Charge Current

The charge current is 500mAor 1200mA by default, which can be set by REG33H[3:0].

Charge Process

If the battery voltage is lower than 3.0V, the charger will automatically enter the pre-charge mode, with charge current be 1⁄10 of the preset value. If the battery voltage is still below 3.0V in 40 minutes (adjustable, see "REG34H"), charger will automatically enter the battery activate mode. Refer to "Battery Activate Mode" section for details.

Once the battery voltage exceeds 3.0V, the charger enters constant current mode. If the charge current is below 65% of the preset value, the system will release IRQ17 to indicate that "drive ability of external power is insufficient, as a result, the charge current is lower than the preset value, which may lead to longer charge time, so stronger power is preferred, or the power-consuming functions should be disabled to shorten the charge time."

When the battery voltage reaches the $V_{TRGT,}$ the charger will switch from the constant current mode to constant voltage mode, and the charge current will fall.

When the charge current is lower than 10% or 15% (adjustable, see register "REG33H") of the preset value, a charge cycle ends, and AXP203 will release IRQ18 while the CHGLED pin will stop indicating the charging state. When the battery voltage is below V_{RCH} again, the automatic charge will restart, and IRQ17 will be released.

In non-precharge mode, if the charge cycle doesn't end within 480 minutes (adjustable, refer to register "REG34H"), the charger will automatically enter the battery activate mode.

Battery Activate Mode

No matter it is from pre-charge mode or constant current mode to the battery activate mode (the timer expires), AXP203 will release IRQ10 in both cases to indicate that the battery may be damaged.

In battery activate mode, the charger always inputs relatively low current to batteries. In this case, if the battery voltage can reach V_{RCH}, AXP203 will exit activate mode and release IRQ11.

AXP203 will indicate whether the charger is in battery activate mode or not in register REG01H.

CHGLED

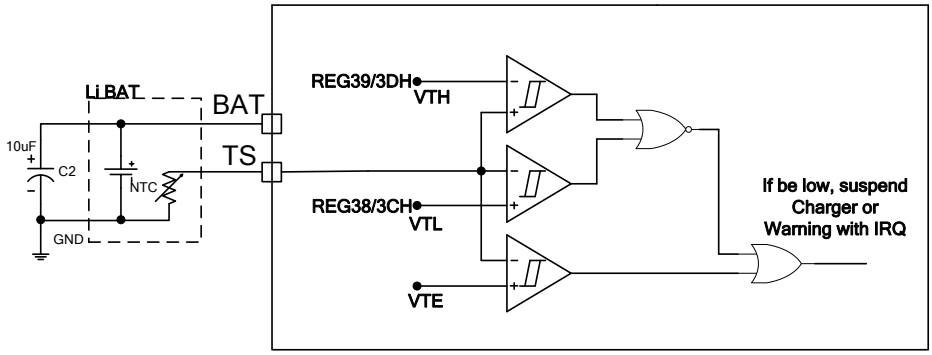
CHGLED pin is used to indicate charge state and warning. It has four states: charge, not charge, battery abnormality warning, and external power over-voltage warning. CHGLED is NMOS Open Drain output, so a LED can be directly driven by a current-limit resistor to show the four states. The following table has displayed its two operation modes.

REG34H[4]	Status	Reaction	Remark
0	Charge	Low Level	
	Not charge	High	

		Resistance	
	Battery Abnormal	1Hz flicker	The charger enters the battery activate mode, or the battery temperature is too high/low.
	Over-Voltage	4Hz flicker	External voltage input is too high.
1	Charge	1Hz flicker	
	Non-chargeable	High Resistance	No external power is available.
	Not charge	Low Level	
	Over-Voltage	4Hz Flicker	External voltage input is too high, or the battery temperature is too high/low.

Battery Temperature Detection

AXP203 can connect a temperature-sensitive resistor via the TS pin to monitor the battery temperature when the battery is charging or discharging. The diagram is shown below.



In the diagram above, VTH/VTL refer to the high temperature threshold and low temperature threshold, which is programmable via registers REG38H/39H/3CH/3DH respectively. VTE=0.2V. The temperature-sensitive resistor is suggested to choose the NTC temperature-sensitive resistor, which is 10Kohm and 1% accuracy at 25℃. AXP203 will send constant current via TS pin, and the current can be set as 20uA、40uA、60uA、and 80uA (See registerREG84H) to adapt to different NTC resistors. When the current goes through the temperature-sensitive resistor, a test voltage is generated, which will be measured by ADC, and compared with regulated value to release corresponding IRQ or suspend the charge.

If the resistance value of temperature-sensitive resistor is too high or too low, extra resistors can be serial or parallel connected to expand the detect extent.

If the battery is free from temperature-sensitive resistor, TS pin can be linked to the ground, and in that case, AXP203 will automatically disable the battery temperature monitoring function.

Battery Detection

AXP203 will automatically detect the battery presence, record the result in registers (refer to REG01H) and

release IRQ13, IRQ14.

The battery detection can be enabled and disabled by Host. (Refer to register REG32H.)

9.4. Backup Battery

AXP203 supports backup battery charge and discharge. When no main power (BAT/ACIN/VBUS) is available, LDO1will choose the backup battery to support the operation of some circuits, such as the system real-time clock, etc.

When there is a main power, REG35H[7] can be set to charge the backup battery, whose target voltage is 3.0V by default (adjustable via REG35H[6:5]) and charge current is 200uA by default (adjustable via REG35H[1:0]).

9.5. Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP203.

Output Path	Type	Default Voltage	Application Examples	Drive Ability
DCDC2	BUCK	Configurable	1.25Vcore	1600 mA
DCDC3	BUCK	Configurable	2.5Vddr	700 mA
LDO1	LDO	Configurable	RTC	30 mA
LDO2	LDO	Configurable	Analog/FM	200 mA
LDO3	LDO	Configurable	1.3V PLL	200 mA
LDO4	LDO	Configurable	1.8V HDMI	200 mA
LDO5	LDO	Configurable	Vmic	50 mA

AXP203 comes with two simultaneous step-down DC-DCs, five LDOs, as well as multiple timing and controlling methods. The work frequency of DC-DC is 1.5MHz by default, which is adjustable via registers. External small inductors and capacitors can be connected as well. In addition, both DC-DCs can be set in PWM mode or auto mode (automatically switchable according to the AXP203 load). See register REG80H.

DC-DC2/3

DCDC3 output voltage ranges from 0.7 V to 3.5V，and DCDC output voltage ranges from 0.7V to 2.275V，which can be programmed via registers.(Refer to register “REG23H 27H”).

DCDC2/3 output capacitor is recommended to use small ESR ceramic capacitors above 10uF X7R；when the output voltage is set above 2.5V，2.2uH inductors is recommended; when the output voltage is set under 2.5V，4.7uH inductors is recommended. Besides, the inductor saturation current should be larger than 50% of the largest demanded current in power circuitry.

The following is a list of recommended inductors and capacitors.

Inductors		
Module NO.	**Current Specification**	**DC Internal Resistance**
Murata LQH55PN2R2NR0	2100mA@2.2uH	30mOhm
Murata LQH55PN4R7NR0	1400mA@4.7uH	60mOhm
Murata LQH44PN2R2MP0	2000mA@2.2uH	49mOhm
Murata LQH44PN4R7MP0	1700mA@2.2uH	80mOhm
TDK VLF5010ST-2R2M2R3	2700mA@2.2uH	41mOhm
TDK VLF5014ST-4R7M1R7	1700mA@4.7uH	98mOhm
TDK SLF6045T-4R7N2R4-3PF	2400mA@4.7uH	27mOhm
Capacitors		
Module NO.	**Temperature Characteristics**	**Allowance**
TDK C2012X5R0J475K	X5R/X7R	10%@4.7uF
TDK C2012X5R0J106K	X5R/X7R	10%@10uF
Murata GRM31E71A475K	X7R	10%@4.7uF
Murata GRM21E71A106K	X7R	10%@10uF
Murata GRM31E71A106K	X7R	10%@10uF

LDO 1

LDO is always powered on to supply continuous power for application RTC. Its drive ability is 30mA.

LDO2/3/4

LDO2/4 output noise is as low as 18uVrms，and can be used to supply power for analog circuits of application system. LDO3can supply power for systems like SRAM or PLL. Their drive ability is 200mA。

LDO5

LDO5also features the low noise design, and its drive ability is 50mA。

Soft Start

All DC-DCs and LDOs support soft start to avoid the impact of dramatic current change on the input path in system boot stage.

Self-Diagnosis: Load Monitoring and Current-Limit Protection

All DC-DCs and LDOs support load monitoring and current-limit functions. When the load current exceeds its drive ability, each output voltage will decrease to protect the internal circuits. When the two DC-DCs output voltage is lower than 85% of the set voltage, AXP203 will automatically shutdown. At the same time, the system will record the detailed output voltage that has led to automatic shutdown (refer to register REG46H[5:2]) and release corresponding IRQ.

All DC-DCs do not require external Schottky diodes and resister divider feedback circuits. If a certain DC-DC is unnecessary in application, just float the corresponding LX pins.

9.6. Default Voltage/Timing Setting

AXP203 can set the default voltage and boot timing of each power.
Boot Timing includes eight levels, and the interval between each level can be set as 1、4、16 and 32mS.
Default voltage setting: each DC-DC/LDO setting ranges from the lowest voltage to the highest voltage.

LDO1SET PIN is used to set the initial voltage of LDO1:

LDO1SET	LDO1SET connected to GND	LDO1SET connected to VINT
LDO1Voltage	1.3V	3.3V

DC3SET PIN is used to set the initial voltage of DC-DC3:

DC3SET	DC3SET connected to GND	DC3SET connected to APS	DC3SET floating
DC-DC3 Voltage	1.8V	3.3V/2.5V	1.2V/1.5V

As for more details, please refer to “Default Configuration Instruction”.

9.7. Signal Capture

Ordinary battery monitor is to estimate the battery energy by measuring the battery voltage. However, the multiple 12-bit ADCs in AXP203 can measure battery voltage, as well as battery current and external power voltage and current. It also integrates battery charge and discharge coulomb counter. According to these data, Host is capable of accurately calculate the battery energy and other battery data, such as the system real-time consumption, remaining battery energy, battery charge progress, remaining battery using time and charge time, etc.

The Enable state controlling and sampling rate of each ADC can be set via registers REG82H、83H、84H. The sampling results will be saved in corresponding registers， and reference can be made to the ADC data in Register Instruction section. The input range of GPIO[1:0] can be set via register REG85H while register REG00H[2] is used to indicate the battery charge/discharge current directions.

Channel	000H	STEP	FFFH
Battery Voltage	0mV	1.1mV	4.5045V
Bat discharge current	0mA	0.5mA	4.095A
Bat charge current	0mA	0.5mA	4.095A
ACIN voltage	0mV	1.7mV	6.9615V
ACIN current	0mA	0.625mA	2.5594A
VBUS voltage	0mV	1.7mV	6.9615V
VBUS current	0mA	0.375mA	1.5356A
Internal temperature	-144.7℃	0.1℃	264.8℃
APS voltage	0mV	1.4mV	5.733V

TS pin input	0mV	0.8mV	3.276V
GPIO0	0/0.7V	0.5mV	2.0475/2.7475V
GPIO1	0/0.7V	0.5mV	2.0475/2.7475V

9.8. Multi-Function Pin Description

GPIO[3:0]:

Can act as GPIO[3:0], ADC Input（monitoring external signals）, and LDO, etc. Please refer to REG90H-96H Instruction for details.

CHGLED:

Features charge state indication, over-temperature/over-voltage warning, and GPO. Please refer to REG32H Instruction section for details.

9.9. Timer

AXP203 features a 7-bit internal timer, whose values can be programmed via register REG8AH[6:0]: when the REG8AH[6:0] is full 0, the timer is disabled; when REG8AH[6:0]=A, the timer counts from 0 to A, and REG8AH[7] is set to 1, and timer interrupt is released at the same time. Writing 1 to REG8AH[7] can clear the flag and restart the counting, while only clearing the interrupt doesn't restart the counting. The minimum time step of timer is one minute, and the timing range is 1~127 minutes.

9.10. Decryption

AXP203 has a decryption module. It can be enabled by writing the data to be decrypted into REG300-REG30F on the part of Host, and then write 1 to register REGB8H[1]. After the decryption, AXP203 will set REGB8[0] to 1, and at that time, decrypted data can be read by Host from REG31x. The status bit will be automatically cleared by AXP203 when decryption is restarted.

9.11. Host Interface and Interrupt (TWSI and IRQ)

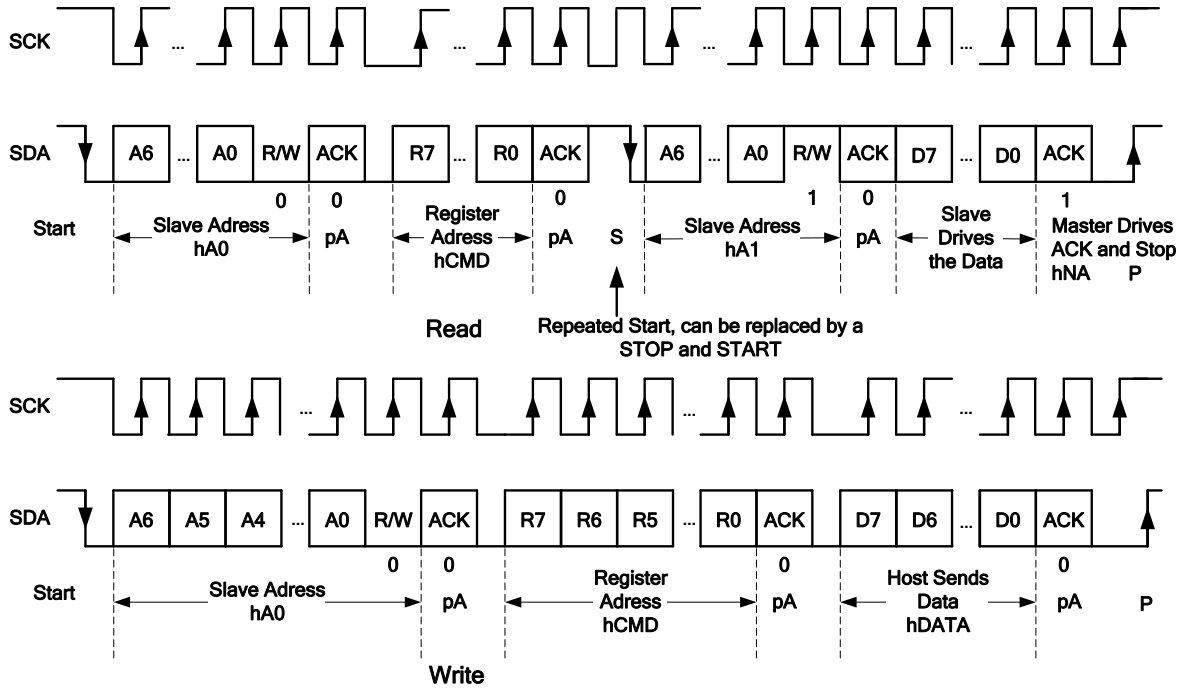


Figure 9-1. Single Read and Write

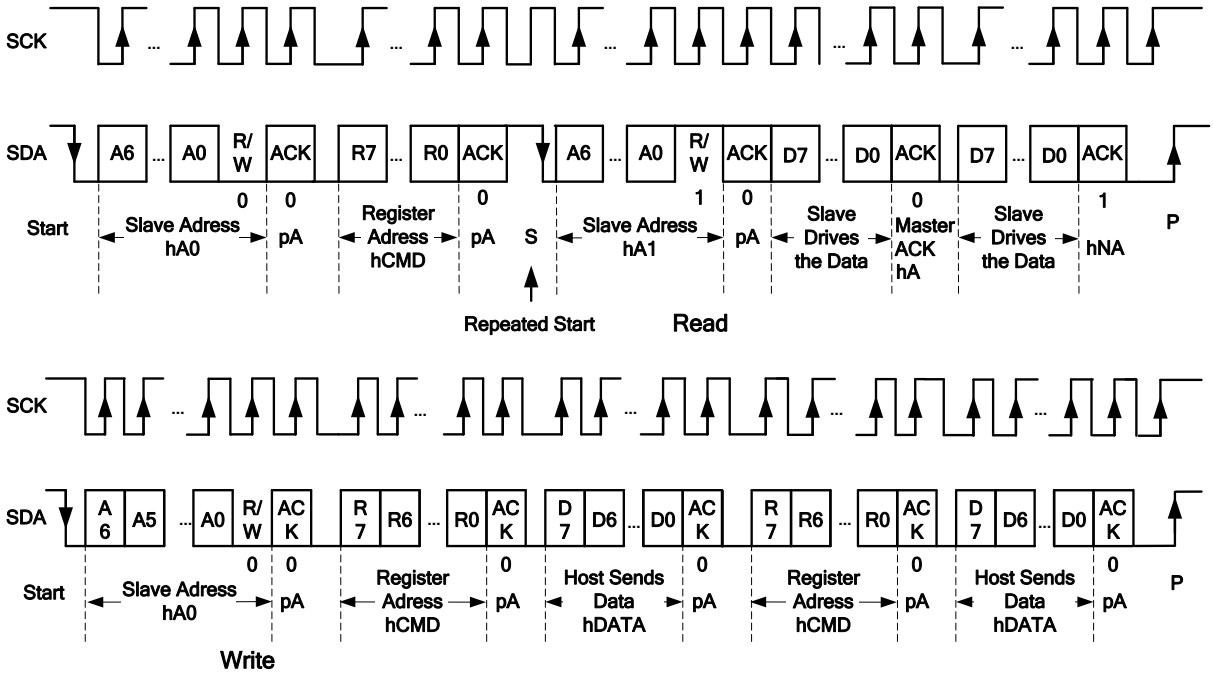


Figure 9-2. Multi Read and Write

Host can visit AXP203 registers via the TWSI interface, and the operation timing is listed above. Standard 100KHz or 400KHz frequency is supported, and the highest rate can reach 1.2KHz. In addition, multi read and write operation is supported, and the device addresses are 69H (READ) and 68H (WRITE).

When certain events occur, AXP203 will inform Host by pulling down the IRQ interrupt mechanism, and the interrupt state will be reserved in interrupt state registers (See registers REG48H, REG49H, REG4AH, REG4BH and

REG4CH). The interrupt can be cleared by writing 1 to corresponding state register bit. When there is no interrupt, IRQ output will be pulled high (51K resistance higher through the external). Each interrupt can be masked via interrupt control registers (Refer to registers REG40H, REG41H, REG42H, REG43H, and REG44H).

Site	Interrupt NO.	Description	Site	Interrupt NO.	Description
REG48H[7]	IRQ1	ACIN over-voltage	REG4AH[3]	IRQ20	DCDC3 under-voltage
REG48H[6]	IRQ2	ACIN connected	REG4AH[2]	Reserved	
REG48H[5]	IRQ3	ACIN removed	REG4AH[1]	IRQ22	PEK short-press
REG48H[4]	IRQ4	VBUS over-voltage	REG4AH[0]	IRQ23	PEK long-press
REG48H[3]	IRQ5	VBUS connected	REG4BH[7]	IRQ24	N_OE power-on
REG48H[2]	IRQ6	VBUS removed	REG4BH[6]	IRQ25	N_OE power-off
REG48H[1]	IRQ7	VBUS voltage is lower than V_{HOLD}	REG4BH[5]	IRQ26	VBUS valid
REG48H[0]	Reserved		REG4BH[4]	IRQ27	VBUS invalid
REG49H[7]	IRQ8	Battery connected	REG4BH[3]	IRQ28	VBUS Session Valid
REG49H[6]	IRQ9	Battery removed	REG4BH[2]	IRQ29	VBUS Session End
REG49H[5]	IRQ10	Enter the battery activate mode	REG4BH[1]	IRQ30	Low power warning LEVEL1
REG49H[4]	IRQ11	Exit the battery activate mode	REG4BH[0]	IRQ31	Low Power Warning LEVEL2
REG49H[3]	IRQ12	Be charging	REG4CH[7]	IRQ32	Timer interrupt
REG49H[2]	IRQ13	Charge finished	REG4CH[6]	IRQ33	PEK Rising edge
REG49H[1]	IRQ14	Battery over-temperature	REG4CH[5]	IRQ34	PEK Falling edge
REG49H[0]	IRQ15	Battery under-temperature	REG4CH[4]	Reserved	
REG4AH[7]	IRQ16	IC internal over-temperature	REG4CH[3]	IRQ35	GPIO3input edge trigger
REG4AH[6]	IRQ17	Insufficient charge current	REG4CH[2]	IRQ36	GPIO2 input edge trigger
REG4AH[5]	IRQ18	DCDC1under-voltage	REG4CH[1]	IRQ37	GPIO1 input edge trigger
REG4AH[4]	IRQ19	DCDC2 under-voltage	REG4CH[0]	IRQ38	GPIO0 input edge trigger

10. Registers

Group 1: Power Control

Address	Register Description	R/W	Default Value
00	Power status register	R	
01	Power mode/ charge state register	R	
02	OTG VBUS state register	R	
04-0F	Data cache register	R/W	00H
12	DC-DC2/3 & LDO2/3/4&EXTEN control register	R/W	XXH
23	DC-DC2 voltage setting register	R/W	XXH
25	DC-DC2/LDO3voltage slope parameter setting register	R/W	00H
27	DC-DC3voltage setting register	R/W	XXH
28	LDO2/3voltage setting register	R/W	XXH
30	VBUS-IPSOUT channel setting register	R/W	60H
31	V_{OFF} shutdown voltage setting register	R/W	X3H
32	Shutdown, battery detection, CHGLED control register	R/W	46H
33	Charge control register1	R/W	CXH
34	Charge control register2	R/W	41H
35	Backup battery charge control register	R/W	22H
36	PEK parameter control register	R/W	5DH
37	DCDC converter work frequency setting register	R/W	08H
38	battery charge low-temperature warning setting register	R/W	A5H
39	battery charge high-temperature warning setting register	R/W	1FH
3A	APS low-power Level1setting register	R/W	68H
3B	APS low-power Level2 setting register	R/W	5FH
3C	battery discharge low-temperature warning setting register	R/W	FCH
3D	battery discharge high-temperature warning setting register	R/W	16H
80	DCDC work mode setting register	R/W	E0H
82	ADC enable setting register1	R/W	83H
83	ADC enable setting register2	R/W	80H
84	ADC sample rate setting，TS pin control register	R/W	32H
85	GPIO [1:0] input range setting register	R/W	X0H
86	GPIO1 ADC IRQ rising edge threshold setting	R/W	FFH
87	GPIO1 ADC IRQ falling edge threshold setting	R/W	00H
8A	Timer control register	R/W	00H
8B	VBUS monitoring setting register	R/W	00H
8F	Over-temperature shutdown control register	R/W	01H

Group 2 GPIO control

Address	Register Description	R/W	Default Value
90	GPIO0 control register	R/W	07H
91	LDO5output voltage setting register	R/W	A0H
92	GPIO1 control register	R/W	07H
93	GPIO2 control register	R/W	07H
94	GPIO[2:0] signal status register	R/W	00H
95	GPIO3 control register	R/W	00H

Group3 Interrupt control

Address	Register Description	R/W	Default Value
40	IRQ enable control register1	R/W	D8H
41	IRQ enable control register2	R/W	FFH
42	IRQ enable control register3	R/W	3BH
43	IRQ enable control register4	R/W	C1H
44	IRQ enable control register5	R/W	00H
48	IRQ status register1	R/W	00H
49	IRQ status register2	R/W	00H
4A	IRQ status register3	R/W	00H
4B	IRQ status register4	R/W	00H
4C	IRQ status register5	R/W	00H

Group4 ADC data

Address	Register Description	R/W
56[7:0]	ACIN voltage ADC data high 8 bits	R
57[3:0]	ACIN voltage ADC data low 4 bits	R
58[7:0]	ACIN current ADC data high 8 bits	R
59[3:0]	ACIN current ADC data low 4 bits	R
5A[7:0]	VBUS voltage ADC data high 8 bits	R
5B[3:0]	VBUS voltage ADC data low 4 bits	R
5C[7:0]	VBUS current ADC data high 8 bits	R
5D[3:0]	VBUS current ADC data low 4 bits	R
5E[7:0]	AXP203 internal temperature monitoring ADC data high 8 bits	R
5F[3:0]	AXP203 internal temperature monitoring ADC data low 4 bits	R
62[7:0]	TS input ADC data high 8 bits，default monitoring battery temperature	R
63[3:0]	TS input ADC data low 4 bits，default monitoring battery temperature	R
64[7:0]	GPIO0 voltage ADC data high 8 bits	R
65[3:0]	GPIO0 voltage ADC data low 4 bits	R
66[7:0]	GPIO1 voltage ADC data high 8 bits	R

67[3:0]	GPIO1 voltage ADC data low 4 bits	R
70[7:0]	Battery instantaneous power high 8 bits	R
71[7:0]	Battery instantaneous power middle 8 bits	R
72[7:0]	Battery instantaneous power low 8 bits	R
78[7:0]	Battery voltage high 8 bits	R
79[3:0]	Battery voltage low 4 bits	R
7A[7:0]	Battery charge current high 8 bits	R
7B[3:0]	Battery charge current low 4 bits	R
7C[7:0]	Battery discharge current high 8 bits	R
7D[4:0]	Battery discharge current low 5 bits	R
7E[7:0]	System IPSOUT voltage high 8 bits	R
7F[3:0]	System IPSOUT voltage low 4 bits	R

Note: the battery power formula:

Pbat =2* register value * Voltage LSB * Current LSB/ 1000.

(Voltage LSB is 1.1mV; Current LSB is 0.5mA, and unit of calculation result is mW.)

Address	Register Description	R/W	Default Value
B0	battery charge coulomb counter data register[31:24]	R/W	00H
B1	battery charge coulomb counter data register[23:16]	R/W	00H
B2	battery charge coulomb counter data register[15:8]	R/W	00H
B3	battery charge coulomb counter data register[7:0]	R/W	00H
B4	battery discharge coulomb counter data register[31:24]	R/W	00H
B5	battery discharge coulomb counter data register[23:16]	R/W	00H
B6	battery discharge coulomb counter data register[15:8]	R/W	00H
B7	battery discharge coulomb counter data register[7:0]	R/W	00H
B8	Coulomb counter and encryption module control register	R/W	00H
B9	Power measurement result register	R/W	00H

Coulomb calculation formula:

C= 65536 * current LSB *（charge coulomb counter value - discharge coulomb counter value）/ 3600 / ADC sample rate.

（Refer to REG84H setting for ADC sample rate；the current LSB is 0.5mA；unit of the calculation result is mAh.）

10.1. REG 00H: Input Power Status

Bit	Description	R/W
7	ACIN presence indication 0:ACIN not exist；1:ACIN exists	R
6	Indicating whether ACIN is usable	R
5	VBUS presence indication 0:VBUS not exist； 1:VBUS exists	R

4	Indicating whether VBUS is usable	R
3	Indicating whether the VBUS voltage is above V_{HOLD} before used.	R
2	Indicating the battery current direction 0: the battery is discharging； 1: the battery is charging	R
1	Indicating whether ACIN and VBUS input short circuit on PCB	R
0	Indicating whether the boot source is ACIN or VBUS 0: Boot source isn't ACIN/VBUS； 1: Boot source is ACIN/VBUS.	R

10.2. REG 01H: Power Work Mode and Charge Status Indication

Bit	Description	R/W
7	Indicating whether AXP203 is over-temperature 0: not over-temperature； 1: over-temperature	R
6	Charge indication 0:not charge or charge finished； 1: in charging	R
5	Battery existence indication 0:no battery connected to AXP203； 1:battery already connected to AXP203	R
4	Reserved and unchangeable	R
3	Indicating whether the battery enters the activate mode 0: not enter the activate mode； 1: already entered the activate mode	R
2	Indicating whether the charging current is lower than the expected current 0:actual charging current is the same as expected current； 1: actual charging current is lower than expected current	R
1-0	Reserved and unchangeable	R

10.3. REG 02H: USB OTG VBUS Status Indication

Bit	Description	R/W
7-3	Reserved and unchangeable	
2	Indicating whether VBUS is valid or not， 1 means "valid"	R
1	Indicating whether VBUS Session A/B is valid， 1 means "valid"	R
0	Indicating Session End status， 1 means "valid"	R

10.4. REG 04-0FH: Data Cache

Note: As long as one of the external powers, batteries or backup batteries exists, this data will be reserved and free from the startup and shutdown influence.

10.5. REG 12H: Power Output Control

Default value: XXH

Bit	Description		R/W	Default Value
7	Reserved and unchangeable		RW	X
6	LDO3 enable and disable control	0: disable； 1: enable	RW	X
5	Reserved and unchangeable		RW	X
4	DC-DC2 enable and disable control	0: disable； 1:enable	RW	X
3	LDO4 enable and disable control		RW	X
2	LDO2 enable and disable control		RW	X
1	DC-DC3 enable and disable control		RW	X
0	EXTEN enable and disable control		RW	X

10.6. REG 23H: DC-DC2 Output Voltage Setting

Default Value: XXH

Bit	Description		R/W	Default Value
7-6	Reserved and unchangeable			
5-0	DC-DC2 output voltage setting	0.7-2.275V，25mV/step Vout=[0.7+(Bit5-0)*0.025]V	RW	X

10.7. REG 25H: DC-DC2/LDO3 Dynamic Voltage Scaling Parameter Setting

Default Value: 00H

Bit	Description		R/W	Default Value
7-4	Reserved and unchangeable			
3	LDO3 VRC ENABLING CONTROL 0: enable； 1: disable		RW	0
2	DC-DC2 VRC enabling control 0: enable； 1: disable		RW	0
1	LDO3 VRC voltage rising slope control	0: 25mV/15.625us=1.6mV/us 1: 25mV/31.250us=0.8mV/us	RW	0
0	DC-DC2 VRC voltage rising slope control	0: 25mV/15.625us=1.6mV/us 1: 25mV/31.250us=0.8mV/us	RW	0

10.8. REG 27H: DC-DC3 Output Voltage Setting

Default Value: XXH

Bit	Description		R/W	Default Value
7	Reserved and unchangeable			
6-0	DC-DC3 output voltage setting	0.7-3.5V， 25mV/step Vout=[0.7+(Bit6-0)*0.025]V	RW	X

10.9. REG 28H: LDO2/4 Output Voltage Setting

Default Value: XXH

Bit	Description		R/W	Default Value
7-4	LDO2 output voltage setting	1.8-3.3V， 100mV/step Vout=[1.8+(Bit7-4)*0.1]V	RW	X
3-0	LDO4 output voltage setting	1.25 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2.0 2.5 2.7 2.8 3.0 3.1 3.2 3.3	RW	X

10.10. REG 29H: LDO3 Output Voltage Setting

Default Value: XXH

Bit	Description		R/W	Default Value
7	LDO3 Mode select： 0：LDO mode，voltage can be set by [6:0] 1： enable/disable control mode，and voltage is determined by LDO3IN.		RW	0
6-0	LDO3 output voltage setting Bit6-Bit0	0.7-2.275V，25mV/step Vout=[0.7+(Bit6-0)*0.025]V	RW	X

10.11. REG 30H: VBUS-IPSOUT Channel Management

Default Value: 6XH

Bit	Description	R/W	Default Value
7	the VBUS-IPSOUT path select control signal when VBUS is usable 0: whether to enable the path is decided by N_VBUSEN pin 1:VBUS-IPSOUT can be enabled，regardless of the N_VBUSEN status	RW	0
6	VBUS V_{HOLD} voltage-limit control	RW	1

	0: not limit the voltage； 1: limit the voltage			
5-3	V_{HOLD} setting	V_{HOLD}= [4.0+(Bit5-3)*0.1]V	RW	100
2	Reserved and unchangeable			
1-0	VBUS current-limit selection when current-limit is enabled 00:900mA ; 01:500mA; 10:100mA; 11:not limit		RW	0

10.12. REG 31H: V_{OFF} Shutdown Voltage Setting

Default Value: X3H

Bit	Description		R/W	Default Value
7-4	Reserved and unchangeable			
3	PEK or GPIO edge wakeup function enable setting in Sleep mode 0：disable 1：enable This bit will be automatically cleared to 0 after writing，so “1 ”should be rewritten whenever enters the Sleep mode.			
2-0	V_{OFF} setting	V_{OFF}=[2.6+(Bit2-0)*0.1]V Default： 2.9V	RW	011

10.13. REG 32H: Shutdown Setting, Battery Detection and CHGLED Pin Control

Default Value: 46H

Bit	Description		R/W	Default Value
7	Shutdown Control Writing “1” to this bit will disable the AXP203 output.		RW	0
6	Battery monitoring function setting bit: 0: disable； 1: enable		RW	1
5-4	CHGLED pin function setting	00: high resistance 01: 25% 1Hz flicker 10: 25% 4Hz flicker 11: low level output	RW	00
3	CHGLED pin control setting	0: controlled by charging 1: controlled by register REG 32H[5:4]	RW	0
2	Output disable timing control	0: disable at the same time 1: contrary to the startup timing	RW	0
1-0	the delayed shutdown time of AXP203 after N_OE changes from low to high	00: 128mS； 01: 1S； 10: 2S； 11: 3S	RW	10

10.14. REG 33H: charging control 1

Default Value: CXH

Bit	Description	R/W	Default Value
7	Charging enable control bit 0: disable， 1:enable	RW	1
6-5	Charging target-voltage setting 00:4.1V； 01:4.15V； 10:4.2V； 11:4.36V	RW	10
4	Charging end-current setting 0: end when the charge current is lower than 10% of the set value 1: end when the charge current is lower than 15% of the set value	RW	0
3-0	Charge current setting I_{charge}= [300+(Bit3-0)*100] mA	RW	X

10.15. REG 34H: Charge Control 2

Default Value: 45H

Bit	Description		R/W	Default Value
7	Pre-charge timeout setting Bit1	00: 40 min； 01: 50min； 10: 60min； 11: 70min	RW	0
6	Pre-charge timeout setting Bit0		RW	1
5	Reserved			
4	CHGLED mode selection 0: always bright when charging 1: flicker when charging		RW	0
3-2	Reserved and unchangeable			
1-0	Constant-current mode timeout setting Bit1-0	00: 6Hours； 01: 8Hours； 10: 10Hours； 11: 12Hours	RW	01

10.16. REG 35H: Backup Battery Charge Control

Default Value: 22H

Bit	Description	R/W	Default Value
7	Backup battery charge enable control 0: disable；1: enable	RW	0
6-5	Backup battery charge target-voltage setting 00:3.1V；01:3.0V；10:3.6V；11:2.5V	RW	01
4-2	Reserved and unchangeable		

1-0	Backup battery charge current setting	00: 50uA； 01: 100uA； 10: 200uA； 11: 400uA	RW	10

10.17. REG 36H: PEK Key Parameters Setting

Default Value: 9DH

Bit	Description		R/W	Default Value
7-6	Startup time setting	00: 128mS； 01: 3S； 10: 1S； 11: 2S.	RW	01
5-4	Long-press time setting	00: 1S； 01: 1.5S； 10: 2S； 11: 2.5S.	RW	01
3	Automatic shutdown setting when the key press-time exceeds the shutdown time 0: disable； 1: enable		RW	1
2	PWROK signal delay after the power startup 0:8mS； 1:64mS		RW	1
1-0	Shutdown time setting	00: 4S； 01: 6S； 10: 8S； 11: 10S.	RW	01

10.18. REG 37H: DC-DC Work Frequency Setting

Default Value: 08H

Bit	Description		R/W	Default Value
7-4	Reserved and unchangeable			
3-0	DC-DC enable/disable frequency setting	Each level changes by 5%， Default Value1.5MHz F=[1+/- (Bit3-0)*5%)]*1.5MHz	RW	1000

10.19. REG 38H: $V_{LTF\text{-}charge}$ Battery Charge Low-temperature Threshold Setting

Default Value: A5H

Bit	Description		R/W	Default Value
7-0	Battery low-temperature threshold setting when the battery is charging, M	M*10H， when M=A5H, corresponding voltage is 2.112V； corresponding voltage ranges from 0V~3.264V	RW	A5H

$V_{LTF\text{-}charge}$ = M *10H * 0.0008V

10.20. REG 39H: $V_{HTF-charge}$ Battery Charge High-Temperature Threshold Setting

Default Value: 1FH

Bit	Description		R/W	Default Value
7-0	The battery high-temperature threshold setting when the battery is charging， N	N*10H，when N=1FH，the corresponding voltage is 0.397V； corresponding voltage ranges from 0V~3.264V	RW	1FH

$V_{HTF-charge}$ = N *10H * 0.0008V

10.21. REG 3AH: System IPSOUT Vwarning Level1

Default Value: 68H

Bit	Description	R/W	Default Value
7-0	System IPSOUT Vwarning Level1	RW	68H

10.22. REG 3BH: System IPSOUT Vwarning Level2

Default Value: 5FH

Bit	Description	R/W	Default Value
7-0	System IPSOUT Vwarning Level2	RW	5FH

Corresponding voltage setting of REG3AH and REG3BH equals to (supposing the register value is n):
Vwarning = 2.8672 + 1.4mV * n * 4

10.23. REG 3CH: $V_{LTF-discharge}$ Battery Discharging Low-Temperature Threshold Setting

Default Value: FCH

Bit	Description		R/W	Default Value
7-0	battery low-temperature threshold setting when the battery is discharging， M	M*10H， when M=FC, corresponding voltage is 3.226V； corresponding voltage ranges from 0V~3.264V	RW	FCH

$V_{LTF-discharge}$ = M *10H * 0.0008V

10.24. REG 3DH: $V_{HTF\text{-}discharge}$ Battery Discharging Threshold Setting

Default Value: 16H

Bit	Description		R/W	Default Value
7-0	The battery high-temperature threshold setting when the battery is discharging， N	N*10H，when N=16H，corresponding voltage is 0.282V；corresponding voltage ranges from 0V~3.264V	RW	16H

$V_{LTF\text{-}discharge}$ = N *10H * 0.0008V

10.25. REG 80H: DC-DC Work Mode Selection

Default Value: E0H

Bit	Description		R/W	Default Value
7-3	Reserved and unchangeable			
2	DC-DC2 work mode control	0:PFM/PWM automatic switching	RW	0
1	DC-DC3 work mode control	1: fixed PWM	RW	0
0	Reserved and unchangeable			

10.26. REG 82H: ADC Enable 1

Default Value: 83H

Bit	Description		R/W	Default Value
7	Battery voltage ADC enable	0: disable， 1: enable	RW	1
6	Battery current ADC enable		RW	0
5	ACIN voltage ADC enable		RW	0
4	ACIN current ADC enable		RW	0
3	VBUS voltage ADC enable		RW	0
2	VBUS current ADC enable		RW	0
1	APS voltage ADC enable		RW	1
0	TS pin ADC function enable		RW	1

10.27. REG 83H: ADC enable2

Default Value: 80H

Bit	Description	R/W	Default

				Value
7	AXP203 internal temperature monitoring ADC enable	0: disable， 1: enable	RW	1
6-4	Reserved and unchangeable			
3	GPIO0 ADC function enable	0: disable， 1: enable	RW	0
2	GPIO1 ADC function enable		RW	0
1-0	Reserved and unchangeable			

10.28. REG 84H: ADC Sample Rate Setting and TS Pin Control

Default Value: 32H

Bit	Description		R/W	Default Value
7-6	ADC sample rate setting	25×2^n The sample rate is 25， 50， 100， 200Hz respectively.	RW	0
5-4	TS pin output current setting: 00:20uA； 01:40uA； 10:60uA； 11:80uA		RW	11
3	Reserved and unchangeable			
2	TS pin function selection 0: battery temperature monitoring function， 1: external independent ADC input		RW	0
1-0	TS pin current output method setting	00: disable 01: current output when charging 10: input when the ADC is sampling，reducing the power consumption 11: always enable	RW RW	1 0

10.29. REG 85H: ADC Input Range

Default Value: X0H

Bit	Description		R/W	Default Value
7-2	Reserved and unchangeable			
1	GPIO1 ADC Input Range	0:0-2.0475V 1:0.7-2.7475V	RW	0
0	GPIO0 ADC Input Range		RW	0

10.30. REG 86H: GPIO1 ADC IRQ Rising Edge Threshold Setting

Default Value: FFH

Bit	Description	R/W	Default Value
7-0	One LSB is 8mV	RW	FF

10.31. REG 87H: GPIO1 ADC IRQ Falling Edge Threshold Setting

Default Value: 00H

Bit	Description	R/W	Default Value
7-0	One LSB is 8mV	RW	00

10.32. REG 8AH: Timer Control

Default Value: 00H

Bit	Description	R/W	Default Value
7	The timer is timeout Write “1” to clear the status.	RW	0
6-0	Set the time， unit: minute Write full 0 to shutdown the timer.	RW	0000000

10.33. REG 8BH: VBUS Pin Detection and SRP Function Control

Default Value: 00H

Bit	Description	R/W	Default Value
7-6	Reserved and unchangeable		
5-4	VBUS valid voltage setting 00:4.0V； 01:4.15V； 10:4.45V； 11:4.55V	RW	00
3	VBUS Valid detect function setting: 0: disable，1: enable	RW	0
2	VBUS Session detect function setting: 0: disable，1: enable	RW	0
1	Discharge VBUS discharge function setting 0: to disable the VBUS discharge resistance；1: to enable the VBUS discharge resistance	RW	0
0	Charge VBUS charge function setting 0: disable the VBUS charge resistance； 1: enable the VBUS charge resistance and charge the VBUS	RW	0

10.34. REG 8FH: Function Setting, Over-temperature Shutdown, etc.

Default Value: 21H

Bit	Description	R/W	Default Value
7-3	Reserved and unchangeable	RW	0
2	AXP203 internal over-temperature shutdown setting 0: not shutdown； 1: shutdown	RW	0
1-0	Reserved and unchangeable		

10.35. REG 90H: GPIO0 function Setting

Default Value: 07H

Bit	Description		R/W	Default Value
7	GPIO0 rising edge IRQ or Wakeup function	0：disable 1：enable	RW	0
6	GPIO0 falling edge IRQ or Wakeup function		RW	0
5-3	Reserved and unchangeable		RW	0
2	GPIO0 pin function setting Bit 2-0	000: output low 001: output high（3.3V） 010: general input function 011: low noise LDO5 100:ADC input 1XX: floating	RW	1
1			RW	1
0			RW	1

10.36. REG 91H: LDO5 Output Voltage and EXTEN/GPIO Output High Level Setting

Default Value: A5H

Bit	Description	R/W	Default Value
7-4	LDO5 output voltage setting Vout=[1.8 +(Bit7-4）*0.1]V； defalt=1.8+10*0.1=2.8V	RW	1010
3	Reserved and unchangeable		
2-0	EXTEN and GPIO[1:0] output high level setting 000:1.8V;001:2.5V;010:2.8V;011:3.0V;100:3.1V;101:3.3V;110:3.4V;111:3.5V	RW	101

10.37. REG 92H: GPIO1 Function Setting

Default Value: 07H

Bit	Description		R/W	Default Value
7	GPIO1 rising edge IRQ or Wakeup function	0：disable 1：enable	RW	0
6	GPIO1 rising edge IRQ or Wakeup function		RW	0
5-3	Reserved and unchangeable		RW	0
2-0	GPIO1 pin function setting	000: output low 001: output high（3.3V） 010: general input function 011: low noise LDO 100:ADC input 1XX: floating	RW	111

10.38. REG 93H: GPIO2 Function Setting

Default Value: 07H

Bit	Description		R/W	Default Value
7	GPIO2 rising edge IRQ or Wakeup function	0：disable 1：enable	RW	0
6	GPIO2 falling edge IRQ or Wakeup function		RW	0
5-3	Reserved and unchangeable		RW	0
2-0	GPIO2 pin function setting	000: output low 001: floating 010: general input function XXX: floating	RW	111

10.39. REG 94H: GPIO [2:0] Signal Status Setting and Monitoring

Default Value: 00H

Bit	Description		R/W	Default Value
7	Reserved and unchangeable		R	
6	GPIO2 input status	0: input low level 1: input high level	R	
5	GPIO1 input status		R	

4	GPIO0 input status		R	
3-0	Reserved and unchangeable			

10.40. REG 95H: GPIO 3 Setting

Default Value: 00H

Bit	Description		R/W	Default Value
7	GPIO3 rising edge IRQ or Wakeup function	0：disable 1：enable	RW	0
6	GPIO3 falling edge IRQ or Wakeup function		RW	0
5-3	Reserved and unchangeable			
2	GPIO3 function setting	0：NMOS Open Drain output 1：number input function	RW	0
1	GPIO3 output status	0: output low level，NMOS enable 1: floating，NMOS disable	RW	1
0	GPIO3 input status	0: input high level 1: input low level	R	

10.41. REG 40H and 48H: IRQ enable1 and IRQ Status 1

IRQ enable1 and REG40H：Default Value: D8H

Bit	Description	R/W	Default Value
7	ACIN over-voltage, IRQ enable	RW	1
6	ACIN connected, IRQ enable	RW	1
5	ACIN removed, IRQ enable	RW	0
4	VBUS over-voltage, IRQ enable	RW	1
3	VBUS connected, IRQ enable	RW	1
2	VBUS removed, IRQ enable	RW	0
1	VBUS is available, but lower than $V_{HOLD,}$ IRQ enable	RW	0
0	Reserved and unchangeable	RW	0

IRQ status 1，REG48H：Default Value: 00H

Bit	Description	R/W	Default Value
7-0	The meaning of status bit respectively corresponds to each bit of 40H； For example：Bit7 is ACIN over-voltage IRQ status bit	RW	0

10.42. REG 41H and 49H: IRQ enable2 and IRQ Status2

IRQ enable2，REG41H：Default Value: FFH

Bit	Description	R/W	Default Value
7	Battery connected, IRQ enable	RW	1
6	Battery removed, IRQ enable	RW	1
5	Battery activate mode, IRQ enable	RW	1
4	Exit battery activate mode, IRQ enable	RW	1
3	Be charging, IRQ enable	RW	1
2	Charge finished, IRQ enable	RW	1
1	Battery over-temperature, IRQ enable	RW	1
0	Battery low-temperature, IRQ enable	RW	1

IRQ status 2，REG49H：Default Value: 00H

Bit	Description	R/W	Default Value
7-0	Meaning of the Status bit respectively corresponds to each bit of 41H.	RW	0

10.43. REG 42H and 4AH: IRQ enable3 and IRQ Status 3

IRQ enable3，REG42H：Default Value: 03H

Bit	Description	R/W	Default Value
7	AXP203 internal over-temperature, IRQ enable	RW	0
6	Charge current is lower than the set current, IRQ enable	RW	0
5	Reserved and unchangeable		
4	DC-DC2 output voltage is lower than the set value, IRQ enable	RW	0
3	DC-DC3output voltage is lower than the set value, IRQ enable	RW	0
2	LDO3output voltage is lower than the set value, IRQ enable		
1	PEK short press, IRQ enable	RW	1
0	PEK long press, IRQ enable	RW	1

IRQ Status 3，REG4AH：Default Value: 00H

Bit	Description	R/W	Default Value
7-0	Meaning of the Status bit respectively corresponds to each bit of 42H.	RW	0

10.44. REG 43H and 4BH: IRQ enable4 and IRQ Status 4

IRQ enable4，REG43H：Default Value: 01H

Bit	Description	R/W	Default Value
7	N_OE startup, IRQ enable	RW	0
6	N_OE shutdown, IRQ enable	RW	0
5	VBUS valid, IRQ enable	RW	0
4	VBUS invalid, IRQ enable	RW	0
3	VBUS Session A/B IRQ enable	RW	0
2	VBUS Session End IRQ enable	RW	0
1	APS low-voltage, IRQ enable（LEVEL1）	RW	0
0	APS low-voltage, IRQ enable（LEVEL2）	RW	1

IRQ status 4，REG4BH：Default Value: 00H

Bit	Description	R/W	Default Value
7-0	Meaning of the Status bit respectively corresponds to each bit of 43H.	RW	0

10.45. REG 44H and 4C: IRQ Enable 5 and IRQ Status 5

IRQenable5，REG44H，Default Value: 00H；

Bit	Description	R/W	Default Value
7	Timer timeout, IRQ enable	RW	0
6	PEK press rising edge, IRQ enable	RW	0
5	PEK press falling edge, IRQ enable	RW	0
4	Reserved and unchangeable	RW	0
3	GPIO3 input edge trigger, IRQ enable	RW	0
2	GPIO2input edge trigger, IRQ enable	RW	0
1	GPIO1input edge trigger or ADC input, IRQ enable	RW	0
0	GPIO0 input edge trigger, IRQ enable	RW	0

IRQ status 5，REG4CH：Default Value: 00H

Bit	Description	R/W	Default Value
7-0	Meaning of the Status bit respectively corresponds to each bit of 44H	RW	0

Note: Writing 1 to all IRQ status register bits will clear corresponding status.

10.46. REG B8H: Coulomb Counter Control

Default Value: 00H

Bit	Description	R/W	Default Value
7	coulomb counter enable/disable control	RW	0
6	Coulomb counter suspend control. Writing “1” to this bit will suspend the Coulomb counter, and this bit will be automatically cleared to 0 as well.	RW	0
5	Coulomb counter clear control. Writing “1” to this bit will clear the coulomb counter, and this bit will automatically be cleared to 0.	RW	0
4-2	Reserved and unchangeable	RW	0
1-0	Decrypt the start bit. Automatically clear to 0 after the decryption.	RW	0
0	Whether the decryption has finished or not 0：not finished 1：finished	RW	0

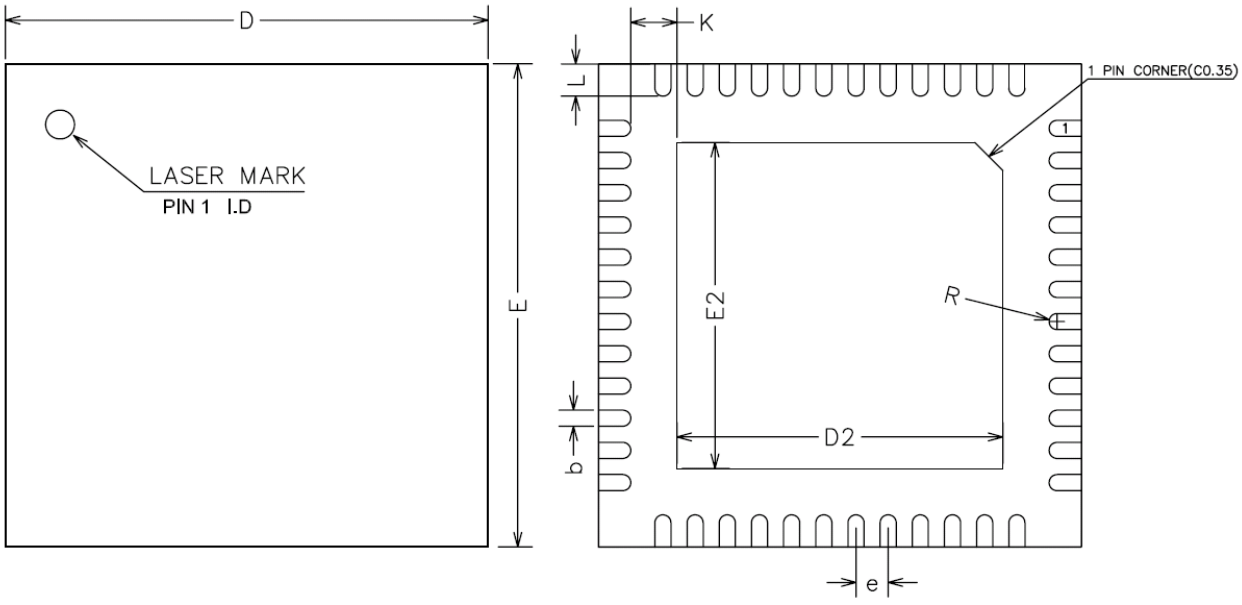
10.47. REG B9H: Power Measurement Result

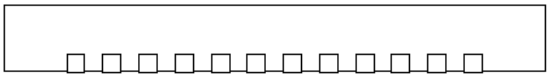
Default Value: 7FH

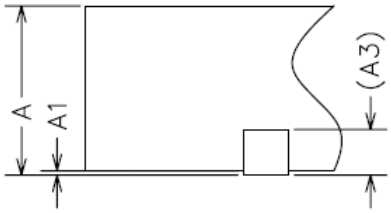
Bit	Description	R/W	Default Value
7	Measure system control 0：normal work mode 1：work suspension	RW	0
6-0	Measure result, percentage	R	7F

11. Package

AXP203：QFN48







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

