Kylie Choi

63A Girrahween Dr, Totara Vale
Auckland 0629, New Zealand
+64-021-143-6104 • kylie.c.8784@gmail.com

OBJECTIVE

A senior CIS Digital Design engineer &
A junior Web developer (Full-Stack)

EDUCATION

<Tasman International Academies>, Auckland, New Zealand, 2017
Level 7 of Multimedia
<Kongju National University>, Cheon-An, Korea, 2011
A Bachelor of electrical engineering (GPA: 4.08/4.50)

EXPERIENCE

<Siliconfile> Company, Bun-Dang, 2011.08.013 ~ 2016.01.15
Digital Design Department (for image sensor)

Timing generator of image sensors
• 2011 ~ 2012
(3M CIS FSI)
- Verilog simulation of CIS timing generator
- Static timing analysis using *Prime time*

• 2013
(13M STACK CIS TEST)
- BLC Digital design
- Verilog simulation of CIS timing generator
- Static timing analysis using *Prime time*

(2M CIS FSI & BSI)
- BLC Digital design
- Verilog simulation of CIS timing generator
- Static timing analysis using *Prime time*
- FPGA module TEST

• 2014
(2M COMPACT CIS FSI)
- BLC Digital design
- Verilog simulation of CIS timing generator
- Static timing analysis using *Prime time*
- FPGA module TEST

(13M CIS FSI)
- BLC Digital design
- Verilog simulation of CIS timing generator

- Static timing analysis using *Prime time*
- FPGA module TEST

● 2015 ~ 2016

(STUDY for OFFSET)

- Offset measurement as Temperature, Gain, Power for suitable dark offset

(8M CIS FSI)

- BLC Digital design
  (Random data generator for reducing noise; fixed pattern)
- Verilog simulation of CIS timing generator
- Static timing analysis using *Prime time*
- FPGA module TEST

<MARU LSI> Company, Su-Won, 2011.02.01 ~ 2012.07.31

Digital Design Department (for image sensor)

Timing generator of image sensors

● 2011/02 ~ 06

- Verilog design & simulation of CIS timing generator: *SVGA(WDR), SXGA(VISP,WDR(2))*
- Synthesis using *Design-Compiler* & Timing simulation
- Static timing analysis using *Prime time*

● 2011/07 ~ 12

- Verilog design & simulation of CIS timing generator: *VGA(VISP,WDR)*
- 32-bit 3-wire Serial interface module
- Clock divider module (1/2, 1/4, 1/8, 1/16)
- LCC Package in Board TEST & Debugging

● 2012/01 ~ 07

- Verilog design & simulation of timing generator: *X_RAY, ENCODER*
- 64-bit 3-wire Serial interface module
- Clock divider module (1/12, 1/24, 1/48, 1/96)
- LCC & CLCC & QFN Package in Board TEST & Debugging

FPGA verification board

● 2011/02 ~ 2012/05

- Board tuning & Pin mapping
- Alter pin assign of UCF

Etc.

● Draw up specifications

ENCODER

- Photo IC
- Signal Processor IC

EXPLANATION

The following sentences summarize by myself
Firstly, I am a morning person.
I start an early day. Because If start the day early, I make a what do to list so that I can have a better day with a routine. So, when I wake up, I think what I can do today. It helps speed things up.

Secondly, I am a friendly person.
I am a kind and nice as like my name.
If I meet with someone new, I can make people comfortable. Therefore, I get along well with many people who I meet on the first day. Also, I get along with customers.

Thirdly, I do not give up.
I do not give up easy. When I worked, I had a project. The deadline was too short. Most of the people said, "It is impossible to finish on time." However, I did not give up. Finally, I had finished the project before the deadline.

Consequently, I can work hard and quickly adapt. Also, I will work with big responsibility.

SKILL

<EDA Tool>

HW

- Synopsys: Design Compiler, Prime Time
- Timing Simulator: Modelsim, NC-SIM
- FPGA: ISE by Xilinx

SW

- Sublime Text
- Workbench

<Computer skill>

- MS-office
- Adobe-series

<Language skill>

- Verilog
- Perl
- C
- HTML
- CSS
- Java, Javascript, Jquery
- PHP

Thank you for reading my Career Description & Curriculum Vitae
I want to work and learn more at your company.