FR5082 Datasheet

Dual Mode Bluetooth Stereo Audio Speaker SOC

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DESCRIPTION

FR5082 is a family of SoC (system on chip) for rapid development of Bluetooth audio related products. With Freq-chip's innovational technology, FR5082 integrates RF, CODEC, PMU, Baseband, Cortex-M3 CPU and Audio DSP all in a single chip, which provides customer with:

1. competitive power consumption
2. outstanding wireless sound quality
3. remarkable Bluetooth range
4. low-cost BOM

FR5082 contains a Dual Mode Bluetooth V5.0 (BR/EDR/LE Mode) fully compliant system with Freq-chip designed Firmware and software stack in ROM. The firmware can be upgraded or customized in order to reduce the production risk and shorten the time to market.

New advanced technology is implemented like: noise suppression, multipoint (2 devices connected), true wireless.

FEATURES

- Extremely low power design
- Bluetooth Dual Mode 5.0 Specification Radio
  - RX sensitivity -90dBm @1Mbps for BR
  - RX sensitivity -92dBm @2Mbps for EDR
  - RX sensitivity -95dBm @1Mpbs for BLE
  - TX Power -20dBm ~ 8dBm
- Bluetooth Dual Mode 5.0 Specification Controller
  - BR/EDR 1Mbps/2Mbps/3Mbps support
  - LE 1Mbps support
- Dedicated Dual-Core processor architecture
  - 32-bit Cortex-M3 CPU inside for communication and application subsystem, frequency is 48MHz.
  - Floating point DSP for audio & other algorithm, frequency is 156MHz.
- Embedded 96KB+416KB SRAM.
- XIP Flash 1MB for Coretex-M3.
- Up to 104 x4 Mbps QSPI interface.
- High performance low power audio
  - 2-ch DAC SNR@96dB
  - 1-ch ADC SNR @84dB
  - 48kHz 24-bit I2S/PCM interfaces
  - Full band configurable EQ
- SoC Peripherals on
  - 4-ch PDM interface for Digital Mic
  - 2-ch I2C
  - Up to 2-ch QSPI
  - 2-ch UART
  - Configurable GPIO x22
  - SDC
  - USB-OTG
  - 6-ch PWM
  - Up to 4-ch external SAR-ADC
- Integrated power management unit
  - Dual DC-DC power supply (SISO)
  - On-chip LDO for digital logic & analog
  - Power switch for different power domain
  - Integrated battery charger supporting (up to 200 mA)
  - Single V-charger pin support Bidirectional Communication.
- Bluetooth Audio Application
  - DSP audio decoder support
  - Freq-chip BLsync technology for True Wireless Stereo & Voice Call.

TYPICAL APPLICATIONS

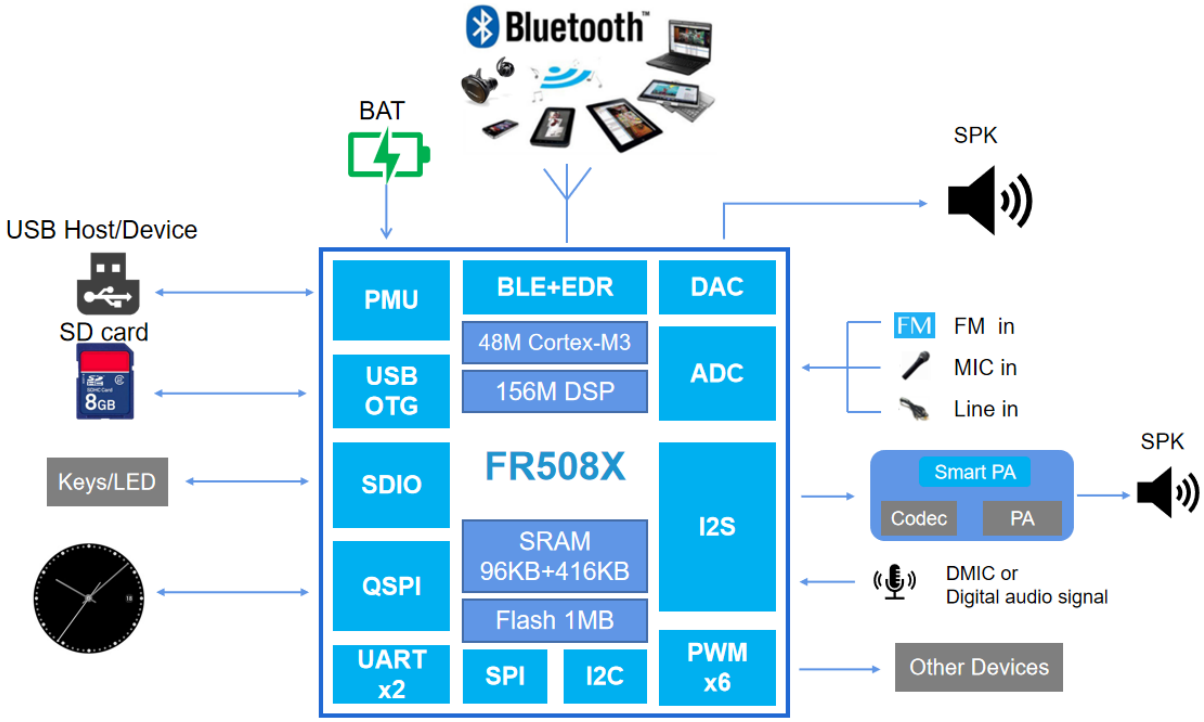
- Bluetooth stereo headsets and headphones
- Portable stereo speakers and speakerphones
- Bluetooth car audio unit
- Bluetooth dongles(USB, TV set, Game player, and Intercom dongle etc)
- Smart Watches
- Device of reception and transmission as one
- Human Interface Devices

ORDERING INFORMATION

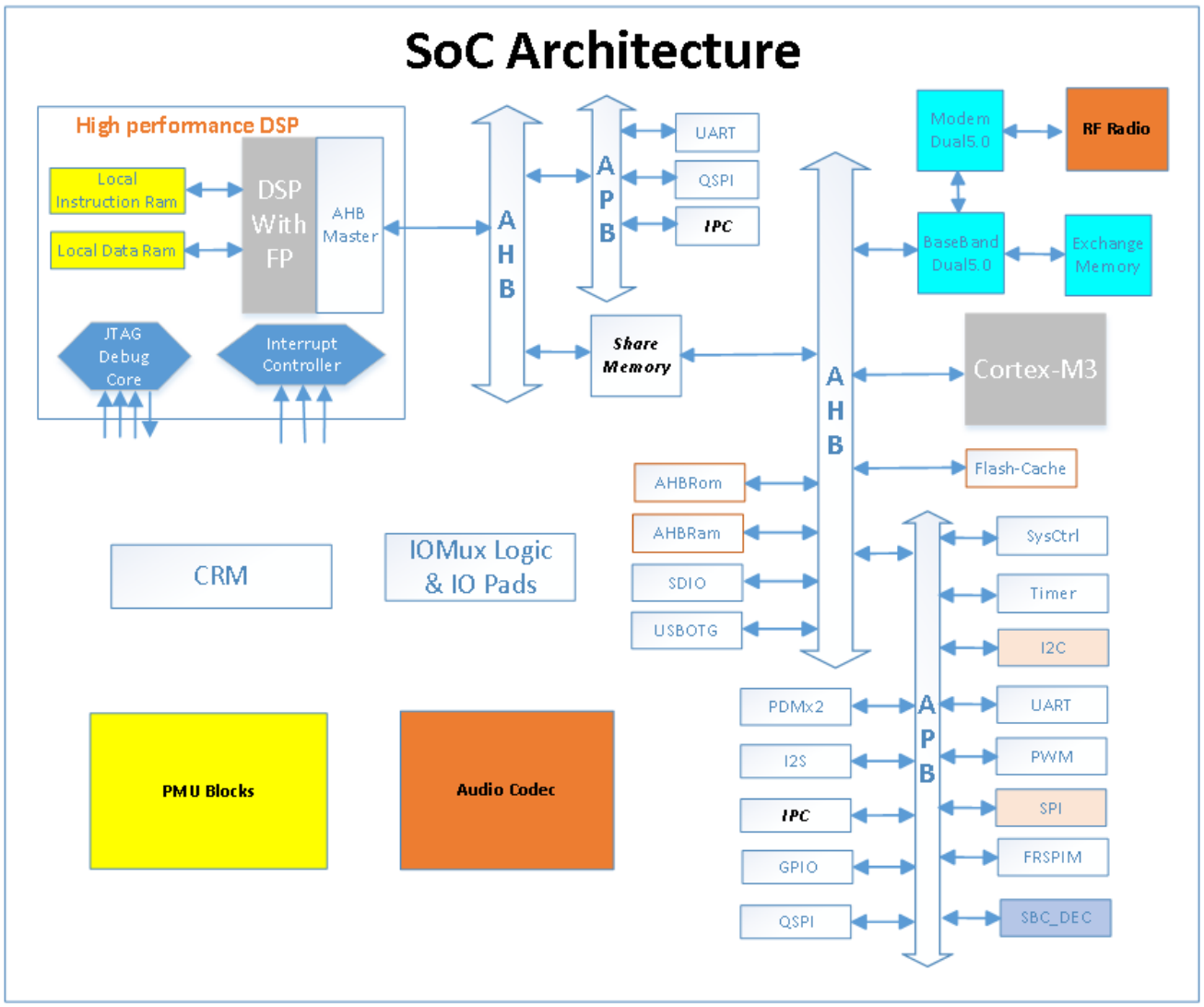
Order code	Temperature rang ℃	Package	Packing
FR5082DM	-40°C ~ +85°C	QFN40 6*4 (P0.4 T0.75)	Tape and reel
FR5082DS	-40°C ~ +85°C	QFN40 6*4 (P0.4 T0.75)	

1. Hardware Details

1.1 Application Diagram



1.2 Block Diagram



1.3 Bluetooth Radio

- On-chip balun (50Ω impedance in TX and RX modes)
- No external trimming is required in production
- Qualified to Bluetooth Dual Mode V5.0 BR/EDR/BLE specification

1.4 Bluetooth Transmitter

- Configurable RF transmit power -20dBm ~ 8dBm
- Class 2 and Class 3 support without need for external power amplifier or TX/RX switch

1.5 Bluetooth Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitized RSSI
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

1.6 Bluetooth Controller

- Embedded 32-bits low power processor with on-chip ROM and RAM
- Embedded 24Mhz Crystal Oscillator Driver
- Embedded low frequency RC Crystal Oscillator for Bluetooth sleep communication
- Processor in 16~48Mhz speed
- Support SCO/eSCO link
- Support Secure Simple Pairing
- Bluetooth 5.0 BR/EDR/BLE Mode support

1.7 Audio Interface

- Embedded 16-bit Audio CODEC
- DAC SNR 96dB, THD -86dB
- ADC SNR 84dB, THD -83dB
- DAC/ADC Support 8k/16k/44.1k/48kHz sample rate
- Full Band configurable EQ
- One analog MIC amplifier, build-in MIC bias generator
- Support 4-ch PDM with Digital microphones input
- One channel Stereo analog MUX
- Output earphone PA with 50mW output power

1.8 Physical Interfaces

- UART port for Debugging and AT Commands
- 1/2/4-bit SPI flash memory interface to support external SPI flash
- IIC interface to support external EEPROM or other devices (like FM Receiver)
- QSPI interface support up to 104x4Mbps data rate.
- Up to 22 general purpose IOs (5082DM has 22 IOs, 5082DS has 18 IOs)

1.9 Integrated Power Control and Regulation

- Embedded Power-On-Reset
- Support ONKEY (switch or long press) power on and power off logic
- Low power core voltage
- On-chip high efficiency switch-mode power supply, 2.5v to 4.3v input direct from battery and programmable output voltage
- On-chip Low Dropout (LDO) Linear Regulator for internal Digital, RF and Analog circuit.
- Power management features include software shutdown and hardware wake-up
- Power-on-reset cell detects low supply voltage

1.10 Battery Charger

- Lithium ion/Lithium polymer battery charger
- Embedded LVD(low voltage detect)
- Programmable charging current. Fast charging support up to 200mA with no external components
- Ultra low power leakage cost with charger plug in @standby mode.

1.11 Package

- QFN40 6*4 (P0.4 T0.75)

2. Solution Details

2.1 Embedded Bluetooth Protocols and Profiles

- Bluetooth Dual Mode V5.0 BR/EDR/BLE specification compliant
- Low level Bluetooth protocols embedded (LMP, L2CAP, RFCOMM, SDP, etc.)
- A2DP V1.3 and AVRCP V1.6 supported
- HFP V1.8 supported
- SPP V1.2 supported

2.2 Music Enhancements and Features

- Configurable full-band EQ for music/voice playback
- Embedded SBC hardware decoder

2.3 AEC/NS Features

- AEC (acoustic echo cancellation) up to 60dB
- Superior full-duplex
- Support one microphone mode, ease for application
- Support dual-microphone mode
- Acoustic echo tail length coverage: up to 64ms ~128ms
- Fast AGC control to improve dynamic range
- Noise suppression up to 20 dB

2.4 Additional Functionality

- Support Alarm Clock
- Support up to 454*454*24bits OLED panel with QSPI port

2.5 System Configuration and Upgrading

- Flexible configuration data (pskeys) and PC helper tools
- Auto reconnection (e.g. power-on or RF signal lost)
- Configurable Button events mapping to specific functions. (e.g. double press on PIO for last number redial)
- Configurable LED indications for states. (e.g. device connected state, pairing state)
- User-defined indication tones for events and ringtones
- Software Code Patch (including Firmware upgrading, bug-fix or customized codes)
- Support upgrading by UART or SPP over air
- XIP support for customer application

2.6 Solution Development Support

- FR5082 Reference Design Circuits and Documents
- Configuration Tool and Documents
- Indication Tone maker Tool
- Application Notes

3. RF Radio Characteristics

3.1 Enhanced Data Rate

3.1.1 Receiver Specifications

Description	Condition	Min	Typ	Max	Unit
Frequency range		2402	-	2480	MHz
Sensitivity with dirty off	π/4 DQPSK,BER < 0.01%	-	-92	-70	
	8PSK, BER <= 0.01%	-	-86	-70	dBm
Maximum received signal	π/4 DQPSK,BER < 0.01%	-20	0	-	dBm
	8PSK, BER <= 0.01%	-20	-2	-	dB
C/I co-channel selectivity	π/4 DQPSK,BER < 0.01%	-	10	13	dB
	8PSK, BER <= 0.01%	-	19	21	dB
C/I 1MHz adj. channel selectivity	π/4 DQPSK,BER < 0.01%	-	-10	0	dB
	8PSK, BER <= 0.01%	-	-1	5	dB
C/I 2MHz adj. channel selectivity	π/4 DQPSK,BER < 0.01%	-	-44	-30	dB
	8PSK, BER <= 0.01%	-	-25	-25	dB
C/I >=3MHz adj. channel selectivity	π/4 DQPSK,BER < 0.01%	-	-40	-40	dB
	8PSK, BER <= 0.01%	-	-41	-33	dB
C/I image channel selectivity	π/4 DQPSK,BER < 0.01%	-	-29	-7	dB
	8PSK, BER <= 0.01%	-	-19	0	dB
C/I image 1MHz adj. channel selectivity	π/4 DQPSK,BER < 0.01%	-	-34	-20	dB
	8PSK, BER <= 0.01%	-	-25	-13	dB

3.1.2 Transmitter Specifications

Description	Condition	Min	Typ	Max	Unit
Frequency range		2402	-	2480	MHz
Maximum transmit power	π/4 DQPSK	-	5	8	dBm
	8PSK	-	5	8	dBm
Relative transmit power	π/4 DQPSK	-4	-3	1	dB
	8PSK	-4	-3	1	dB
Freq. stability ω0	π/4 DQPSK	-10	-1	10	KHz
	8PSK	-10	-1	10	KHz
Freq. stability ω1	π/4 DQPSK	-75	11	75	KHz
	8PSK	-75	11	75	KHz
|ω0 + ω1|	π/4 DQPSK	-75	11	75	KHz
	8PSK	-75	11	75	KHz
RMS DEVM	π/4 DQPSK	-	5	20	%
	8PSK	-	4	13	%
99% DEVM	π/4 DQPSK	-	11	30	%
	8PSK	-	10	20	%
Peak DEVM	π/4 DQPSK	-	8	35	%
	8PSK	-	8	25	%
In-band spurious emission	π/4 DQPSK, ±1MHz offset	-	-36	-26	dBm
	8PSK, ±1MHz offset	-	-37	-26	dBm
	π/4 DQPSK, ±2MHz offset	-	-36	-20	dBm
	8PSK, ±2MHz offset	-	-35	-20	dBm
	π/4 DQPSK, ±3MHz offset	-	-42	-40	dBm
	8PSK, ±3MHz offset	-	-42	-40	dBm

3.2 LE 1M Data Rate

3.2.1 Receiver Specifications

Description	Condition	Min	Typ	Max	Unit
Frequency range		2402	-	2480	MHz
Receiver sensitivity	PER < 30.8%	-	-95	-89	dBm
Max. detectable input power	PER < 30.8%	-	0	-	dBm
C/I co-channel selectivity	PER < 30.8%	-	6	21	dB
C/I 1MHz adj. channel selectivity	PER < 30.8%	-	0	15	dB
C/I 2MHz adj. channel selectivity	PER < 30.8%	-	-22	-17	dB
C/I 3MHz adj. channel selectivity	PER < 30.8%	-	-45	-27	dB
C/I image channel selectivity	PER < 30.8%	-	-23	-9	dB
C/I image 1MHz adj. channel selectivity	PER < 30.8%	-	-22	-15	dB
Out-of-band blocking	30MHz ~ 2000MHz	-	-	-30	dBm
	2001MHz ~ 2399MHz	-	-	-35	dBm
	2501MHz ~ 3000MHz	-	-	-35	dBm
	3001MHz ~ 12.75GHz	-	-	-30	dBm

3.2.2 Transmitter Specifications

Description	Condition	Min	Typ	Max	Unit
Frequency range		2402	-	2480	MHz
Maximum transmit power		-20	8	10	dBm
Gain Step		0.5	1	2	dB
Modulation characteristic	Δf1avg	225	262	275	KHz
	Δf2max	185	222	-	KHz
	Δf1avg/ Δf2avg	0.8	0.88	-	
Carrier frequency offset & drift	Frequency offset	-150	±12	150	KHz
	Frequency drift	-50	±4	50	KHz
	Maximum drift rate	-20	±4	20	KHz/uS
In-band spurious emission	±2MHz offset	-	-42	-20	dBm
	±3MHz offset	-	-42	-30	dBm
	>±3MHz offset	-	-52	-30	dBm

4. Audio CODEC Characteristics

Digital to Analogue Converter (Stereo)					
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Resolution	-	-	-	20	Bits
Sampling frequency (Fs)*	The synchronized clock signal	8	-	48	kHz
SNR (Signal to Noise Ratio)	Fin=1kHz B/W=20Hz—20KHz A-Weighted THD_N<0.01% Fs(8K,16K,32K,44.1K,48K)	-	96	-	dB
Digital Gain	Digital Gain Resolution=1/48dB	-48	-	32	dB
Analogue Gain	Analog Gain Resolution = 3dB	0	-	-30	dB
Output voltage fulls-cale	AULDO_OUT=1.8V	-	900	-	mV
Stopband attenuation		65	-	-	dB
Analog to Digital Converter (Mono)					
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Resolution	-	-	-	16	Bits
Sampling frequency (Fs)*	The synchronized clock signal	8	-	48	kHz
Signal to Noise Ratio	A-weighted	-	79	-	dBFS
	W/O weighting	-	79	-	dBFS
Digital Gain	Digital Gain Resolution=1/48dB	-48	-	32	dB
Analogue Gain	Analog Gain Resolution = 3dB	0	-	30	dB
Microphone Bias					
Bias Voltage	MBVSEL=0	-	0.6*AU_BFB	-	V
	MBVSEL=1	-	0.9*AU_BFB	-	V
Bias Current Source	VMICBIAS within +/-3%	-	-	3	uA
Output Noise Voltage	1kHz to 20kHz	-	15	-	nV/sqrt(Hz)

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Continuous operation at or beyond these conditions may permanently damage the device.

Rating		Min	Max	Unit
Storage Temperature		-55	125	℃
Core Supply Voltage		0.9	1.3	V
I/O Voltage	IOLDO_OUT	1.8	3.3	V
Audio Voltage	AULDO_OUT(AU_BFB)	1.65	2.5	V
Supply Voltage	VBAT	2.5	4.3	V
	VCHG	4.75	5.25	V

5.2 IOLDO Characteristics

Parameter	Min	Typ	Max	Unit
Input voltage	2.5	3.7	4.3	V
Output voltage	1.8	2.5	3.3	V
Max Output current	-	120	-	mA
Ripple	-	25	-	mV

5.3 System DC-DC Characteristics

Parameter	Min	Typ	Max	Unit
Input voltage	2.5	3.7	4.3	V
Output voltage	1.2	1.4	1.6	V
Max Output current	80	-	-	mA
Switch frequency	-	2.5	-	MHz
PWM Mode Ripple	-	10	-	mV
PFM Mode Ripple	-	30	-	mV
Efficiency(PWM)	-	85	-	%
Efficiency(PFM)	-	85	-	%
Leakage current (Power down)	-	< 25	-	nA

5.4 Audio DC-DC Characteristics

Parameter	Min	Typ	Max	Unit
Input voltage	2.5	3.7	4.3	V
Output voltage	1.65	1.8	2.5	V
Max Output current	80	-	-	mA
Switch frequency	-	2.5	-	MHz
PWM Mode Ripple	-	10	-	mV
PFM Mode Ripple	-	30	-	mV
Efficiency (PWM)	-	85	-	%
Efficiency (PFM)	-	85	-	%
Leakage current (Power down)	-	< 15	-	nA

5.5 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range		-40	25	85	℃
Core Supply Voltage	/	0.9	1.2	1.3	V
I/O Voltage	IOLDO_OUT	1.8	2.5	3.3	V
Audio Voltage	AULDO_OUT(AU_BFB)	1.65	1.8	1.95	V
Supply Voltage	VBAT	2.5	3.7	4.3	V
Charge input voltage	VCHG	4.75	5	5.25	V

5.6 Power Consumption

Operation Mode	Average	Maximum	Unit
Bluetooth A2DP (SBC Audio)	<6.5	-	mA
Bluetooth ESCO +AEC/NS(Phone call)	<8	-	mA
Standby(500ms Sniff, 1 attempt, 0 timeout, 3.3V supply voltage)	<70	-	uA
Power off	<3	-	μA

5.7 Inductance

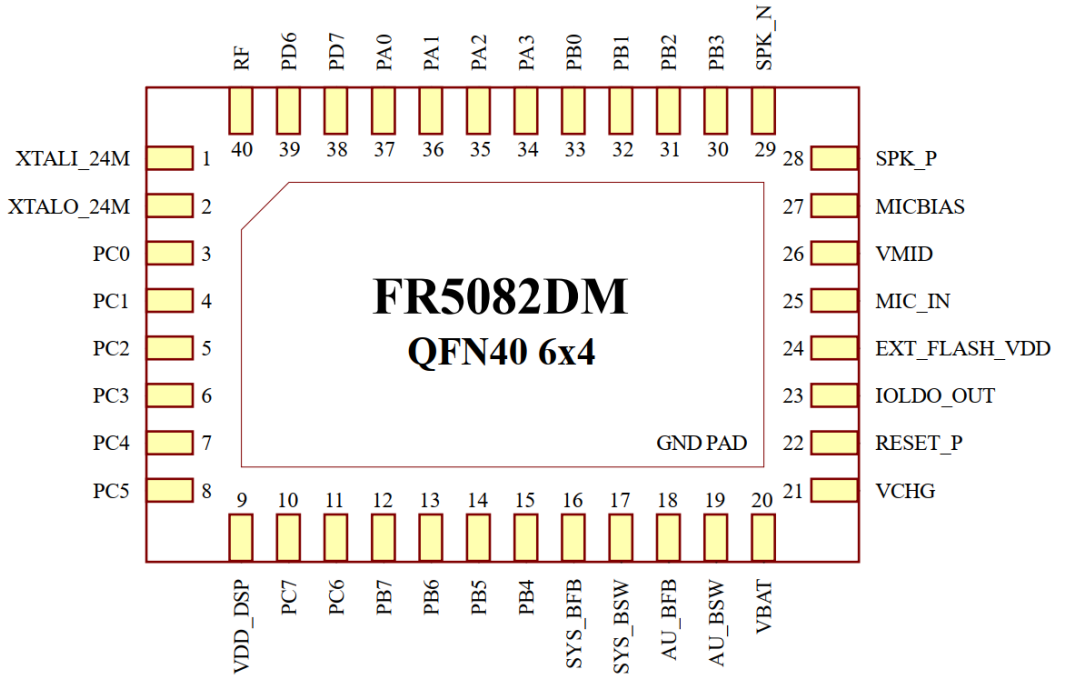
Parameter	Min	Typ	Max	Unit
Saturated Current	80	-	-	mA
Self Resonant Frequency	10	-	-	MHz
Direct Current Resistance	-	-	1K	ohm

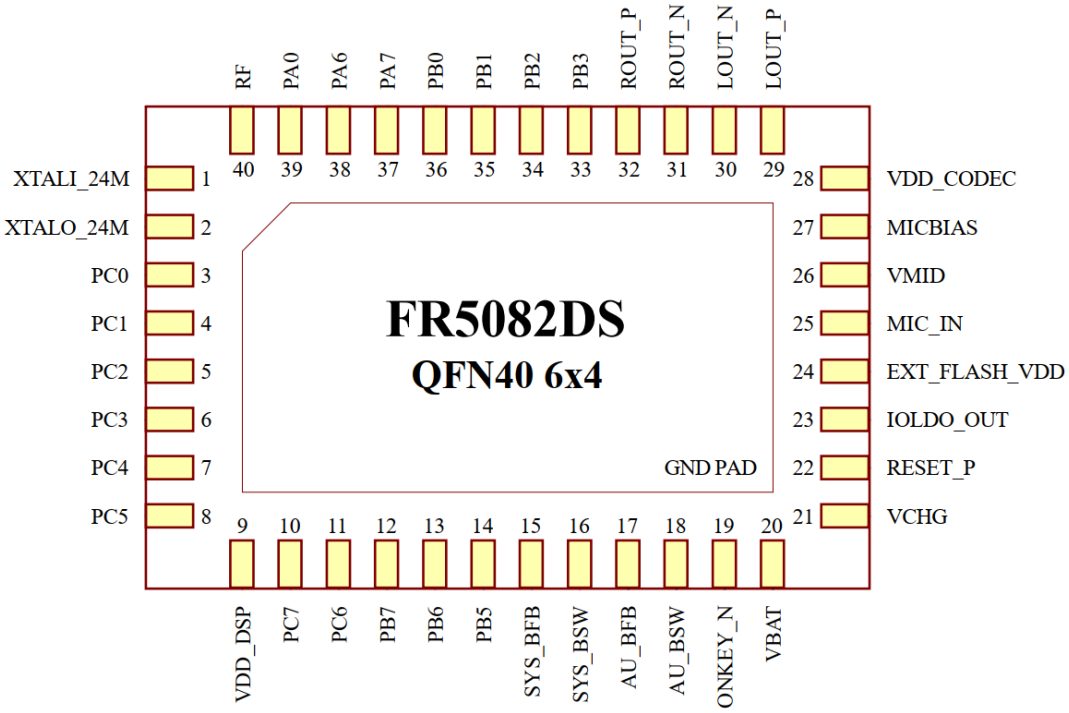
5.8 Crystal oscillator

Parameter	Min	Typ	Max	Unit
Clock Frequency	24	24	24	Mhz
CL Load capacitance	-	9	12	pF
Tolerance	-	+-10	-	ppm
Motional resistance	-	-	60	R
Shunt capacitance	-	-	2	pF

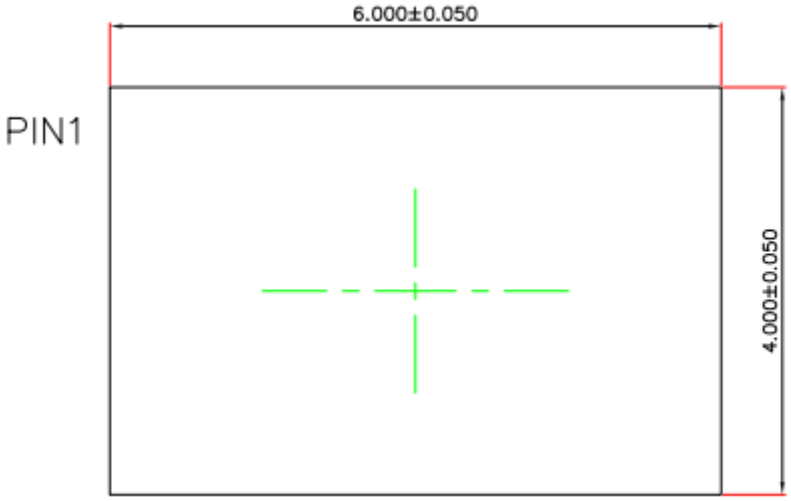
6. FR5082 QFN40 Package and Pin Information

6.1 Package

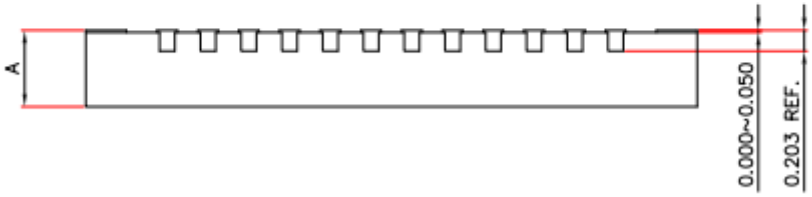




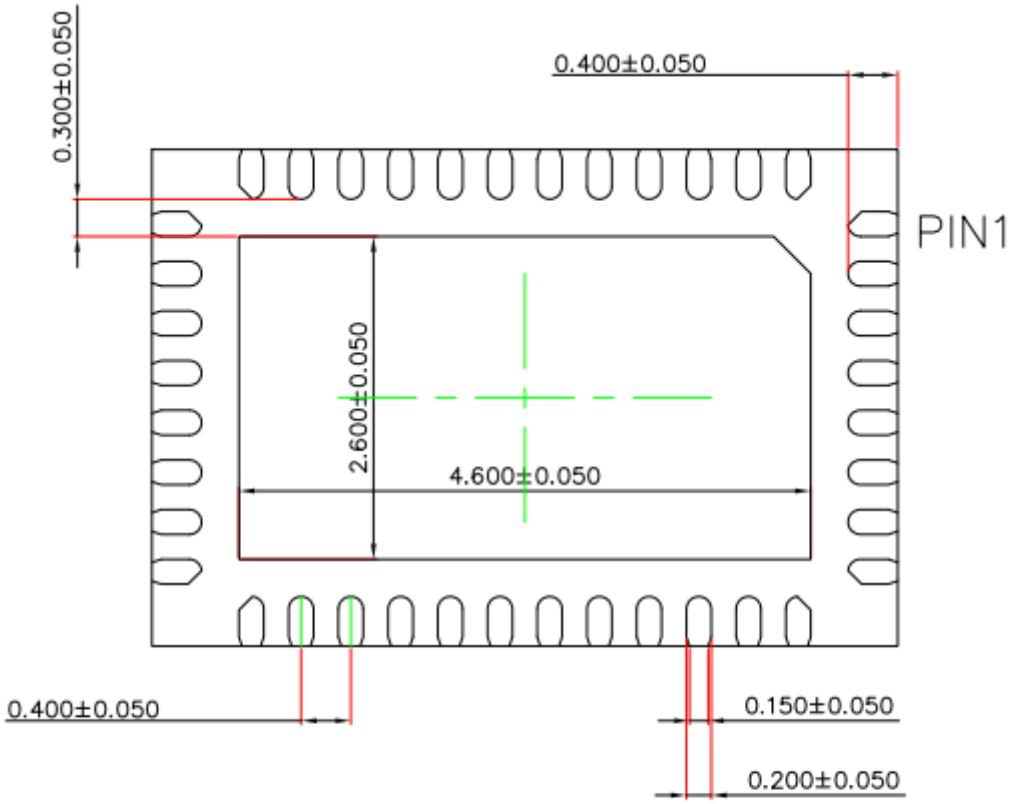
6.2 Package Physical Dimensions



TOP VIEW



SIDE VIEW



BOTTOM VIEW

	MIN.	NORM.	MAX.
A	0.700	0.750	0.800
	0.800	0.850	0.900

6.3 Pins Description

FR5082 is a CMOS device. Floating level on input signals will cause unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Digital Input
O	Digital Output
I/O	Bidirectional(digital)
AI	Analog input
AO	Analog output
AI/O	Bidirectional(analog)
OD	Open Drain
PWR	Power
GND	Ground

Pin number		Pin name	Type	Description
FR5082DM	FR5082DS			
1	1	XTALI_24M	AI	Crystal oscillator input
2	2	XTALO_24M	AO	Crystal oscillator output
3	3	PC0	I/O	Multi-Function GPIO
4	4	PC1	I/O	Multi-Function GPIO
5	5	PC2	I/O	Multi-Function GPIO
6	6	PC3	I/O	Multi-Function GPIO
7	7	PC4	I/O	Multi-Function GPIO
8	8	PC5	I/O	Multi-Function GPIO
9	9	VDD_DSP	AO	DSP block core power
10	10	PC7	I/O	Multi-Function GPIO
11	11	PC6	I/O	Multi-Function GPIO
12	12	PB7	I/O	Multi-Function GPIO
13	13	PB6	I/O	Multi-Function GPIO
14	14	PB5	I/O	Multi-Function GPIO
15	/	PB4	I/O	Multi-Function GPIO
16	15	SYS_BFB	AI	System DC/DC feedback input terminal

17	16	SYS_BSW	AO	System DC/DC output terminal
18	17	AU_BFB	AI	Audio codec DC/DC feedback input terminal
19	18	AU_BSW	AO	Audio codec DC/DC output terminal
/	19	ONKEY_N	AI	Always-on input pin
20	20	VBAT	PWR	Chip power
21	21	VCHG	AI	Charger pin
22	22	RESET_P	AI	Chip Reset Pin (high active)
23	23	IOLDO_OUT	AO	Power supply for IO
24	24	EXT_FLASH_VDD	AO	Power supply for extemal flash
25	25	MIC_IN	AI	Microphone input
26	26	VMID	AO	The middle voltage of codec
27	27	MICBIAS	AO	Micbias output
/	28	VDD_CODEC	AO	Audio codec LDO output
28	29	SPK_P / LOUT_P	AO	Audio LR mix / left channel positive output
29	30	SPK_N / LOUT_N	AO	Audio LR mix / left channel negative output
/	31	ROUT_N	AO	Audio right channel negative output
/	32	ROUT_P	AO	Audio right channel positive output
30	33	PB3	I/O	Multi-Function GPIO
31	34	PB2	I/O	Multi-Function GPIO
32	35	PB1	I/O	Multi-Function GPIO
33	36	PB0	I/O	Multi-Function GPIO
/	37	PA7	I/O	Multi-Function GPIO
/	38	PA6	I/O	Multi-Function GPIO
34	/	PA3	I/O	Multi-Function GPIO
35	/	PA2	I/O	Multi-Function GPIO
36	/	PA1	I/O	Multi-Function GPIO
37	39	PA0	I/O	Multi-Function GPIO
38	/	PD7	I/O	Multi-Function GPIO
39	/	PD6	I/O	Multi-Function GPIO
40	40	RF	AI/O	RF input and output

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	acoustic echo cancellers
AGC	Automatic Gain Control
ANS	Automatic Noise Suppression
ADC	Analog-to-Digital-Converter
DAC	Digital-to-Analog-Converter
GPIO	General Purpose Input Output
MIC	Microphone
PMU	Power Management Unit
OSC	Oscillator
PA	Power Amplifier
SoC	system on chip
Codec	Coder-Decoder

Contact Information

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Revision History

Feedback:

Freqchip welcomes feedback on this product and this document. If you have comments or suggestions, please send an email to doc@freqchip.com.

Reversion Number	Reversion Date	Description
V1.0	2020.12.11	Initial Draft