200-mA Low-Noise, High-PSRR, Negative-Output, Low-Dropout Linear Regulators

Check for Samples: TPS72301-Q1, TPS72325-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Ultralow Noise: 60 μV_{RMS} Typical**
- **High PSRR: 65 dB Typical at 1kHz**
- **Low Dropout Voltage: 280 mV Typical at 200 mA, 2.5 V**
- **Available in –2.5 V and Adjustable (–1.2 V to –10 V) Versions**
- **Stable With a 2.2-µF Ceramic Output Capacitor**
- **Less Than 2-µA Typical Quiescent Current in Shutdown Mode**
- **2% Overall Accuracy (Line, Load, Temperature)**
- **Thermal and Overcurrent Protection**
- **SOT23-5 (DBV) Package**
- **Operating Junction Temperature Range: –40°C to 125°C**

APPLICATIONS

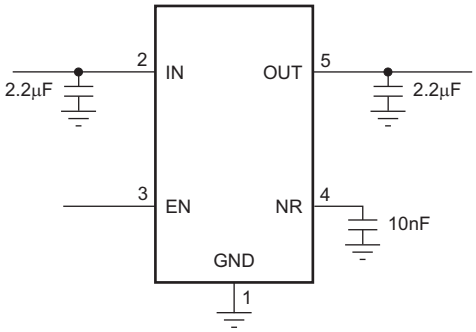
- **Optical Drives**
- **Optical Networking**
- **Noise-Sensitive Circuitry**
- **GaAs FET Gate Bias**
- **Video Amplifiers**

DESCRIPTION

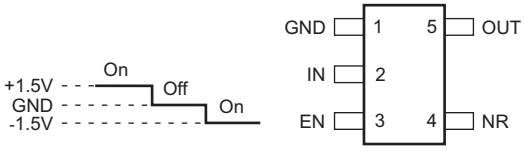
The TPS723xx-Q1 family of low-dropout (LDO) negative voltage regulators offers an ideal combination of features to support low-noise applications. This device is capable of operating with input voltages from –10 V to –2.7 V. The TPS72325-Q1 regulator is stable with small, low-cost ceramic capacitors, and includes enable (EN) and noise-reduction (NR) functions. Internal detection and shutdown logic provide thermal short-circuit and overcurrent protection. High PSRR (65 dB at 1 kHz) and low noise (60 μV_{RMS}) make the TPS723xx-Q1 ideal for low-noise applications.

The TPS723xx-Q1 uses a precision voltage reference to achieve 2% overall accuracy over load, line, and temperature variations. Available in a small SOT23-5 package, the TPS723xx-Q1 specification covers the full temperature range of –40°C to 125°C.

Typical Application Circuit



DBV PACKAGE
(TOP VIEW)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1) (2)

PRODUCT	V_{OUT} (2)	TOP-SIDE MARKING
TPS72301QDBVRQ1	Adjustable output voltage	PPHQ
TPS72325QDBVRQ1	Nominal output voltage = 2.5 V	PSBQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Output voltages from –1.2 V to –9 V in 100-mV increments are available. Minimum order quantities apply; contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1) (2)

Over operating temperature range, unless otherwise noted.

		VALUE	UNITS
Input voltage range, V_{IN}		–11 to 0.3	V
Noise reduction pin voltage range, V_{NR}		–11 to 5.5	V
Enable voltage range, V_{EN}		$–V_{IN}$ to 5.5	V
Output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Continuous total power dissipation, P_D		See Power Dissipation Ratings table	
Junction temperature range, T_J		–55 to 150	°C
Storage temperature range, T_{stg}		–65 to 150	°C
Latch-up performance meets 100 mA per AEC-Q100 | Class I		100	mA
ESD ratings	Human-body model	2000	kV
	Machine model	200	V
	Charged-device model	500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

POWER DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A ≤ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	DBV	64°C / W	255°C / W	3.9 mW / °C	390 mW	215 mW	155 mW
High-K(2)	DBV	64°C / W	180°C / W	5.6 mW / °C	560 mW	310 mW	225 mW

(1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch × 3- inch (7,62-cm × 7,62-cm), two-layer board with 2-ounce (0.071-mm thick) copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch (7,62-cm × 7,62-cm), multilayer board with 1-ounce (0.035-mm thick) internal power and ground planes and 2-ounce (0.071-mm thick) copper traces on the top and bottom of the board.

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ELECTRICAL CHARACTERISTICS

Over operating junction temperature range, $V_{IN} = V_{OUTnom} – 0.5V$, I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	TPS723xx-Q1			UNITS
				MIN	TYP	MAX	
V_{IN}	Input voltage range(1)			–10		–2.7	V
V_{OUT}	Accuracy	Nominal	T_J = 25°C	–1		1	%
		TPS723xx-Q1 versus V_{IN} / I_{OUT} / T	–10V ≤ V_{IN} ≤ V_{OUT} – 0.5V, 10 µA ≤ I_{OUT} ≤ 200 mA	–2	±1	2	%
V_{OUT}% / V_{IN}	Line regulation		–10 V ≤ V_{IN} ≤ $V_{OUT(nom)}$ – 0.5 V		0.04		% / V
V_{OUT}% / I_{OUT}	Load regulation		0 mA ≤ I_{OUT} ≤ 200 mA		0.002		% / mA
V_{DO}	Dropout voltage at V_{OUT} = 0.96 × V_{OUTnom}		I_{OUT} = 200 mA		280	500	mV
I_{CL}	Current limit		V_{OUT} = 0.85 × $V_{OUT(nom)}$	300	550	800	mA
I_{GND}	Ground pin current		I_{OUT} = 0 mA (I_Q), –10 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V		130	200	µA
			I_{OUT} = 200 mA, –10 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V		350	500	
I_{SHDN}	Shutdown ground pin current		–0.4 V ≤ V_{EN} ≤ 0.4 V, –10V ≤ V_{IN} ≤ V_{OUT} – 0.5 V		0.1	2	µA
PSRR	Power-supply rejection ratio		I_{OUT} = 200 mA, 1 kHz, C_{IN} = C_{OUT} = 10 µF		65		dB
			I_{OUT} = 200 mA, 10 kHz, C_{IN} = C_{OUT} = 10 µF		48		
V_n	Output noise voltage		C_{OUT} = 10 µF, 10 Hz to 100 kHz, I_{OUT} = 200 mA		60		$µV_{RMS}$
t_{STR}	Startup time		V_{OUT} = –2.5 V, C_{OUT} = 1 µF, R_L = 25 Ω		1		ms
$V_{EN(HI)}$	Enable threshold positive			1.5			V
$V_{EN(LO)}$	Enable threshold negative					–1.5	V
$V_{DIS(HI)}$	Disable threshold positive					0.4	V
$V_{DIS(LO)}$	Disable threshold negative			–0.4			V
I_{EN}	Enable pin current		–10 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V, –10 V ≤ V_{EN} ≤ ±3.5 V		0.1	2	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		
T_J	Operating junction temperature			–40		125	°C

(1) Maximum V_{IN} = (V_{OUT} – V_{DO}) or – 2.7 V, whichever is more negative.

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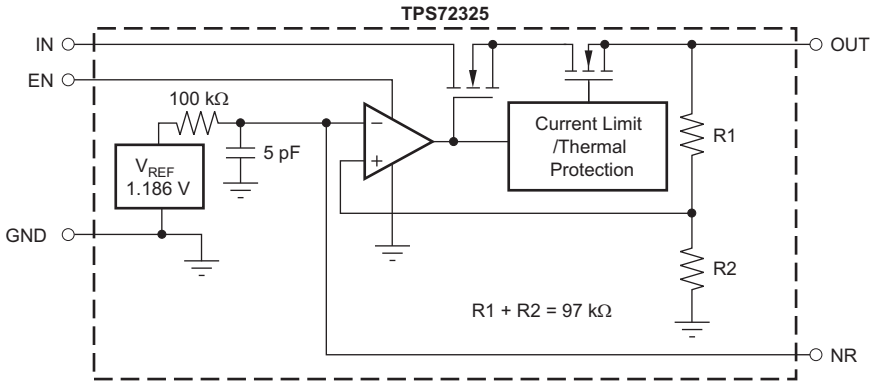
FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	1	Ground
IN	2	Input supply
EN	3	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode.
NR	4	Fixed-voltage versions only. Connecting an external capacitor between this pin and ground bypasses noise generated by the internal band gap. This configuration allows output noise to be reduced to very low levels.
OUT	5	Regulated output voltage. The device requires the connection of a small 2.2-μF ceramic capacitor from this pin to GND to ensure stability.

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TYPICAL CHARACTERISTICS

TPS723xx-Q1 at V_{IN} = V_{OUTnom} – 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.5 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.

OUTPUT VOLTAGE versus INPUT VOLTAGE

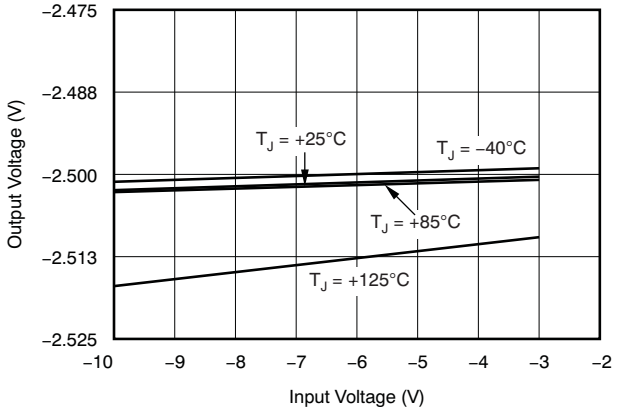

Figure 1.

OUTPUT VOLTAGE versus AMBIENT TEMPERATURE

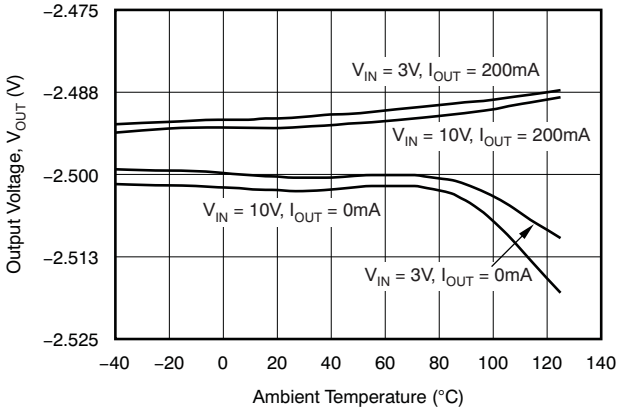

Figure 2.

DROPOUT VOLTAGE versus OUTPUT CURRENT

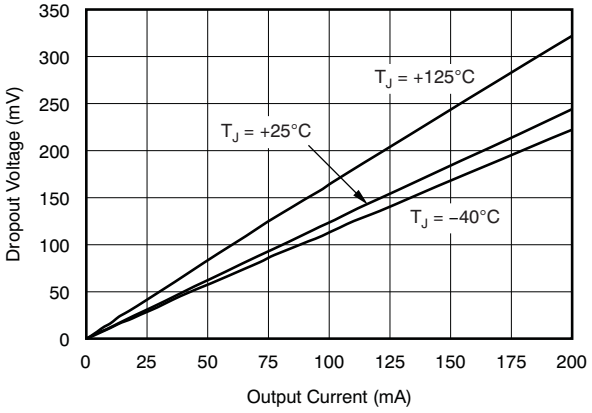

Figure 3.

TPS723xx-Q1
DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

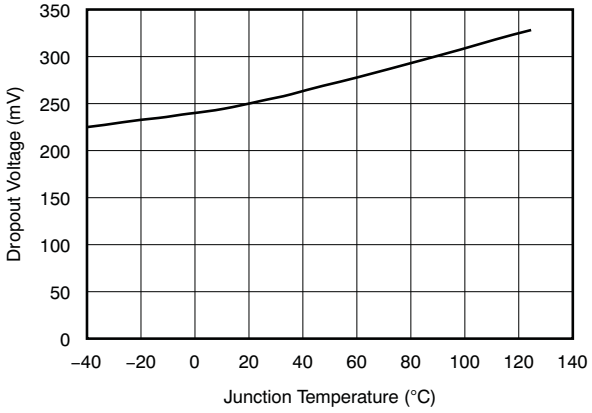

Figure 4.

GROUND CURRENT versus INPUT VOLTAGE

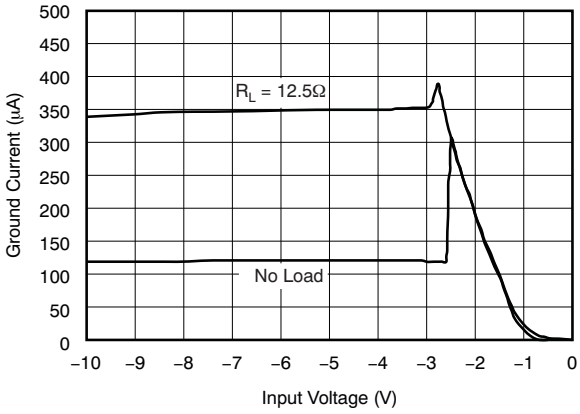

Figure 5.

GROUND CURRENT versus OUTPUT CURRENT

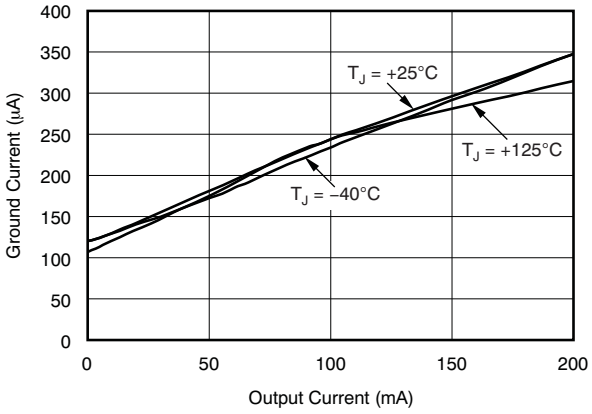

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

TPS723xx-Q1 at V_{IN} = V_{OUTnom} – 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.5 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.

GROUND CURRENT versus JUNCTION TEMPERATURE

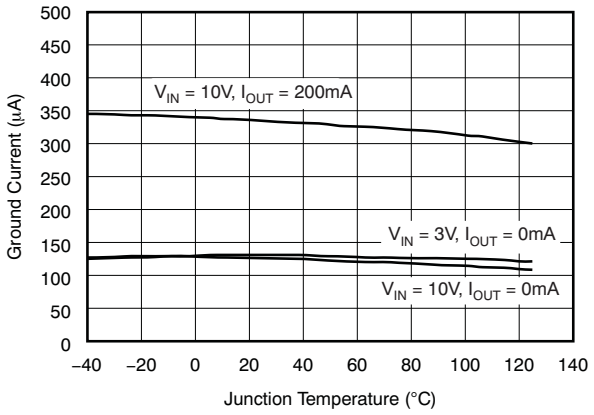

Figure 7.

CURRENT LIMIT versus JUNCTION TEMPERATURE

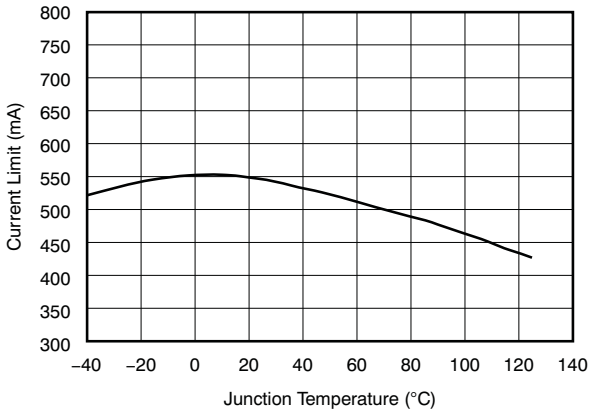

Figure 8.

STANDBY CURRENT versus JUNCTION TEMPERATURE

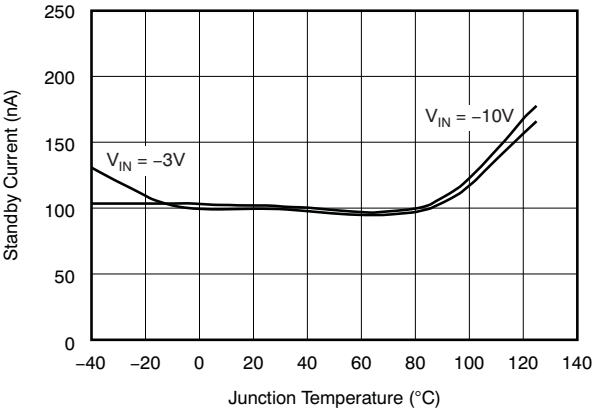

Figure 9.

ENABLE PIN CURRENT versus JUNCTION TEMPERATURE

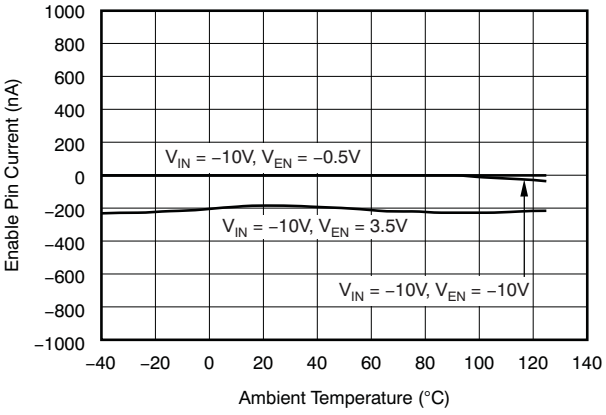

Figure 10.

LINE AND LOAD REGULATION versus JUNCTION TEMPERATURE

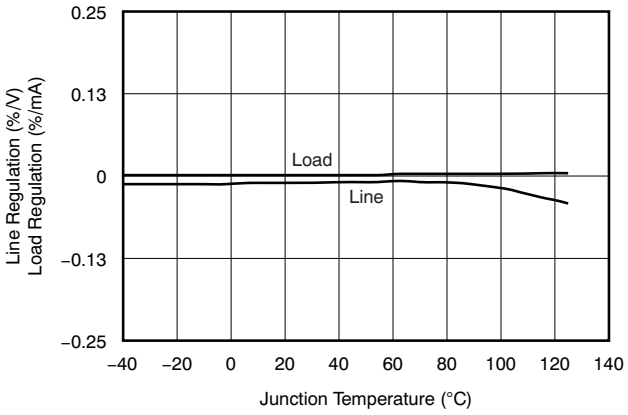

Figure 11.

LINE TRANSIENT RESPONSE

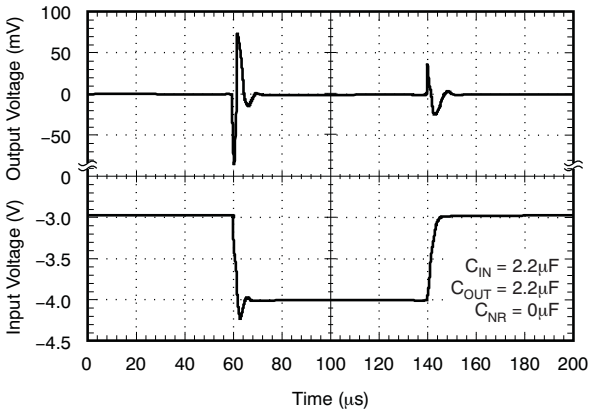

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

TPS723xx-Q1 at V_{IN} = V_{OUTnom} – 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.5 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.

LOAD TRANSIENT RESPONSE

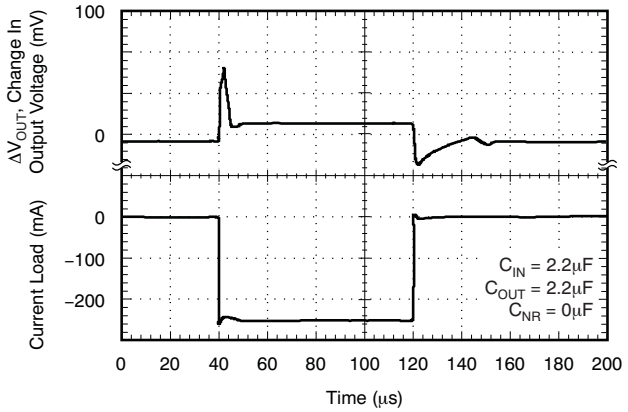

Figure 13.

LOAD TRANSIENT RESPONSE

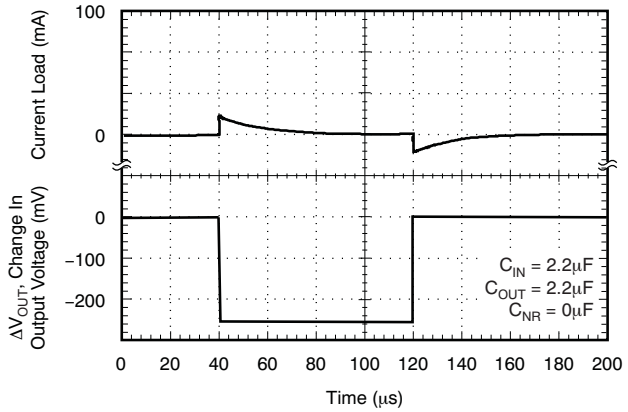

Figure 14.

START-UP RESPONSE

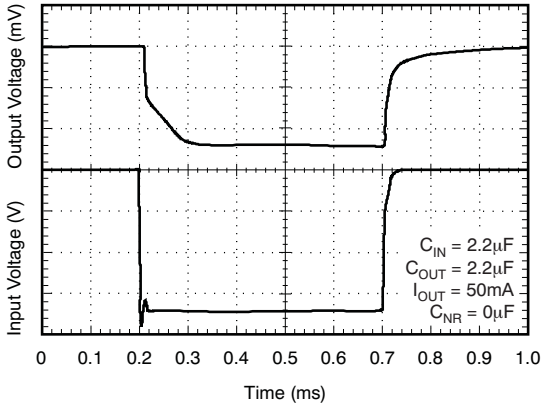

Figure 15.

START-UP RESPONSE

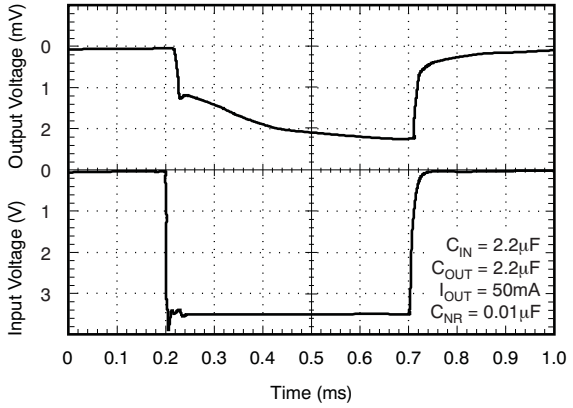

Figure 16.

POWER UP AND POWER DOWN

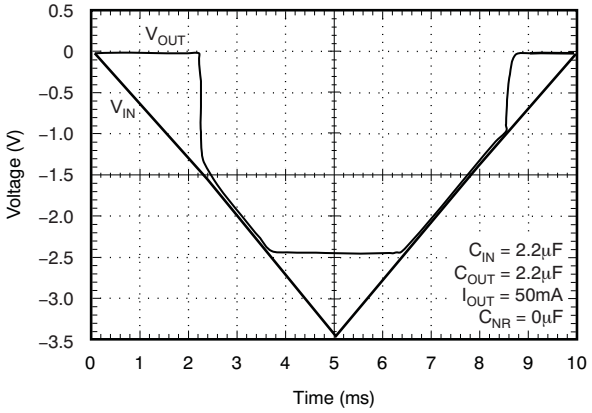

Figure 17.

TOTAL NOISE versus C_{NR} (10Hz to 100kHz)

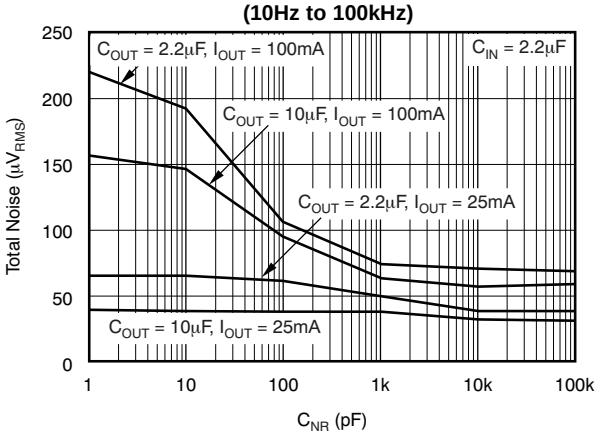

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

TPS723xx-Q1 at V_{IN} = V_{OUTnom} – 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.5 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.

OUTPUT NOISE versus TIME

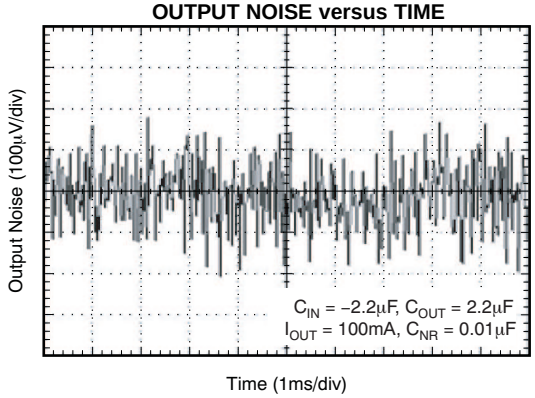

Figure 19.

NOISE SPECTRAL DENSITY versus FREQUENCY

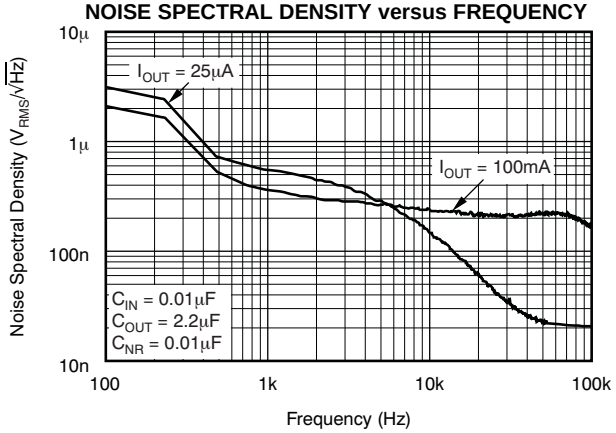

Figure 20.

NOISE SPECTRAL DENSITY versus FREQUENCY

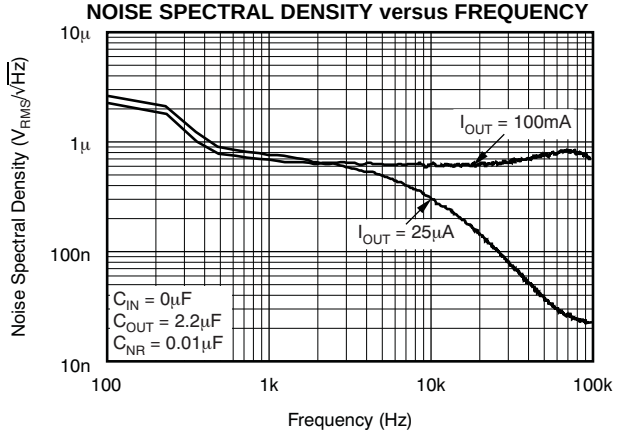

Figure 21.

PSRR versus FREQUENCY

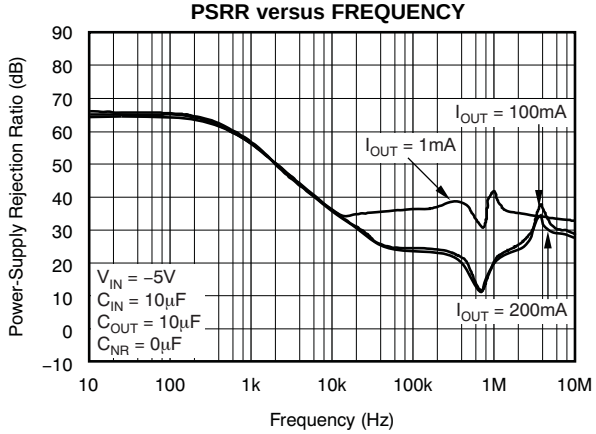

Figure 22.

PSRR versus FREQUENCY

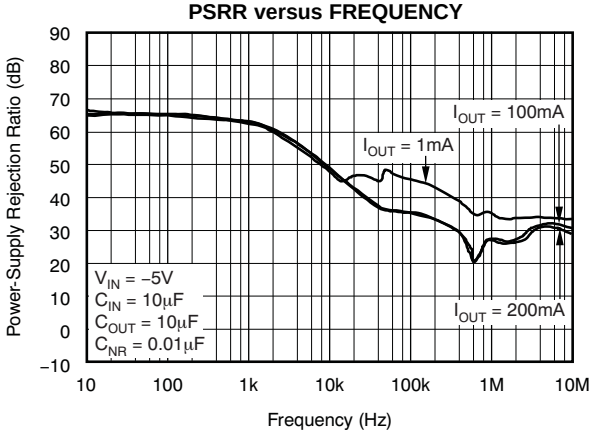

Figure 23.

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APPLICATION INFORMATION

DEVICE OPERATION

The TPS723xx-Q1 is a low-dropout negative linear voltage regulator with a rated current of 200 mA. It features very low noise and high power-supply rejection ratio (PSRR), making it ideal for high-sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to 2 µA maximum over temperature and process. The TPS723xx-Q1 comes in a small SOT23 package, specified over a –40°C to 125°C junction-temperature range.

ENABLE

The enable pin is active above 1.5 V and below –1.5 V, allowing control by a standard TTL signal or by connection to V_I if not used. Driving the pin to GND turns off most internal circuitry, putting the TPS723xx-Q1 into shutdown mode, drawing 2-µA maximum ground current.

CAPACITOR SELECTION FOR STABILITY

Use appropriate input and output capacitors for the intended application. The TPS723xx-Q1 only requires the use of a 2.2-µF ceramic output capacitor for stable operation. Both the capacitor value and ESR affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2-µF ceramic output capacitor located close to the regulator is sufficient.

OUTPUT NOISE

Without external bypassing, output noise of the TPS723xx-Q1 from 10 Hz to 100 kHz is 200 μV_{RMS} typical. The dominant contributor to output noise is the internal band-gap reference. Adding an external 0.01-µF capacitor to ground reduces the noise to 60 μV_{RMS}. To achieve best noise performance, use appropriate low-ESR capacitors for bypassing noise at the NR and OUT pins. See Figure 18 in the Typical Characteristics section.

POWER-SUPPLY REJECTION

The TPS723xx-Q1 offers a very high PSRR for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high-quality input and output capacitors.

CURRENT LIMIT

The TPS723xx-Q1 has internal circuitry that monitors and limits output current to protect the regulator from damage under all load conditions. When output current reaches the output-current limit (550 mA typical), protection circuitry turns on, reducing output voltage to ensure that current does not increase. See Figure 8 in the Typical Characteristics section.

Do not drive the output more than 0.3 V above the input. Doing so biases the body diode in the pass FET, allowing current to flow from the output to the input. The device does not limit this current. If this condition is likely, take care to limit the reverse current externally.

THERMAL PROTECTION

As protection from damage due to excessive junction temperatures, the TPS723xx-Q1 has internal protection circuitry. When junction temperature reaches approximately 165°C, the output device turns off. After the device has cooled by about 20°C, the output device turns on, allowing normal operation. For reliable operation, design is for worst-case junction temperature of ≤ 125°C, taking into account worst-case ambient temperature and load conditions.

ADJUSTABLE VOLTAGE APPLICATIONS

The TPS72301-Q1 allows designers to specify any output voltage from –10 V to –1.2 V. As shown in the application circuit in Figure 24, use of an external resistor divider scales the output voltage (V_{OUT}) to the reference voltage. For best accuracy, use precision resistors for R1 and R2. Use the equations in Figure 24 to determine the values for the resistor divider.

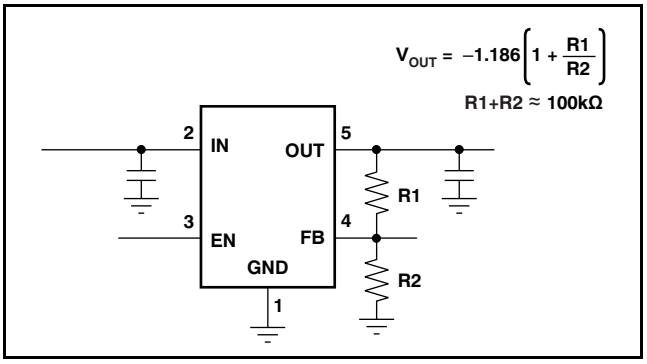

Figure 24. TPS72301-Q1 Adjustable LDO Regulator Programming

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72301QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PPHQ	Samples
TPS72325QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PSBQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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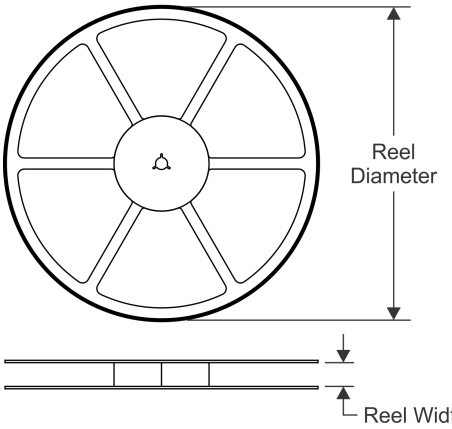
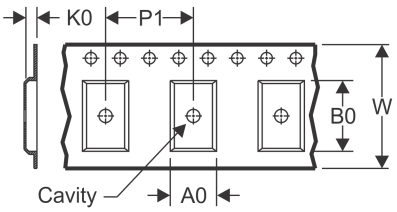
TAPE AND REEL INFORMATION

REEL DIMENSIONS

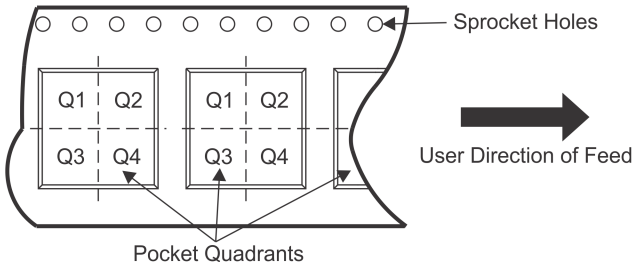


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

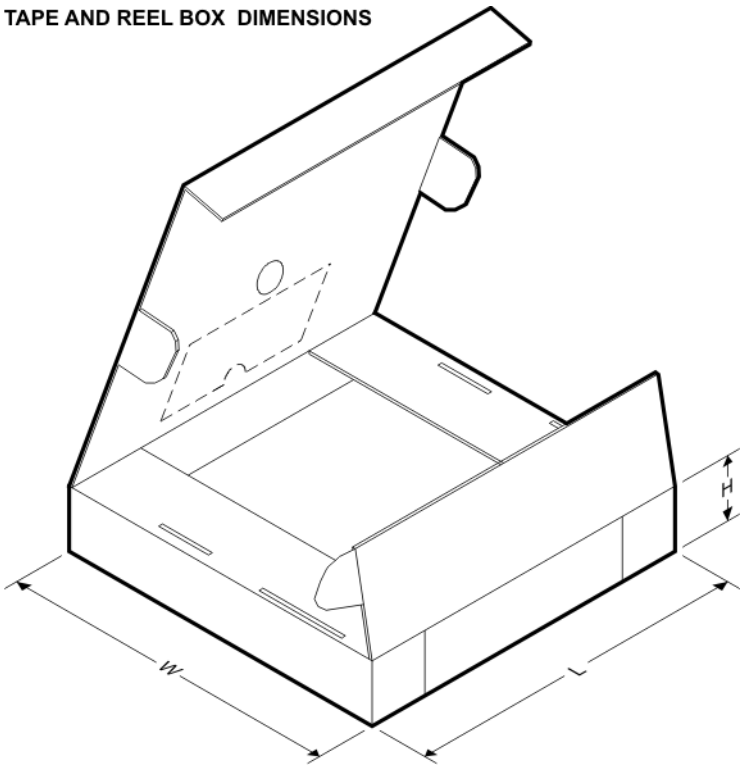
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72301QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

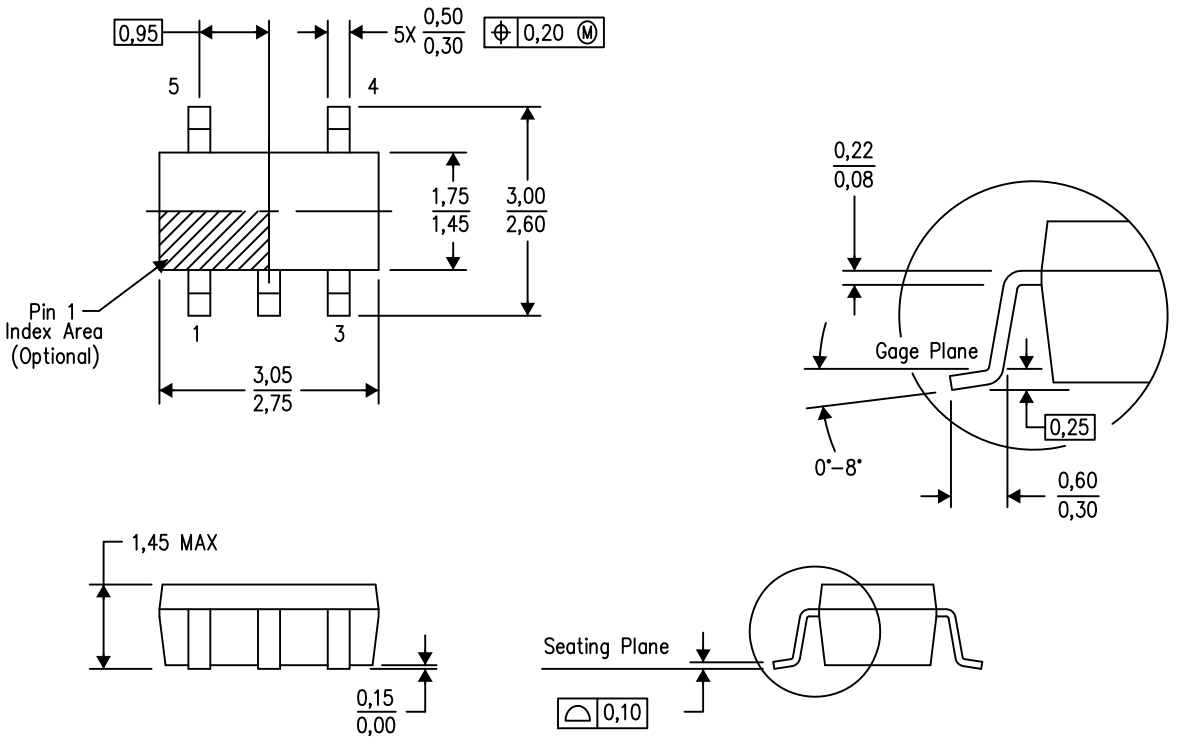
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72301QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS72325QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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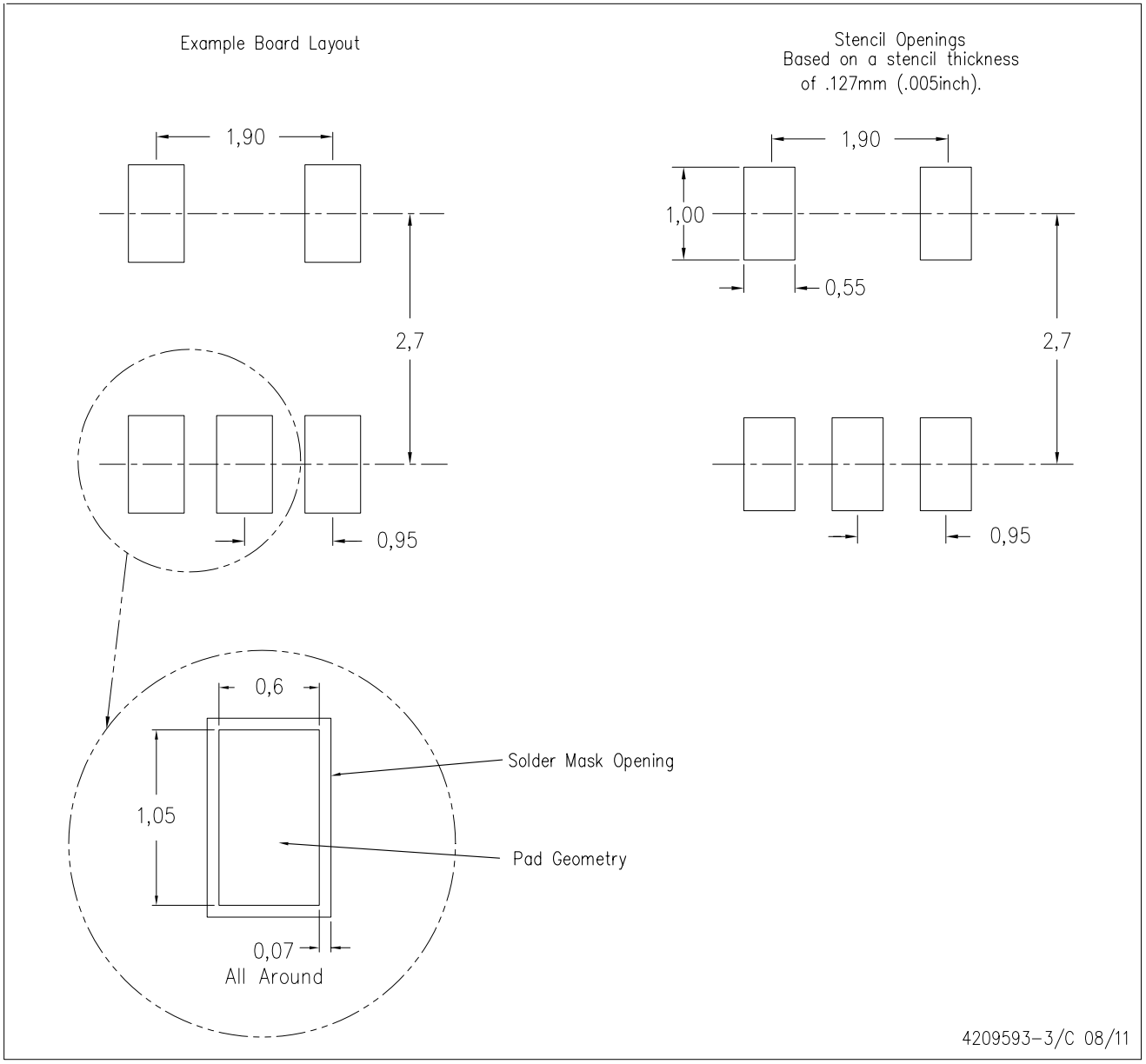
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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