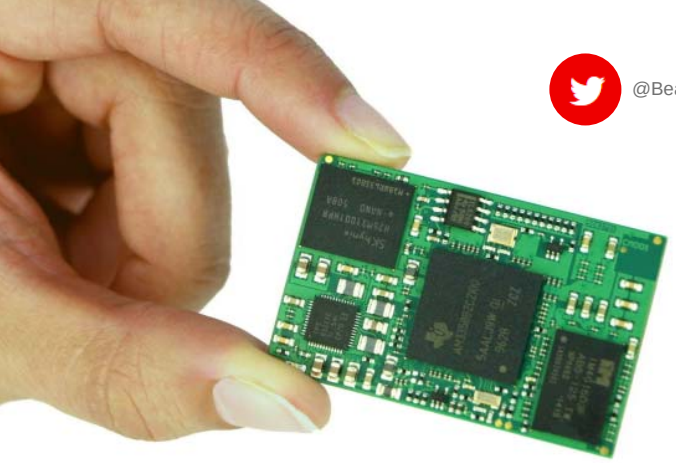

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BEAGLECORE™ BCM1

SYSTEM REFERENCE MANUAL

Revision 1.2

DISCLAIMER

The design materials referred to in this document are based on the BeagleBone Black and are neither supported nor do they constitute a reference design. If you are looking for support, please join the BeagleBoard Community over at BeagleBoard.org/discuss.

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Please read the System Reference Manual and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages.

For additional information, please visit beaglecore.com.

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INTRODUCTION

This document is the System Reference Manual for BeagleCore™ BCM1. It is intended as a guide to assist anyone purchasing or who are considering purchasing the board to understand the overall system design and the features of the BeagleCore™ BCM1. It can also be used as a reference for the design for those who are implementing this design into their own product.

This design is subject to change without notice as we will work to keep improving the design as the product matures.

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KNOWN ISSUES

For an up to date list of all known issues per revision, please refer to the BeagleCore GitHub repository and the issues listed there: https://github.com/BeagleCore/Hardware/issues.

CONTENTS

1. WHAT IS BEAGLECORE™?

The BeagleCore™ BCM1 is a miniaturized computer module for industrial or commercial applications covering all core features of BeagleBone Black. It is designed to address the Open Source Community, early adopters, and anyone interested in a low cost ARM Cortex A8 based processor. It enables users to design their own embedded devices while remaining a maximum compatibility with the BeagleBone Black.

2. FEATURES

This section covers the specifications of the BeagleCore™ BCM1.

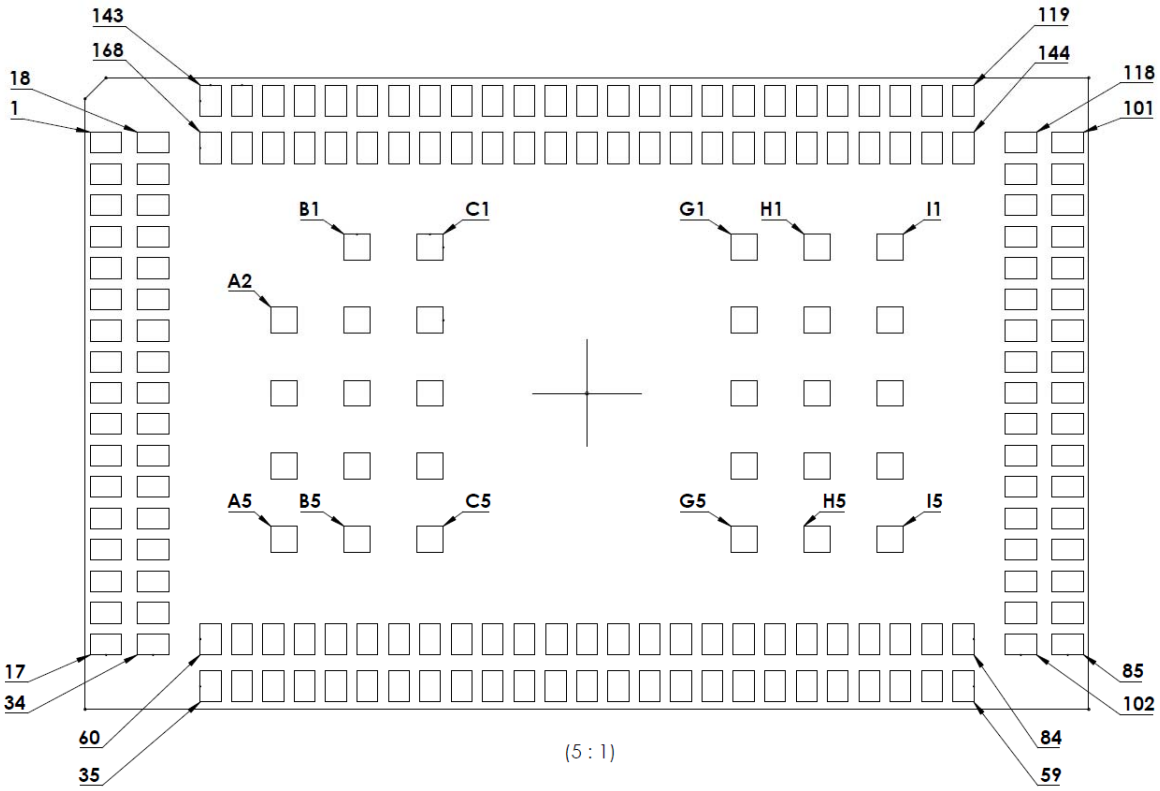
- Dimensions (WDH): 48 mm × 31 mm × 3,5 mm
- Processor: Texas Instruments AM335x Cortex-A8 “Sitara”
- Clock rate: 1.0GHz
- Memory: 512 MB DDR3
- Flash: 4 GB 8-bit eMMC
- Temperature range: 0…60°C (optionally: -40…85°C)
- Operating: 10 to 90% r. H. non cond.
  Storage: 5 to 95% r. H. non cond.
- Supported interfaces / extensions:
  - 1 × RGMII Interface for 10/100/1000 Mbit LAN
  - 2 × USB 2.0 Host / Client
  - 1 × SDIO (for SD memory cards)
  - 1 × UART / 1 × JTAG (for debugging)
  - up to 59 × GPIO for HDMI, CAN, I2C, etc.

For further details we would like to refer to the latest documentation for BeagleBone Black available at http://beagleboard.org/static/beaglebone/latest/Docs/Hardware/.

3. SPECIFICATIONS

3.1 PIN-SIGNALS GRAPHIC OVERVIEW

This section covers the pin-signals of the BeagleCore™ BCM1 and provides descriptions of the major components and interfaces that make up the BeagleCore™ BCM1.



Img. 1: Pin-signals for BeagleCore™ BCM1 (top view)

3.2 PIN-SIGNALS TABLE

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
1	USB0_D_P	N17		
2	USB0_D_N	N18		
3	DGND			
4	MII1_RXD2	L16		GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/ UART1_RIN/MCASP0_AXR1/GPIO2_19
5	MII1_RXD3	L17		GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/ UART1_DTRN/MCASP0_AXR0/GPIO2_18
6	MII1_RXCLK	L18		GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT6/MMC1_DAT1/ UART1_DSRN/MCASP0_FSX/GPIO3_10
7	MII1_TXD1	K16		GMII1_TXD1/RMII1_TXD1/RGMII1_TD1/MCASP1_FSR/MCASP1_AXR1/ EQEP0A_IN/MMC1_CMD/GPIO0_21
8	MII1_TXD3	J18		GMII1_TXD3/DCAN0_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSX/ MMC2_DAT1/MCASP0_FSR/GPIO0_16
9	MII1_RXDV	J17		GMII1_RXDV/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/ MCASP1_ACLKX/MMC2_DAT0/MCASP0_ACLKR/GPIO3_4
10	MII1_TXEN	J16		GMII1_TXEN/RMII1_TXEN/RGMII1_TCTL/TIMER4/MCASP1_AXR0/ EQEP0_INDEX/MMC2_CMD/GPIO3_3
11	MII1_REFCLK	H18		RMII1_REFCLK/XDMA_EVENT_INTR2/SPI1_CS0/UART5_TXD/ MCASP1_AXR3/MMC0_POW/MCASP1_AHCLKX/GPIO0_29
12	MII1_COL	H16		GMII1_COL/RMII2_REFCLK/SPI1_SCLK/UART5_RXD/MCASP1_AXR2/ MMC2_DAT3/MCASP0_AXR2/GPIO3_0
13	BKL_ISET2		36	
14	BKL_ISET1		35	
15	BKL_L4		37	
16	BKL_FB_WLED		38	
17	DGND			
18	DGND			
19	MDIO_DATA	M17		MDIO_CLK/TIMER5/UART5_TXD/UART3_RTSN/MMC0_SDWP/ MMC1_CLK/MMC2_CLK/GPIO0_1
20	MDIO_CLK	M18		MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/ MMC1_CMD/MMC2_CMD/GPIO0_0
21	MII1_RxD0	M16		GMII1_RXD0/RMII1_RXD0/RGMII1_RD0/MCASP1_AHCLKX/ MCASP1_AHCLKR/MCASP1_ACLKR/MCASP0_AXR3/GPIO2_21
22	MII1_RxD1	L15		GMII1_RXD1/RMII1_RXD1/RGMII1_RD1/MCASP1_AXR3/MCASP1_FSR/ EQEP0_STROBE/MMC2_CLK/GPIO2_20

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
23	MII1_TXCLK	K18		GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7/MMC1_DAT0/ UART1_DCDN/MCASP0_ACLKX/GPIO3_9
24	MII1_TxD0	K17		GMII1_TXD0/RMII1_TXD0/RGMII1_TD0/MCASP1_AXR2/ MCASP1_ACLKR/EQEP0B_IN/MMC1_CLK/GPIO0_28
25	MII1_TxD2	K15		GMII1_TXD2/DCAN0_RX/RGMII1_TD2/UART4_TXD/MCASP1_AXR0/ MMC2_DAT2/MCASP0_AHCLKX/GPIO0_17
26	DGND			
27	MII1_RXERR	J15		GMII1_RXERR/RMII1_RXERR/SPI1_D1/I2C1_SCL/MCASP1_FSX/ UART5_RTSN/UART2_TXD/GPIO3_2
28	MII1_CRS_DV	H17		GMII1_CRS/RMII1_CRS_DV/SPI1_D0/I2C1_SDA/MCASP1_ACLKX/ UART5_CTSN/UART2_RXD/GPIO3_1
29	DGND			
30	BKL_ISINK2		33	
31	BKL_ISINK1		34	
32	I2C0_SCL	C16		I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT////GPIO3_6
33	I2C0_SDA	C17		I2C0_SDA/TIMER4/UART2_CTSN/ECAP2_IN_PWM2_OUT////GPIO3_5
34	DGND			
35	UART4_TXD	U17		GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/ PR1_MDIO_MDCLK/UART4_TXD/GPIO0_31
36	UART4_RXD	T17		GPMC_WAIT0/GM112_CRS/GPMC_CSN4/RMII2_CRS_DV/ MMC1_SDCD/PR1_MII1_RXDV/UART4_RXD/GPIO0_30
37	GPIO1_28	U18		GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/ PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28
38	EHRPWM1A	U14		GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/ PR1_MII1_TXD2/EHRPWM1A/GPIO1_18
39	EHRPWM1B	T14		GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/ PR1_MII1_TXD1/EHRPWM1B/GPIO1_19
40	MMC0_DAT3	F17		MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/ PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26
41	MMC0_DAT1	G15		MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/ PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28
42	MMC0_CD	C15		SPI0_CS1/UART3_RXD/ECAP1_IN_PWM1_OUT/MMC0_POW/ XDMA_EVENT_INTR2/MMC0_SDCD/EMU4/GPIO0_60

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
43	XDMA_EVENT_INTR0	A15		EVENT_INTR0/TIMER4/CLKOUT1/SPI1_CS1/PR1PRU1R31_16/EMU2/ GPIO0_19
44	UART0_CTS#	E18		Reserved for future use
45	UART0_RTS#	E17		Reserved for future use
46	UART0_TX	E16		UART0_TXD/SPI1_CS1/DCAN0_RX/I2C2_SCL/ECAP1_IN_PWM1_OUT/ PR1_PRU1_PRU_R30_15/PR1_PRU1_PRU_R31_15/GPIO1_11
47	UART0_RX	E15		UART0_RXD/SPI1_CS0/DCAN0_TX/I2C2_SDA/ECAP2_IN_PWM2_OUT/ PR1_PRU1_PRU_R30_14/PR1_PRU1_PRU_R31_14/GPIO1_10
48	SYS_RESETn	A10		
49	I2C1_SDA	B16		SPI0_D1/MMC1_SDWP/I2C1_SDA/EHRPWM0_TRIPZONE_INPUT/ PR1_UART0_RXD/PR1_EDIO_DATA_IN0/PR1_EDIO_DATA_OUT0/GPIO0_4
50	I2C1_SCL	A16		SPI0_CS0/MMC2_SDWP/I2C1_SCL/EHRPWM0_SYNCI_O/ PR1_UART0_TXD/PR1_EDIO_DATA_IN1/PR1_EDIO_DATA_OUT1/GPIO0_5
51	JTAG_EMU1	B14		
52	JTAG_TCK	A12		
53	JTAG_TDO	A11		
54	JTAG_TRSTn	B10		
55	GNDA_ADC			
56	AIN6	A8		
57	AIN4	C8		
58	AIN2	B7		
59	AIN0	B6		
60	BAT1		4,5	
61	BAT_SENSE		6	
62	BAD_TS		11	
63	PWR_BUT		25	
64	MMC0_CMD	G18		MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/ PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31
65	MMC0_CLKO	G17		MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/ PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30
66	MMC0_DAT2	F18		MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/ PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
67	MMC0_DAT0	G16		MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/ PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29
68	GPIO0_7SRC	C18		ECAP0_IN_PWM0_OUT/UART3_TXD/SPI1_CS1/ PR1_ECAP0_ECAP_CAPIN_APWM_O/SPI1_SCLK/MMC0_SDWP/ XDMA_EVENT_INTR2/GPIO0_7
69	UART2_RXD	A17		SPI0_SCLK/UART2_RXD/I2C2_SDA/EHRPWM0A/PR1_UART0_CTS_N/ PR1_EDIO_SOF/EMU2/GPIO0_2
70	UART2_TXD	B17		SPI0_D0/UART2_TXD/I2C2_SCL/EHRPWM0B/PR1_UART0_RTS_N/ PR1_EDIO_LATCH_IN/EMU3/GPIO0_3
71	I2C2_SDA	B16		UART1_CTSN/TIMER6/DCAN0_TX/I2C2_SDA/SPI1_CS0/PR1_UART0_CTS_ N/PR1_EDC_LATCH0_IN/GPIO0_124
72	I2C2_SCL	A16		UART1_RTSN/TIMER5/DCAN0_RX/I2C2_SCL/SPI1_CS1/PR1_UART0_RTS_ N/PR1_EDC_LATCH1_IN/GPIO0_13
73	UART1_RXD	D16		UART1_RXD/MMC1_SDWP/DCAN1_TX/I2C1_SDA//PR1_UART0_RXD/ PR1_PRU1_PRU_R31_16/GPIO0_14
74	UART1_TXD	D15		UART1_TXD/MMC2_SDWP/DCAN1_RX/I2C1_SCL//PR1_UART0_TXD/ PR1_PRU0_PRU_R31_16/GPIO0_15
75	DGND			
76	CLKOUT_SRC	D14		EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1PRU0_PRUR31_16/ EMU3/GPIO0_20
77	JTAG_EMU0	C14		
78	JTAG_TDI	B11		
79	JTAG_TMS	C11		
80	GNDA_ADC			
81	VDD_ADC			
82	AIN5	B8		
83	AIN3	A7		
84	AIN1	C7		
85	GPIO3_18	B12		MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/ MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18
86	GPIO3_19	C13		MCASP0_FSR/EQEP0B_IN/MCASP0_AXR3/MCASP1_FSX/EMU2/ PR1_PRU0_PRU_R30_5/PR1_PRU0_PRU_R31_5/GPIO3_19

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
87	GPIO3_20	D13		MCASP0_AXR1/EQEP0_INDEX//MCASP1_AXR0/EMU3/ PR1_PRU0_PRU_R30_6/PR1_PRU0_PRU_R31_6/GPIO3_20
88	GPIO3_21	A14		MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/ EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21
89	USB1_ID	P17		
90	DGND			
91	USB1_D_P	R17		
92	USB1_D_N	R18		
93	USB1_Ocn	T16		GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/ PR1_MII1_CRS/MCASP0_AXR0/GPIO1_26
94	LCD_DATA0	R1		LCD_DATA0/GPMC_A0//EHRPWM2A//PR1_PRU1_PRU_R30_0/ PR1_PRU1_PRU_R31_0/GPIO2_6
95	LCD_DATA2	R3		LCD_DATA2/GPMC_A2//EHRPWM2_TRIPZONE_INPUT// PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8
96	LCD_DATA4	T1		LCD_DATA4/GPMC_A4//EQEP2A_IN//PR1_PRU1_PRU_R30_4/ PR1_PRU1_PRU_R31_4/GPIO2_10
97	LCD_DATA6	T3		LCD_DATA6/GPMC_A6/PR1_EDIO_DATA_IN6/EQEP2_INDEX/ PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/ GPIO2_12
98	LCD_DATA8	U1		LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/ MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14
99	LCD_DATA10	U3		LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0// PR1_MII0_RXD1/UART3_CTSN/GPIO2_16
100	LCD_DATA12	V2		LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASP0_ACLKR/ MCASP0_AXR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8
101	LCD_DATA14	V4		LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASP0_AXR1/UART5_RXD/ PR1_MII_MR0_CLK/UART5_CTSN/GPIO0_10
102	DGND			
103	SPI1_SCLK	A13		MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/ PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14
104	SPI1_D0	B13		MCASP0_FSX/EHRPWM0B//SPI1_D0/MMC1_SDCD/ PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15
105	SPI1_D1	D12		MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/ PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
106	SPI1_CS0	C12		MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/ PR1_PRU0_PRU_R31_3/GPIO3_17
107	USB1_DRVVBUS	F15		USB1_DRVVBUS/GPIO3_13
108	USB1_CE	P18		
109	USB1_VBUS	F15		
110	DGND			
111	LCD_DATA1	R2		LCD_DATA1/GPMC_A1//EHRPWM2B//PR1_PRU1_PRU_R30_1/ PR1_PRU1_PRU_R31_1/GPIO2_7
112	LCD_DATA3	R4		LCD_DATA3/GPMC_A3//EHRPWM2_SYNCI_O//PR1_PRU1_PRU_R30_3/ PR1_PRU1_PRU_R31_3/GPIO2_9
113	LCD_DATA5	T2		LCD_DATA5/GPMC_A5//EQEP2B_IN//PR1_PRU1_PRU_R30_5/ PR1_PRU1_PRU_R31_5/GPIO2_11
114	LCD_DATA7	T4		LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/ PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/ GPIO2_13
115	LCD_DATA9	U2		LCD_DATA9/GPMC_A13/EHRPWM1_SYNCI_O/MCASP0_FSX/UART5_RXD/ PR1_MII0_RXD2/UART2_RTSN/GPIO2_15
116	LCD_DATA11	U4		LCD_DATA11/GPMC_A15/EHRPWM1B/MCASP0_AHCLKR/MCASP0_AXR2/ PR1_MII0_RXD0/UART3_RTSN/GPIO2_17
117	LCD_DATA13	V3		LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASP0_FSR/MCASP0_AXR3/ PR1_MII0_RXER/UART4_RTSN/GPIO0_9
118	LCD_DATA15	T5		LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASP0_AHCLKX/ MCASP0_AXR3/PR1_MII0_RXDV/UART5_RTSN/GPIO0_11
119	DGND			
120	LCDDE	R6		LCD_AC_BIAS_EN/GPMC_A11//PR1_EDIO_DATA_IN5/ PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/ PR1_PRU1_PRU_R31_11/GPIO2_25
121	DGND			
122	eMMC_RSTn	über Inverter R14		GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/ PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20
123	MMC1_DAT0	U7		GPMC_AD0/MMC1_DAT0//////GPIO1_0
124	MMC1_DAT1	V7		GPMC_AD1/MMC1_DAT1//////GPIO1_1
125	MMC1_DAT2	R8		GPMC_AD2/MMC1_DAT2//////GPIO1_2

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
126	MMC1_DAT3	T8		GPMC_AD3/MMC1_DAT3//////GPIO1_3
127	MMC1_DAT4	U8		GPMC_AD4/MMC1_DAT4//////GPIO1_4
128	MMC1_DAT5	V8		GPMC_AD5/MMC1_DAT5//////GPIO1_5
129	MMC1_DAT6	R9		GPMC_AD6/MMC1_DAT6//////GPIO1_6
130	MMC1_DAT7	T9		GPMC_AD7/MMC1_DAT7//////GPIO1_7
131	MMC1_CLK	U9		GPMC_CSN1/GPMC_CLK/MMC1_CLK/PRT1EDIO_DATA_IN6/ PRT1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/ PR1_PRU1_PRU_R31_12/GPIO1_30
132	DGND			
133	GPIO0_26	T11		GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/ EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26
134	GPIO0_27	U12		GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/ EHRPWM2_SYNCI_O/PR1_MII0_TXD3//GPIO0_27
135	HDMI_INT	U16		GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/ PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25
136	HDMICLK_DISn	V17		GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/ PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27
137	GPIO1_13	R12		GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/ PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13
138	GPIO1_15	U13		GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/ PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15
139	GPIO1_16	R13		GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/ PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16
140	USR1	U15		GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/ PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22
141	USR3	V16		GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/ PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24
142	USB0_VBUS			
143	USB0_CE	M15		
144	LCDPCLK	V5		LCD_PCLK/GPMC_A10//PR1_EDIO_DATA_IN4/PR1_EDIO_DATA_OUT4/ PR1_PRU1_PRU_R30_10/PR1_PRU1_PRU_R31_10/GPIO2_24
145	LCDHSYNC	R5		LCD_HSYNC/GPMC_A9//PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/ PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23
146	LCDVSYNC	U5		LCD_VSYNC/GPMC_A8//PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/ PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
147	DGND			
148	TIMER4	R7		GPMC_ADVN_ALE/TIMER4/GPIO2_2
149	TIMER5	T6		GPMC_BE0N_CLE/TIMER5/GPIO2_5
150	TIMER6	U6		GPMC_WEN/TIMER6/GPIO2_4
151	TIMER7	T7		GPMC_OEN_REN/TIMER7/EMU4/GPIO2_3
152	DGND			
153	GPIO1_29	V6		GPMC_CSN0/GPIO1_29
154	EHRPWM2A	U10		GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/ PR1_MII_MT0_CLK//GPIO0_22
155	EHRPWM2B	T10		GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/ PR1_MII0_CRS//GPIO0_23
156	MMC1_CMD	V9		GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/ PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/ PR1_PRU1_PRU_R31_13/GPIO1_31
157	DGND			
158	GPIO2_1	V12		GPMC_CLK/LCD_MEM_CLK/GPMC_WAIT1/MMC2_CLK/ PRT1_MII1_TXEN/MCASP0_FSR/GPIO2_1
159	GPIO2_0	T13		GPMC_CSN3/MMC2_CMD/PR1_MDIO_DATA/GPIO2_0
160	GPIO1_17	V14		GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/ PR1_MII1_TXD3/EHRPWM1_SYNCI_O/GPIO1_17
161	DGND			
162	GPIO1_12	T12		GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/ PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12
163	GPIO1_14	V13		GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/ PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14
164	USR0	V15		GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/ PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21
165	USR2	T15		GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/ PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23
166	DGND			
167	USB0_ID	P16		
168	USB0_DRVVBUS	F16		Reserved for future use

Pin on BGA	Transfer-Signal on BGA	from Pin AM3358BZCZ100	from Pin TPS65217CRSLR	comment
A2	DGND			
A3	VDD_CORE			
A4	VDD_5V			
A5	VDD_5V			
B1	VDD_3V3B			
B2	DGND			
B3	VDD_MPU			
B4	SYS_5V			
B5	VDD_USB_DC			
C1	VDD_3V3B			
C2	VDD_PLL			
C3	VDD_1V8			
C4	VDD_1V8			
C5	VDD_S			
G1	VDD_3V3A			
G2	DGND			
G3	VDD_S			
G4	DGND			
G5	DGNDA_ADC			
H1	VDD_CORE			
H2	DGND			
H3	DGND			
H4	DGND			
H5	VDD_ADC			
I1	VDD_CORE			
I2	DGND			
I3	VDDS_DDR			
I4	DGND			
I5	VDDS_DDR			

3.3 COLOR-LEGEND FOR SIGNAL-TYPE

MII
USB
BKL
UART
JTAG
MMC
JTAG
AIN
LCD
eMMC
Reserved for future use

4. CHANGE HISTORY

The following table reflects the changes made to BeagleCore™ BCM1.

Revision	Comments	Date	Editor
1.0	Original release	2016-03-07	ANS
1.1	Correction Signals Pin 71 and 72 and footprint drawing	2016-07-19	FIN
1.2	Correction in Pin Signals Table (B4: SYS_5V)	2017-11-30	ANS

5. OPEN HARDWARE

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