**DAC8532**



SBAS246A – DECEMBER 2001 – MAY 2003

**Dual Channel, Low Power, 16-Bit, Serial Input DIGITAL-TO-ANALOG CONVERTER**

**FEATURES** **DESCRIPTION**

* ***micro*POWER OPERATION: 500**µ**A at 5V**
* **POWER-ON RESET TO ZERO-SCALE**
* **POWER SUPPLY: +2.7V to +5.5V**
* **16-BIT MONOTONIC OVER TEMPERATURE**
* **SETTLING TIME: 10**µ **s to** ± **0.003% FSR**
* **ULTRA-LOW AC CROSSTALK: –100dB typ**
* **LOW-POWER SERIAL INTERFACE WITH SCHMITT-TRIGGERED INPUTS**
* **ON-CHIP OUTPUT BUFFER AMPLIFIER WITH RAIL-TO-RAIL OPERATION**
* **DOUBLE BUFFERED INPUT ARCHITECTURE**
* **SIMULTANEOUS OR SEQUENTIAL OUTPUT UPDATE AND POWERDOWN**
* **TINY MSOP-8 PACKAGE**

**APPLICATIONS**

* **PORTABLE INSTRUMENTATION**
* **CLOSED-LOOP SERVO-CONTROL**
* **PROCESS CONTROL**
* **DATA ACQUISITION SYSTEMS**
* **PROGRAMMABLE ATTENUATION**
* **PC PERIPHERALS**

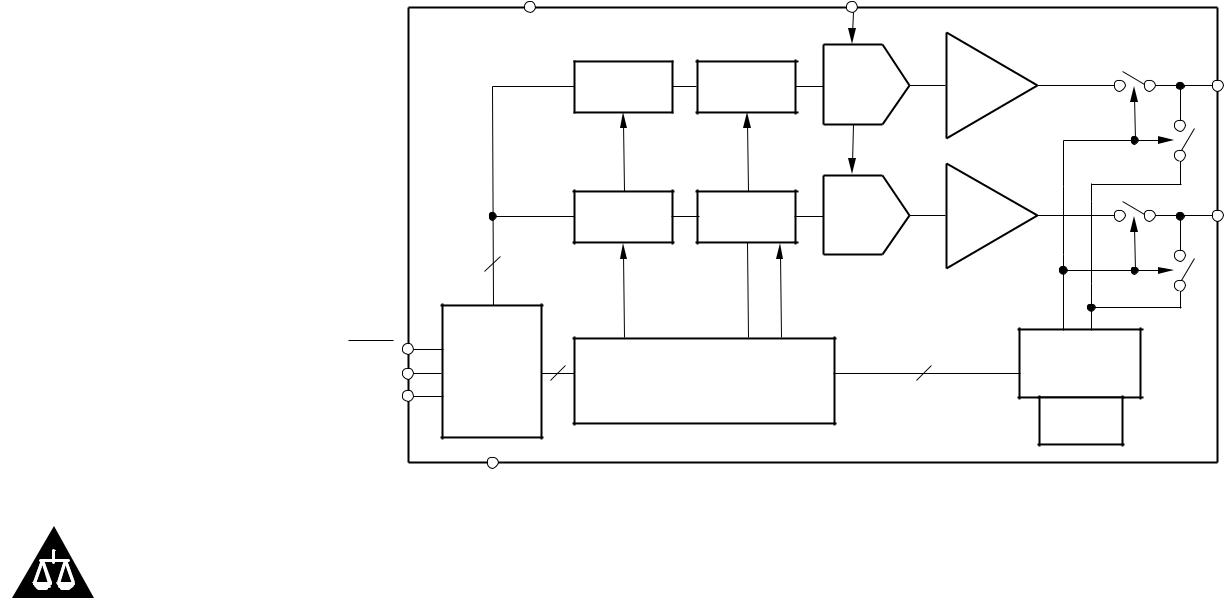
The DAC8532 is a dual channel, 16-bit Digital-to-Analog Converter (DAC) offering low power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7V to 5.5V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30MHz for VDD = 5V.

The DAC8532 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8532 provides a flexible power-down feature, accessed over the serial inter-face, that reduces the current consumption of the device to 200nA at 5V.

The low-power consumption of this device in normal opera-tion makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 2.5mW at 5V, reducing to 1µ W in power-down mode.

The DAC8532 is available in a MSOP-8 package with a specified operating temperature range of –40° C to +105° C.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | VDD |  |  | VREF |  |  |
|  |  | Data | DAC | DAC A | VOUTA |  |
|  |  | Buffer A | Register A |  |
|  |  | Data | DAC | DAC B | VOUTB |  |
|  |  | Buffer B | Register B |  |
|  | 16 |  |  |  |  |  |
|  | 24-Bit |  |  |  |  |  |
| SYNC | Serial-to- | Channel | Load |  | Power-Down |  |
| SCLK | Parallel | Select | Control |  | Control Logic |  |
| DIN | Shift | 8 |  |  | 2 |  |
|  | Register | Control Logic | |  | Resistor |  |
|  |  |  |  | Network |  |
|  |  |  |  |  |  |
|  | GND |  |  |  |  |  |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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**ABSOLUTE MAXIMUM RATINGS(1)**

|  |  |
| --- | --- |
| VDD to GND ........................................................................... | –0.3V to +6V |
| Digital Input Voltage to GND ................................. | –0.3V to +VDD + 0.3V |
| VOUTA or VOUTB to GND .......................................... | –0.3V to +VDD + 0.3V |
| Operating Temperature Range ...................................... | –40° C to +105° C |
| Storage Temperature Range ......................................... | –65° C to +150° C |
| Junction Temperature Range (TJ max) ........................................ | +150° C |
| Power Dissipation ........................................................ | (TJ max — TA)/*θ* JA |
| *θ* JAThermal Impedance ......................................................... | 206° C/W |
| *θ* JCThermal Impedance .......................................................... | 44° C/W |
| Lead Temperature, Soldering: |  |
| Vapor Phase (60s) ............................................................... | +215° C |
| Infrared (15s) ........................................................................ | +220° C |
|  |  |

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

**ELECTROSTATIC**  **DISCHARGE SENSITIVITY**



This integrated circuit can be damaged by ESD. Texas Instru-ments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGE/ORDERING INFORMATION**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | **SPECIFICATION** |  |  |  |
|  |  | **PACKAGE** | **TEMPERATURE** | **PACKAGE** | **ORDERING** | **TRANSPORT** |
| **PRODUCT** | **PACKAGE-LEAD** | **DESIGNATOR(1)** | **RANGE** | **MARKING** | **NUMBER** | **MEDIA, QUANTITY** |
| DAC8532 | MSOP-8 | DGK | –40° C to +105° C | D32E | DAC8532IDGK | Tube, 80 |
|  | " | " | " | " | DAC8532IDGKR | Tape and Reel, |
|  |  |  |  |  |  | 2500 |
|  |  |  |  |  |  |  |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

**ELECTRICAL CHARACTERISTICS**

VDD = +2.7V to +5.5V. –40° C to +105° C, unless otherwise specified.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | **DAC8532** |  |  |  |  |
|  |  |  |  |  |  | |  |
| **PARAMETER** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** | |  |
|  |  |  |  |  |  |  |  |
| **STATIC PERFORMANCE (1**) |  |  |  |  |  |  |  |
| Resolution |  | 16 |  |  | Bits | |  |
| Relative Accuracy |  |  |  | ± 0.0987 | % of FSR | |  |
| Differential Nonlinearity | 16-Bit Monotonic |  |  | ± 1 | LSB | |  |
| Zero-Scale Error |  |  | +5 | +25 | mV | |  |
| Full-Scale Error |  |  | –0.15 | –1.0 | % of FSR | |  |
| Gain Error |  |  |  | ± 1.0 | % of FSR | |  |
| Zero-Scale Error Drift |  |  | ± 20 |  | µ V/° C | |  |
| Gain Temperature Coefficient | RL = 2kΩ , CL = 200pF |  | ± 5 |  | ppm of FSR/° C | |  |
| Channel-to-Channel Matching |  | 15 |  | mV | |  |
| PSRR |  |  | 0.75 |  | mV/V | |  |
|  |  |  |  |  |  |  |  |
| **OUTPUT CHARACTERISTICS (2)** |  |  |  |  |  |  |  |
| Output Voltage Range | To ± 0.003% FSR | 0 |  | VREF | V | |  |
| Output Voltage Settling Time |  |  |  | µ |  |  |
|  | 0200H to FD00H |  | 8 | 10 | s |  |
|  | RL = 2kΩ ; 0pF < CL < 200pF |  |  |  |  |  |  |
|  | RL = 2kΩ ; CL = 500pF |  | 12 |  | µ | s |  |
| Slew Rate | RL = ∞ |  | 1 |  | V/µ s | |  |
| Capacitive Load Stability |  | 470 |  | pF | |  |
|  | RL = 2kΩ |  | 1000 |  | pF | |  |
| Code Change Glitch Impulse | 1LSB Change Around Major Carry |  | 20 |  | nV-s | |  |
| Digital Feedthrough |  |  | 0.5 |  | nV-s | |  |
| DC Crosstalk |  |  | 0.25 |  | LSB | |  |
| AC Crosstalk |  |  | –100 | –96 | dB | |  |
| DC Output Impedance |  |  | 1 |  | Ω |  |  |
| Short-Circuit Current | VDD = +5V |  | 50 |  | mA | |  |
|  | VDD = +3V |  | 20 |  | mA | |  |
| Power-Up Time | Coming Out of Power-Down Mode |  |  |  |  |  |  |
|  | VDD = +5V |  | 2.5 |  | µ | s |  |
|  | Coming Out of Power-Down Mode |  |  |  |  |  |  |
|  | VDD = +3V |  | 5 |  | µ | s |  |
| **AC PERFORMANCE** | BW = 20kHz, VDD = 5V |  |  |  |  |  |  |
| SNR | FOUT = 1kHz, 1st 19 Harmonics Removed |  | 94 |  | dB | |  |
|  |  |  |  |
| THD |  |  | 67 |  | dB | |  |
| SFDR |  |  | 69 |  | dB | |  |
| SINAD |  |  | 65 |  | dB | |  |
|  |  |  |  |  |  |  |  |

2  **DAC8532**



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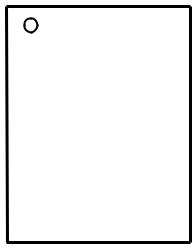
**ELECTRICAL CHARACTERISTICS (Cont.)**

VDD = +2.7V to +5.5V. –40° C to +105° C, unless otherwise specified.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | **DAC8532** |  |  |  |
|  |  |  |  |  |  |  |
| **PARAMETER** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |  |
|  |  |  |  |  |  |  |
| **REFERENCE INPUT** |  |  |  |  |  |  |
| Reference Current | VREF = VDD = +5V |  | 67 | 90 | µ A |  |
|  | VREF = VDD = +3V |  | 40 | 54 | µ A |  |
| Reference Input Range |  | 0 |  | VDD | V |  |
| Reference Input Impedance |  |  | 75 |  | kΩ |  |
|  |  |  |  |  |  |  |
| **LOGIC INPUTS (2)** |  |  |  |  |  |  |
| Input Current |  |  |  | ± 1 | µ A |  |
| VINL, Input LOW Voltage | VDD = +5V |  |  | 0.8 | V |  |
| VINL, Input LOW Voltage | VDD = +3V |  |  | 0.6 | V |  |
| VINH, Input HIGH Voltage | VDD = +5V | 2.4 |  |  | V |  |
| VINH, Input HIGH Voltage | VDD = +3V | 2.1 |  |  | V |  |
| Pin Capacitance |  |  |  | 3 | pF |  |
|  |  |  |  |  |  |  |
| **POWER REQUIREMENTS** |  |  |  |  |  |  |
| VDD |  | 2.7 |  | 5.5 | V |  |
| IDD (normal mode) | DAC Active and Excluding Load Current |  |  |  | µ A |  |
| VDD = +3.6V to +5.5V | VIH = VDD and VIL = GND |  | 500 | 800 |  |
| VDD = +2.7V to +3.6V | VIH = VDD and VIL = GND |  | 450 | 750 | µ A |  |
| IDD (all power-down modes) |  |  |  |  | µ A |  |
| VDD = +3.6V to +5.5V | VIH = VDD and VIL = GND |  | 0.2 | 1 |  |
| VDD = +2.7V to +3.6V | VIH = VDD and VIL = GND |  | 0.05 | 1 | µ A |  |
|  |  |  |  |  |  |  |
| **POWER EFFICIENCY** |  |  |  |  |  |  |
| IOUT/IDD | ILOAD = 2mA, VDD = +5V |  | 89 |  | % |  |
| **TEMPERATURE RANGE** |  |  |  |  |  |  |
| Specified Performance |  | –40 |  | +105 | ° C |  |
|  |  |  |  |  |  |  |

NOTES: (1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded. (2) Ensured by design and characterization, not production tested.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **PIN CONFIGURATION** | | |  |  |  |  |  | **PIN DESCRIPTIONS** | | | | | | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Top View** |  |  |  |  |  |  | **MSOP-8** |  | **PIN** | **NAME** | | | **DESCRIPTION** | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | 1 |  | VDD | | Power supply input, +2.7V to +5.5V. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 2 |  | VREF | | Reference voltage input. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 3 | VOUTB | | | Analog output voltage from DAC B. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 4 | VOUTA | | | Analog output voltage from DAC A. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 5 |  | SYNC |  | Level triggered | | | | | SYNC | input (active LOW). This is the | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | frame synchronization signal for the input data. | | | | | | | | |  |
| VDD | 1 |  |  | 8 | GND | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | |  | |  |  |  |  |  |
|  |  |  |  |  |  |  | When | | SYNC | | goes LOW, it enables the input shift | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | register and data is transferred on the falling edge of | | | | | | | | |  |
| VREF | 2 |  |  | 7 | DIN | | |  |  |  |  |  |  |
|  | **DAC8532** |  |  |  |  |  | SCLK. The action specified by the 8-bit control byte | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  | and 16-bit data word is executed following the 24th | | | | | | | | |  |
| VOUTB | 3 |  |  | 6 | SCLK | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | falling SCLK clock edge (unless SYNC is taken | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VOUTA | 4 |  |  | 5 |  | SYNC |  |  |  |  |  |  | HIGH before this edge in which case the rising edge | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  | of SYNC acts as an interrupt and the write sequence | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | is ignored by the DAC8532). | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 6 |  | SCLK | | Serial Clock Input. Data can be transferred at rates | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | up to 30 MHz at 5V. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 7 |  | DIN | | Serial Data Input. Data is clocked into the 24-bit | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | input shift register on each falling edge of the serial | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | clock input. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  | 8 |  | GND | | Ground reference point for all circuitry on the part. | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



**DAC8532**  3

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**TIMING CHARACTERISTICS(1, 2)**

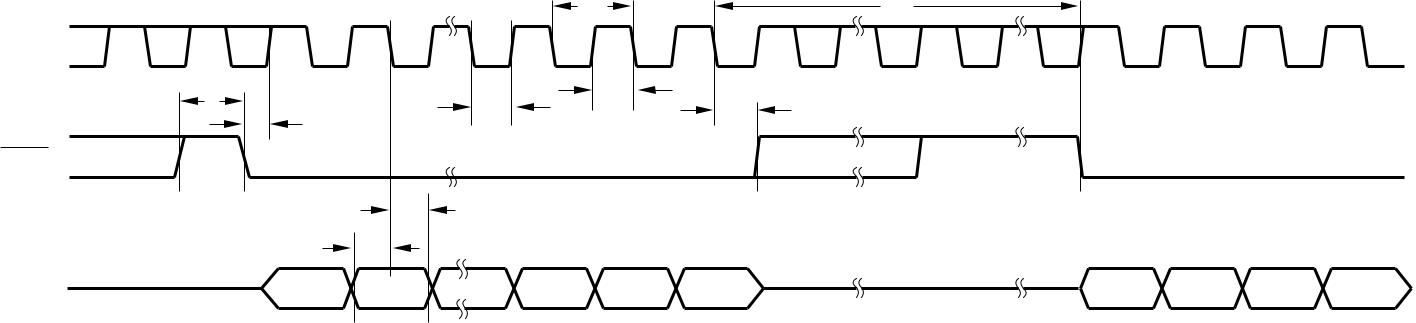
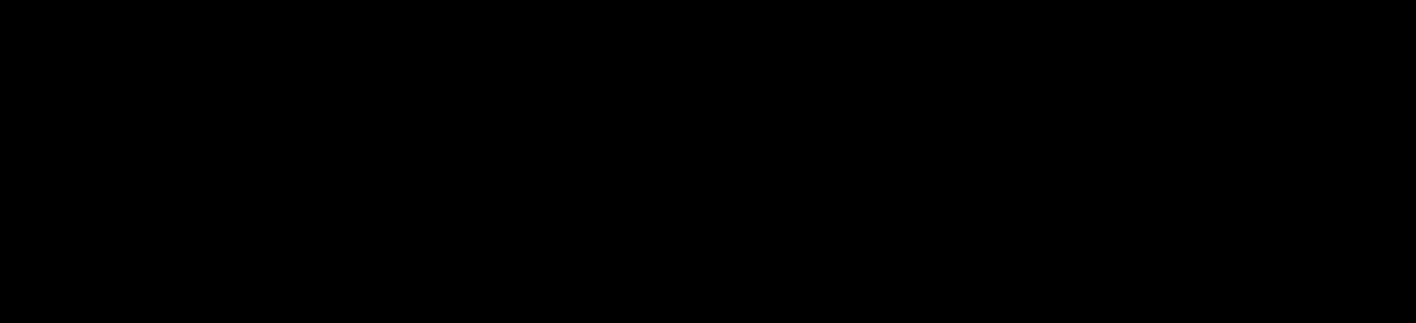
VDD = +2.7V to +5.5V; all specifications –40° C to +105° C unless otherwise noted.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  | **DAC8532** |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **PARAMETER** |  |  |  | **DESCRIPTION** | | | | | | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| t (3) |  |  |  | SCLK Cycle Time | | | | | |  |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |  |  |  | VDD = 2.7V to 3.6V | 50 |  |  | ns | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| t2 |  |  |  | SCLK HIGH Time | | | | | | VDD = 3.6V to 5.5V | 33 |  |  | ns | |  |
|  |  |  | VDD = 2.7V to 3.6V | 13 |  |  | ns | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| t3 |  |  |  | SCLK LOW Time | | | | | | VDD = 3.6V to 5.5V | 13 |  |  | ns | |  |
|  |  |  | VDD = 2.7V to 3.6V | 22.5 |  |  | ns | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| t4 |  |  |  |  |  |  |  |  |  | VDD = 3.6V to 5.5V | 13 |  |  | ns | |  |
| SYNC to SCLK Rising | | | | | | | | |  |  |  |  |  |  |  |
|  |  |  |  | Edge Setup Time | | | | | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  | VDD = 2.7V to 3.6V | 0 |  |  | ns | |  |
| t5 |  |  |  | Data Setup Time | | | | | | VDD = 3.6V to 5.5V | 0 |  |  | ns | |  |
|  |  |  | VDD = 2.7V to 3.6V | 5 |  |  | ns | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| t6 |  |  |  | Data Hold Time | | | | | | VDD = 3.6V to 5.5V | 5 |  |  | ns | |  |
|  |  |  | VDD = 2.7V to 3.6V | 4.5 |  |  | ns | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| t7 | 24th SCLK Falling Edge to | | | | | | | | | VDD = 3.6V to 5.5V | 4.5 |  |  | ns | |  |
|  |  |  |  |  |  |  |
|  |  |  |  | SYNC | | | | Rising Edge | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  | VDD = 2.7V to 3.6V | 0 |  |  | ns | |  |
| t8 |  |  |  |  |  |  |  |  |  | VDD = 3.6V to 5.5V | 0 |  |  | ns | |  |
| Minimum | | | | | SYNC | | | HIGH Time |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  | VDD = 2.7V to 3.6V | 50 |  |  | ns | |  |
|  |  |  |  |  |  |  |  |  |  | VDD = 3.6V to 5.5V | 33 |  |  | ns | |  |
| t9 | 24th SCLK Falling Edge to | | | | | | | | | VDD = 2.7V to 5.5V | 100 |  |  | ns | |  |
|  |  |  | SYNC | | | | Falling Edge | | |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

NOTES: (1) All input signals are specified with tR = tF = 5ns (10% to 90% of VDD) and timed from a voltage level of (VIL + VIH)/2. (2) See Serial Write Operation timing diagram, below. (3) Maximum SCLK frequency is 30MHz at VDD = +3.6V to +5.5V and 20MHz at VDD = +2.7V to +3.6V.

**SERIAL WRITE OPERATION**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | t1 |  |  | t9 |  |
| SCLK |  | 1 | 24 |  |  |  |
|  | t8 | t3 | t2 |  |  |  |
|  |  | t | 7 |  |  |
|  |  | t4 |  |  |  |
|  |  |  |  |  |  |
| SYNC |  |  |  |  |  |  |
|  |  | t6 |  |  |  |  |
|  |  | t5 |  |  |  |  |
| DIN |  | DB23 | DB0 | | DB23 |  |



4  **DAC8532**

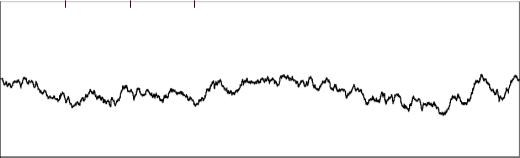
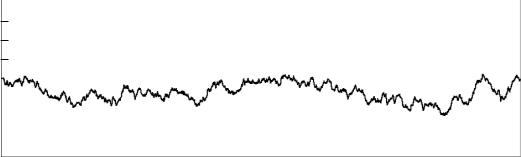


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**TYPICAL CHARACTERISTICS**

At TA = +25° C, unless otherwise noted.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  | LINEARITY ERROR AND | | | | | | | |  |  |  |  |  |
|  |  |  |  |  | DIFFERENTIAL LINEARITY ERROR vs CODE | | | | | | | | | | | |  |  |  |
|  | 64 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 48 |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | VDD = VREF = 5V, TA = 25° C, | | | | |  |  |  |  |  |  |  |  |  |  |  |
| (LSB) | 32 |  |  |  | Channel A Output | | | |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 16 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| LE | –16 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| –32 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –48 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –64 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 2.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 1.5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (LSB) | 1.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0.5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| DLE | 0.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| –0.5 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –1.0 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –1.5 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –2.0 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 2000H 4000H 6000H 8000H A000H | | | | | | | |  |  |  |  |  |  |  |
|  | 0000H | | | | C000H | | E000H | | FFFFH | |  |
|  |  |  |  |  |  |  | Digital Input Code | | | | | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | LINEARITY ERROR AND | | | | | | | |  |  |  |  |  |
|  |  |  |  |  | DIFFERENTIAL LINEARITY ERROR vs CODE | | | | | | | | | | | |  |  |  |
|  | 64 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 48 |  |  | VDD = VREF = 2.7V, TA = 25° C, | | | | | |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| (LSB) | 32 |  |  |  | Channel A Output | | | | |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 16 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| LE | –16 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| –32 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –48 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –64 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 2.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 1.5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (LSB) | 1.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0.5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| DLE | 0.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| –0.5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –1.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –1.5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –2.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 2000H 4000H 6000H 8000H A000H | | | | | | | |  |  |  |  |  |  |  |
|  | 0000H | | | | C000H | | E000H | | FFFFH | |  |



|  |
| --- |
| LE (LSB) |

|  |
| --- |
| DLE (LSB) |

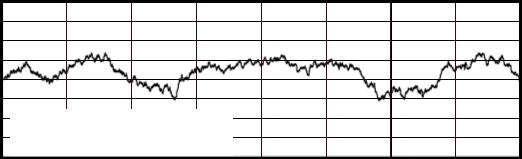
|  |
| --- |
| LE (LSB) |

|  |
| --- |
| DLE (LSB) |

LINEARITY ERROR AND

DIFFERENTIAL LINEARITY ERROR vs CODE

64



48

32

16

0

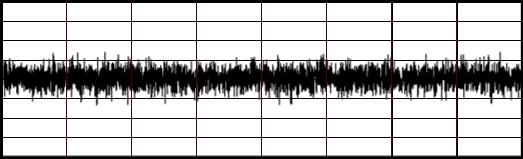
–16

–32 VDD = VREF = 5V, TA = 25° C,

–48 Channel B Output

–64

2.0



1.5

1.0

0.5

0.0

–0.5

–1.0

–1.5

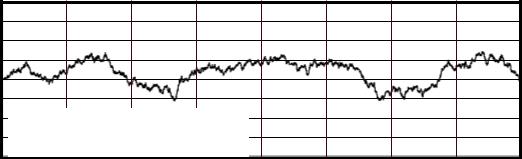
–2.0

0000H 2000H 4000H 6000H 8000H A000H C000H E000H FFFFH Digital Input Code

LINEARITY ERROR AND

DIFFERENTIAL LINEARITY ERROR vs CODE

64



48

32

16

0

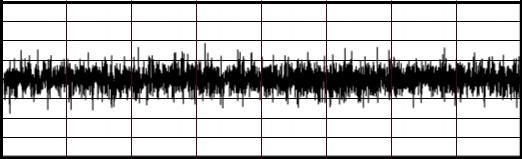
–16

–32 VDD = VREF = 2.7V, TA = 25° C,

–48 Channel B Output

–64

2.0



1.5

1.0

0.5

0.0

–0.5

–1.0

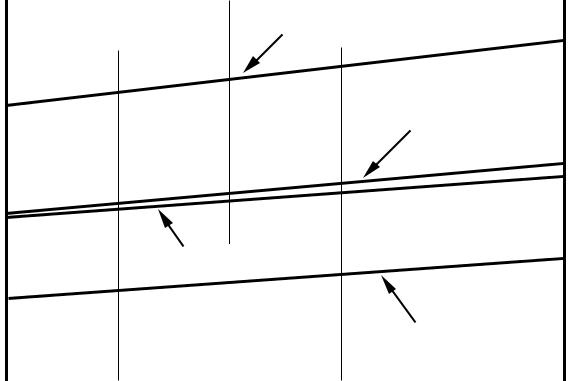
–1.5

–2.0

0000H 2000H 4000H 6000H 8000H A000H C000H E000H FFFFH

Digital Input Code

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | ZERO-SCALE ERROR vs TEMPERATURE | | | | | | | | |  |
| 25 |  |  |  |  |  |  |  |  |  |  |  |
|  |  | VDD = VREF | | | V | DD = 5V, CH | | | B |  |  |
| 20 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | V = 5V, CH A | | |  |

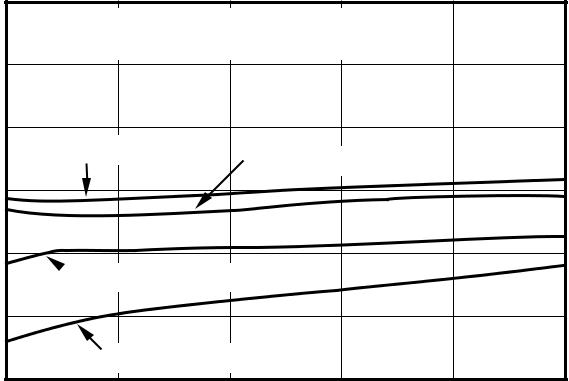


15

10

Digital Input Code

FULL-SCALE ERROR vs TEMPERATURE



(To avoid clipping of the output signal

during the test, VREF = VDD – 10mV)

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| (mV) |  |  |  |  |  |  | DD | |  |  |  |
| 15 |  |  |  |  |  |  |  |  |  |  |
| Error |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| Output | 10 |  |  |  |  |  |  |  |  |  |  |
|  |  | VDD = 2.7V, CH B | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | 5 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | VDD = 2.7V, CH A | |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | –40 | | –10 | 20 | | 50 | 80 | | 105 | |  |
|  |  |  |  | Temperature (° C) | | |  |  |  |  |  |



|  |
| --- |
| Output Error (mV) |



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 5 |  |  |  |  |
| VDD | = 2.7V, CH B | VDD | = 5V, CH B |  |
|  |  |  |
| 0 |  |  |  |  |

–5

 VDD = 2.7V, CH A

–10

VDD = 5V, CH A

–15

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| –40 | –10 | 20 | 50 | 80 | 105 |
|  |  | Temperature (° C) | |  |  |

**DAC8532**  5

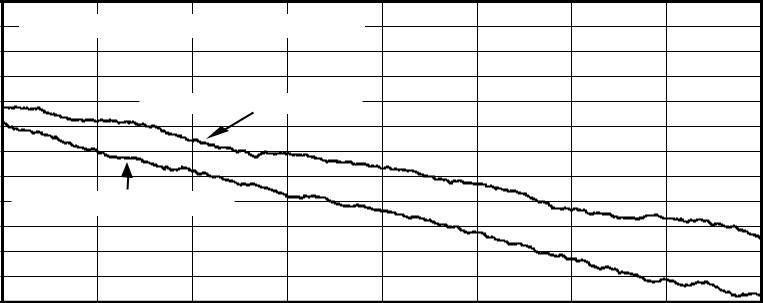
SBAS246A **www.ti.com**

**TYPICAL CHARACTERISTICS (Cont.)**

At TA = +25° C, unless otherwise noted.

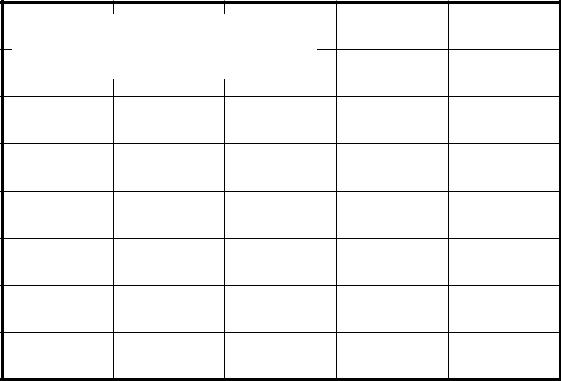
ABSOLUTE ERROR

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 30 |  |  |  |  |  |  |  |  |
|  | 25 | VDD = VREF = 5V, TA = 25° C | |  |  |  |  |  |  |
|  | 20 |  |  |  |  |  |  |  |  |
|  | 15 |  |  |  |  |  |  |  |  |
| (mV) | 10 |  | Channel B Output | |  |  |  |  |  |
| 5 |  |  |  |  |  |  |  |  |
| Error |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |
| Output | –5 |  |  |  |  |  |  |  |  |
| –10 | Channel A Output | |  |  |  |  |  |  |
|  | –15 |  |  |  |  |  |  |  |  |
|  | –20 |  |  |  |  |  |  |  |  |
|  | –25 |  |  |  |  |  |  |  |  |
|  | –30 |  |  |  | A000H |  |  |  |  |
|  | 0000H 2000H | | 4000H 6000H | 8000H | C000H | E000H | FFFFH |  |



Digital Input Code

OUTPUT VOLTAGE DRIFT



VDD = VREF = 5V, TA = 25° C (± 1° C),

Digital Code = 7FFFH

|  |
| --- |
| (25µ V/div) |

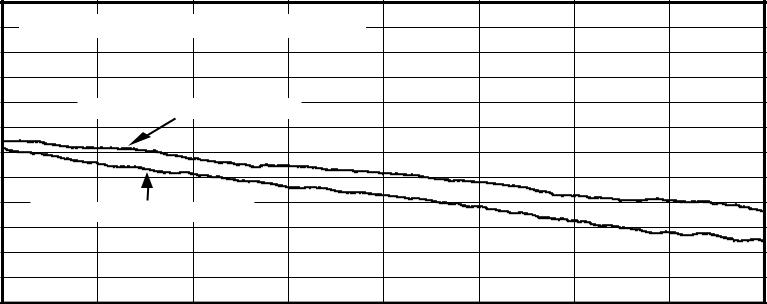
|  |
| --- |
| OUT |

|  |
| --- |
| V |

Time (1min/div)

ABSOLUTE ERROR

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 30 |  |  |  |  |  |  |  |  |  |
|  | 25 | VDD = VREF = 2.7V, TA = 25° C | | | |  |  |  |  |  |
|  | 20 |  |  |  |  |  |  |  |  |  |
|  | 15 |  |  |  |  |  |  |  |  |  |
| (mV) | 10 |  | Channel B Output | |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |  |  |  |
| Error |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |
| Output | –5 |  |  |  |  |  |  |  |  |  |
| –10 |  | Channel A Output | |  |  |  |  |  |  |
|  | –15 |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  | –20 |  |  |  |  |  |  |  |  |  |
|  | –25 |  |  |  |  |  |  |  |  |  |
|  | –30 |  |  |  |  | A000H |  |  |  |  |
|  | 0000H | | 2000H | 4000H 6000H | 8000H | C000H | E000H | FFFFH |  |



Digital Input Code

HISTOGRAM OF CURRENT CONSUMPTION

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 2500 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | VDD = VREF = 5V, | | | |  |  |
|  | 2000 |  |  |  |  | Reference Current Included | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Frequency | 1500 |  |  |  |  |  |  |  |  |  |  |  |
| 1000 |  |  |  |  |  |  |  |  |  |  |  |
|  | 500 |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |  |
|  | 400 | 440 | 480 | 520 | 560 | 600 | 640 | 680 | 720 | 760 | 800 |  |
|  |  |  |  |  | IDD (µ A) | |  |  |  |  |  |  |

|  |
| --- |
| Frequency |

HISTOGRAM OF CURRENT CONSUMPTION

2500

VDD = VREF = 2.7V,

Reference Current Included

2000

1500

1000

500

0

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 280 | 320 | 360 | 400 | 440 | 480 | 520 | 560 | 600 | 640 | 680 |
|  |  |  |  | IDD (µ A) | |  |  |  |  |  |

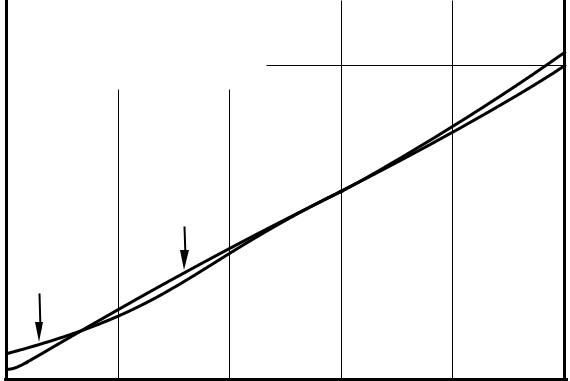
|  |
| --- |
| (V) |

|  |
| --- |
| OUT |

|  |
| --- |
| V |

SINK CURRENT CAPABILITY

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 0.15 |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
| 0.125 |  | VREF = VDD – 10mV | | |  |  |
|  | DAC Loaded with 0000H | | |  |  |
|  |  |  |
|  |  |  |  |
| 0.1 |  |  |  |  |  |  |
|  |  |  |  |  |  |
| 0.075 |  |  |  |  |  |  |
|  |  | VDD = 2.7V | | |  |
|  |  |  |  |
| 0.05 |  |  |  |  |  |  |
| VDD = 5V | | | | |  |
|  |  |
| 0.025 |  |  |  |  |  |  |
|  |  |  |  |  |  |



0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 1 | 2 | 3 | 4 | 5 |
|  |  | ISINK (mA) |  |  |  |

6  **DAC8532**



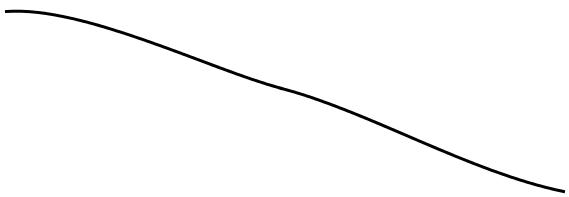
**www.ti.com** SBAS246A

**TYPICAL CHARACTERISTICS (Cont.)**

At TA = +25° C, unless otherwise noted.

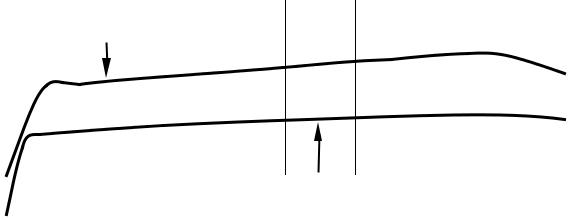
SOURCE CURRENT CAPABILITY

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 5 |  |  |  |  |  |  |  |  |  |  |  |  |
| (V) | 4.95 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| 4.9 |  |  |  |  |  |  |  |  |  |  |  |  |
| OUT |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| V |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 4.85 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | VREF = VDD – 10mV | | | |  |  |  |  |  |  |  |
|  |  |  | DAC Loaded with FFFFH | | | |  |  |  |  |  |  |  |
|  | 4.8 |  | VDD = 5V | |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 | | 1 | | 2 | | 3 | | 4 | | 5 | |  |



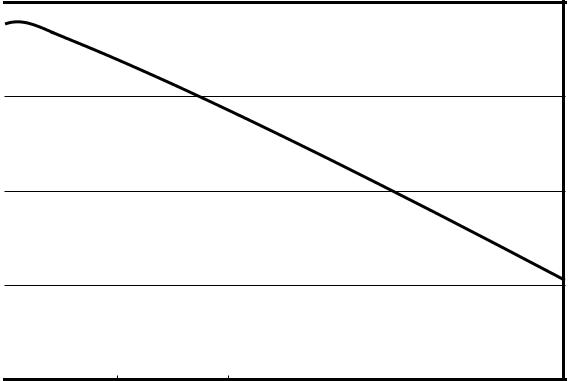
ISOURCE (mA)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | SUPPLY CURRENT vs DIGITAL INPUT CODE | | | | | | | | | | | |  |
|  | 700 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | VDD | = VREF | = 5V |  |  |  |  |  |  |  |  |  |  |
|  | 600 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| µ(A) | 500 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 400 |  |  |  |  |  |  | VDD = VREF = 2.7V | | | |  |  |  |  |
| DD |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 300 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 200 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 100 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0000H 2000H 4000H 6000H 8000H A000H C000H E000H FFFFH | | | | | | | | | | | | | |  |
|  |  |  |  |  |  | Digital Input Code | | | | | | | | |  |



SOURCE CURRENT CAPABILITY

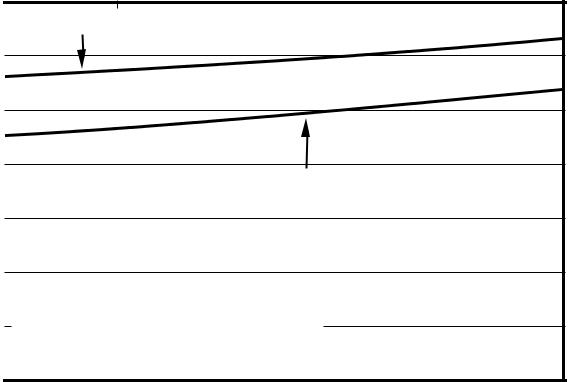
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 2.7 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 2.65 |  |  |  |  |  |  |  |  |  |  |
| (V) | 2.6 |  |  |  |  |  |  |  |  |  |  |
| OUT |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| V |  |  |  |  |  |  |  |  |  |  |  |
|  | 2.55 |  |  |  |  |  |  |  |  |  |  |
|  |  |  | VREF = VDD – 10mV | | | |  |  |  |  |  |
|  |  |  | DAC Loaded with FFFFH | | | |  |  |  |  |  |
|  | 2.5 |  | VDD = 2.7V | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 0 | | 1 | | 2 | | 3 | | 4 | |  |



ISOURCE (mA)

SUPPLY CURRENT vs TEMPERATURE

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 700 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | VDD = VREF = 5V | |  |  |  |  |  |  |  |  |
|  | 600 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 500 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A) | 400 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| µ( |  |  |  |  |  |  |  |  | VDD = VREF | | = 2.7V |  |  |  |
| DD | 300 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| I |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 200 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 100 |  |  |  |  |  | |  | |  |  |  |  |  |
|  |  |  |  | Reference | Current | | Included, | |  |  |  |  |  |
|  |  |  | CH A and CH B Active, No Load | | | | | | |  |  |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | –40 | | | | –10 | | 20 | | | 50 | | 80 | |  |
|  |  |  |  |  |  |  | Temperature (° C) | | | | |  |  |  |



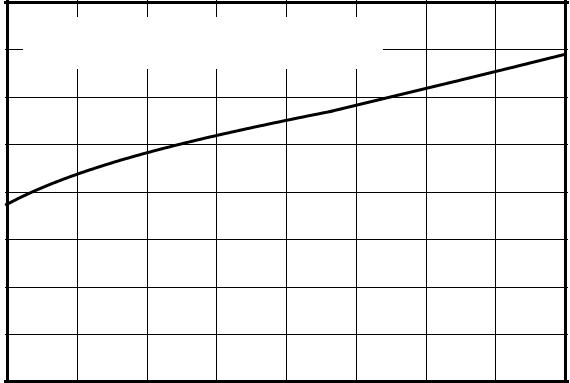
5

105

|  |
| --- |
| DD I (µ A) |

SUPPLY CURRENT vs SUPPLY VOLTAGE

800



VREF = VDD, Both DACs Active,

1. Reference Current Included, No Load

400

2.7 3.05 3.4 3.75 4.1 4.45 4.8 5.15 5.5

VDD (V)



|  |
| --- |
| (nA) |

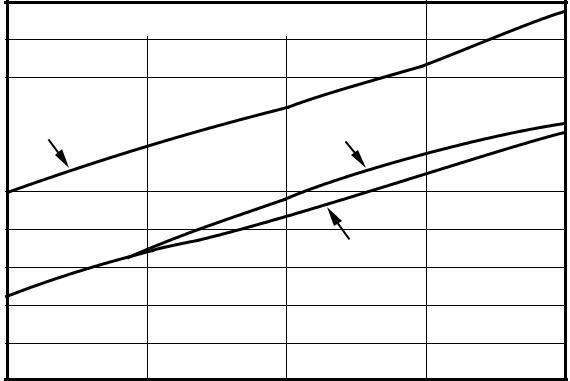
|  |
| --- |
| DD |

|  |
| --- |
| I |



POWER-DOWN CURRENT vs SUPPLY VOLTAGE

50



Reference Current Excluded

45

40

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 35 |  |  |  |  |
| TA | = +105° C | TA = –40° C |  |
| 30 |  |
|  |  |  |  |
|  |  |  |  |

25

20

TA = +25° C

15

10

5

0

2.7 3.4 4.1 4.8 5.5

VDD (V)

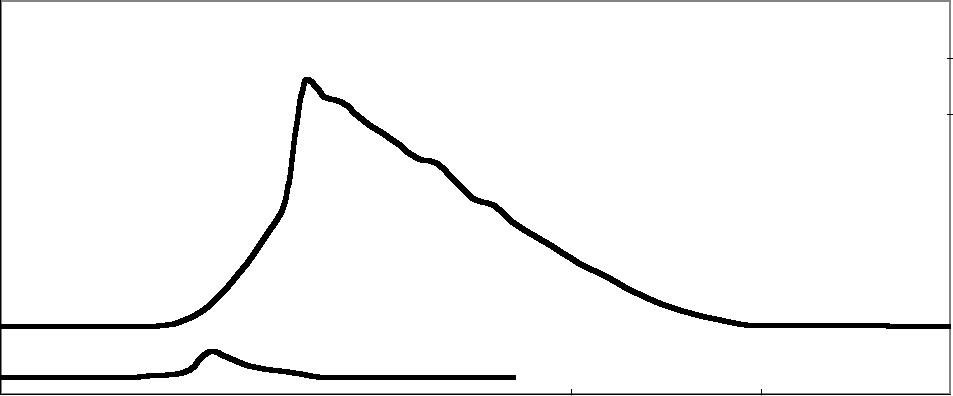
**DAC8532**  7

SBAS246A **www.ti.com**

**TYPICAL CHARACTERISTICS**

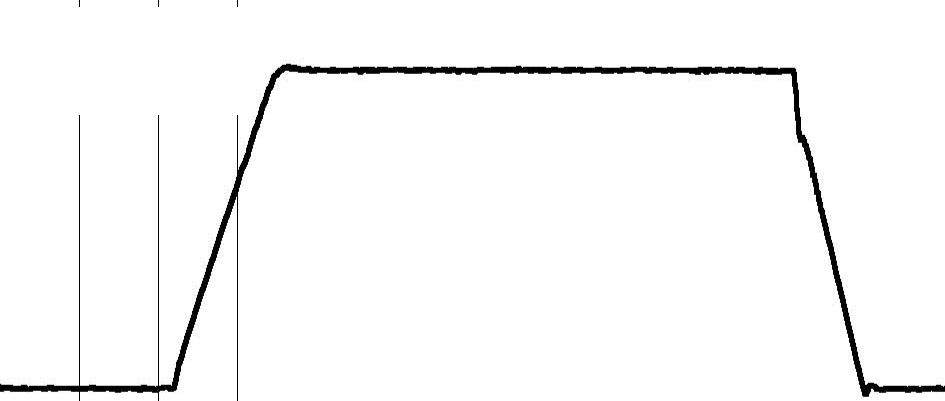
At TA = +25° C, unless otherwise noted.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | SUPPLY CURRENT vs LOGIC INPUT VOLTAGE | | | | | | | | | | | | | | |  |  |  |
|  | 1150 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | TA = 25° C, | | SYNC | | |  | Input (All Other | | | Inputs = GND) | | | | | |  |  |
|  | 1050 |  |  |  |  |  |  |  |  | Reference Current | | | | | | | Included, | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  | CHA and CHB | | | | | Active, | |  |  |
|  | 950 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | No Load | | |  |  |
|  |  |  |  |  |  |  |  | VDD = VREF = 5V | | | | | |  |  |  |  |  |  |  |
| A) | 850 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| µ( |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| DD | 750 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 650 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 550 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 450 |  |  |  |  |  |  |  |  | VDD = VREF = 2.7V | | | | | | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 | | 1 | | | 2 | | 3 | | | | 4 | | | |  |  | 5 | |  |



VLOGIC (V)

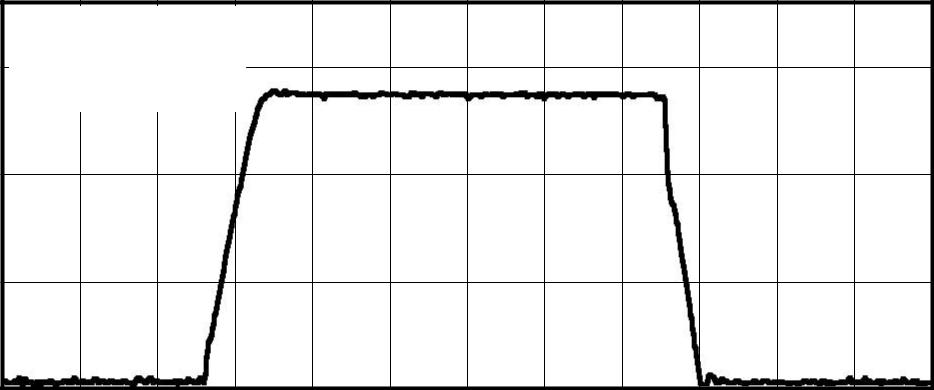
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | HALF-SCALE SETTLING TIME | | | | | | | | |  |
|  |  |  |  | (Large Signal) | | | | | | | |  |
|  | 3 |  |  |  |  |  |  |  |  |  |  |  |
|  | VDD | = VREF = 5V, |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 2.5 | Output Loaded with | |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | 2kΩ | and 200pF |  |  |  |  |  |  |  |  |  |
|  |  | to GND. | |  |  |  |  |  |  |  |  |  |
| (V) | 2 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| 1.5 |  |  |  |  |  |  |  |  |  |  |  |
| OUT |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| V |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 1 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0.5 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | Time (2µ s/div) | | | | | | | |  |
|  |  |  |  |  |



HALF-SCALE SETTLING TIME

(Large Signal)

VDD = VREF = 2.7V,



Output Loaded with

1.5 2kΩ and 200pF

to GND.

|  |  |
| --- | --- |
| (V) | 1 |
| OUT |  |
| V |  |

0.5

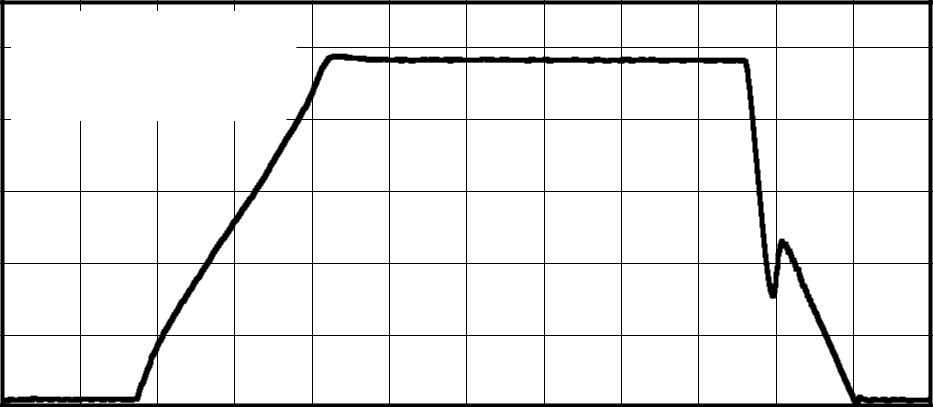
0

Time (2µ s/div)

**(Cont.)**

FULL-SCALE SETTLING TIME

(Large Signal)



VDD = VREF = 5V,

1. Output Loaded with 2kΩ and 200pF to

4 GND

|  |  |  |
| --- | --- | --- |
| (V) | 3 |  |
| OUT |  |
|  |  |
| V |  |  |

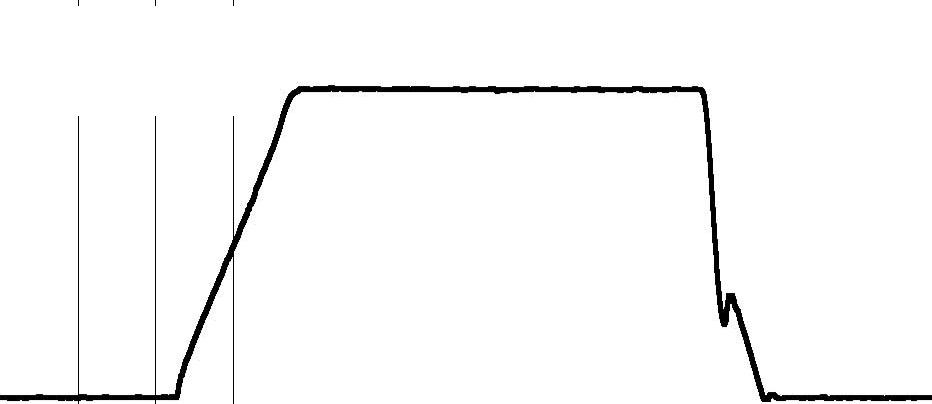
2

1

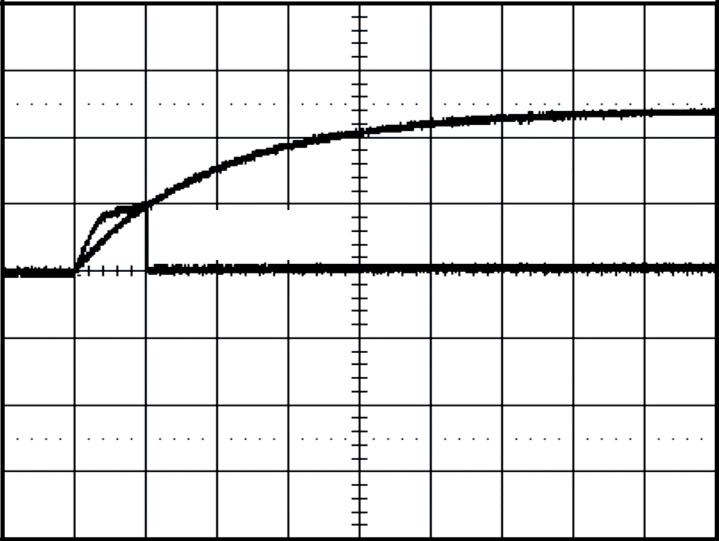
0

Time (2µ s/div)

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | FULL-SCALE SETTLING TIME | | | | | | | | |  |
|  |  |  |  | (Large Signal) | | | | | | | |  |
|  | 3.5 |  |  |  |  |  |  |  |  |  |  |  |
|  | VDD | = VREF = 2.7V, |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 3 | Output Loaded with | |  |  |  |  |  |  |  |  |  |
|  | 2kΩ | and 200pF |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 2.5 | to GND. | |  |  |  |  |  |  |  |  |  |
| (V) |  |  |  |  |  |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| OUT | 1.5 |  |  |  |  |  |  |  |  |  |  |  |
| V |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 1 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0.5 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | Time (2µ s/div) | | | | | | | |  |
|  |  |  |  |  |



POWER-ON RESET TO ZERO-SCALE



Loaded with 2kΩ to GND

VDD (2V/div)

VOUT (1V/div)

Time (100µ s/div)

8  **DAC8532**

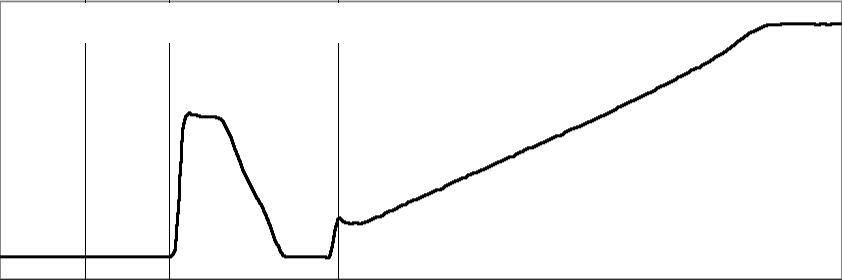


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**TYPICAL CHARACTERISTICS**

At TA = +25° C, unless otherwise noted.

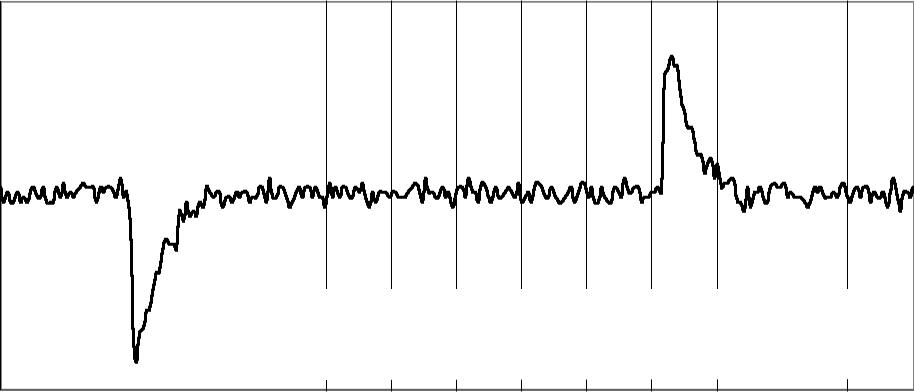
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  | EXITING POWER-DOWN MODE | | | | | | |  |
|  | 5.5 |  |  |  |  |  |  |  |  |  |  |
|  | VDD | = VREF | = 5V |  |  |  |  |  |  |  |
|  | 5 |  |  |  |  |  |  |  |
|  | Power Up to Code | | | FFFFH |  |  |  |  |  |  |
|  | 4.5 |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 4 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 3.5 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| (V) | 3 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| 2.5 |  |  |  |  |  |  |  |  |  |  |
| OUT |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| V | 2 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 1.5 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 1 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 0.5 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | 0 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  | –0.5 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | Time (1µ s/div) | | | | | |  |
|  |  |  |  |  |  |



OUTPUT GLITCH

(Mid-Scale)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 2.54 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 20mV/div) | 2.52 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| 2.5 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| (V, | 2.48 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| OUT | 2.46 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| V |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 2.44 |  |  |  |  | VDD = VREF = 5V | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | Code 8000H to 7FFF | | H to | 8000 | H |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | (Glitch Occurs Every | | N • 4096 | | Code | | Boundary) |  |
|  | 2.42 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | Time (1µ s/div) | | | | | |  |
|  |  |  |  |  |  |  |  |

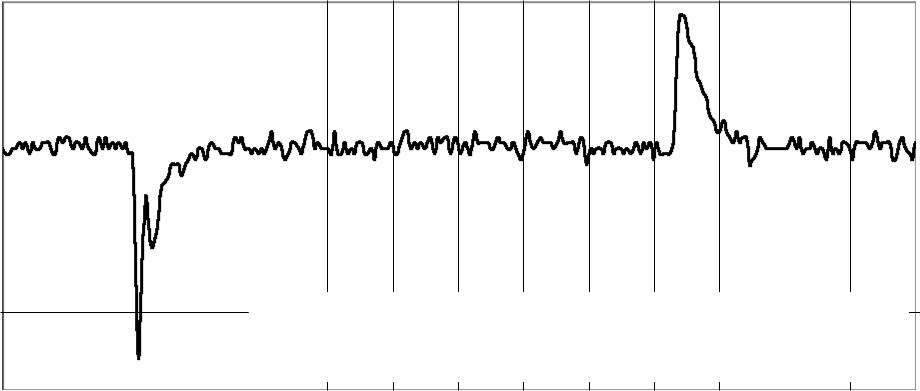


**(Cont.)**

OUTPUT GLITCH

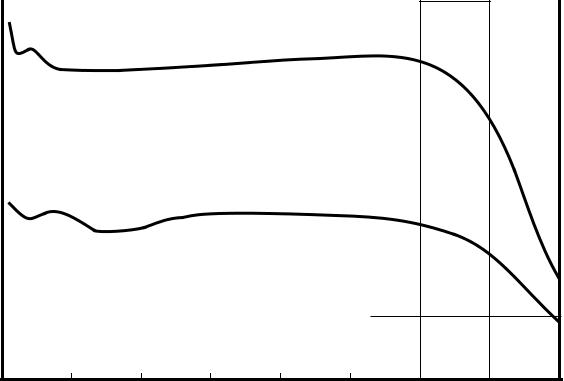
(Worst Case)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 4.72 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | 4.7 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | 4.68 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 20mV/div) | 4.66 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 4.64 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| (V, | 4.62 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 4.6 |  |  |  |  |  |  |  |  |
| OUT |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| V | 4.58 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | 4.56 |  |  |  |  | VDD = VREF = 5V | |  |  |
|  | 4.54 |  |  |  |  | Code F000H to EFFFH to F000H | |  |  |
|  |  |  |  |  | (Glitch Occurs Every N • 4096 Code | | Boundary) |  |
|  |  |  |  |  |  |  |
|  | 4.52 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | Time (1µ s/div) | |  |
|  |  |  |  |  |  |  |  |



SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 96 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 94 |  |  |  | VDD = 5V | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| (dB) | 92 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 90 |  |  | VDD = 2.7V | |  |  |  |  |  |  |  |  |
| SNR |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 88 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 86 |  |  | VDD = | VREF | | | |  |  |  |  |  |
|  |  |  | –1dB FSR Digital Input, FS | | | | | = 52ksps | | |  |  |
|  |  |  |  |  |  |
|  |  |  |  | Measurement Bandwidth = 20kHz | | | | | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |



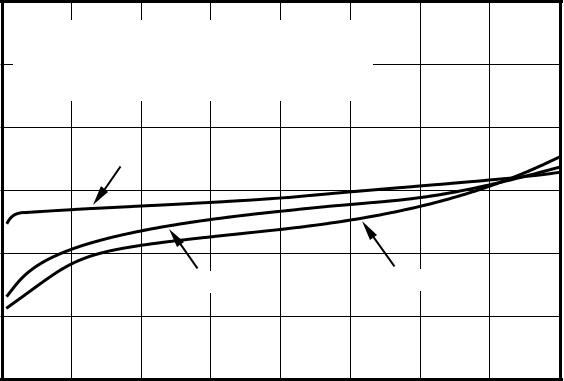
84

1. 500 1000 1500 2000 2500 3000 3500 4000 Output Frequency (Hz)

TOTAL HARMONIC DISTORTION

vs OUTPUT FREQUENCY

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 0 |  |  |  |  |  |  |  |  |  |
|  |  | VDD = VREF = 5V | |  |  |  |  |  |  |  |
|  | –20 | –1dB FSR Digital Input, FS = 52ksps | | | | |  |  |  |  |
|  |  | Measurement Bandwidth = 20kHz | | | | |  |  |  |  |
|  | –40 |  |  |  |  |  |  |  |  |  |
| (dB) |  |  | THD |  |  |  |  |  |  |  |
| –60 |  |  |  |  |  |  |  |  |  |
| THD |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  | –80 |  |  |  |  |  |  |  |  |  |
|  |  |  | 2nd Harmonic | | | 3rd Harmonic | | |  |  |
|  | –100 |  |  |  |  |  |  |  |  |  |
|  | –120 |  |  |  |  |  |  |  |  |  |
|  | 0 | 500 | 1000 | 1500 | 2000 | 2500 | 3000 | 3500 | 4000 |  |



Output Frequency (Hz)



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**THEORY OF OPERATION**

**DAC SECTION**

The architecture of each channel of the DAC8532 consists of a resistor string DAC followed by an output buffer amplifier. Figure 1 shows a simplified block diagram of the DAC architecture.

|  |  |  |
| --- | --- | --- |
|  | VREF |  |
|  | REF (+) |  |
| DAC Register | Resistor String | VOUTX |
|  | REF(–) |  |
|  |  | Output |
|  |  | Amplifier |
|  | GND |  |

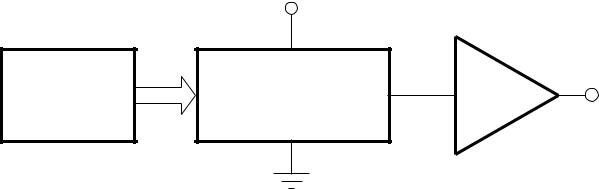


FIGURE 1. DAC8532 Architecture.

The input coding for each device is unipolar straight binary, so the ideal output voltage is given by:

|  |  |  |  |
| --- | --- | --- | --- |
| VOUTX = | VREF• | D |  |
|  |  |
| 65536 |  |
|  |  |  |

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535. VOUTX refers to channel A or B.

**RESISTOR STRING**

The resistor string section is shown in Figure 2. It is simply a divide-by-2 resistor followed by a string of resistors, each of value R. The code loaded into the DAC register deter-mines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

**OUTPUT AMPLIFIER**

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output which approaches an output range of 0V to VDD (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabili-ties of the output amplifier can be seen in the typical charac-teristics.

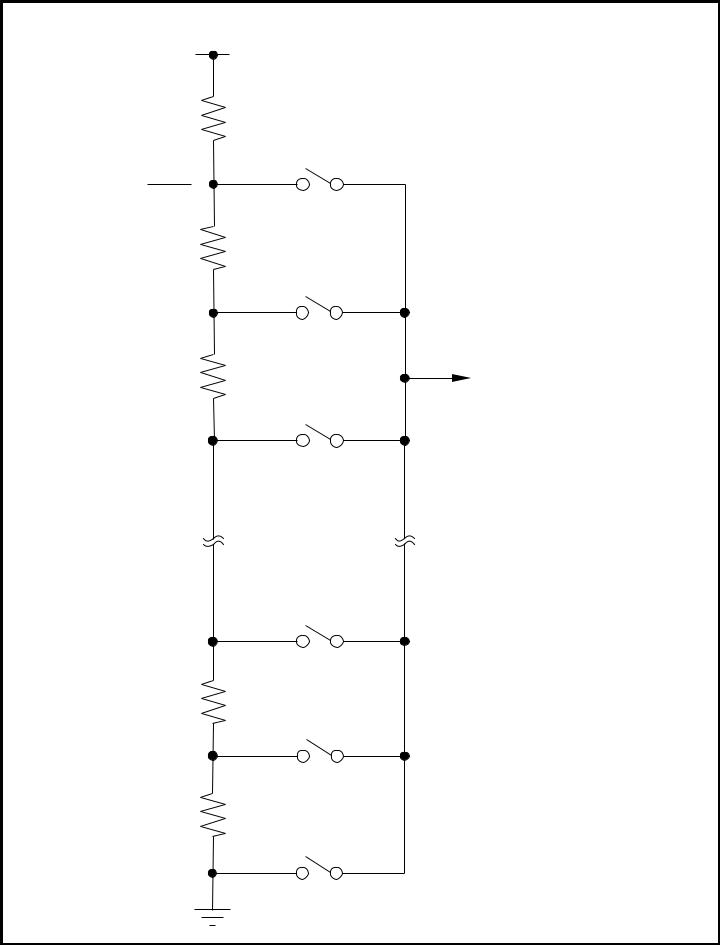
**SERIAL INTERFACE**

The DAC8532 uses a 3-wire serial interface (SYNC, SCLK, and DIN), which is compatible with SPI™, QSPI™, and Microwire™ interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

SPI and QSP are registered trademarks of Motorola.

Microwire is a registered trademark of National Semiconductor.

VREF



RDIVIDER

VREF

2

R

To Output

R

Amplifier

(2x Gain)

R

R

FIGURE 2. Resistor String.

The write sequence begins by bringing the SYNC line LOW. Data from the DIN line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8532 compatible with high speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the programmed function is executed (i.e., a change in Data Buffer contents, DAC Register contents, and/or a change in the power-down mode of a specified channel or channels).

At this point, the SYNC line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th

falling SCLK edge to the next falling SYNC edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the digital input levels are as close to each rail as possible. (Please refer to the “Typical Characteristics” sec-tion for the “Supply Current vs Logic Input Voltage” transfer characteristic curve).

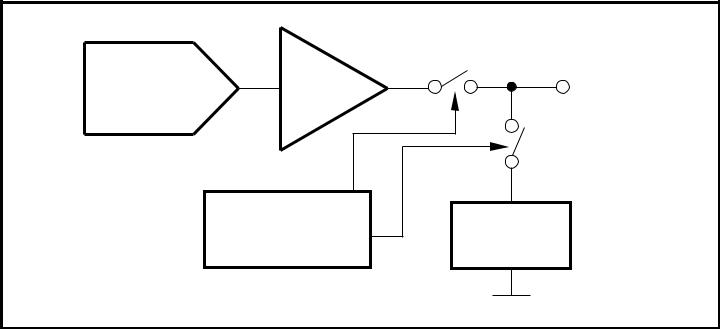
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**INPUT SHIFT REGISTER**

The input shift register of the DAC8532 is 24 bits wide (see Figure 5) and is made up of 8 control bits (DB16-DB23) and 16 data bits (DB0-DB15). The first two control bits (DB22 and DB23) are reserved and must be “0” for proper operation. LD A (DB20) and LD B (DB21) control the updating of each analog output with the specified 16-bit data value or power-down command. Bit DB19 is a “Don't Care” bit which does not affect the operation of the DAC8532 and can be 1 or 0. The following control bit, Buffer Select (DB18), controls the destination of the data (or power-down command) between DAC A and DAC B. The final two control bits, PD0 (DB16) and PD1 (DB17), select the power-down mode of one or both of the DAC channels. The four modes are normal mode or any one of three power-down modes. A more complete description of the operational modes of the DAC8532 can be found in the Power-Down Modes section. The remaining sixteen bits of the 24-bit input word make up the data bits. These are transferred to the specified Data Buffer or DAC Register, depending on the command issued by the control byte, on the 24th falling edge of SCLK. Please refer to Tables II and III for more information.



|  |  |  |  |
| --- | --- | --- | --- |
| Resistor | Amplifier | VOUTX |  |
| String DAC |  |

Power-down Resistor

Circuitry Network



FIGURE 3. Output Stage During Power-Down (High-Impedance)

**SYNC INTERRUPT**

In a normal write sequence, the SYNC line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if SYNC is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents or a change in the operating mode occurs (see Figure 4).

**POWER-ON RESET**

The DAC8532 contains a power-on reset circuit that con-trols the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages

**DAC8532**

are set to zero-scale; they remain there until a valid write sequence and load command is made to the respective DAC channel. This is useful in applications where it is important to know the state of the output of each DAC output while the device is in the process of powering up.

No device pin should be brought high before power is applied to the device.

**POWER-DOWN MODES**

The DAC8532 utilizes four modes of operation. These modes are accessed by setting two bits (PD1 and PD0) in the control register and performing a “Load” action to one or both DACs. Table I shows how the state of the bits correspond to the mode of operation of each channel of the device. (Each DAC channel can be powered down simultaneously or indepen-dently of each other. Power-down occurs after proper data is written into PD0 and PD1 and a “Load” command occurs.) Please refer to the "Operation Examples" section for addi-tional information.

|  |  |  |
| --- | --- | --- |
| **PD1 (DB17)** | **PD0 (DB16)** | **OPERATING MODE** |
|  |  |  |
| 0 | 0 | Normal Operation |
| — | — | Power-Down Modes |
| 0 | 1 | Output Typically 1kΩ to GND |
| 1 | 0 | Output Typically 100kΩ to GND |
| 1 | 1 | High Impedance |
|  |  |  |

TABLE I. Modes of Operation for the DAC8532.

When both bits are set to 0, the device works normally with a typical power consumption of 500µ A at 5V. For the three power-down modes, however, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options for power-down: The output is con-nected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Impedance). The output stage is illustrated in Figure 3.

All analog circuitry is shut down when the power-down mode is activated. Each DAC will exit power-down when PD0 and PD1 are set to 0, new data is written to the Data Buffer, and the DAC channel receives a “Load” command. The time to exit power-down is typically 2.5µ s for VDD = 5V and 5µ s for VDD = 3V (See the Typical Characteristics).



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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 24th Falling | | | |  |  |  |  |  |  | 24th Falling | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Edge | | |  |  |  |  |  |  | Edge | |  |  |  |  |
|  |  |  |  |  |  | SCLK | | | | |  |  |  |  |  | 1 |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  | 1 |  | 2 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | SYNC | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | | | | | | | | | | | | |  |  |  |  | | | | | |  | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | Invalid Write-Sync Interrupt: | | | | | | | | | | | | | | |  |  |  | Valid Write -Buffer/DAC Update: | | | | | | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  | SYNC HIGH before 24th Falling Edge | | | | | | | | | | | | | | | | | | | SYNC HIGH after 24th Falling Edge | | | | | | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | DIN | | |  |  |  |  |  | DB23 DB22 | | | | |  |  |  |  | DB0 | | |  |  |  | DB23 DB22 | | |  |  | DB1 DB0 | | |  |  |  |  |  |  |
|  | | | | | | | | | | | |  | |  | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | | | | | | | | | | | | | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| FIGURE 4. Interrupt and Valid | | | | | | | | | | | | SYNC | | Timing. | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **DB23** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **DB12** |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 0 |  |  |  | 0 |  |  |  |  | LDB |  |  | LDA | | |  |  | X | | |  | Buffer Select | | | | | | | |  | PD1 | | PD0 |  |  | D15 | |  | D14 |  | D13 |  | D12 |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **DB11** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **DB0** |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | D11 | |  |  | D10 | |  |  |  | D9 |  |  | D8 | | |  |  | D7 | | |  |  |  |  | D6 | | |  |  |  | D5 | | D4 |  |  | D3 | |  | D2 |  | D1 |  | D0 |  |
|  | |  |  |  |  |  |  | |  | |  |  |  |  |  | |  | | |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| FIGURE 5. DAC8532 Data Input Register Format. | | | | | | | | | | | | | | | | | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **D23** | |  |  | **D22** | **D21** | |  |  | **D20** |  |  | **D19** | |  | **D18** | |  |  |  | **D17** |  |  |  | **D16** | | | **D15** | | | **D14** |  | **D13-D0** |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **DESCRIPTION** | | | |  |  |
|  | Reserved | | Reserved | | | Load B | |  | Load A | | Don’t Care | | | |  | Buffer Select | | | |  | PD1 |  |  |  | PD0 | | | MSB | | | MSB-1 | MSB-2...LSB | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | |  | |  |  |  |  |  |  |
|  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | (Always |  | | Write 0) | |  |  |  |  |  |  |  |  |  |  | 0 = A, 1 = B | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | |  |  |  | |  |  |  |  | |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | | |  |  |  |  |
| 0 | |  | 0 | | | 0 |  |  | 0 | |  |  | X | |  | # | |  |  |  | 0 |  |  | 0 | | |  |  |  |  | Data | |  |  |  | WR Buffer # w/Data | | | | |  |  |  |  |
|  | |  |  |  | |  |  |  |  | |  |  |  |  |  |  | |  |  |  |  | |  |  |  |  |  |  |  |  |  | |  |  |  |  |  | | | | | |  |  |
| 0 | |  | 0 | | | 0 |  |  | 0 | |  |  | X | |  | # | |  |  |  | (see | | | Table III) | | | |  |  |  | X | |  |  |  | WR Buffer # w/Power-Down Command | | | | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | |  | 0 | | | 0 |  |  | 1 | |  |  | X | |  | # | |  |  |  | 0 |  |  | 0 | | |  |  |  |  | Data | |  |  |  | WR Buffer # w/Data and Load DAC A | | | | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | | | | | |  |
| 0 | |  | 0 | | | 0 |  |  | 1 | |  |  | X | |  | 0 | |  |  |  | (see | | Table III) | | | | |  |  |  | X | |  |  |  | WR Buffer A w/Power-Down Command and LOAD DAC A | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (DAC A Powered Down) | | | | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | |  |  | | |  |  |  |  | |  |  |  |  |  |  | |  |  |  |  | | | | |  |  |  |  |  |  | |  |  |  |  |  | | | | | | |  |
| 0 | |  | 0 | | | 0 |  |  | 1 | |  |  | X | |  | 1 | |  |  |  | (see | | Table III) | | | | |  |  |  | X | |  |  |  | WR Buffer B w/Power-Down Command and LOAD DAC A | | | | | | | |  |
|  | |  |  |  | |  |  |  |  | |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  | | | | | |  |  |
| 0 | |  | 0 | | | 1 |  |  | 0 | |  |  | X | |  | # | |  |  |  | 0 |  |  | 0 | | |  |  |  |  | Data | |  |  |  | WR Buffer # w/Data and Load DAC B | | | | | | |  |  |
|  | |  |  |  | |  |  |  |  | |  |  |  |  |  |  | |  |  |  |  | |  |  |  |  |  |  |  |  |  | |  |  |  |  |  | | | | | | |  |
| 0 | |  | 0 | | | 1 |  |  | 0 | |  |  | X | |  | 0 | |  |  |  | (see | | Table III) | | | | |  |  |  | X | |  |  |  | WR Buffer A w/Power-Down Command and LOAD DAC B | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  | | | | | | |  |
| 0 | |  | 0 | | | 1 |  |  | 0 | |  |  | X | |  | 1 | |  |  |  | (see | | Table III) | | | | |  |  |  | X | |  |  |  | WR Buffer B w/ Power-Down Command and LOAD DAC B | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (DAC B Powered Down) | | | | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | |  | 0 | | | 1 |  |  | 1 | |  |  | X | |  | # | |  |  |  | 0 |  |  | 0 | | |  |  |  |  | Data | |  |  |  | WR Buffer # w/Data and Load DACs A and B | | | | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  | | | | | | |  |
| 0 | |  | 0 | | | 1 |  |  | 1 | |  |  | X | |  | 0 | |  |  |  | (see Table III) | | | | | | |  |  |  | X | |  |  |  | WR Buffer A w/Power-Down Command and Load DACs A | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | and B (DAC A Powered Down) | | | | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  | | | | | | |  |
| 0 | |  | 0 | | | 1 |  |  | 1 | |  |  | X | |  | 1 | |  |  |  | (see Table III) | | | | | | |  |  |  | X | |  |  |  | WR Buffer B w/Power-Down Command and Load DACs A | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | and B (DAC B Powered Down) | | | | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | |  |  |  | |  | | |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| TABLE II. Control Matrix. | | | | | | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | **D17** | |  |  |  |  |  |  |  | **D16** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **OUTPUT IMPEDANCE POWERDOWN COMMANDS** | | | | | | | | | |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | PD1 | |  |  |  |  |  |  |  | PD0 | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 0 | | |  |  |  |  |  | 1 | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1kΩ | | |  |  |  |  |  |  |
|  |  |  | 1 | | |  |  |  |  |  | 0 | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 100kΩ | | |  |  |  |  |  |  |
|  |  |  | 1 | | |  |  |  |  |  | 1 | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | High Impedance | | | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

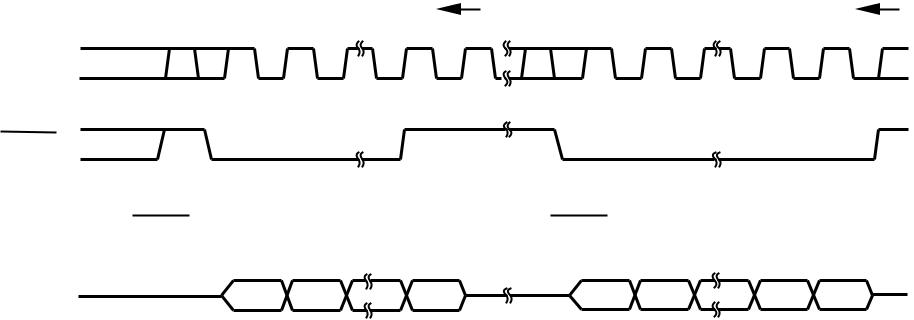


TABLE III. Power-Down Commands.

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**OPERATION EXAMPLES**

**Example 1: Write to Data Buffer A; Write to Data Buffer B; Load DACA and DACB Simultaneously** • 1st—Write to Data Buffer A:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** | **......** | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 0 | 0 | X | 0 | 0 | 0 | D15 | ..... | D1 | D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

• 2nd—Write to Data Buffer B and Load DAC A and DAC B simultaneously:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** | **......** | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 1 | 1 | X | 1 | 0 | 0 | D15 | ..... | D1 | D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

The DACA and DACB analog outputs simultaneously settle to the specified values upon completion of the 2nd write sequence. (The “Load” command moves the digital data from the data buffer to the DAC register at which time the conversion takes place and the analog output is updated. “Completion” occurs on the 24th falling SCLK edge after SYNC LOW.)

**Example 2: Load New Data to DACA and DACB Sequentially**

• 1st—Write to Data Buffer A and Load DAC A: DACA output settles to specified value on completion:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** | **......** | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 0 | 1 | X | 0 | 0 | 0 | D15 | ..... | D1 | D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

• 2nd—Write to Data Buffer B and Load DAC B: DACB output settles to specified value on completion:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** | **......** | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 0 | X | 1 | 0 | 0 | D15 | ..... | D1 | D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |

After completion of the 1st write cycle, the DACA analog output settles to the voltage specified; upon completion of write cycle 2, the DACB analog output settles.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Example 3: Power-Down DACA to 1k**Ω | | | | | **and Power-Down DACB to 100k**Ω **Simultaneously** | | | | | |  |  |  |  |
| • 1st—Write power-down command to Data Buffer A: | | | | | | |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** |  | **......** |  | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 0 | 0 | X | 0 | 0 | 1 |  |  |  | Don’t Care | |  |
|  |  |  |  |  |  |  |  |  |  |  | |  |  |  |
| • 2nd—Write power-down command to Data Buffer B and Load DACA and DACB simultaneously: | | | | | | | | | | | |  |  |  |
|  |  |  |  |  |  |  |  |  |  | |  |  |  |  |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** |  | **......** |  | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 1 | 1 | X | 1 | 1 | 0 |  |  |  | Don’t Care | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

The DACA and DACB analog outputs simultaneously power-down to each respective specified mode upon completion of the 2nd write sequence.

**Example 4: Power-Down DACA and DACB to High Impedance Sequentially:**

• 1st—Write power-down command to Data Buffer A and Load DAC A: DAC A output = High-Z:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** | **......** |  | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 0 | 1 | X | 0 | 1 | 1 |  |  | Don’t Care | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |

• 2nd—Write power-down command to Data Buffer B and Load DAC B: DAC B output = High-Z:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Reserved** | **Reserved** | **LDB** | **LDA** | **DC** | **Buffer Select** | **PD1** | **PD0** | **DB15** | **......** |  | **DB1** | **DB0** |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 | | 0 | 1 | 0 | X | 1 | 1 | 1 |  |  | Don’t Care | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |

The DACA and DACB analog outputs sequentially power-down to high impedance upon completion of the 1st and 2nd write sequences, respectively.



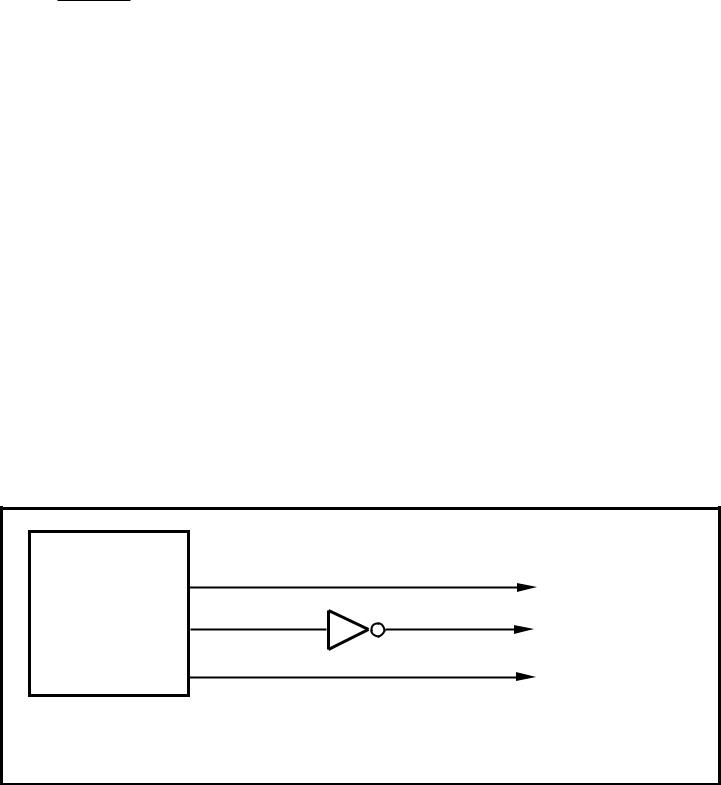
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**MICROPROCESSOR INTERFACING**

**DAC8532 to 8051 INTERFACE**

Figure 6 shows a serial interface between the DAC8532 and a typical 8051-type microcontroller. The setup for the inter-face is as follows: TXD of the 8051 drives SCLK of the DAC8532, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8532, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle is initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which presents the LSB first, while the DAC8532 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and “mirror” the data as needed.

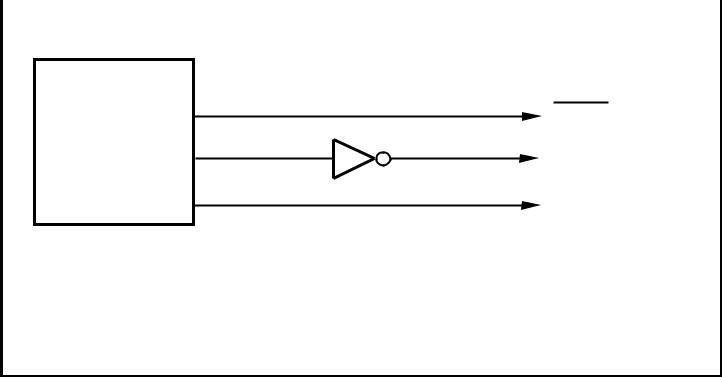
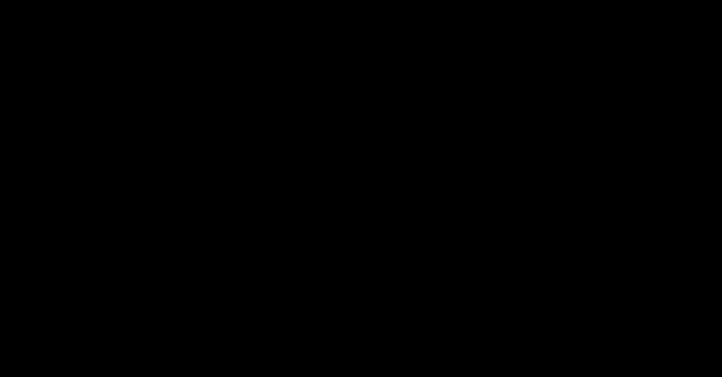


|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 80C51/80L51(1) |  | **DAC8532**(1) | |  |
| P3.3 |  |  |  |  |
| SYNC |  |
| TXD | SCLK | | |  |
| RXD | DIN | | |  |
| NOTE: (1) Additional pins omitted for clarity. |  |  |  |  |

FIGURE 6. DAC8532 to 80C51/80L51 Interface.

**DAC8532 to Microwire INTERFACE**

Figure 7 shows an interface between the DAC8532 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8532 on the rising edge of the SK signal.



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| MicrowireTM | | | **DAC8532**(1) |  |
|  |  |  | SYNC |  |
|  | CS |  |
|  | SK | | SCLK |  |
| SO | | | DIN |  |

NOTE: (1) Additional pins omitted for clarity.

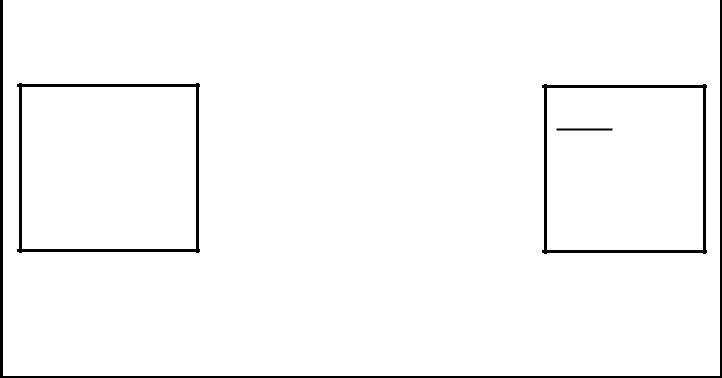
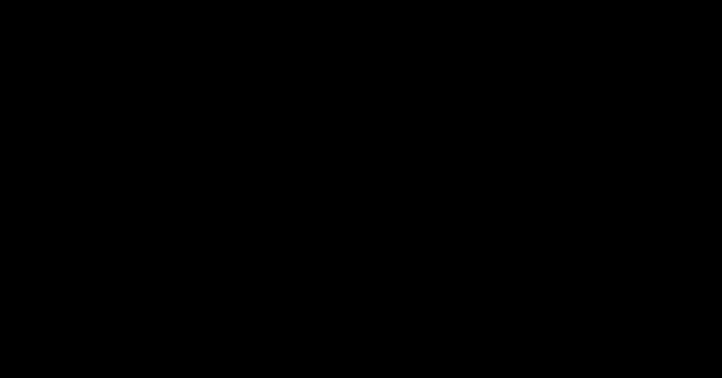
Microwire is a registered trademark of National Semiconductor.

FIGURE 7. DAC8532 to Microwire Interface.

**DAC8532 to 68HC11 INTERFACE**

Figure 8 shows a serial interface between the DAC8532 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8532, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to the 8051 diagram.

|  |  |
| --- | --- |
| 68HC11(1) | **DAC8532**(1) |



PC7  SYNC

SCK  SCLK

MOSI  DIN

NOTE: (1) Additional pins omitted for clarity.

FIGURE 8. DAC8532 to 68HC11 Interface.

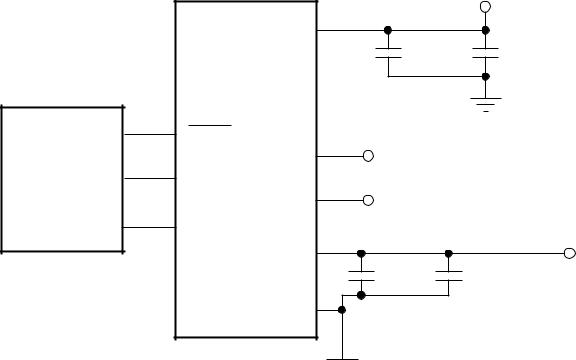
The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration causes data appear-ing on the MOSI output to be valid on the falling edge of SCK.

When data is being transmitted to the DAC, the SYNC line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8532, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

**DAC8532 to TMS320 DSP INTERFACE**

Figure 9 shows the connections between the DAC8532 and a TMS320 digital signal processor. By decoding the FSX signal, multiple DAC8532s can be connected to a single serial port of the DSP.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **DAC8532** | Positive Supply | |
|  | VDD |  |  |
|  |  | 0.1µ F | 10µ F |
| **TMS320 DSP** |  |  |  |
| FSX | SYNC |  |  |
|  | VOUTA | Output A |  |
| DX | DIN |  |  |
|  | VOUTB | Output B |  |



CLKX SCLK

|  |  |  |  |
| --- | --- | --- | --- |
| VREF |  | Reference |  |
|  | Input |  |
| 0.1µ F | 1µ F to 10µ F |  |
|  |  |
| GND |  |  |  |



FIGURE 9. DAC8532 to TMS320 DSP.

**APPLICATIONS**

**CURRENT CONSUMPTION**

The DAC8532 typically consumes 250uA at VDD = 5V and 225uA at VDD = 3V for each active channel, including refer-ence current consumption. Additional current consumption can occur at the digital inputs if VIH<<VDD. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC.

In power-down mode, typical current consumption is 200nA. A delay time of 10 to 20ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10µ A.

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**DRIVING RESISTIVE AND CAPACITIVE LOADS**

The DAC8532 output stage is capable of driving loads of up to 1000pF while remaining stable. Within the offset and gain error margins, the DAC8532 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2kΩ can be driven by the DAC8532 while achieving a typical load regu-lation of 1%. As the load resistance drops below 2kΩ , the load regulation error increases. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20mV of the DAC’s digital input-to-voltage output transfer characteristic. The reference voltage applied to the DAC8532 may be reduced below the supply voltage applied to VDD in order to eliminate this condition if good linearity is a requirement at full scale (under resistive loading conditions).

**CROSSTALK AND AC PERFORMANCE**

The DAC8532 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5LSBs. The AC crosstalk measured (for a full-scale, 1kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under –100dB.

In addition, the DAC8532 can achieve typical AC perfor-mance of 96dB SNR (Signal-to-Noise Ratio) and 65db THD (Total Harmonic Distortion), making the DAC8532 a solid choice for applications requiring low SNR at output frequen-cies at or below 4kHz.

**OUTPUT VOLTAGE STABILITY**

The DAC8532 exhibits excellent temperature stability of 5ppm/° C typical output voltage drift over the specified tem-perature range of the device. This enables the output voltage of each channel to stay within a ± 25µ V window for a ± 1° C ambient temperature change.

Good Power-Supply Rejection Ratio (PSRR) performance reduces supply noise present on VDD from appearing at the outputs to well below 10µ V-s. Combined with good DC noise performance and true 16-bit differential linearity, the DAC8532 becomes a perfect choice for closed-loop control applica-tions.

**SETTLING TIME AND OUTPUT GLITCH PERFORMANCE**

Settling time to within the 16-bit accurate range of the DAC8532 is achievable within 10µ s for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2µ s, en-abling update rates up to 500ksps for digital input signals changing code-to-code. The high-speed serial interface of the DAC8532 is designed in order to support these high update rates.



For full-scale output swings, the output stage of each DAC8532 channel typically exhibits less than 100mV of overshoot and undershoot when driving a 200pF capacitive load. Code-to-code change glitches are extremely low (~10uV) given that the code-to-code transition does not cross an Nx4096 code boundary. Due to internal segmen-tation of the DAC8532, code-to-code glitches occur at each crossing of an Nx4096 code boundary. These glitches can approach 100mVs for N = 15, but settle out within ~2µ s.

**USING REF02 AS A POWER SUPPLY FOR DAC8532**

Due to the extremely low supply current required by the DAC8532, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC8532's supply input as well as the reference input, as shown in Figure 10. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8532. If the REF02 is used, the current it needs to supply to the DAC8532 is 567µ A typical and 890µ A max for VDD = 5V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5kΩ load on a given DAC output) is:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | 567µ A + (5V/ 5kΩ ) = 1.567mA | |  |  |
|  | +15 |  |  |  |
|  | **REF02** | +5V |  |  |
|  |  |  |  |
|  |  | 1.567mA |  |  |
|  | SYNC | VDD, VREF |  |  |
| 3-Wire |  | VOUT | = 0V to 5V |  |
|  |  |  |
| Serial | SCLK | **DAC8532** |  |  |
|  |  |  |
| Interface | |  |  |  |
|  | DIN |  |  |  |

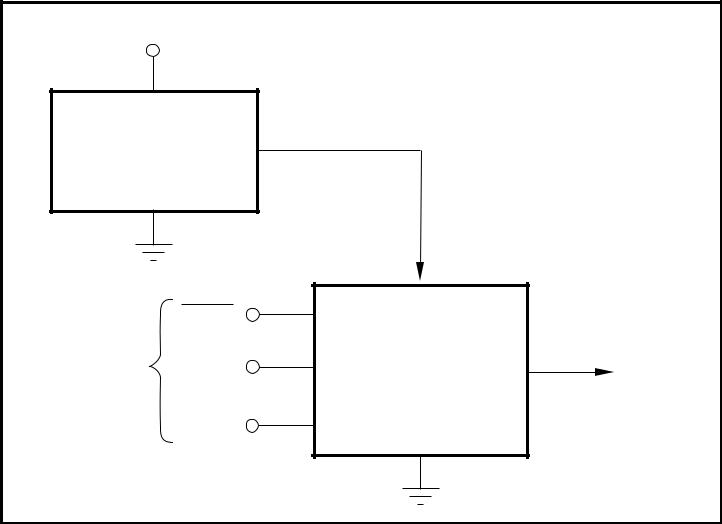


FIGURE 10. REF02 as a Power Supply to the DAC8532.

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 392µ V for the 1.5mA current drawn from it. This corresponds to a 5.13LSB error for a 0V to 5V output range.

**BIPOLAR OPERATION USING THE DAC8532**

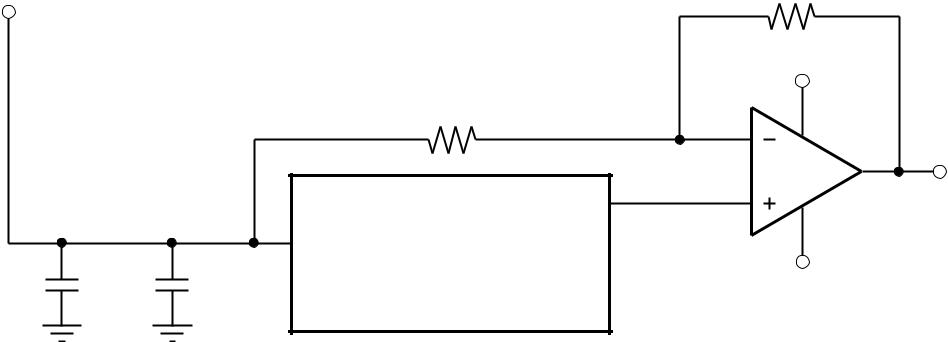
The DAC8532 has been designed for single-supply opera-tion but a bipolar output range is also possible using the circuit in Figure 11. The circuit shown will give an output voltage range of ± VREF. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, see Figure 11.



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|  |  |  |  |
| --- | --- | --- | --- |
| +5V |  | R2 |  |
|  | 10kΩ |  |
|  | R1 | +5V |  |
|  |  |  |
|  | 10kΩ |  |  |
|  |  | **OPA703** |  |
|  | VOUTX | ± 5V |  |
|  | VDD, VREF **DAC8532** |  |  |
| 10µ F | 0.1µ F | –5V |  |



(Other pins omitted for clarity.)

FIGURE 11. Bipolar Operation with the DAC8532.

The output voltage for any input code can be calculated as follows:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | D |  | R + R | | 2 |  | R | | 2 |  | |  |
| VOUTX = VREF • |  | • | 1 |  | – VREF • |  |  |  |  |
|  |  |  | 1 |  |  |  | 1 |  |  |  |
|  |  | 65536 | |  |  |  |  |  |  |  |  |
|  | R |  | R | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |

where D represents the input code in decimal (0–65535).

With VREF = 5V, R1 = R2 = 10kΩ :

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| VOUTX = |  | 10 • D | |  |
|  |  | – 5V |  |
|  |  |
|  |  | 65536 | |  |

This is an output voltage range of ± 5V with 0000H corre-sponding to a –5V output and FFFFH corresponding to a +5V output. Similarly, using VREF = 2.5V, a ± 2.5V output voltage range can be achieved.

**LAYOUT**

A precision analog component requires careful layout, ad-equate bypassing, and clean, well-regulated power supplies.

The DAC8532 offers single-supply operation, and it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switch-ing speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8532, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to VDD should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connec-tions and analog output.

As with the GND connection, VDD should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, a 1µ F to 10µ F capacitor in parallel with a 0.1µ F bypass capacitor is strongly recom-mended. In some situations, additional bypassing may be required, such as a 100µ F electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply, removing the high-frequency noise.

16  **DAC8532**



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**PACKAGE OPTION ADDENDUM**



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**PACKAGING INFORMATION**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Orderable Device** | **Status** | **Package Type** | **Package** | **Pins** | **Package** | **Eco Plan** | **Lead/Ball Finish** | **MSL Peak Temp** | **Op Temp (°C)** | **Top-Side Markings** | **Samples** |
|  | (1) |  | **Drawing** |  | **Qty** | (2) |  | (3) |  | (4) |  |
| DAC8532IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | D32E |  |
|  |  |  |  |  |  | & no Sb/Br) |  |  |  |  |  |
| DAC8532IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | D32E |  |
|  |  |  |  |  |  | & no Sb/Br) |  |  |  |  |  |
| DAC8532IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | D32E |  |
|  |  |  |  |  |  | & no Sb/Br) |  |  |  |  |  |
| DAC8532IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | D32E |  |
|  |  |  |  |  |  | & no Sb/Br) |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |



1. The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

1. Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent>for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances,including the requirement thatlead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used betweenthe die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weightin homogeneous material)

1. MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
2. Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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Addendum-Page 1

**PACKAGE OPTION ADDENDUM**



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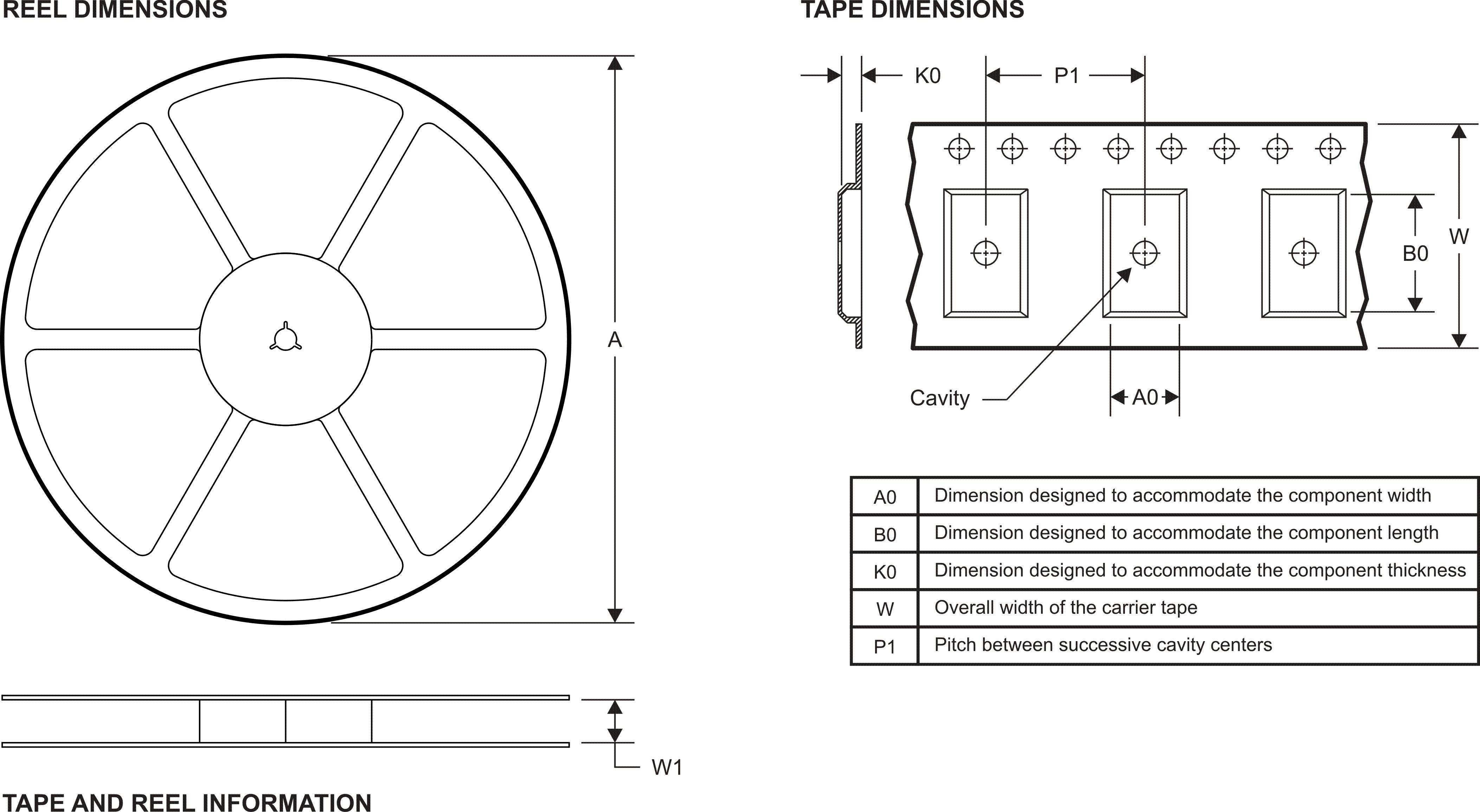
Addendum-Page 2

**PACKAGE MATERIALS INFORMATION**



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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

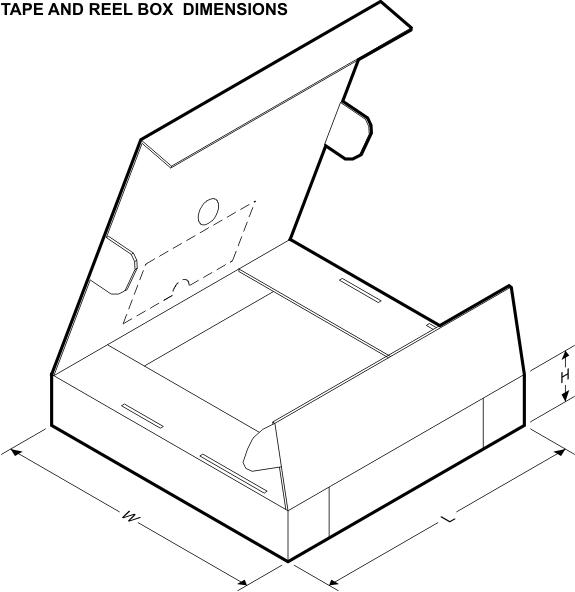
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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Package** | **Package** | **Pins** | **SPQ** | **Reel** | **Reel** | **A0** | **B0** | **K0** | **P1** | **W** | **Pin1** |
|  | **Type** | **Drawing** |  |  | **Diameter** | **Width** | **(mm)** | **(mm)** | **(mm)** | **(mm)** | **(mm)** | **Quadrant** |
|  |  |  |  |  | **(mm)** | **W1 (mm)** |  |  |  |  |  |  |
| DAC8532IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

Pack Materials-Page 1

**PACKAGE MATERIALS INFORMATION**



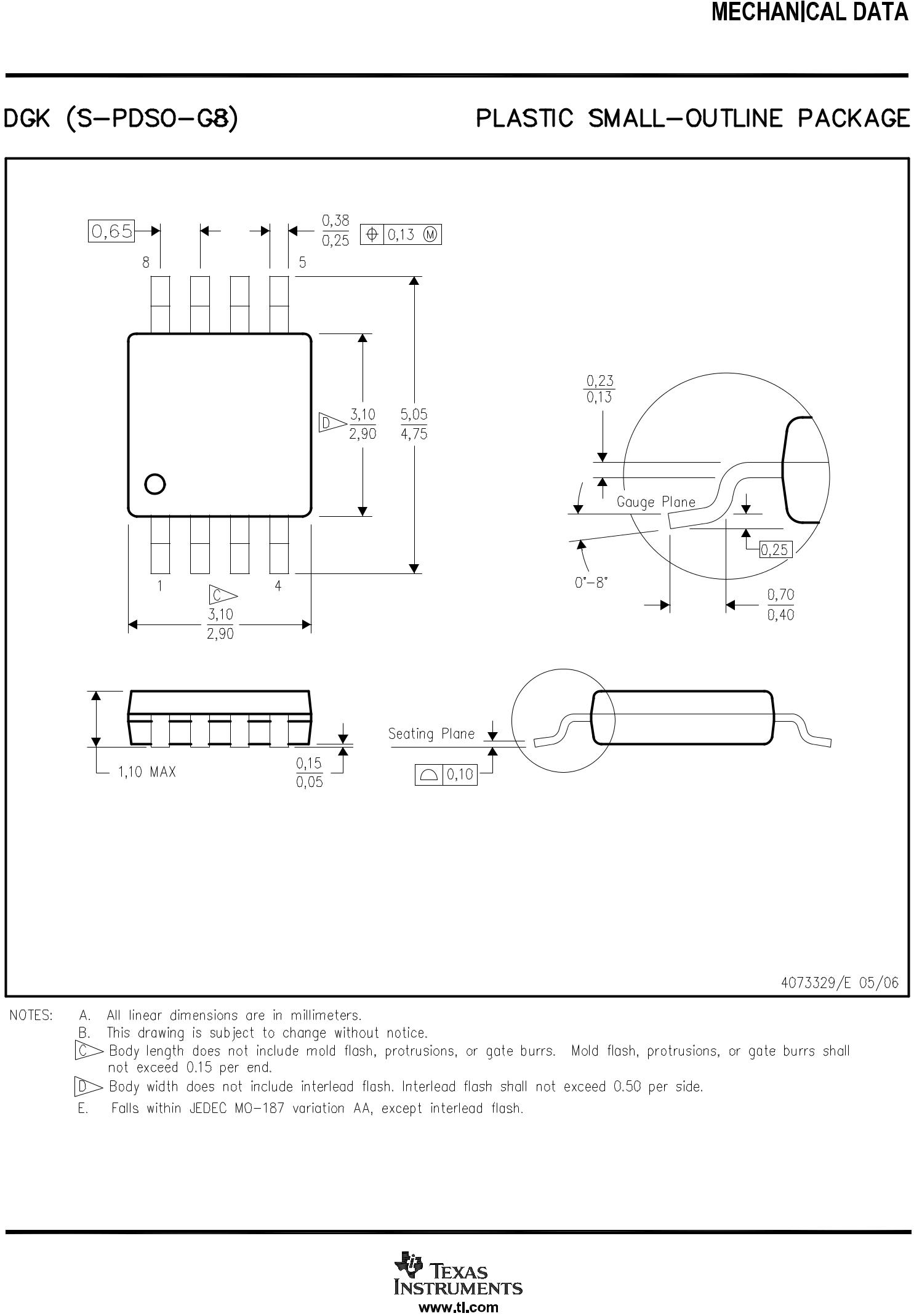
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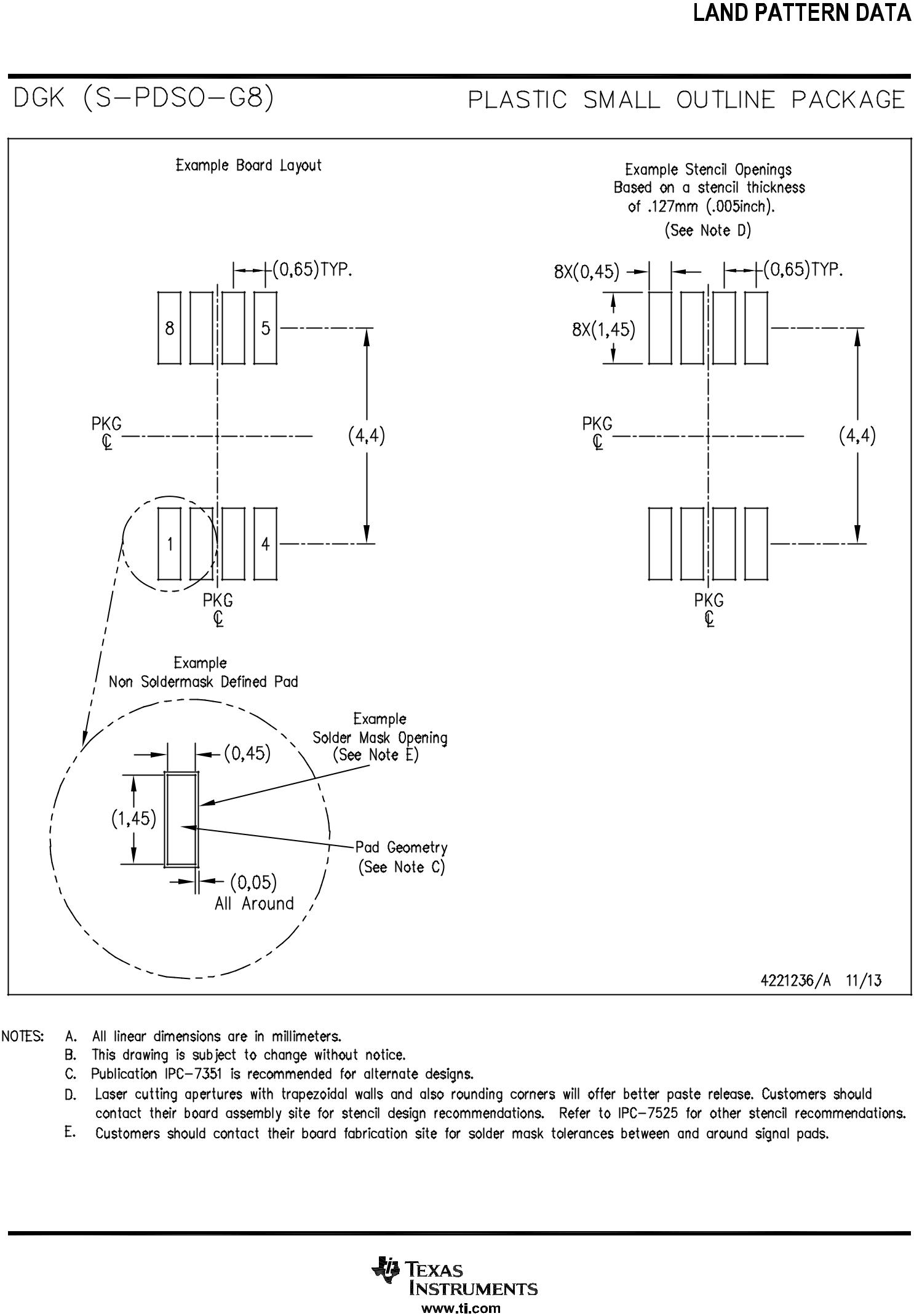


\*All dimensions are nominal

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| --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Length (mm)** | **Width (mm)** | **Height (mm)** |
|  |  |  |  |  |  |  |  |
| DAC8532IDGKR | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
|  |  |  |  |  |  |  |  |

Pack Materials-Page 2





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