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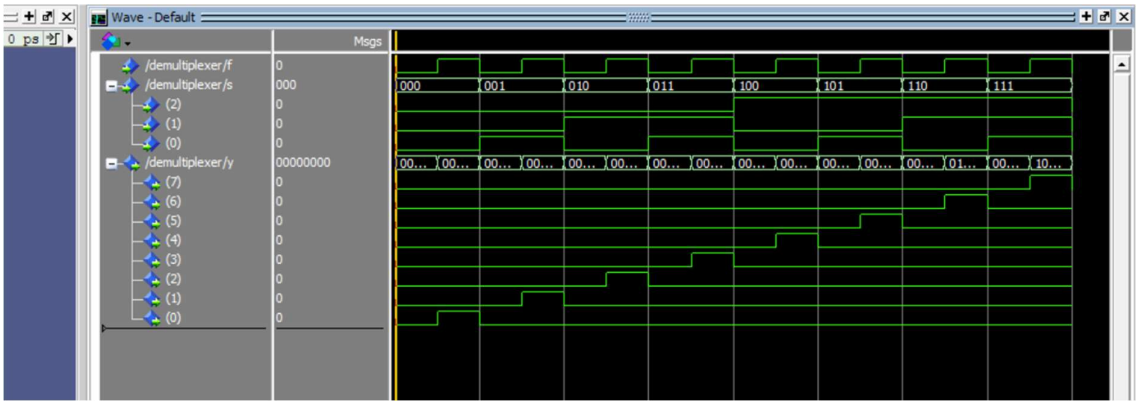
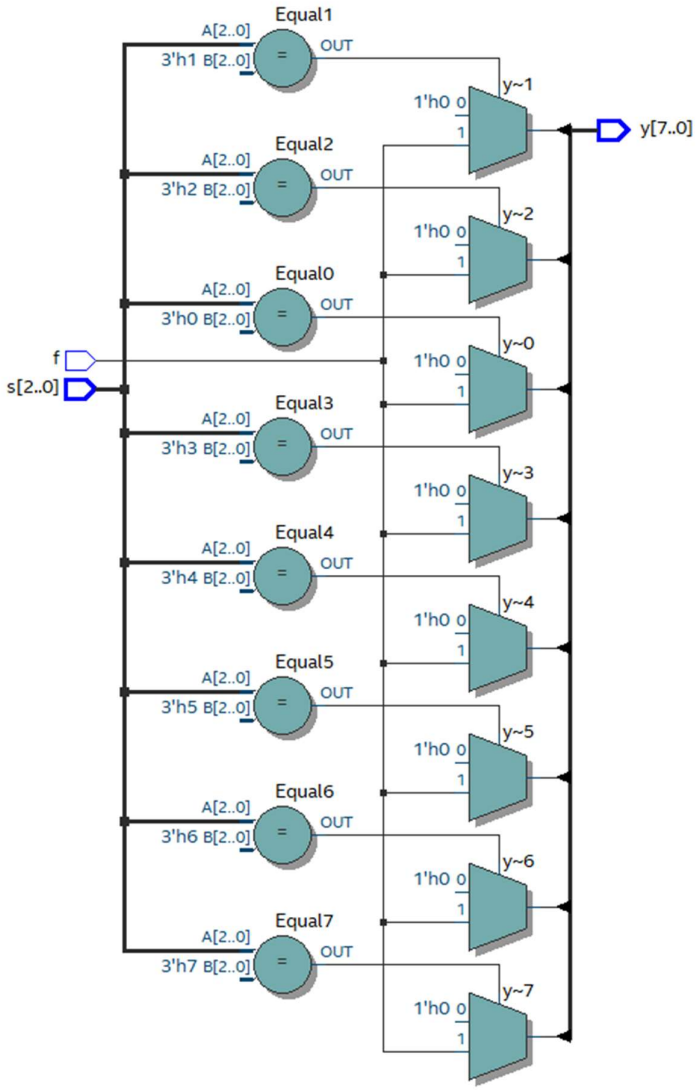
BSCpE-3A

DEMULTIPLEXER

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6     entity  demultiplexer is
7     port(f:in std_logic;
8     s:in std_logic_vector(2 downto 0);
9     y:out std_logic_vector(7 downto 0));
10    end demultiplexer;
11
12 architecture behavioral of demultiplexer is
13 begin
14    y(0)<=f when s="000"else'0';
15    y(1)<=f when s="001"else'0';
16    y(2)<=f when s="010"else'0';
17    y(3)<=f when s="011"else'0';
18    y(4)<=f when s="100"else'0';
19    y(5)<=f when s="101"else'0';
20    y(6)<=f when s="110"else'0';
21    y(7)<=f when s="111"else'0';
22 end behavioral;
```




Equal1
A[2..0]
3'h1 B[2..0]
=
OUT
Equal2
A[2..0]
3'h2 B[2..0]
=
OUT
Equal0
A[2..0]
3'h0 B[2..0]
=
OUT
f
s[2..0]
Equal3
A[2..0]
3'h3 B[2..0]
=
OUT
Equal4
A[2..0]
3'h4 B[2..0]
=
OUT
Equal5
A[2..0]
3'h5 B[2..0]
=
OUT
Equal6
A[2..0]
3'h6 B[2..0]
=
OUT
Equal7
A[2..0]
3'h7 B[2..0]
=
OUT
y~1
y~2
y~0
y~3
y~4
y~5
y~6
y~7
1'h0 0
1
y[7..0]