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BSCpE-3A

XNOR Gate

VHDL Code:

```vhdl
Library IEEE;
use IEEE.std_logic_1164.all;

entity ex_nor_gate is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end ex_nor_gate;

-- Behavioral model
architecture behav2 of ex_nor_gate is
begin
  process (x, y)
  begin
    if (x = y) then  -- XNOR logic: output is 1 if inputs are the same
      Z <= '1';
    else
      Z <= '0';
    end if;
  end process;
end behav2;

```