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BSCpE-3A

ASYNCHRONOUS BINARY UP COUNTER

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3   use IEEE.STD_LOGIC_ARITH.ALL;
4   use IEEE.STD_LOGIC_UNSIGNED.ALL;
5   entity asybin is
6   Port (rs,clk: in STD_LOGIC;
7   q: inout STD_LOGIC_VECTOR (3 downto 0));
8   end asybin;
9   architecture Behavioral of asybin is
10  signal div:std_logic_vector(22 downto 0);
11  signal temp:STD_LOGIC_VECTOR (3 downto 0);
12  signal clkd:std_logic;
13  begin
14  process(clk)
15  begin
16  if rising_edge(clk)then
17  div<= div+1;
18  end if;
19  end process;
20  clkd<=div(22);
21  process(clkd,rs)
22  begin
23  if(rs='1')then temp<=(others=>'0');
24  elsif(clkd='1' and clkd'event) then
25  temp<=temp+1;
26  q<= temp;
27  end if;
28  end process;
29  end Behavioral;
```