Mark Nelson A. Bentulan
BSCpE-3A

FULL ADDER

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5  entity full_adder is
6  Port (a,b,ci: in STD_LOGIC; s,co: out STD_LOGIC);
7  end full_adder;
8  architecture Behavioral of full_adder is
9  begin
10 s<=a xor b xor ci;
11 co<=(a and b)or (b and ci)or (ci and a);
12 end Behavioral;
```

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2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
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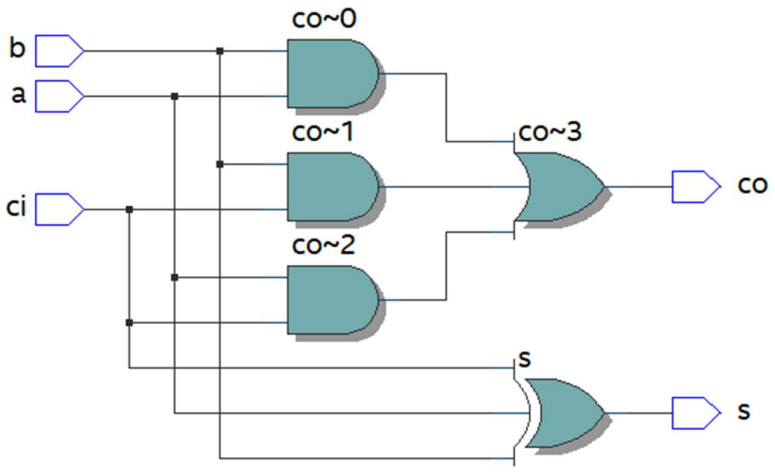
5  entity full_adder is
6  Port (a,b,ci: in STD_LOGIC; s,co: out STD_LOGIC);
7  end full_adder;
8  architecture Behavioral of full_adder is
9  begin
10 process(a,b,ci)
11 begin
12 s<=a xor b xor ci;
13 co<=(a and b)or (b and ci)or (ci and a);
14 end process;
15 end Behavioral;
```


co~0
b
a
co~1
co~3
co
ci
co~2
s
s