Mark Nelson A. Bentulan
BSCpE-3A

T FLIP FLOP

t_flip_flop.vhd

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity t_flip_flop is
    Port (
        t   : in  STD_LOGIC;
        clk : in  STD_LOGIC;
        rst : in  STD_LOGIC;
        q   : inout  STD_LOGIC
    );
end t_flip_flop;

architecture Behavioral of t_flip_flop is
    signal div  : std_logic_vector(22 downto 0);
    signal clkd : std_logic;
begin

    -- Falling edge instead of rising edge
    process(clk)
    begin
        if falling_edge(clk) then
            div <= div - 1;  -- reverse addition
        end if;
    end process;

    clkd <= not div(20);  -- reverse signal logic

    process(clkd, rst)
    begin
        if (rst = '0') then   -- reverse active-high reset to active-low
            q <= '1';         -- reverse reset value
        elsif (clkd'event and clkd = '0' and t = '0') then  -- reverse clock and T logic
```