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BSCpE-3A

BCD UP COUNTER

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity bcdupcount is
    Port (
        clk : in STD_LOGIC;        -- 100 MHz clock
        rs  : in STD_LOGIC;        -- Active low reset
        q   : out STD_LOGIC_VECTOR (3 downto 0) -- Active-low outputs (LEDs turn OFF when '1')
    );
end bcdupcount;

architecture Behavioral of bcdupcount is
    -- Constants for 1-second timing at 100MHz
    constant CLOCK_FREQ : natural := 10000000; -- 100 MHz
    constant ONE_SECOND : natural := CLOCK_FREQ - 1;

    signal div : natural range 0 to ONE_SECOND;
    signal clkd : std_logic;
    signal q_int : std_logic_vector(3 downto 0);
begin
    -- Clock divider process (1 second)
    process(clk)
    begin
        if rising_edge(clk) then
            if rs = '0' then
                div <= 0;
                clkd <= '0';
            elsif div = ONE_SECOND then
                div <= 0;
                clkd <= '1';
            else
                div <= div + 1:
```