Mark Nelson A. Bentulan
BSCpE-3A

XOR Gate

VHDL Code:

```vhdl
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor_gate is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end xor_gate;

-- Behavioral model
architecture behav2 of xor_gate is
begin
  process (x, y)
  begin
    if (x /= y) then  -- XOR logic: output is 1 if inputs are different
      Z <= '1';
    else
      Z <= '0';
    end if;
  end process;
end behav2;
```