

Mark Nelson A. Bentulan
BSCpE-3A

NOR Gate

VHDL Code:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity nor_gate is
5  Port (
6      X: in STD_LOGIC;
7      Y: in STD_LOGIC;
8      Z: out STD_LOGIC
9  );
10 end nor_gate;
11
12 -- Corrected Behavioral model
13 architecture behav2 of nor_gate is
14 begin
15     process (x, y)
16     begin
17         Z <= not (x or y); -- NOR logic implemented correctly
18     end process;
19 end behav2;
20
```

