Binary to gray (USING EXOR GATES)

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       library IEEE;
 1
       use IEEE.STD_LOGIC_1164.ALL; use IEEE.STD_LOGIC_ARITH.ALL;
 3
       use IEEE.STD_LOGIC_UNSIGNED.ALL;
     pentity bin_gray_exor_gate is port(
 6
             port(
    b: in std_logic_vector(3 downto 0); -- Binary Input
    g: out std_logic_vector(3 downto 0) -- Gray Output
 7
 8
 9
      end bin_gray_exor_gate;
10
11
12
       architecture behavioral of bin_gray_exor_gate is
13
     ⊟begin
14
             g(3) <= b(3);
g(2) <= b(3) xor b(2);
g(1) <= b(2) xor b(1);
g(0) <= b(1) xor b(0);
15
16
17
18
19
      Lend behavioral;
20
```



