1. Module ADF4351

A circuit board

Description generated with very high confidenceA screenshot of a cell phone

Description generated with high confidence

***FEATURES***

Output frequency range: 137.5 MHz to 4400 MHz Fractional-N synthesizer and integer-N synthesizer Low phase noise VCO Programmable divide-by-1/-2/-4/-8/-16 output Typical rms jitter: <0.4 ps rms Power supply: 3.0 V to 3.6 V Logic compatibility: 1.8 V Programmable dual-modulus prescaler of 4/5 or 8/9 Programmable output power level RF output mute function 3-wire serial interface Analog and digital lock detect Switched bandwidth fast-lock mode Cycle slip reduction

***APPLICATIONS***

Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)

Test equipment Wireless LANs, CATV equipment Clock generation

1. Module AD8302

A circuit board

Description generated with very high confidenceA close up of a piece of paper

Description generated with very high confidence

***FEATURES***

Measures Gain/Loss and Phase up to 2.7 GHz Dual Demodulating Log Amps and Phase Detector Input Range –60 dBm to 0 dBm in a 50 ⍀ System Accurate Gain Measurement Scaling (30 mV/dB) Typical Nonlinearity < 0.5 dB

Accurate Phase Measurement Scaling (10 mV/Degree) Typical Nonlinearity < 1 Degree

Measurement/Controller/Level Comparator Modes Operates from Supply Voltages of 2.7 V–5.5 V Stable 1.8 V Reference Voltage Output Small Signal Envelope Bandwidth from DC to 30 MHz

***APPLICATIONS***

RF/IF PA Linearization Precise RF Power Control

Remote System Monitoring and Diagnostics Return Loss/VSWR Measurements Log Ratio Function for AC Signals

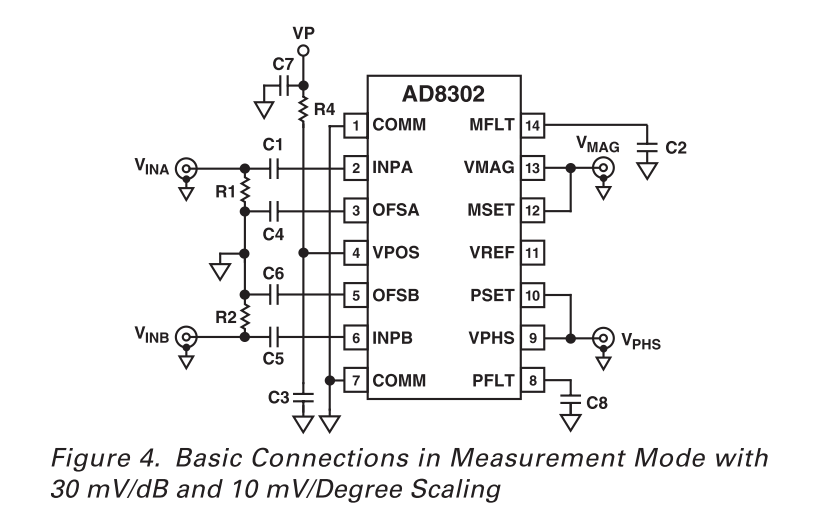
***BASIC CONNECTIONS***

***Measurement Mode***

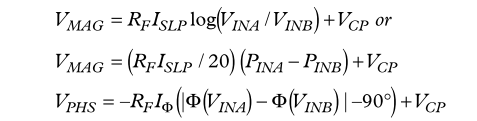
The basic function of the AD8302 is the direct measurement of gain and phase. When the output pins, VMAG and VPHS, are connected directly to the feedback setpoint input pins, MSET and PSET, the default slopes and center points are invoked. This basic connection shown in Figure 4 is termed the measurement mode. The current from the setpoint interface is forced by the integrator to be equal to the signal currents coming from the log amps and phase detector. The closed loop transfer function is thus given by:

VI R OUT IN F VCP=+ /() +()1 sT (7) 900mV

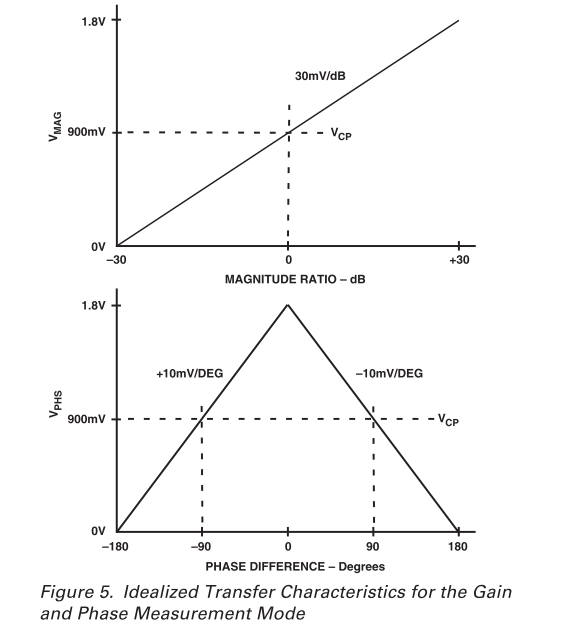
The time constant T represents the single-pole response to the envelope of the dB-scaled gain and the degree-scaled phase functions. A small internal capacitor sets the maximum envelope bandwidth to approximately 30 MHz. If no external CFLT is used, the AD8302 can follow the gain and phase envelopes within this bandwidth. If longer averaging is desired, CFLT can be added as necessary according to T (ns) = 3.3 × CAVE (pF). For best transient response with minimal overshoot, it is recommended that 1 pF minimum value external capacitors be added to the MFLT and PFLT pins.



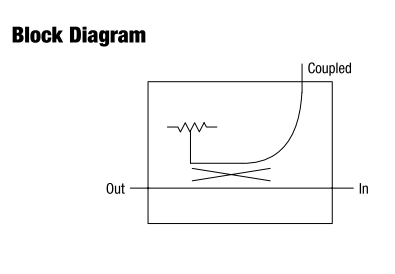
In the low frequency limit, the gain and phase transfer functions given in Equations 4 and 5 become:



which are illustrated in Figure 5. In Equation 8b, PINA and PINB are the power in dBm equivalent to VINA and VINB at a specified reference impedance. For the gain function, the slope represented by RFISLP is 600 mV/decade or, dividing by 20 dB/decade, 30 mV/dB. With a center point of 900 mV for 0 dB gain, a range of –30 dB to +30 dB covers the full-scale swing from 0 V to 1.8 V. For the phase function, the slope represented by RFIΦ is 10 mV/degree. With a center point of 900 mV for 90°, a range of 0° to 180° covers the full-scale swing from 1.8 V to 0 V. The range of 0° to –180° covers the same full-scale swing but with the opposite slope.



1. Module 0873 Directional Coupler 0.3–2.7 GHz



***Features***

● Low cost

● Low profile

● Small SOT-6 package ● Available on tape and reel

● Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

***Description***

The DC08-73 is a monolithic directional coupler optimized for the 0.81–0.96 GHz band. It offers low loss, good isolation, good input/output matching and exceptional coupling repeatability. It may be used at higher frequencies when stronger coupling is required. It is available in the SOT-6 surface mount package.

1. LCD Nokia 5110
2. A picture containing red, sitting, microwave, oven

   Description generated with high confidence

***FEATURES***

• Single chip LCD controller/driver

• 48 row, 84 column outputs

• Display data RAM 48 × 84 bits

• On-chip: – Generation of LCD supply voltage (external supply also possible)

– Generation of intermediate LCD bias voltages – Oscillator requires no external components (external clock also possible).

• External RES (reset) input pin

• Serial interface maximum 4.0 Mbits/s

• CMOS compatible inputs • Mux rate: 48

• Logic supply voltage range VDD to VSS: 2.7 to 3.3 V

• Display supply voltage range VLCD to VSS – 6.0 to 8.5 V with LCD voltage internally generated (voltage generator enabled)

– 6.0 to 9.0 V with LCD voltage externally supplied (voltage generator switched-off).

• Low power consumption, suitable for battery operated systems

• Temperature compensation of VLCD • Temperature range: −25 to +70 °C

***GENERAL DESCRIPTION***

The PCD8544 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.

The PCD8544 interfaces to microcontrollers through a serial bus interface.

The PCD8544 is manufactured in n-well CMOS technology.

***APPLICATIONS***

• Telecommunications equipment.