TCK Noise and Intel Pentium® 4 and Xeon™ Processors

An Application Note
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Overview

Intel's recommendations for TCK on the ITP-700 debug port requires a 27.4 ohm termination resistor to GND at the debug port, then directs the board designer to route separate unterminated stubs, in a star topology, to the TCK input of each processor. An additional requirement is to route one processor's TCK signal back to the FBO pin of the debug port. The debugger has a partial termination (82 Ohms to GND on FBO) internally. This arrangement minimizes the number of components on the motherboard (a single resistor), but does not properly terminate the TCK signal for high edge rate signals. Therefore, the debugger must limit the edge rate (dv/dt*) of the TCK signal.

Problems

Three problems arise when feeding signals with slow edge rates into a high speed logic input:

1. As the signal passes slowly through the input's logic threshold, the digital level seen by the input becomes undefined (i.e., ambiguous). This may not be a problem on a signal that is a piece of data that is sampled after the transition has completed, but for an edge-activated signal, like a clock input, the result can be the apparent reception of multiple clock edges. Since TCK controls the progress of the JTAG interface through the 16 JTAG states or controls the progression of data through the serial data chain, mistaken reception of multiple clock edges results in unrecoverable errors.

2. Some logic inputs can be damaged by simultaneous conduction currents that arise when the two input buffer transistors of the input buffer are both turned on by the signal sitting in the threshold region for an extended amount of time. At a minimum, these simultaneous conduction currents increase system noise, which leads to the third problem.

3. Even if the logic is capable of properly receiving the slow transition and is not damaged by simultaneous conduction currents, system noise disturbances can easily be large enough to cause a single transition to appear as multiple transitions. As the signal gets close to the logic input threshold, smaller and smaller disturbances can make the signal appear to cross the threshold repeatedly. These disturbances can be internal or external to the device. External sources include power supply noise due to varying current loads, power supply switching noise, or crosstalk from nearby signals. Noise sources internal to the device can be ground-bounce or power-supply-bounce due to output switching transients or due to simultaneous conduction current transients. Crosstalk can also occur internally.

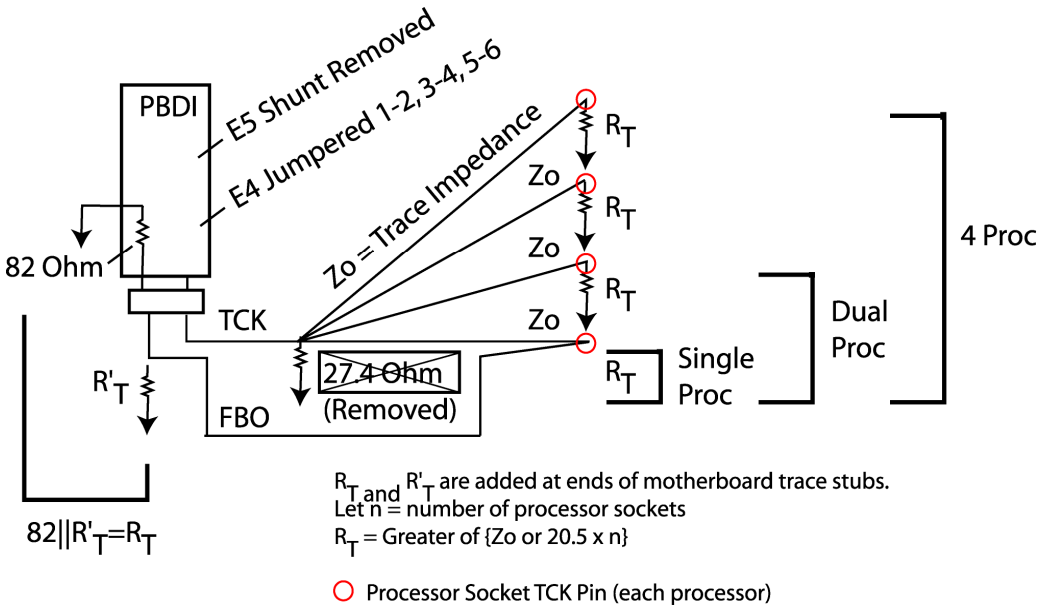
* Dv/dt is a shorthand notation for "change in voltage per change in time." A larger value indicates that the signal changes voltage more quickly.

Solution

An input can be designed to minimize its susceptibility to the above issues by adding circuitry to create hysteresis in the input's behavior. When the incoming signal is low and rising, the input's threshold is shifted a bit higher, and as the signal first crosses threshold, the threshold is shifted lower. The amplitude and speed of this threshold shift appear to add to the signal's edge rate, and the problems of slow transition are reduced or disappear entirely (if the amplitude and/or speed of the shift are great enough to overcome all noise sources combined).

Intel designed hysteresis into the TCK input of their processors, but in later steppings of the Intel® Pentium® 4 microprocessor and the Xeon™ microprocessors, sensitivity to slow TCK edge rates appeared. The likely causes are higher speed logic inputs, increased system noise due to higher speed outputs and larger power supply transients, plus higher internal noise due to the same causes.

Extreme measures are needed to attack the problem. The single largest contribution to containing the problem comes from bypassing the edge rate filtering on the debugger so that the TCK inputs see a very high dv/dt, and properly end-terminating the TCK net's stubs to avoid problems due to overshoot, undershoot, and the associated ringing.



Summary

Intel specified a routing method for TCK that requires slow edge rates. High-speed, edge-activated driven inputs with slow edge rates present a potential problem. Receiver hysteresis can overcome the problem if system noise dv/dt can be kept smaller than the hysteresis dv/dt plus the signal dv/dt. Later Intel processor steppings have been shown to have more problems with the slow edge rates. The best fix is to increase dv/dt of the debugger's TCK output. The value may be increased by increasing the amount of voltage change or decreasing the time it takes for the voltage to change, or both.

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