Debug Port Design Guide for Target Systems Based on a Single Intel® Celeron™ Processor (PGA-370)

An Application Note

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This design guide applies to target systems with the following processor characteristics. If your target system does not match the following chart, please contact American Arium for the appropriate design guide that matches your target system.

Processor Type	Number of Processors	Package Type
Celeron	Single Processor	PGA-370

Debug Port Ground Pins

Signal	Pin	Description	Suggested Termination
GND	2, 4, 6, 13, 15, 17, 19, 21, 23, 25, & 27	Signal grounds.	Connect to ground

Debug Port Output Signal Pins (Driven By Target)

Signal	Pin	Description	Suggested Termination
TDO	10	TAP Data Out (From last processor of scan chain to debug port)	150Ω to V_{CC}
PRDY0#	18	Processor PRDY signal. From 1st processor in single/multiprocessor system.	See below Note 1
PRDY1#	22	Processor PRDY signal. Not used. From 2nd processor in a multiprocessor system.	1KΩ to V_{CC}
PRDY2#	26	Processor PRDY signal. Not used. From 3rd processor in a multiprocessor system.	1KΩ to V_{CC}
PRDY3#	30	Processor PRDY signal. Not used. From 4th processor in a multiprocessor system.	1KΩ to V_{CC}
RESET#	1	Processor RESET signal. This allows the emulator to sense when the processor is being reset.	See below Note 2
V_{TT}	9	Target V_{TT}. The emulator uses V_{TT} to detect target power and establish the GTL+ threshold.	1.5KΩ to V_{TT}
BCLK	29	Private copy of BCLK. This allows the emulator to provide a TCK that is synchronous with BCLK.	

Debug Port Input Signal Pins (Driven By Emulator)

Signal	Pin	Description	Suggested Termination
TDI	8	TAP Data In (From debug port to TDI of first processor in scan chain)	200-300Ω to V_{CC}
TMS	7	TAP Mode Select	See below Note 3
TCK	5	TAP Clock. Of the debug port signals, this is the most critical signal.	See below Note 3
TRST#	12	TAP Reset	500-680Ω to ground
BSEN#	14	Boundary scan (TAP) enable. Emulator has access to TAP signals of CPU when low	See below Note 4
PREQ0#	16	Processor PREQ signal. To 1st processor in a single/multiprocessor system.	See below Note 5
PREQ1#	20	Processor PREQ signal. Not Used. To 2nd processor in a multiprocessor system.	No Connection
PREQ2#	24	Processor PREQ signal. Not Used. To 3rd processor in a multiprocessor system.	No Connection
PREQ3#	28	Processor PREQ signal. Not Used. To 4th processor in a multiprocessor system.	No Connection
DBRESET#	3	Target reset. When driven low, the target should reset the system and CPU.	See below Note 6
DBINST#	11	Emulator installed. Debug cable grounds this signal, allowing target to detect the emulator.	See below Note 4

The resistor values given are in ohms and are typical values. Actual values are dependent on the target layout. Resistors should have a 1%.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

The Debug Port connection is achieved by way of a 30-pin connector specified as AMP 104068-3. See the following pin numbering diagram.

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29

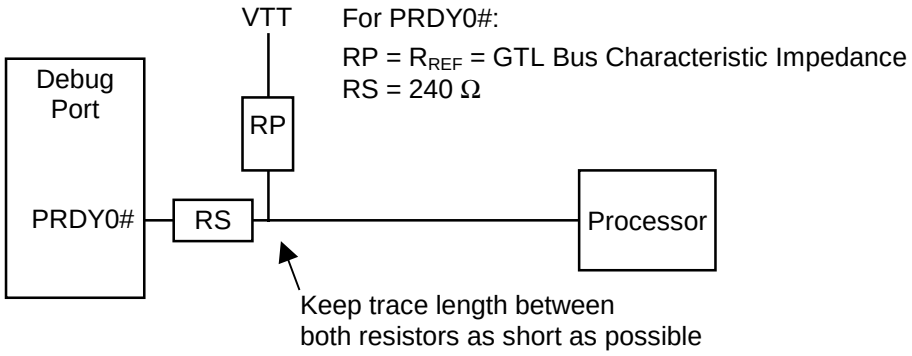
Top View Of Connector With Pin Numbering

Voltage Definitions

V_{CC}	Defined as the voltage level used to determine the processor CMOS logic high level (2.5V).
V_{TT}	Defined as the voltage level used to determine the processor GTL+ logic high level.

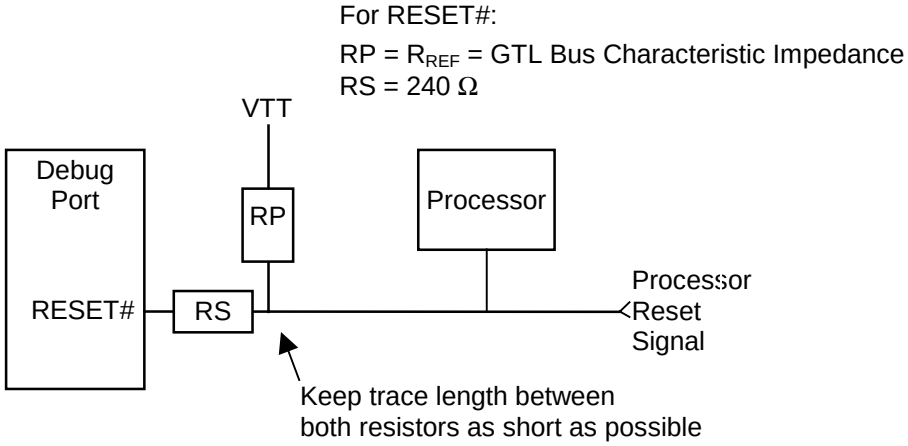
Note 1:

The PRDY0# signal is a GTL+ signal and should be end terminated to V_{TT} through a resistor equal to the characteristic impedance of the target's GTL bus. The signal supplied to the debug port should pass through a 240Ω series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of these traces. End termination resistor values for GTL signals vary according to the effective trace impedance and V_{TT} power dissipation issues.



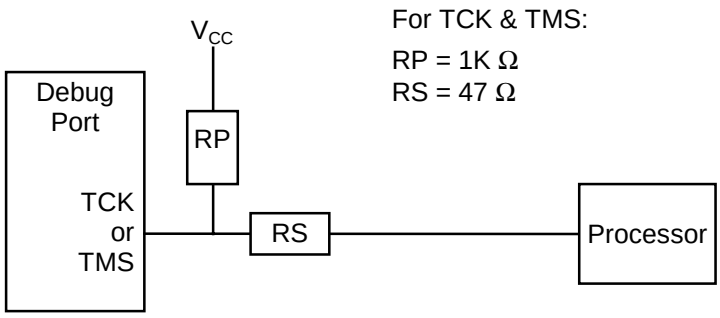
Note 2:

RESET# is a GTL+ signal and should be end terminated to V_{TT} through a resistor equal to the characteristic impedance of the target's GTL bus. The signal supplied to the debug port should pass through a 240Ω series resistor located as close as possible to the nearest terminated end. Do not add any stubs off of this trace.



Note 3:

TCK is the most critical of the debug port signals. In the case of a single processor, TCK may be pulled up to V_{CC} through a 1KΩ resister and then passed through a 47Ω series resistor before being routed to the processor as shown in the following figure. This note also applies to TMS and it should be terminated in the same manner.



Note 4:

BSEN# and DBINST# are driven by open drain devices. If these signals are used by the target, they should each be pulled up to their own V_{OH} level (not to exceed 5.5V) through a resistor that will limit I_{OL} current to 48 mA. If these signals are not used by the target, they may be left open.

Note 5:

PREQ0# should be pulled up to VCC using a resistor in the range of 200Ω to 300Ω.

Note 6:

DBRESET# is driven by an open drain device. It should be pulled up to its V_{OH} level (not to exceed 5.5V) through a resistor that will limit I_{OL} current to 48 mA. Intel recommends 240Ω.

DISCLAIMER: In cases where the preceding guidelines differ from the current guidelines provided by Intel, the Intel guidelines will take precedence.