Debug Port Requirements for the Pentium® Pro Processor

An Application Note

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The following is American Arium's recommendation for implementation of a Pentium® Pro target debug port.

Debug Port Signal Description

Signal	Pin	Dir	Description	Suggested Termination
TDO	10	O	TAP Data Out (From last processor of scan chain to ITP port)	See below Note 1
TDI	8	I	TAP Data In (ITP port to first processor of scan chain)	See below Note 1
TMS	7	I	TAP Mode Select	240Ω to VCC (3.3V)
TCK	5	I	TAP Clock. Of the ITP signals, this is the most critical signal.	See below Note 2
TRST#	12	I	TAP Reset	470Ω to ground
BSEN#	14	I	Boundary scan (TAP) enable. ICE has access to TAP signals of CPU when low	See below Note 6
PRDY0#	18	O	Processor PRDY signal. From 1st processor in single/multiprocessor system.	See below Note 3
PRDY1#	22	O	Processor PRDY signal. From 2nd processor in a multiprocessor system.	See below Note 3
PRDY2#	26	O	Processor PRDY signal. From 3rd processor in a multiprocessor system.	See below Note 3
PRDY3#	30	O	Processor PRDY signal. From 4th processor in a multiprocessor system.	See below Note 3
PREQ0#	16	I	Processor PREQ signal. To 1st processor in a single/multiprocessor system.	See below Note 4
PREQ1#	20	I	Processor PREQ signal. To 2nd processor in a multiprocessor system.	See below Note 4
PREQ2#	24	I	Processor PREQ signal. To 3rd processor in a multiprocessor system.	See below Note 4
PREQ3#	28	I	Processor PREQ signal. To 4th processor in a multiprocessor system.	See below Note 4
RESET#	1	O	Processor RESET signal.	See below Note 5
DBRESET#	3	I	ICE reset output. When driven low, the target should reset the system and CPU.	240Ω to VCC (3.3V)
DBINST#	11	I	ICE installed. Debug cable grounds this signal, allowing target to detect the ICE.	See below Note 6
VTT	9	O	Target VTT. The ICE uses this to detect target power and establish GTL+ threshold.	1KΩ to VTT (1.5V)
GND	2, 4, 6, 13, 15, 17, 19, 21, 23, 25, 27, & 29		Signal grounds. Pin 2 (or sometimes 13) is unique in that it is sensed to determine if a target is attached.	Connect to ground

The resistor values given are typical values. Actual values are dependent on the target layout.

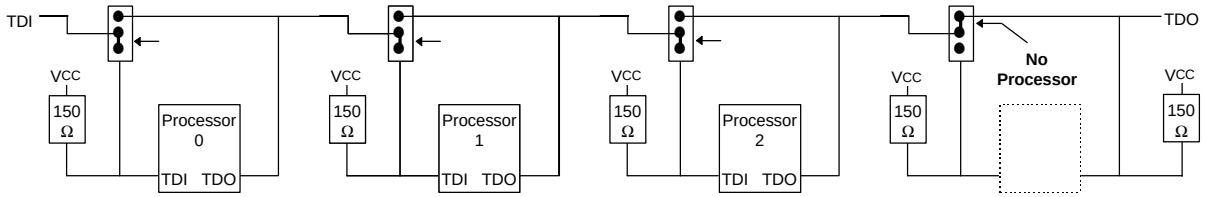
Dir (Signal Direction) is relative to target board. O (Out) is from target to ITP port. I (In) is from ITP port to target.

The Debug Port connection is achieved by way of a 30-pin connector specified as an AMP 104068-3. The pinout and suggested circuitry are fully described in the 1995 edition of the Pentium®Pro Processor Family User's Manual, Volume 1: Specifications, chapters 10 and 16 from Intel Corporation.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

Note 1:

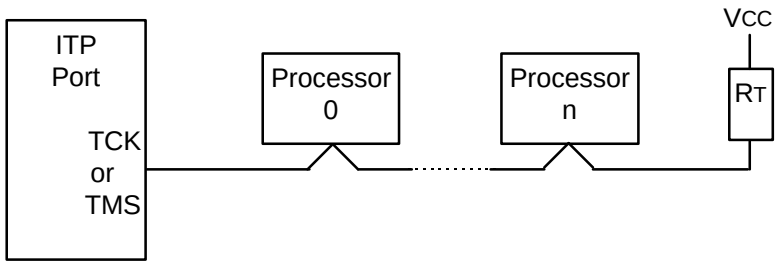
The TDO pin on each processor requires a 150Ω pull up resistor to V_{CC} (3.3V). Bypassing TDI to TDO using a jumper when a processor socket is not populated must not result in more than one pull up resistor on any TDO output. The jumper implementation shown below will accomplish this and insure that there is only one pull up on each TDO.



Note 2:

TCK is the most critical of the ITP signals. This note also applies to TMS. Both are best implemented as a daisy chain to each processor with a terminating resistor (R_T) to V_{CC} (3.3V) at the terminal end (located farthest from the debug port). The actual R values depend on the trace impedance of the target board but the following table has suggested values:

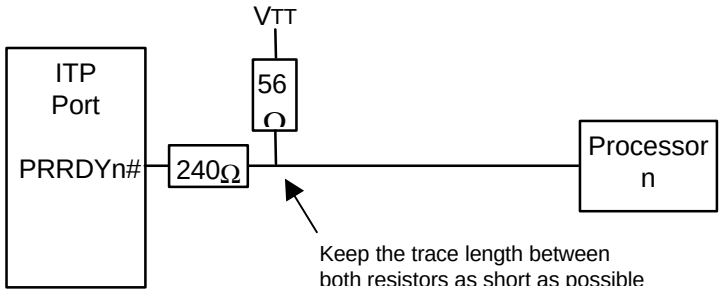
Run Length	R_T for TCK	R_T for TMS
0-12”	150 ohms	240 ohms
12-15”	120 ohms	240 ohms
15-18”	100 ohms	240 ohms
18-21”	82 ohms	240 ohms
>21”	62 ohms	240 ohms



Note 3:

All four PRDYn# signals are GTL+ signals and should be end terminated to V_{TT} (1.5V) through a 56Ω resistor on the target. The signal supplied to the debug port should pass through a 240 ohm series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of these traces. End termination resistor values for GTL signals vary according to the effective trace impedance and V_{TT} power dissipation issues.

Note 3 (Continued):

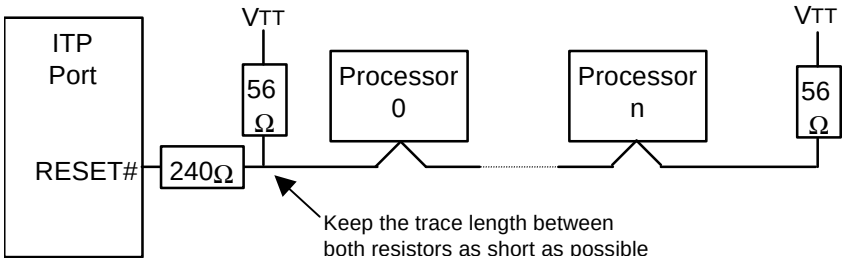


Note 4:

PREQn# signals should be pulled up to VCC (3.3V) in the range of 270 ohms to 10K ohms on the target.

Note 5:

RESET# is a GTL+ signal and should be terminated to VTT (1.5V) through 56Ω resistors at both ends of the signal. The signal supplied to the debug port should pass through a 240 ohm series resistor located as close as possible to the nearest terminated end. Do not add any stubs off of this trace.



Note 6:

BSEN# and DBINST# should be pulled up to VCC with a 10K resistor if this signal is used by the target. Otherwise, it may be left open.

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