Debug Port Design Guide for Target Systems Based on a Single Intel® Pentium® III Processor (.13 micron)

An Application Note

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This design guide applies to target systems with the following processor characteristics. If your target system does not match the following chart, please contact American Arium for the appropriate design guide that matches your target system.

Processor Type	Number of Processors	Package Type	Core Clock
Pentium III (.13 micron)	Single Processor	FC-PPGA (370) Micro-FCPGA (478) Micro-PCBGA (479)	1.13 GHz or higher

Debug Port Ground And Key Pins

Signal	Pin	Description	Suggested Termination
GND	1, 3, 5, 14, 16, 18, 20, 22, 24, 26, & 28	Signal grounds.	Connect to ground
Keyed	3	This pin of the receptacle is plugged and acts as a key.	Connect to ground

Debug Port Output Signal Pins (Driven By Target)

Signal	Pin	Description	Suggested Termination
TDO	9	TAP Data Out (From last processor of scan chain to debug port)	150Ω to V_CMOS
PRDY0#	17	Processor PRDY signal. From 1st processor in single/multiprocessor system.	See below Note 1
PRDY1#	21	Processor PRDY signal. Not used. From 2nd processor in a multiprocessor system.	1KΩ to V_CMOS
PRDY2#	25	Processor PRDY signal. Not used. From 3rd processor in a multiprocessor system.	1KΩ to V_CMOS
PRDY3#	29	Processor PRDY signal. Not used. From 4th processor in a multiprocessor system.	1KΩ to V_CMOS
RESET#	2	Processor RESET signal. This allows the emulator to sense when the processor is being reset.	See below Note 2
V_{TT}	10	Target V_{TT}. The emulator uses V_{TT} to detect target power and establish the GTL+ threshold.	1.5KΩ to V_{TT}
BCLK	30	Private copy of BCLK. This allows the emulator to provide a TCK that is synchronous with BCLK.	

Debug Port Input Signal Pins (Driven By Emulator)

Signal	Pin	Description	Suggested Termination
TDI	7	TAP Data In (From debug port to TDI of first processor in scan chain)	200-300Ω to V_CMOS
TMS	8	TAP Mode Select	See below Note 3
TCK	6	TAP Clock. Of the debug port signals, this is the most critical signal.	See below Note 4
TRST#	11	TAP Reset	500-680Ω to ground
BSEN#	13	Boundary scan (TAP) enable. Emulator has access to TAP signals of CPU when low	See below Note 5
PREQ0#	15	Processor PREQ signal. To 1st processor in a single/multiprocessor system.	See below Note 6
PREQ1#	19	Processor PREQ signal. Not Used. To 2nd processor in a multiprocessor system.	No Connection
PREQ2#	23	Processor PREQ signal. Not Used. To 3rd processor in a multiprocessor system.	No Connection
PREQ3#	27	Processor PREQ signal. Not Used. To 4th processor in a multiprocessor system.	No Connection
DBRESET#	4	Target reset. When driven low, the target should reset the system and CPU.	See below Note 7
DBINST#	12	Emulator installed. Debug cable grounds this signal, allowing target to detect the emulator.	See below Note 4

The resistor values given are in ohms and are typical values. Actual values are dependent on the target layout. Resistors should have a 1%.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

The Debug Port connection is achieved by way of a 30-pin connector specified as AMP P/N 104078-4. The plug that is used to key pin 3 is a Framatone Connectors International (FCI) part number 90543-001. See the following pin numbering diagram.

1		5	7	9	11	13	15	17	19	21	23	25	27	29
2	4	6	8	10	12	14	16	18	20	22	24	26	28	30

Top View Of Connector With Pin Numbering

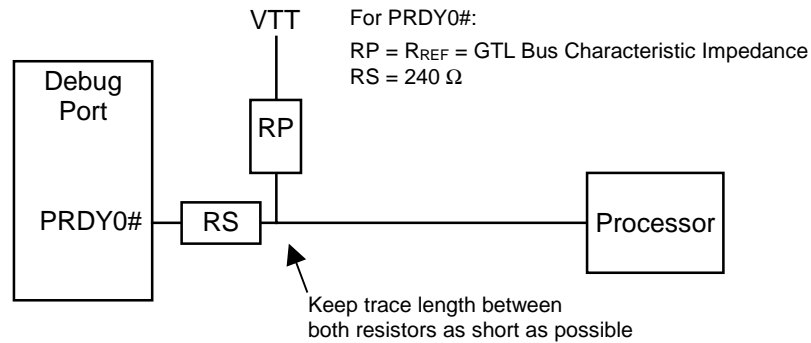Note: Pin 3 of the receptacle is plugged and acts as a key.

Voltage Definitions

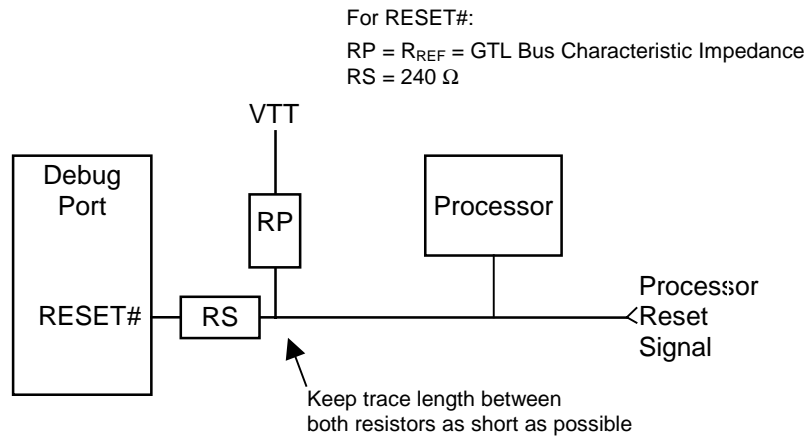|	
V_CMOS	Defined as the voltage level used to determine the processor CMOS logic high level.
V$_{TT}$	Defined as the voltage level used to determine the processor GTL+ logic high level.

Note 1:

The PRDY0# signal is a GTL+ signal and should be end terminated to V$_{TT}$ through a resistor equal to the characteristic impedance of the target's GTL bus. The signal supplied to the debug port should pass through a 240Ω series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of these traces. End termination resistor values for GTL signals vary according to the effective trace impedance and V$_{TT}$ power dissipation issues.

VTT

For PRDY0#:
RP = R$_{REF}$ = GTL Bus Characteristic Impedance
RS = 240 Ω

Debug Port

RP

PRDY0#   RS   Processor

Keep trace length between both resistors as short as possible

Note 2:

RESET# is a GTL+ signal and should be end terminated to V$_{TT}$ through a resistor equal to the characteristic impedance of the target's GTL bus. The signal supplied to the debug port should pass through a 240Ω series resistor located as close as possible to the nearest terminated end. Do not add any stubs off of this trace.

For RESET#:

RP = R_{REF} = GTL Bus Characteristic Impedance

RS = 240 Ω

VTT

| Debug Port | | | | |

RESET#   RS   RP   Processor

Processor Reset Signal

Keep trace length between both resistors as short as possible

Note 3:

TMS should be pulled up to V_CMOS through a 39Ω resister and then passed to the processor as shown in the following figure.

V_CMOS

For TMS:

RP = 39 Ω

Debug Port

RP
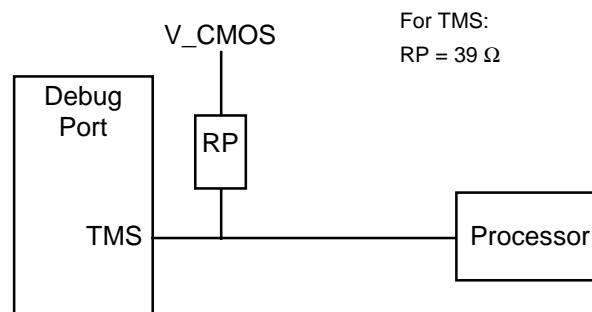
TMS   Processor

Note 4:

TCK is the most critical of the debug port signals. In the case of a single processor, TCK should be pulled to ground through a 39Ω resister and then passed to the processor as shown in the following figure.

Debug Port

For TCK:

RP = 39 Ω

TCK   Processor

RP
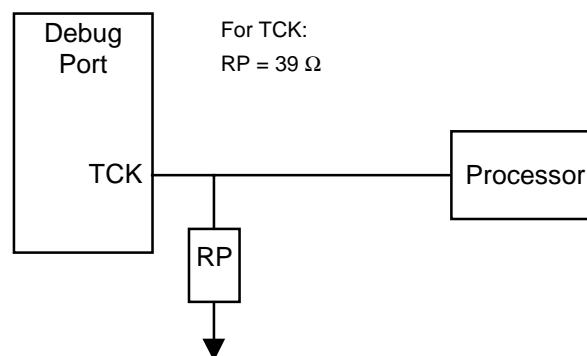
Note 5:

BSEN# and DBINST# are driven by open drain devices. If these signals are used by the target, they should each be pulled up to their own V_{OH} level (not to exceed 5.5V) through a resistor that will limit I_{OL} current to 48 mA. If these signals are not used by the target, they may be left open.

Note 6:

PREQ0# should be pulled up to V_CMOS using a resistor in the range of 200Ω to 300Ω.

Note 7:

DBRESET# is driven by an open drain device. It should be pulled up to its V_{OH} level (not to exceed 5.5V) through a resistor that will limit I_{OL} current to 48 mA. Intel recommends 240Ω.

DISCLAIMER: In cases where the preceding guidelines differ from the current guidelines provided by Intel, the Intel guidelines will take precedence.