PBD-XDP

GETTING STARTED

Overview

The purpose of the PBD-XDP module is to act as a buffer between the target debug/ITP port and the ECM-50. This allows the ECM to work with a number of different processors.

Note: *PBD-XDP modules are specifically designed for use only with the ECM-50.*

Caution: *It is extremely important that the jumpers are in the correct position PRIOR to installation. Jumpers set in the wrong position may cause damage to the target system.*

Installing the PBD

1. Determine if the target has proper end-termination on the signals TMS, TCK1, and TCK0. (See Figure 1 on back.)

   - Under normal circumstances, the TMS, TCK1, and TCK0 edge rates should be set to “fast.” This is the default setting.
   - If any one of the signals TMS, TCK1, or TCK0 has stubs or is not terminated in its characteristic impedence, set that jumper to “slow.”

2. Adjust shunts on JP1 through JP16. (See Figure 2 on back.)
   Jumpers JP1 through JP16 provide a means to connect or disconnect any combination of the sixteen signals the PBD-XDP terminates and potentially uses for control and triggering. A shunt MUST be REMOVED if there is a signal present on the corresponding XDP pin AND that signal is NOT the corresponding BPM[n]# signal. If no target signal is connected to a particular pin, the shunt may be installed or removed. A shunt MUST be INSTALLED if BPM5# or BPM4# from one or more processors is connected to the corresponding XDP pin. A shunt MUST be INSTALLED if BPM2#, BPM1# or BPM0# of a processor that supports bus analyzer triggers is connected to the XDP pin.

3. If the targed needs a reset signal in addition to the reset signal present on the debug port, a reset out FET closure is available on a two-pin connector labelled RST OUT. These pins are not ground-referenced and can be connected at any two points in the target circuit where a switch closure will cause a system reset.

4. The PWR ON THRESH selects the threshold above which the debug hardware determines target power is on. The default is 0.64 V. If that does not work, change the jumper setting to 0.96V or 0.48V, as appropriate.

5. Connect the PBD to the emulator with its 68-pin-conductor cable.

6. Connect the rigid-flex cable assembly to the XDP connector on the target.

7. For processors that support bus analyzer trigger, some adjustment of JP17 and JP18 may be necessary:
   JP17 and JP18 allow BCLK0 and BCLK1 (a differential pair that logically form BCLK) to be swapped if needed, causing the PBD to operate from an inverted clock. Because the layout guidelines do not enforce any particular routing (therefore timing) of BPM[0-5]# relative to BCLK, inversion of the clock may be needed to properly sample BPM[0-2]# on processors that provide bus analyzer trigger capability. If the PBD samples during transitions of BPM[0-2]#, it may skip breakpoints. The solution is to try the other edge of BCLK, which should then occur one-half clock away from transitions. With JP17 and JP18 shunts installed parallel to the length of the PBD-XDP, BCLK is not inverted (indicated as "NON" on the board legend). With JP17 and JP18 shunts installed perpendicular to the length of the PBD-XDP, BCLK is inverted (indicated as "INV" on the board legend).

   The XDP connector is a Samtec 60-pin BSH-030-01 series connector. Specific plating types, locking clips, and alignment pins versions of this connector can be obtained from Samtec. To determine the proper pinout, refer to your Intel documentation for details.

   Note: *Observe proper Pin 1 orientation.*

   Caution: *The rigid-flex cable is fragile. The minimum bend radius is one-fourth inch.*

If you have any problems or questions, contact Technical Support at 877-508-3970 toll free in the US or 714-731-1661 in North America. For support elsewhere, contact or your local distributor or e-mail support@arium.com for assistance.

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Adjusting Shunts on JP1 - JP16

The jumpers are numbered and also labeled. The labels are a shorthand notation consisting of a number and a letter. The number corresponds the the BPM[n]# number (n), and the letter corresponds to Intel's signal groups A through D, which generally correspond to processor numbers 0 through 3, respectively. In some cases BPM[n]# signals of more than one processor may be bussed (connected in common) to a pin on the XDP, in which case a letter designation will correspond to more than one processor. Neither of the BPM3# signals in the following list is used by the PBD-XDP, so JP5 and JP13 need not have shunts installed.

JPn	Label	XDP Pin	Remove shunt if not open & not connected to :
JP1	5A	3	BPM5# of processor(s)
JP2	5C	4	BPM5# of processor(s)
JP3	4A	5	BPM4# of processor(s)
JP4	4C	6	BPM4# of processor(s)
JP5*	3A	9	BPM3# of processor(s)
JP6	2A	11	BPM2# of processor(s)
JP7	1A	15	BPM1# of processor(s)
JP8	0A	17	BPM0# of processor(s)
JP9	5B	21	BPM5# of processor(s)
JP10	5D	22	BPM5# of processor(s)
JP11	4B	23	BPM4# of processor(s)
JP12	4D	24	BPM4# of processor(s)
JP13*	3B	27	BPM3# of processor(s)
JP14	2B	29	BPM2# of processor(s)
JP15	1B	33	BPM1# of processor(s)
JP16	0B	35	BPM0# of processor(s)

* Never used, no shunt need be installed.

Typical applications would need only the following shunts installed on locations JP1 through JP16:

- Target with single processor socket (UP target) : JP1 and JP3
- Single processor target with bus analyzer trigger capability: JP1, JP3, JP6-JP8
- Dual processor socket target (DP) with separate BPM5# and BPM4# connections: JP1, JP3, JP9, JP11
- DP target with BPM5# and BPM4# bussed on a single pair of pins: JP1 and JP3
- Four processor socket target (MP) with separate BPM5# and BPM4# connections: JP1-JP4, JP9-JP12
- MP target with BPM5# and BPM4# from pairs of processors bussed (total of four pins): JP1-JP4
- DP target with bus analyzer trigger capability, separate BPM signals (not bussed): JP1, JP3, JP6-8, JP9, JP 11, and JP14-16.

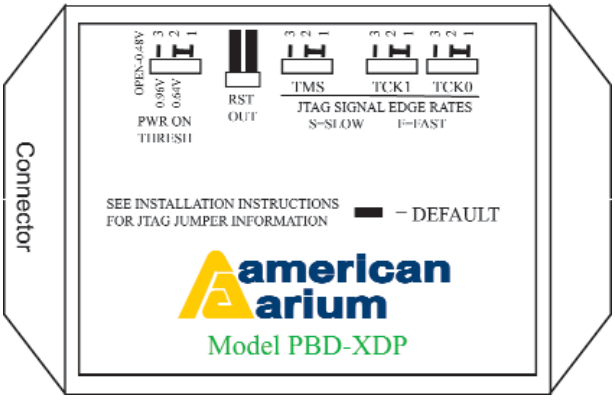

Figure 1

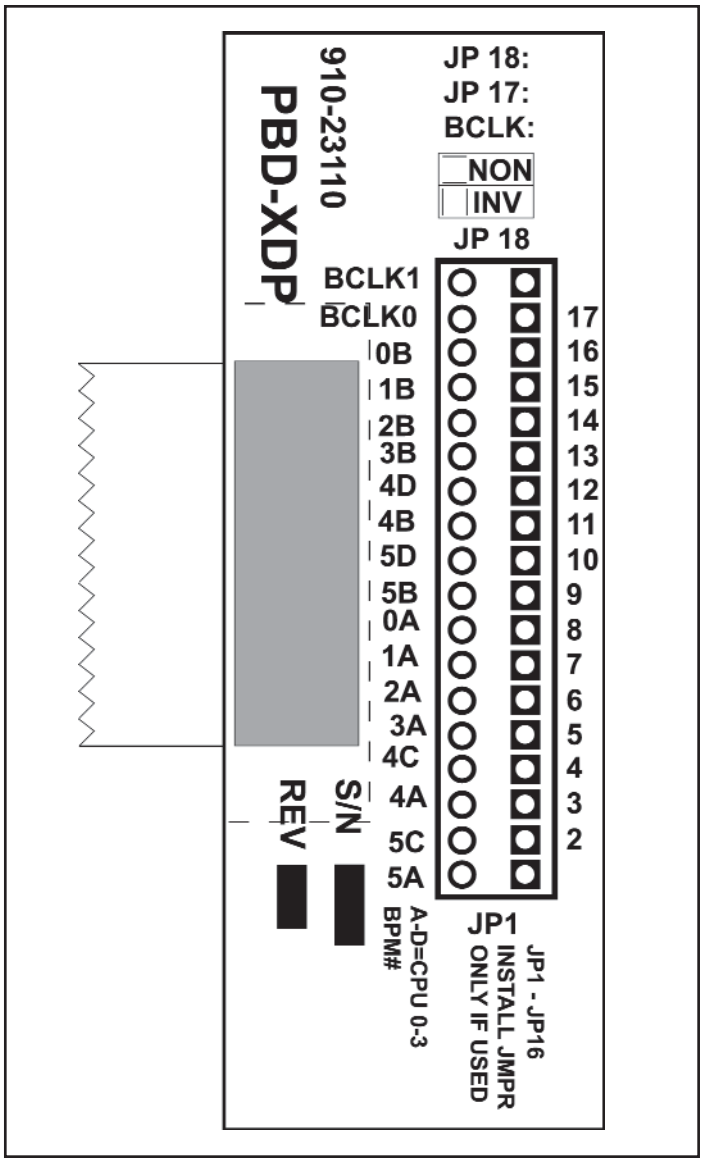

Figure 2