Debug Port Design Guide for Target Systems Based on Intel® Pentium® II or Pentium III Xeon™ Processors

An Application Note

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This design guide applies to target systems with the following processor characteristics. If your target system does not match the following chart, please contact American Arium for the appropriate design guide that matches your target system.

Processor Type	Number of Processors	Package Type
Pentium II Pentium III	1 to 4 Processors	SC330 Cartridge

Debug Port Ground Pins

Signal	Pin	Description	Suggested Termination
GND	2, 4, 6, 13, 15, 17, 19, 21, 23, 25, & 27	Signal grounds.	Connect to ground

Debug Port Output Signal Pins (Driven By Target)

Signal	~~Pin~~	Description	Suggested Termination
TDO	10	TAP Data Out (From last processor of scan chain to debug port)	See below Note 1
PRDY0#	18	Processor PRDY signal. From 1st processor in single/multiprocessor system.	See below Note 2
PRDY1#	22	Processor PRDY signal. From 2nd processor in a multiprocessor system.	See below Note 2
PRDY2#	26	Processor PRDY signal. From 3rd processor in a multiprocessor system.	See below Note 2
PRDY3#	30	Processor PRDY signal. From 4th processor in a multiprocessor system.	See below Note 2
RESET#	1	Processor RESET signal. This allows the emulator to sense when the processor is being reset.	See below Note 3
V_{TT}	9	Target V_{TT}. The emulator uses V_{TT} to detect target power and establish the GTL+ threshold.	1.5KΩ to V_{TT}
BCLK	29	Private copy of BCLK. This allows the emulator to provide a TCK that is synchronous with BCLK.	

Debug Port Input Signal Pins (Driven By Emulator)

Signal	Pin	Description	Suggested Termination
TDI	8	TAP Data In (From debug port to TDI of first processor in scan chain)	See below Note 1
TMS	7	TAP Mode Select	See below Note 4
TCK	5	TAP Clock. Of the debug port signals, this is the most critical signal.	See below Note 5
TRST#	12	TAP Reset	470Ω to ground
BSEN#	14	Boundary scan (TAP) enable. Emulator has access to TAP signals of CPU when low	See below Note 6
PREQ0#	16	Processor PREQ signal. To 1st processor in a single/multiprocessor system.	See below Note 7
PREQ1#	20	Processor PREQ signal. To 2nd processor in a multiprocessor system.	See below Note 7
PREQ2#	24	Processor PREQ signal. To 3rd processor in a multiprocessor system.	See below Note 7
PREQ3#	28	Processor PREQ signal. To 4th processor in a multiprocessor system.	See below Note 7
DBRESET#	3	Target reset. When driven low, the target should reset the system and CPU.	See below Note 8
DBINST#	11	Emulator installed. Debug cable grounds this signal, allowing target to detect the emulator.	See below Note 6

The resistor values given are in ohms and are typical values. Actual values are dependent on the target layout. Resistors should have a 1% or better tolerance.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

The Debug Port connection is achieved by way of a 30-pin connector specified as AMP 104068-3. See the following pin numbering diagram.

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29

Top View Of Connector With Pin Numbering

Voltage Definitions

V_CMOS	Defined as the voltage level used to determine the processor CMOS logic high level (2.5V).
V$_{TT}$	Defined as the voltage level used to determine the processor GTL+ logic high level.

Note 1:

TDI on each processor has it's own pull-up on TDI. The last processor in the JTAG scan chain should have it's TDO signal pulled up to V_{CC} with a 150Ω resistor. If jumpers are used to configure the target system debug port to accommodate the processors present, the following jumper scheme will accomplish this. If the system will be designed as a two processor system, delete the circuitry associated with processors 1 and 2.
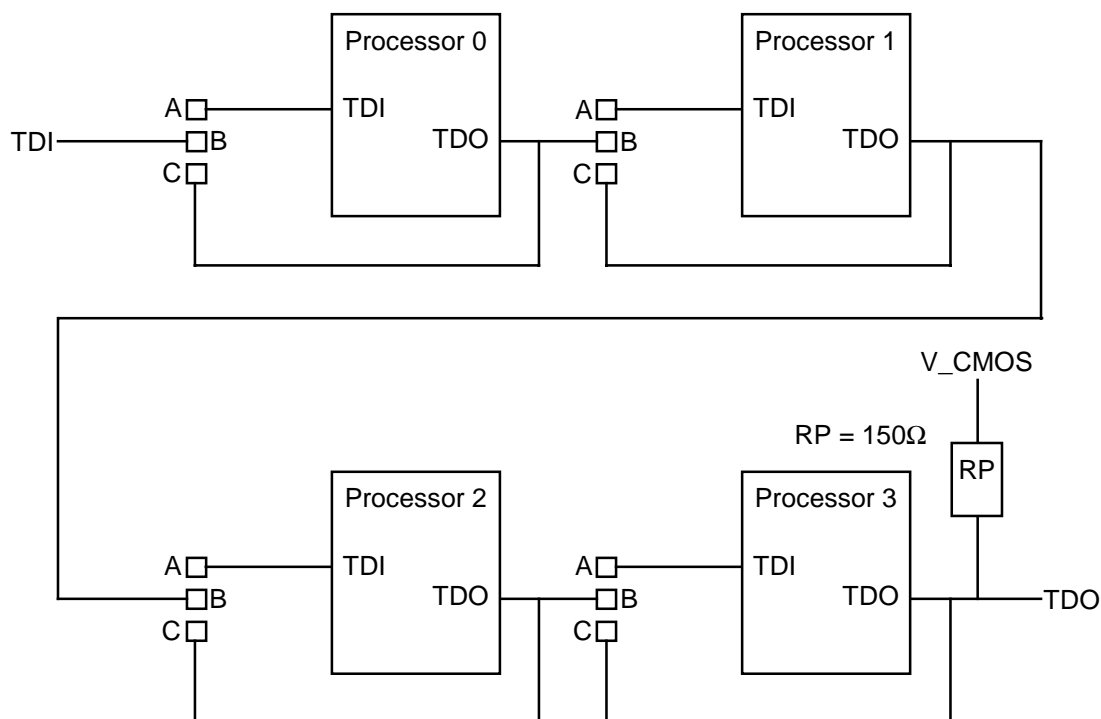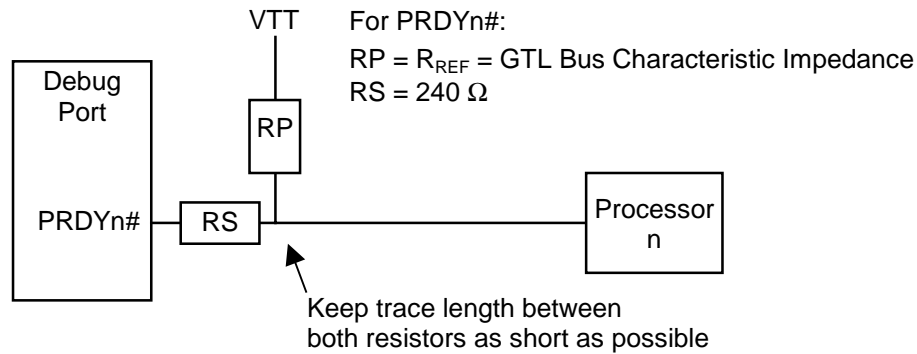
Processor Status	Jumper Setting
Processor Installed	A to B
Processor Not Installed	B to C

Note: PII and PIII Xeon processors have internal 150Ω pull-up resistors on their TDI pins.
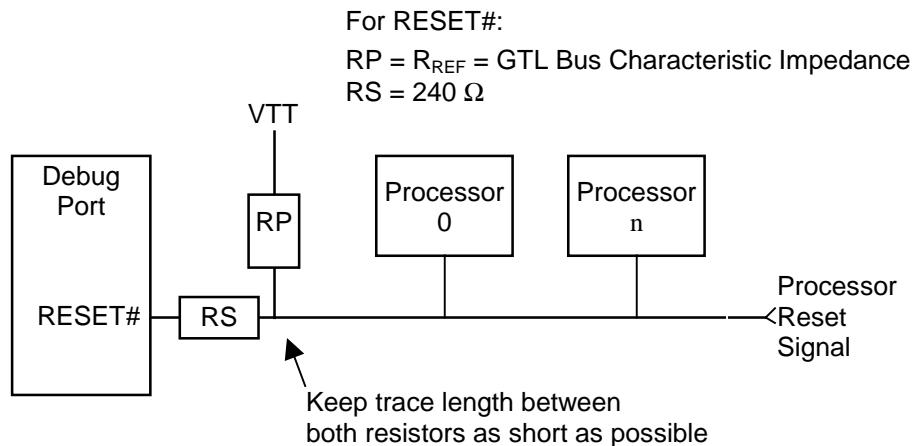
Note 2:

The PRDYn# signals are GTL+ signals and should be end terminated to V_{TT} through a resistor equal to the characteristic impedance of the target's GTL bus. The signal supplied to the debug port should pass through a 240Ω series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of these traces. End termination resistor values for GTL signals vary according to the effective trace impedance and V_{TT} power dissipation issues.

VTT

For PRDYn#:

RP = R_{REF} = GTL Bus Characteristic Impedance

RS = 240 Ω

Debug Port

RP

PRDYn# RS

Processor n

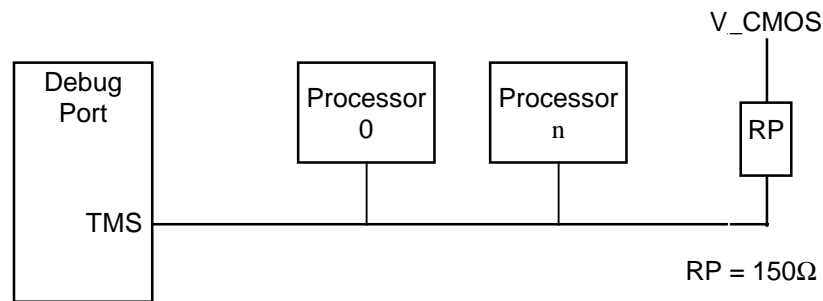Keep trace length between both resistors as short as possible

Note 3:

RESET# is a GTL+ signal and should be end terminated to V_{TT} through a resistor equal to the characteristic impedance of the target's GTL bus. The signal supplied to the debug port should pass through a 240Ω series resistor located as close as possible to the nearest terminated end. Do not add any stubs off of this trace.

For RESET#:

RP = R_{REF} = GTL Bus Characteristic Impedance

RS = 240 Ω

VTT

Debug Port

RP

Processor 0

Processor n

RESET# RS

Processor Reset Signal

Keep trace length between both resistors as short as possible

Note 4:

TMS should be end terminated with a 150Ω resister to V_CMOS.

V_CMOS

| Debug Port | | Processor 0 | | Processor n | | RP |

TMS ————————————————————————————————

RP = 150Ω

Note 5:

TCK is the most critical of the ITP signals. A separately buffered copy of this signal must be provided to each processor as shown below. The actual value of the first series resistor (indicated below as 5Ω) depends on the output resistance of the driver. The combined resistance of the driver and the first series resistor should be 22Ω. In most cases this resistor will be about 5Ω. A 2.5V buffer such as a 74LVQ244 or equivalent should be used.

The combined resistance of the driver and the first series resistor should be 22Ω.

Vcc

1K Ω

TCK From Debug Port ———— #0 ——— 5Ω ——— 33nH ——— 22Ω ——— TCK To Processor 0

100 pF

#1 ----

#2 ----

#3 ----
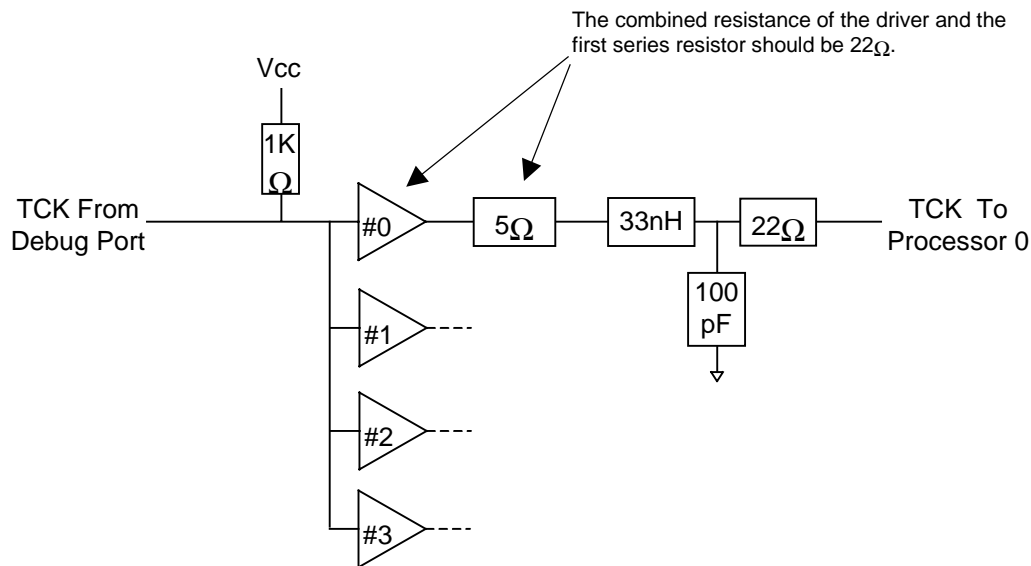
Note 6:

BSEN# and DBINST# are driven by open drain devices. If these signals are used by the target, they should each be pulled up to their own V_{OH} level (not to exceed 5.5V) through a resistor that will limit I_{OL} current to 48 mA. If these signals are not used by the target, they may be left open.

Note 7:

PREQ0# and PREQ1# should be pulled up to V_CMOS using a resistor in the range of 200Ω to 300Ω.

Note 8:

DBRESET# is driven by an open drain device. It should be pulled up to its V_{OH} level (not to exceed 5.5V) through a resistor that will limit I_{OL} current to 48 mA. Intel recommends 240Ω.

DISCLAIMER:

In cases where the preceding guidelines differ from the current guidelines provided by Intel, the Intel guidelines will take precedence.