Debug Port Design Guide for Target Systems Based on a Single Intel® Pentium® 4 Processor (PGA-423)

An Application Note

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This design guide applies to target systems with the following processor characteristics. If your target system does not match the following chart, please contact American Arium for the appropriate design guide that matches your target system.

Processor Type	Number of Processors	Package Type
Pentium 4	Single Processor	PGA-423

Debug Port Ground And Key Pins

Signal	Pin	Description	Suggested Termination
GND	1, 2, 8, 20, & 25	Signal grounds.	Connect to ground
Key	26	Pin 26 must be removed to act as a key	Connect to ground

Debug Port Input Signal Pins (Driven By Emulator)

Signal	Pin	Description	Suggested Termination
23	BPM5DR#	Used by the emulator to request control of the processor(s). Similar to the function of PREQ on earlier processors.	See note A
4	DBA#	Debugger Acknowledge. Debugger has access to TAP signals of CPU when low.	See note B
6	DBR#	Target Reset. When driven low, the target should reset the system and CPU.	See note C
10	TDI	TAP Data In (To first processor in scan chain)	See note D
12	TMS	TAP Mode Select	See note E
14	TRST#	TAP Reset	See note F
16	TCK	TAP Clock. Of the debug port signals, this is the most critical signal.	See note G
18	FBI	Unfiltered copy of TCK for optional use by target platform.	See note H

Debug Port Output Signal Pins (Driven By Target)

Signal	Pin	Description	Suggested Termination
3	BPM[0]#	Break Point Monitor 0.	See note I
5	BPM[1]#	Break Point Monitor 1.	See note I
7	BPM[2]#	Break Point Monitor 2.	See note I
9	BPM[3]n	Break Point Monitor 3.	See note I
11	BPM[4]#	Break Point Monitor 4. Monitored by emulator to detect emulator control of processor(s).	See note I
13	BPM[5]#	Break Point Monitor 5. Monitored by emulator to detect emulator control of processor(s).	See note I
15	RST#	Processor RESET Signal. This allows the emulator to sense when the processor is being reset.	See note I
17	FBO	TCK signal fed back to debug port.	See note J
19	BCLKp	Private copy of the differential BCLK active on it's rising edge. This allows the emulator to provide a TCK that is synchronous with BCLK.	See note K
21	BCLKn	Private copy of the differential BCLK active on it's falling edge. This allows the emulator to provide a TCK that is synchronous with BCLK.	See note K
24	TDO	TAP Data Out (From last processor of scan chain to debug port)	See note L
22	Power	Target V_{CC}. The emulator uses V_{CC} to detect target power and establish threshold levels.	1.5K to VTERM

The resistor values given are in ohms and are typical values. Actual values are dependent on the target layout. Resistors should have a 1%.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

The Debug Port connection is achieved by way of a 26-pin connector specified as Framatone Connectors International part number 61641-303 or 61698-302TR. Pin 26 of the connector is removed and acts as a key. See the following pin numbering diagram.

2	4	6	8	10	12	14	16	18	20	22	24	
1	3	5	7	9	11	13	15	17	19	21	23	25

Top View Of Connector With Pin Numbering

Note A:

BPM5DR# should be tied to BPM5# at the debug port

Note B:

DBA# is driven by an open drain device. If this signal is used by the target, it should each be pulled up to V_{CC} through a resistor placed as close as possible to the debug port that will limit I_{OL} current to 48 mA. Intel recommends 150Ω to 240Ω.

Note C:

DBR# is driven by an open drain device. It should each be pulled up to V_{CC} through a resistor placed as close as possible to the debug port that will limit I_{OL} current to 48 mA. Intel recommends 150Ω to 240Ω.

Note D:

TDI should be pulled up to VTAP with a 150Ω resistor placed as close as possible to TDI on the processor.

Note E:

TMS should be pulled up to VTAP with a 39Ω resistor placed as close as possible to the debug port.

Note F:

TRST# should be pulled down to ground with a resistor. Intel recommends 500Ω to 680Ω.

Note G:

TCK should be pulled down to ground with a 27Ω resistor placed as close as possible to the debug port.

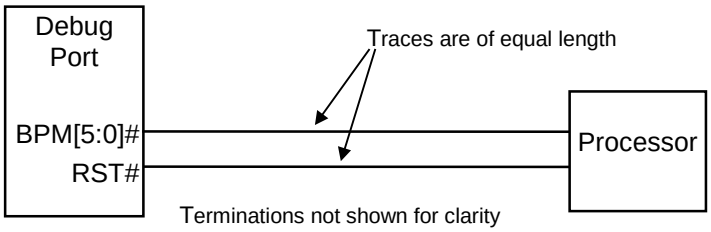
Note H:

If FBI is used by the target to produce a TCK signal, it should be terminated with a 220Ω resistor to ground at the input of the device receiving the signal.

Note I:

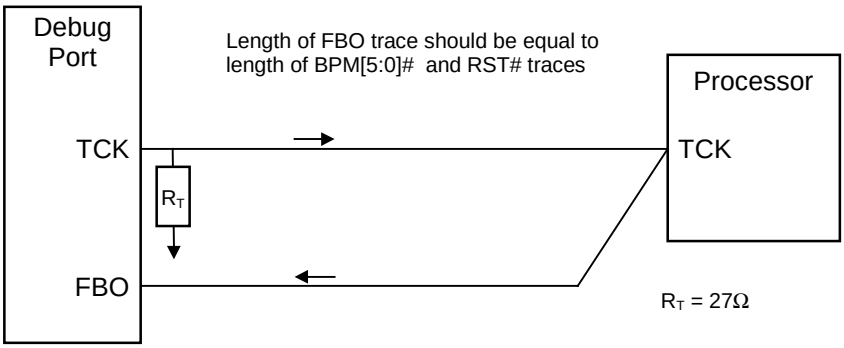
It is critical that the BPM[5:0]# and RST# signals have a matched flight time between the processor and the debug port. This is achieved in part by making the BPM[5:0]# and RST# traces of equal length. These signals must have a specific time correlation to BCLK (see Note K).

The BPM[5:0]# and RST# signals are all GTL+ signals and should be properly end terminated (at both ends) with resistors to VTERM. The value of the resistors is dependent on the impedance of the target system's GTL+ bus.



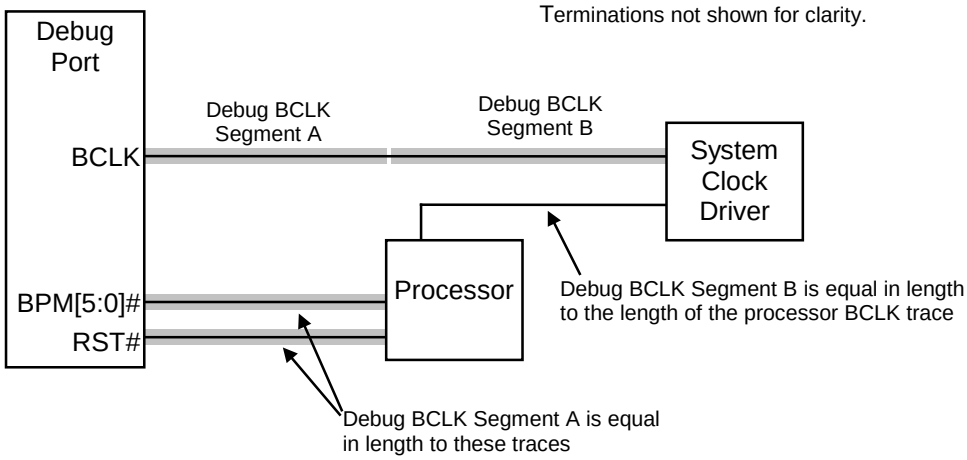
Note J:

The FBO is a feedback of the TCK (or filtered FBI) signal. It is not used by American Arium emulators. However, American Arium emulators terminate it to ground through an 82Ω resistor to insure compatibility.



Note K:

BCLKp and BCLKn should be terminated in a manner that is consistent with the needs of the target design. This pair of traces delivering a private copy of the differential BCLK to the debug port should have a specific length. This length is equal to the length of the BPB[5:0]# or RST# traces to the nearest processor (see Segment A below) plus the length of the BCLK traces to the processors (see Segment B below).



Note L:

TDO should be pulled up to VTAP with a 75Ω resistor placed as close as possible to the debug port.

DISCLAIMER:

In cases where the preceding guidelines differ from the current guidelines provided by Intel, the Intel guidelines will take precedence.

14811 Myford Road, Tustin, CA 92780 Voice: 877-508-390 Fax: 714-731-6344 E-mail: info @arium.com Web www.arium.com

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