PBDS-PSC

Overview

The purpose of the PBDS-PSC module is to act as a buffer and provide voltage level shifting between the target debug/ITP port and the ECM-20 or TRC-20 for Intel® Pentium® 4 and Xeon™ family processors and other future processors. This allows the ECM or TRC to work with a number of different processors using the ITP700 Debug Port specified by Intel Corporation.

The PBDS-PSC is composed of two modules connected by ribbon cable:

PBD-PSC: A personality module that resides between the ECM/TRC and the PBDI-PSC. It provides power and signal conversion for the PBDI-PSC.

PBDI-PSC: An interface module that connects the PBD-PSC to the target system's debug/ITP port and buffers the signals going back to the PBD-PSC.

Note: The PBDS-PSC is specifically designed for use with the ECM-20 or TRC-20. It is extremely important that the jumpers are in the correct position PRIOR to installation. Jumpers set in the wrong position may cause damage to the target system, processor, or base unit.

I/O Voltage Jumper Settings for Intel Pentium 4 and Xeon Family Processors

Figure 1 shows the JTAG I/O voltage produced by the PBDS-PSC based on the PBD-PSC module jumper settings for jumpers E9 and E10. The default positions are denoted by bold-faced text. These settings should be satisfactory for all Pentium 4 and Xeon family processors.

Certain processors may require tracking of the GTL bus termination voltage (VTT) to define the JTAG I/O voltage. The default positions listed in Figure 1 should satisfy current and future processor requirements. For additional information, see Intel processor documentation or contact American Arium Technical Support at 877-508-3970 toll free in the US or 714-731-1661 outside the US or e-mail support@arium.com.

Threshold and Filter Jumper Settings

Figures 2, 3, and 4 show jumper settings for threshold and filters integrated into the PBDI-PSC module. The default settings are satisfactory for most targets and should not be modified. Please contact American Arium for additional information regarding filter design.

E9 Jumper Position	E10 Jumper Position	I/O Voltage
FIXED	1.25V	1.25 VOLTS
FIXED	1.40V	1.40 VOLTS
FIXED	1.70V	1.70 VOLTS
FIXED	1.58V	1.58 VOLTS
TRACKING VTT	1.25V	VTT + 0.015 VOLTS
TRACKING VTT	**1.40V**	**VTT + 0.165 VOLTS**
TRACKING VTT	1.70V	VTT + 0.465 VOLTS
TRACKING VTT	1.58V	VTT + 0.345 VOLTS

Figure 1: I/O voltage jumper settings for Pentium 4 and Xeon family processors (Information in bold face indicates default settings.)

E1 JUMPER POSITION	TDO RECEIVE THRESHOLD
1-2	**2/3 OF TARGET POWER-ON VOLTAGE FROM PIN 22 OF DEBUG PORT**
2-3	1/2 OF LOGIC HI LEVEL SET THROUGH E9/E10 OF PBDS-PSC

Figure 2: Threshold anfilter jumper settings for E1 jumper position. (Information in bold face indicates default settings.)

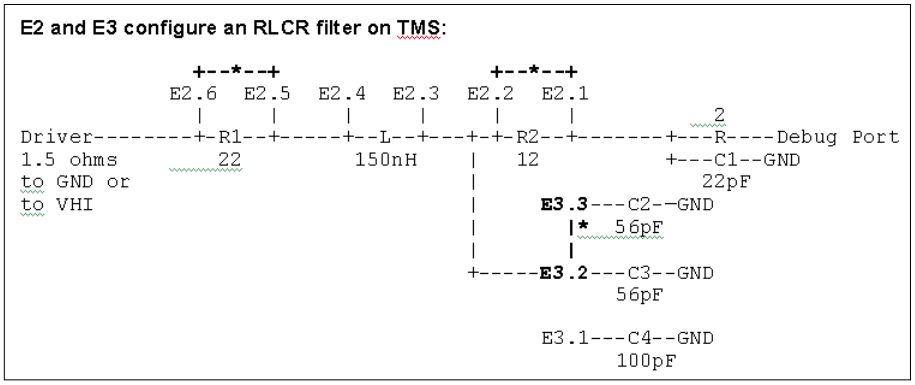

Figure 3: E2 and E3 configure an RLCR filter on TMS

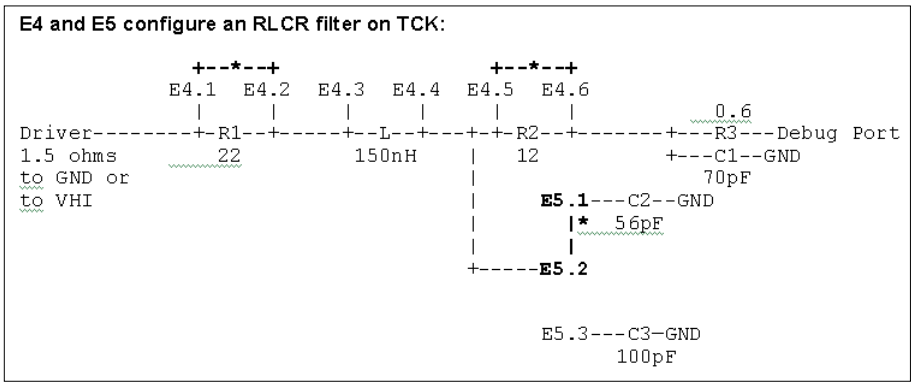

Figure 4: E4 and E5 configure an RLCR filter on TCK