American Arium
Application Note

Disabling the TCO Timer in an Intel I/O Controller Hub (ICH)

Overview

American Arium has found that target motherboards with Intel I/O Controller Hubs (ICHs) may not progress through the Power On Self-Test when held at the reset vector by an ECM-20/50. This is caused by the expiration of the TCO Timer in the ICH. The expiration of the TCO timer can cause an SMI#, set status bits, or cause a system reboot.

When the American Arium ECM-20/50 emulator is connected to a target with an ICH, the processor is held at the reset vector and does not execute any instructions until the ECM releases it. However, the TCO Timer counts independently of the processor. Therefore, it is necessary to disable the TCO timer in the ICH to allow the user to stop the processor for extended periods of time.

Disabling the TCO timer

The TCO Timer should be disabled immediately following a target reset or power-up. Using a macro that resets the target is an easy way of doing this. Disabling the TCO Timer is a simple matter of halting the TCO Timer, clearing TCO status bits, and disabling the TCO reboot.

At reset, the TCO registers are not yet available, so the PMBASE register of the LPC device must be set to the I/O base address of the TCO registers. Also, I/O decode of the TCO registers is enabled by the ACPI_EN bit in the ACPI_CNTL register.

The following registers should be written:

1. Set NO_REBOOT (bit 1) in GEN_STA register of the LPC device
2. Set ACPI Base Address (I/O) in PMBASE (bits 7-15 only)
3. Set ACPI_EN (bit 4) in ACPI_CNTL register to enable I/O decode
4. Disable TCO timer (TCO_TMR_HLT, bit 11) in TCO1_CNT
5. Clear SECOND_TO_STS (bit 1) in TCO2_STS
6. Clear BOOT_STS (bit 2) in TCO2_STS
7. Clear TIMEOUT (bit 3) in TCO1_STS

These steps are included in the sample macro on the following page. This macro is also available for download at www.arium.com/support/techdocs.html.

```
reset

#define LPC_BUS 0
#define LPC_DEV 0x1F
#define LPC_FUN 0
#define LPC_BDF 0x80000000 + (LPC_BUS << 16t) \
                           + (LPC_DEV << 11t) \
                           + (LPC_FUN << 8t)

// LPC PCI configuration registers
#define GEN_STA   (LPC_BDF + 0xD4)
#define PMBASE    (LPC_BDF + 0x40)
#define ACPI_CNTL (LPC_BDF + 0x44)

// The PMBASE_ADDR is a settable value written to PMBASE PCI register
#define PMBASE_ADDR    0x800
#define TCOBASE_ADDR   (PMBASE_ADDR+0x60)

// System Management TCO registers
#define TCO1_STS  (TCOBASE_ADDR + 0x4)
#define TCO2_STS  (TCOBASE_ADDR + 0x6)
#define TCO1_CNT  (TCOBASE_ADDR + 0x8)

//-------------------------------------------------------------
// Set NO_REBOOT (bit 1) in GEN_STA register
dport 0xCF8 = GEN_STA
dport 0xCFC |= 0x2

//Set ACPI Base Address (I/O) in PMBASE (bits 7-15 only)
dport 0xCF8 = PMBASE
dport 0xCFC |= PMBASE_ADDR

// Set ACPI_EN (bit 4) in ACPI_CNTL register to enable I/O decode
dport 0xCF8 = ACPI_CNTL
dport 0xCFC |= 0x10

//Disable TCO timer (TCO_TMR_HLT, bit 11) in TCO1_CNT
wport TCO1_CNT |= 0x800

//Clear SECOND_TO_STS (bit 1) in TCO2_STS
wport TCO2_STS |= 0x2

//Clear BOOT_STS (bit 2) in TCO2_STS
wport TCO2_STS |= 0x4

//Clear TIMEOUT (bit 3) in TCO1_STS
wport TCO1_STS |= 0x8

//clean up variables
#undef LPC_BUS
#undef LPC_DEV
#undef LPC_FUN
#undef LPC_BDF
#undef GEN_STA
#undef PMBASE
#undef ACPI_CNTL
#undef PMBASE_ADDR
#undef TCOBASE_ADDR
#undef TCO1_STS
#undef TCO2_STS
#undef TCO1_CNT
```

SourcePoint commands to disable ICH TCO Timer.

Additional Resources

http://developer.intel.com/design/chipsets/datashts/ (See ICH datasheets).

Contact American Arium Support at 877-508-3970, or email support@arium.com for any other questions regarding this update.

14811 Myford Road, Tustin, CA 92780 Voice: 877-508-3970 in the US, 714-731-1661 outside the US Fax: 714-731-6344
E-mail: info@arium.com Web www.arium.com

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