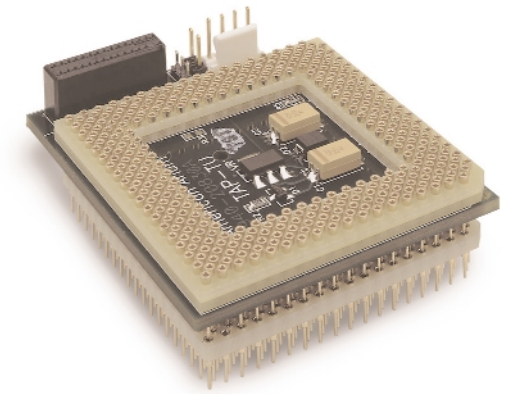
Getting Started Guide

TAP-TU



Overview

The TAP-TU is the debug port adapter for Intel® Celeron™, Pentium® III, and Pentium III-new processor target systems using the PGA370 package. It provides debug access to target systems that have been designed or built without a debug/ITP port or systems where the debug/ITP port is not operating correctly.

Unpacking the Equipment

Carefully remove the equipment from the box and refer to the enclosed packing list to ensure that you received all items.

TAP-TU Installation

1. Using the table below, confirm jumper settings.

Processor	Jumper E1 (top)	Jumper E2 (bottom)
Pentium III-new	VTT position	NOT installed
Pentium III	VCM position	NOT installed
Celeron	VCM position	Installed

2. Remove the processor from the target and insert it into the TAP-TU. Ensure that the processor is correctly inserted into the socket on the TAP-TU. Find the "notched" corner on the socket.

3. Carefully insert the TAP-TU (with processor) into the target processor socket. Ensure that the TAP-TU is correctly inserted into the target board socket.

4. *Note: For Celeron and Pentium III processors, skip to Step 5.*

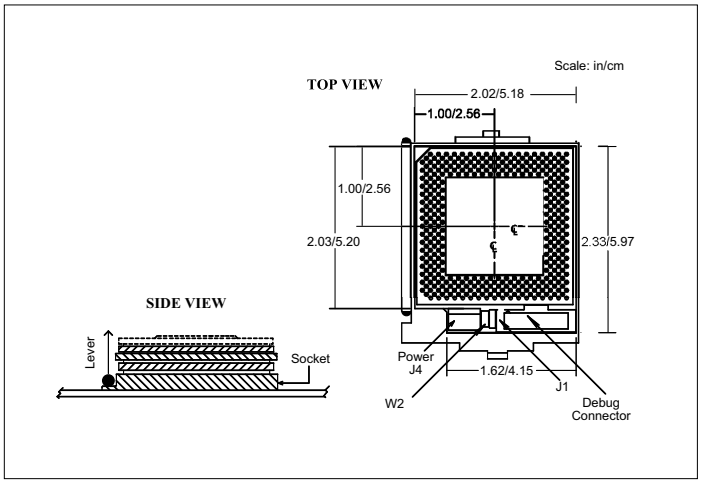
   For Intel Pentium III-new processors, connect the TAP-TU to a voltage supply. Use the supplied power cable to connect the TAP-TU to the target system's 5V supply (via disk drive supply).

   Note: The 4-pin connector on the TAP-TU has the pinout: + G G +. This power input will work with any voltage from +3.3V to +12V. A 12V-tolerant transient voltage suppressor diode from the (+) to GND protects the TAP-TU from over-voltage or reverse polarity. This supply provides the TAP-TU the input pullup supply voltage required for operation.

5. Connect the twisted yellow and black DBRESET# cable from the 2-pin header on the TAP-TU to the target system's RESET button posts.

   Note: The header pin near the processor is GND, and the pin away from the processor is DBRESET#. Use an ohm-meter to determine which of the target RESET post pair is GND, and orient the cable connectors such that the black wire is contacting the GND post on either end.

6. Connect the debugger (PBD-S2V) cable assembly to the 30-pin Debug/ITP connector (J1) on the TAP-TU. You will need the following information:
   - The PBD-S2V must be set for 1.58 Volts out (jumper removed) for Intel Pentium III and Pentium III-new processor operation.
   - For Celeron processors, the setting is dependent on the VCMOS level, typically 1.5v or 2.5v - check your target system for correct level.
   - The TCK Current Level setting in SourcePoint (via the Emulation Configuration window) should be set at level 4 for proper operation.



If you have any problems or questions, contact American Arium Technical Support at 877-508-3970 toll free or 714-731-1661 outside the US or e-mail support@arium.com for assistance.