

## Overview

The TAP-PSC is the debug port adapter for Intel® Pentium® 4 processor target systems using a 478-pin uFCPGA package. It provides debug access to target systems that have been designed or built without a debug/ITP port or systems where the built-in debug/ITP port is not operating correctly.

## Unpacking the Equipment

Carefully remove the equipment from the box and refer to the enclosed packing list to ensure that you received all items.

## TAP-PSC Installation

1. Remove the processor from the target and insert it into the TAP-PSC. Ensure that the processor is correctly inserted into the socket on the TAP-PSC.

*Note: This socket is not keyed; Pin 1 is identified by the RED inked corner. Disregard the socket pin indicators on the TAP-PSC.*

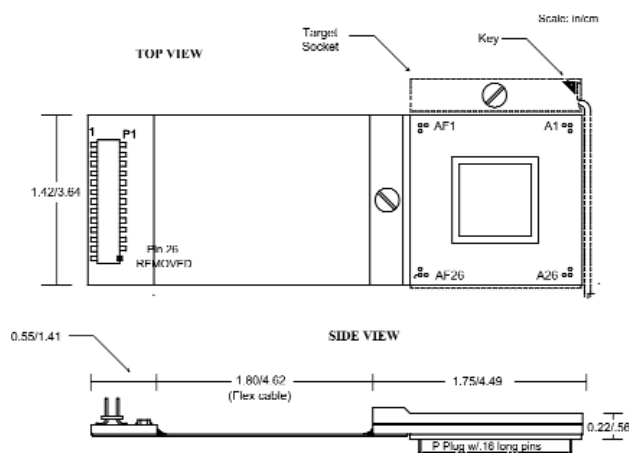
2. Carefully insert the TAP-PSC (with processor) into the target processor connector. Ensure that the TAP-PSC is correctly inserted into the target board socket with pin 1 of the processor oriented to the motherboard socket. The TAP-PSC pins have been keyed to assist placement. Place the processor heat sink on the processor die.
3. If the system has a built-in debug port, it is possible that three (3) debug signals have not been connected to the processor socket:
  - ITP\_CLK0
  - ITP\_CLK1
  - DBRESET#.

Some systems may be reconfigurable to route the two clocks to the socket instead of the built-in debug port. These clocks are REQUIRED by the TAP-PSC.

If DBRESET# is not connected to the processor socket, connect the reset adapter (yellow and black twisted pair cable provided with the ECM-20 or PBDS-700) between the target system's reset connector (if available) and the base unit connector labeled "TARGET RESET OUT" or PBD connector labelled "RSTSW."

*Note: The reset adapter is not polarized and does not need to be connected in any particular orientation since it is effectively just a switch closure. It should be connected to the target system wherever a reset switch would normally be connected.*

4. Connect the PBDS-WF/NW/PSC/700 to the P1 connector of the TAP-PSC using the PBDI-WF/NW/PSC/700 interface module.



5. Connect the entire PBDS assembly to the base unit via the 40-pin connector.
6. When using the TAP-PSC in conjunction with an Arium PBDS-WF/NW/PSC/700, JTAG communication can be improved if E4 pins 3 and 4 are jumpered on the respective PBDI. If no jumper is available, the E5 jumper may be removed and installed on E4 (E4 will then have 3 jumpers installed: 1-2, 3-4, 5-6).



Jumpers should be installed to their default positions when using the PBDS assembly with a built-in debug/ITP port.