IDE Host Controller Data Sheet

Proven System Block (PSB) for QuickLogic Customer Specific Standard Products (CSSPs)

Features

The QuickLogic IDE Host Controller has the following features:

- Supports PIO Mode 0 to PIO Mode 4
- Supports Multiword DMA Mode 0 to Mode 2 with maximum Multiword DMA Mode 2 performance up to 16.7 Mbytes/sec. (excluding OS overhead)
  - Greater than 10 Mbytes/sec. transfer rate measured under WinCE 5.0
- Supports Ultra-DMA (UDMA) Mode 0 to Mode 4 with maximum UDMA Mode 4 performance up to 66 Mbytes/sec.
- Supports connection to hard disk drives and/or CD-ROM/DVD-ROM (ATAPI) devices and is also compatible with Compact Flash/PCMCIA card in TRUE-IDE/ATA mode
- Internal IDE sector buffering for increased performance ("prefetch" sector transfers)
- 3.3 V IDE signaling

Overview

In spite of rapid growth in NAND flash memory, hard disk drives (HDDs) still hold a big advantage of much lower cost per Megabyte, which is expected to continue in the foreseeable future. For high-capacity media players, portable media servers and data backup systems, the hard disk drive is the number one choice over flash.

The traditional HDD interface is called IDE or P-ATA, which is a parallel interface requiring many I/O pins. Most of application processors do not support it natively due to the high pin count. The IDE Host Controller offered by QuickLogic, as a PSB, seamlessly adds HDD or DVD ROM storage capability to a host processor. The IDE Host Controller connects to the CPU through its memory interface. It controls and manages traffic between the host processor and the HDD. Utilizing the hardware DMA on the processor, the IDE Host Controller off-loads the CPU during data transfers to and from the HDD, providing high throughput to improve system performance while consuming very little power.

Table 1 and **Table 2** show performance values using the PXA320 processor with a 1.8 in. HDD.

Table 1: Performance Values from Processor to IDE

Operating System	Read	Write
Linux	13 MBytes/sec.	11 MBytes/sec.
WinCE	10 MBytes/sec.	10 MBytes/sec.

Table 2: Performance Values from USB to IDE

Operating System	Read	Write
Linux	30 MBytes/sec.	24 MBytes/sec.
WinCE	30 MBytes/sec.	21 MBytes/sec.

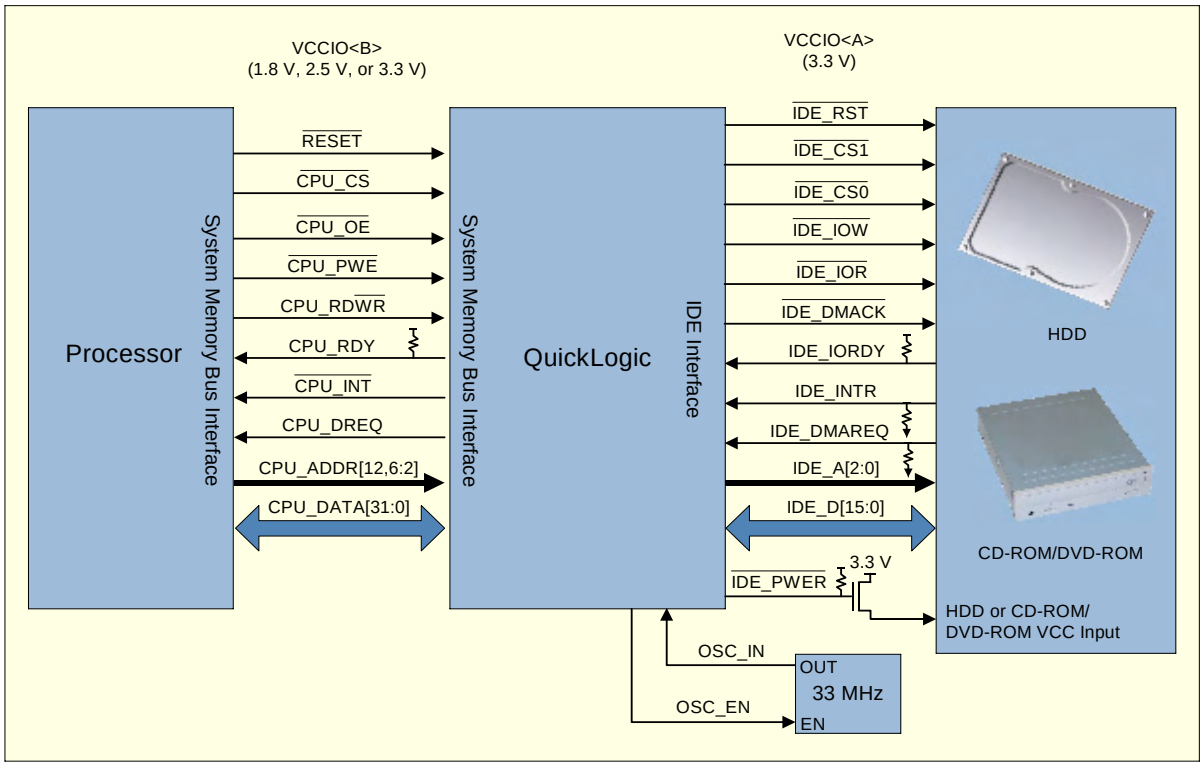
IDE Host Controller Architecture

The host processor communicates to the IDE Host Controller via its system memory interface. QuickLogic CSSPs are based on its proprietary ViaLink® programmable fabric technology and therefore can be customized to seamlessly interface with any types of host processors. The CSSP performs internal decoding of the local address and directs the memory data transaction towards the status/control registers or IDE interface. By using the CSSP, designers are provided with the ability to seamlessly add IDE connectivity not natively supported.

The IDE Host Controller uses an on-board sector buffer RAM so that the CPU can perform read and write operations in full 512-byte sectors without interruption or waiting for the externally connected IDE Host Controller to be ready. 16-bit wide IDE data words are stacked in the internal sector buffers so that all read and write operations to the IDE Host Controller from the host processor can be performed in 32-bit mode.

Figure 1 shows a system level block diagram of the IDE Host Controller.

Figure 1: IDE Host Controller System Level Block Diagram



Interface List and Description

Table 3 summarizes the IDE Host Controller interface signals.

Table 3: Pin Descriptions

Pin	Type[a]	I/O Rail Voltage	Description
General Signals			
OSC_IN	I	VCCIO<A>	**Clock Input.** This input should be driven by a 33 MHz clock source. Alternatively, a 26 MHz to 66 MHz oscillator may be used. However, the software driver must be modified to support a frequency other than 33 MHz.
OSC_EN	O	VCCIO<A>	**Oscillator Enable.** When high, this pin indicates that the external oscillator providing the OSC_IN input must be enabled.
$\overline{\text{RESET}}$	I	VCCIO<B>	**Reset Input.** Active low asynchronous hardware reset input.
$\overline{\text{IDE\_PWER}}$	OZ	VCCIO<A>	**IDE Power Control.** When low, this signal indicates that power must be applied to the externally connected HDD or CD-ROM/DVD-ROM device. This is an open collector output. This signal must be pulled up to a voltage equal to or less than VCCIO<A>.
Host Interface			
CPU_ADDR [12, 6:2]	I	VCCIO<B>	System Memory Interface address bus.
CPU_DATA[31:0]	I/O	VCCIO<B>	System Memory Interface data bus. This bus is Hi-Z when $\overline{\text{RESET}}$ or LPM is asserted.
$\overline{\text{CPU\_CS}}$	I	VCCIO<B>	System Memory Interface active low chip select.
$\overline{\text{CPU\_OE}}$	I	VCCIO<B>	System Memory Interface active low output enable.
$\overline{\text{CPU\_PWE}}$	I	VCCIO<B>	CPU active low write enable.
CPU_RDY	OZ	VCCIO<B>	CPU ready signal, open drain output. Pull high (to VCCIO<B>) with a 10 K Ohm resistor. This is a shared (wire OR'd) signal with other system memory bus components. This signal is Hi-Z when $\overline{\text{RESET}}$ or LPM is asserted.
CPU_RD$\overline{\text{WR}}$	I	VCCIO<B>	System Memory Interface read / not write indicator.
$\overline{\text{CPU\_INT}}$<B>	O	VCCIO<B>	CPU active low interrupt. Two outputs are provided, one in Bank A and one in Bank B. Either may be chosen based upon system I/O voltage requirements.
$\overline{\text{CPU\_INT}}$<A>	O	VCCIO<A>	
CPU_DREQ<B>	O	VCCIO<B>	CPU DMA request. Two outputs are provided, one in Bank A and one in Bank B. Either may be chosen based upon system I/O voltage requirements.
CPU_DREQ<A>	O	VCCIO<A>	

Table 3: Pin Descriptions *(Continued)*

Pin	Type[a]	I/O Rail Voltage	Description
IDE Interface			
IDE_A[2:0]	O	VCCIO<A>	ATA address bus.
IDE_D[15:0]	I/O	VCCIO<A>	ATA data bus. This bus is Hi-Z when $\overline{\text{RESET}}$ or LPM is asserted.
$\overline{\text{IDE\_RST}}$	O	VCCIO<A>	ATA active low reset.
$\overline{\text{IDE\_CS1}}$	O	VCCIO<A>	ATA active low control block select.
$\overline{\text{IDE\_CS0}}$	O	VCCIO<A>	ATA active low command block select.
$\overline{\text{IDE\_IOR}}$	O	VCCIO<A>	ATA active low I/O read strobe.
$\overline{\text{IDE\_IOW}}$	O	VCCIO<A>	ATA active low I/O write strobe.
IDE_IORDY	I	VCCIO<A>	ATA I/O ready. Pull high (to VCCIO<A>) with a 10 K Ohm resistor.
IDE_INTR	I	VCCIO<A>	ATA interrupt request. Pull low (to GND) with a 10 K Ohm resistor.
$\overline{\text{IDE\_DMACK}}$	O	VCCIO<A>	ATA active low DMA acknowledge.
IDE_DMAREQ	I	VCCIO<A>	ATA DMA request. Pull low (to GND) with a 10 K Ohm resistor.

a. I = Input
O = Output
I/O = Bidirectional
OZ = Open drain

Register Sets

Memory Map

Table 4 shows the memory map of the IDE Host Controller register set.

Table 4: IDE Host Controller Memory Map

Offset Address	Description
0x00 to 0x3C	ATA I/O Registers
0x40 to 0x5D	Configuration and Status Registers
0x1XXX	ATA Data Port

The ATA I/O registers are implemented in the IDE mass storage device. These registers are mapped into the host processor system memory address space from offset 0x00 to 0x3C. The QuickLogic CSSP generates IDE bus cycles to access these registers in the mass storage device.

The IDE Host Controller configuration and status registers are mapped into the processor system memory address space from offset 0x40 to 0x5D.

Register Descriptions

ATA I/O Registers

Communication between the host processor and the QuickLogic CSSP is performed using the ATA I/O registers. The Command Block registers are used for sending commands to the device or posting device status. The Control Block registers are used for controlling the device or posting device status. For a complete description of the ATA I/O registers, refer to the *ATA Specification*.

The ATA I/O registers are accessed using PIO transfers. The signals $\overline{\text{IDE\_CS1}}$, $\overline{\text{IDE\_CS0}}$, and IDE_A[2:0] are mapped into the host processor system memory address space using the CPU address lines [6:2] as shown in **Table 5**.

Table 5: ATA I/O Registers

Host Address	ATA I/O Address					Functions	
	$\overline{\text{IDE\_CS1}}$	$\overline{\text{IDE\_CS0}}$	IDE_A[2]	IDE_A[1]	IDE_A[0]	Read ($\overline{\text{IDE\_IOR}}$)	Write (IDE_IOW)
Command Block Registers							
0x00	1	0	0	0	0	Data	Data
0x04	1	0	0	0	1	Error	Features
0x08	1	0	0	1	0	Sector Count	Sector Count
0x0C	1	0	0	1	1	Sector Number	Sector Number
0x10	1	0	1	0	0	Cylinder Low	Cylinder Low
0x14	1	0	1	0	1	Cylinder High	Cylinder High
0x18	1	0	1	1	0	Device/Head	Device/Head
0x1C	1	0	1	1	1	Status	Command
Control Block Registers							
0x38	0	1	1	1	0	Alternate Status	Device Control
0x3C	0	1	1	1	1	Drive Address	Not Used

Configuration and Status Registers

Name	Address	Size	Type	Description
IDE_CFG	0x40	16	R/W	Configuration Register
IDE_CTL_STAT	0x44	16	R/W	Status Register
IDE_T1	0x50	16	R/W	IDE Timing Register 1
IDE_T2	0x54	16	R/W	IDE Timing Register 2

IDE_CFG - Configuration Register

Address Offset: 0x40
Size: 16-bits
Type: Read/Write
Reset Value: 0x1300

Table 6: Configuration Registers

Name	Bit(s)	Type	Reset Value	Description
REV_ID	15:12	RO	The current revision of the IP	Revision ID
RESERVED	11	RO	0	N/A
CLK_ENB	10	R/W	0	Internal Clock Enable 0 – Internal Clock enabled 1 – Internal Clock disabled
RP_EN	9	RO	1	Read Prefetching Enable 0 – PIO Read Prefetching disabled 1 – PIO Read Prefetching enabled
WP_EN	8	RO	1	Write Posting Enable 0 – PIO Write Posting disabled 1 – PIO Write Posting enabled
RESERVED	7	RO	0	N/A
MODE_SETTING	6:5	R/W	00	Operating Mode 00 – PIO mode 01 – Ultra DMA mode 10 – Multiword DMA mode 11 – reserved
RESERVED	4:3	RO	0	N/A
IDE_RST	2	R/W	0	IDE Reset 0 – IDE Reset de-asserted 1 – IDE Reset asserted
RESERVED	1	RO	0	N/A
IDE_PWR_TG	0	R/W	0	IDE Power Toggle 0 – IDE Power OFF 1 – IDE Power ON **NOTE:** Bit 1 must be set to '1' for Bit 0 to toggle IDE power.

Bit 1	Bit 0	IDE Power
0	X	ON
1	0	ON
1	1	OFF

IDE_CTL_STAT – Control/Status Register

Address Offset: 0x44
Size: 16-bits
Type: Read/Write
Reset Value: 0x0014

Table 7: Control/Status Registers

Name	Bit(s)	Type	Reset Value	Description
RESERVED	15:12	RO	0	N/A
SOFT_RST	11	R/W	0	IDE Host Controller soft reset
DMA_DIR	10	R/W	0	DMA direction bit, self-clearing 0 – UDMA datapath will be through CPU 1 – UDMA datapath will be through USB
WRITE_DMA_START	9	R/W	0	Write DMA start bit, self-clearing
READ_DMA_START	8	R/W	0	Read DMA start bit, self-clearing
RFIFO_THRESHOLD_EN	7	RO	0	Read FIFO threshold interrupt enable
WFIFO_THRESHOLD_EN	6	RO	0	Write FIFO threshold interrupt enable
RESERVED	5	RO	0	N/A
IDE_INT_EN	4	R/W	1	IDE Interrupt Enable 0 – IDE Interrupt disabled 1 – IDE Interrupt enabled
RFIFO_THRESHOLD	3	RO	0	Read FIFO threshold – Read FIFO has at least 512 bytes of data
WFIFO_THRESHOLD	2	RO	1	Write FIFO threshold –Write FIFO has room for at least 512 bytes of data
DMARQ	1	RO	Reflects the value of the IDE DMA request pin.	IDE DMA Request 0 – IDE DMA Request Signal NOT asserted 1 – IDE DMA Request Signal asserted
IDE_INT	0	RO	Reflects the value of the IDE interrupt input pin.	IDE Interrupt 0 – IDE Interrupt NOT asserted 1 – IDE Interrupt asserted

IDE_T1 – IDE Timing Register 1

Address Offset: 0x50
Size: 16-bits
Type: Read/Write
Reset Value: 0x0502

Table 8: IDE Timing Register 1

Name	Bit(s)	Type	Reset Value	Description
RESERVED	15:13	RO	0	N/A
T2	12:8	R/W	00101	$\overline{\text{IDE\_IOR}}$/$\overline{\text{IDE\_IOW}}$ pulse width
RESERVED	7:2	RO	0	N/A
T1	1:0	R/W	10	Address valid to $\overline{\text{IDE\_IOR}}$/$\overline{\text{IDE\_IOW}}$ setup

IDE_T2 – IDE Timing Register 2

Address Offset: 0x54
Size: 16-bits
Type: Read/Write
Reset Value: 0x0458

Table 9: IDE Timing Register 1

Name	Bit(s)	Type	Reset Value	Description
RESERVED	15:11	RO	0	N/A
Teoc	10:8	R/W	100	End of cycle time for PIO/MWDMA modes
RESERVED	7	RO	0	N/A
Tdvs	6:4	R/W	101	Data/CRC valid setup time for UDMA mode
Tcyc	3:0	R/W	1000	Cycle time for UDMA mode

PIO Timing Parameters

This section provides details on programming the PIO Timing registers for the QuickLogic CSSP. **Table 10** lists the PIO timing parameters.

Table 10: PIO Data Port Transfer Timing Parameters

Parameter	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
T0: Cycle time	600	383	240	180	120
T1: Address valid to $\overline{\text{IDE\_IOR}}$/$\overline{\text{IDE\_IOW}}$ setup	70	50	30	30	25
T2: $\overline{\text{IDE\_IOR}}$/$\overline{\text{IDE\_IOW}}$ pulse width	165	125	100	80	70
T4: $\overline{\text{IDE\_IOW}}$ data hold	30	20	15	10	10
Teoc: End of cycle time (T0 – T2)	435	258	140	100	50

For a given system clock frequency, the register values should be programmed based on the minimum number of clock cycles required to meet (or exceed) the timing parameters. The minimum value allowed for each register setting is one.

Example 1: PIO Mode 4; 66 MHz (15 ns period) system clock:

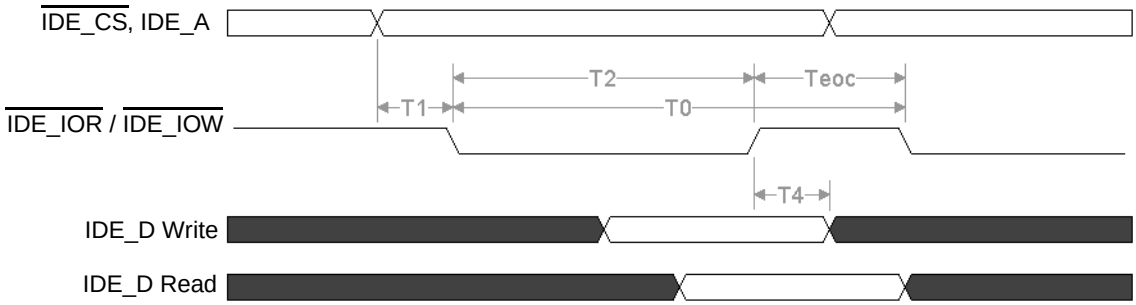
T1 = 25 ns ≤ 2 clock periods (30 ns), therefore T1_REG = 10
T2 = 70 ns ≤ 5 clock periods (75 ns), therefore T2_REG = 00101
Teoc = 50 ns ≤ 4 clock periods (60 ns), therefore Teoc_REG = 100

Example 2: PIO Mode 4; 33 MHz (30 ns period) system clock:

T1 = 25 ns ≤ 1 clock period (30 ns), therefore T1_REG = 01
T2 = 70 ns ≤ 3 clock periods (90 ns), therefore T2_REG = 00011
Teoc = 50 ns ≤ 2 clock periods (60 ns), therefore Teoc_REG = 010

Figure 2 illustrates the PIO timing process.

Figure 2: PIO Timing

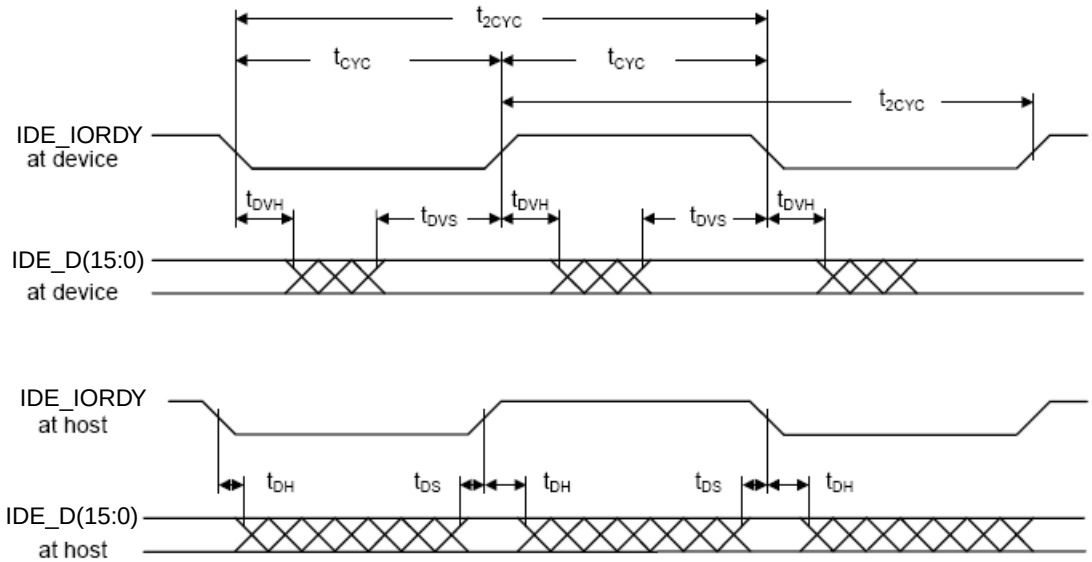


NOTE: The T4 timing value is not register programmable. The IDE Host Controller ensures that T4 is always equal to or greater than 30 ns.

UDMA Timing Parameters

Figure 3 illustrates the sustained UDMA data in burst.

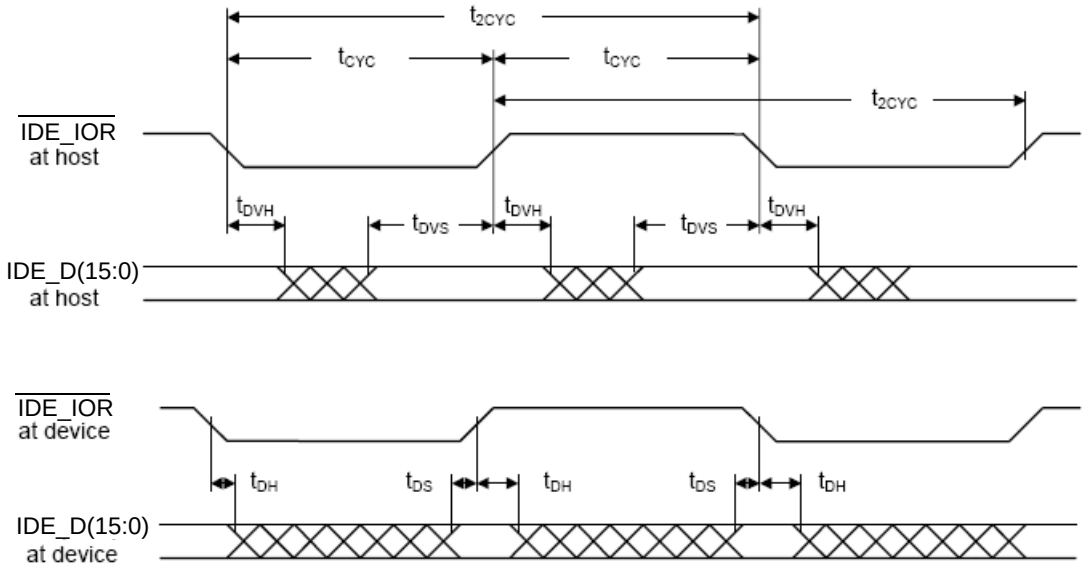
Figure 3: Sustained UDMA Data In Burst



NOTE: IDE_D(15:0) and IDE_IORDY signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 4 illustrates the sustained UDMA data out burst.

Figure 4: Sustained UDMA Data Out Burst



NOTE: IDE_D(15:0) and $\overline{\text{IDE\_IOR}}$ signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

ATA Data Port

The QuickLogic CSSP ATA Data Port is used to read and write data to the externally connected ATA device. **Table 11** provides a description of the ATA Data Port.

Table 11: QuickLogic CSSP ATA Data Port

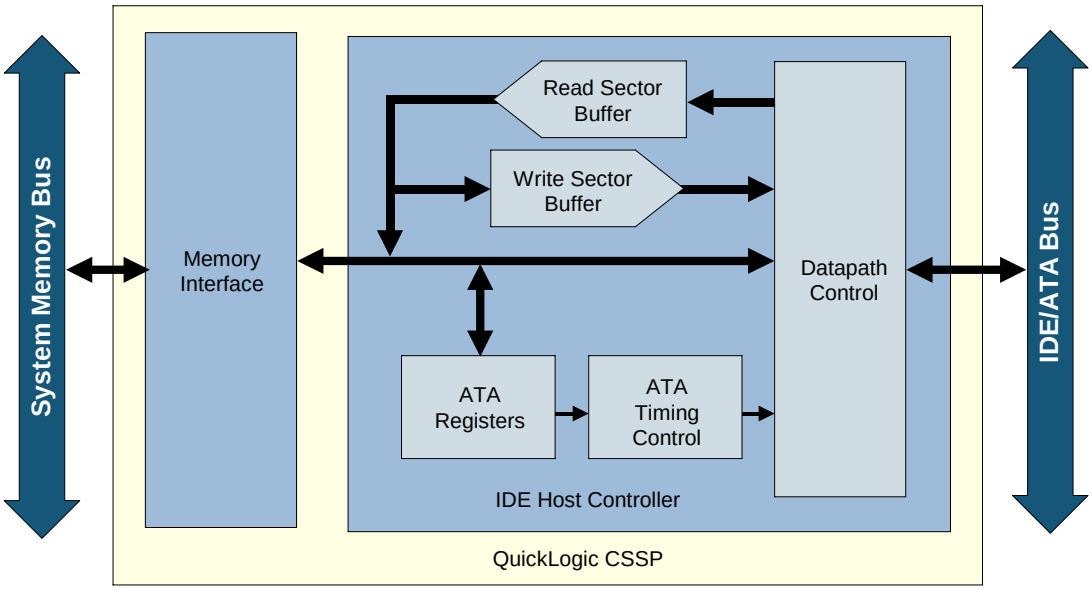
Name	Address	Size	Type	Description
ATA Data Port	0x1XXX	32-bit or 16-bit[a]	R/W	Data Port for all ATA accesses. The Data Port is selected for access whenever the CPU_ADDR[12] is high.

a. See the CPU_DBW bit in the Configuration Register.

Functional and Module Description

The IDE Host Controller implements connectivity for HDD or DVD ROM to the processor, and consists of the following functional blocks as shown in **Figure 5**.

Figure 5: IDE Host Controller Block Diagram



Memory Interface

The Memory Interface communicates to the System Memory Bus. It is responsible for decoding the local address of the transfer, and steering the transaction to the CSSP registers, or the IDE interface. All local bus byte lanes are assumed to be enabled at all times.

The processor can access the hard-drive via this module. Depending on the decoded local address, this module will activate the IDE interface or internal registers to complete the transaction.

IDE/ATA Interface

PIO Transfers: The QuickLogic CSSP can perform transfers to IDE peripherals in any of the PIO modes (0 through 4). Access timing is controlled by the settings programmed into the Bridge's PIO Timing registers. The settings used depend on the system clock frequency.

PIO Read Prefetching: The QuickLogic CSSP read prefetching capability enables IDE data port read accesses to be performed back to back to increase the PIO data transfer rates. The read prefetching buffer can hold up to 512 bytes of data. Data prefetching is initiated when an IDE data port read occurs. The first data port read of an IDE device sector is called the *demand read*. Subsequent data port reads from the same sector are called *prefetch reads*.

PIO Write Posting: The QuickLogic CSSP write posting capability allows the write transactions to complete on the system memory bus immediately after the data is received by the controller. The QuickLogic CSSP will then perform the IDE PIO write transfer to the IDE data port. The write posting buffer can hold up to 512 bytes of data.

Multiword DMA Mode: The QuickLogic CSSP supports Multiword DMA Mode 0 to Mode 2 with maximum Multiword DMA Mode 2 performance up to 16.7 Mbytes/sec. (excluding OS overhead). Greater than 10 Mbytes/sec. transfer rate measured under WinCE 5.0.

Ultra DMA Mode: The QuickLogic CSSP supports Ultra DMA Mode 0 to Mode 4 with maximum UDMA Mode 4 performance up to 66 Mbytes/sec.

ATA Registers

The ATA Registers block has several registers used for setting the controller mode, indicating the state machine status, and setting the PIO mode timings related to the chosen input clock frequency.

ATA Timing Control

The ATA Timing Control is used to control any device supporting PIO modes 0 through 4. The PIO mode timing is determined from the PIO mode timing registers. All timing is based on the frequency of the input clock.

Sector Buffers

The IDE Host Controller includes two sector buffers, each of which can hold 512 bytes of information for read and write. The buffers can also be configured in bypass mode.

Datapath Control

The datapath control module manages the ATA signal I/O pins and supports multi-word DMA (MWDMA) operation.

Supported Operating Systems

The IDE Host Controller PSB supports the following operating systems:

- Windows® CE
- Windows Mobile®
- Linux®

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Revision History

Revision	Date	Originator and Comments
A	July 2008	First release.

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