Reconfigurable Systems

Jorge Semião

Instituto Superior de Engenharia

www.ualg.pt

Final Project

- The purpose of this project is to define several blocks/entities in VHDL and design controllers for each blocks
- Send encrypted data with UART, receive and decrypt
- Reuse the already developed blocks
- Implement 2 big entities: one for the sender and the other for the receiver

Final Project (cont.)

- Objective 1: Create one test bench to simulate both entities in modelsim, and simulate the all system.

- Objective 2: Implement both entities in an FPGA board, connecting externally both entities with a wire in the FPGA board, and observe the output in an oscilloscope by using a DAC (Digital to Analog Converter) in the lab to convert the digital word to an analog signal (you can use an Arduino or a DAC converter).

Final Project – block digram