Reconfigurable Systems

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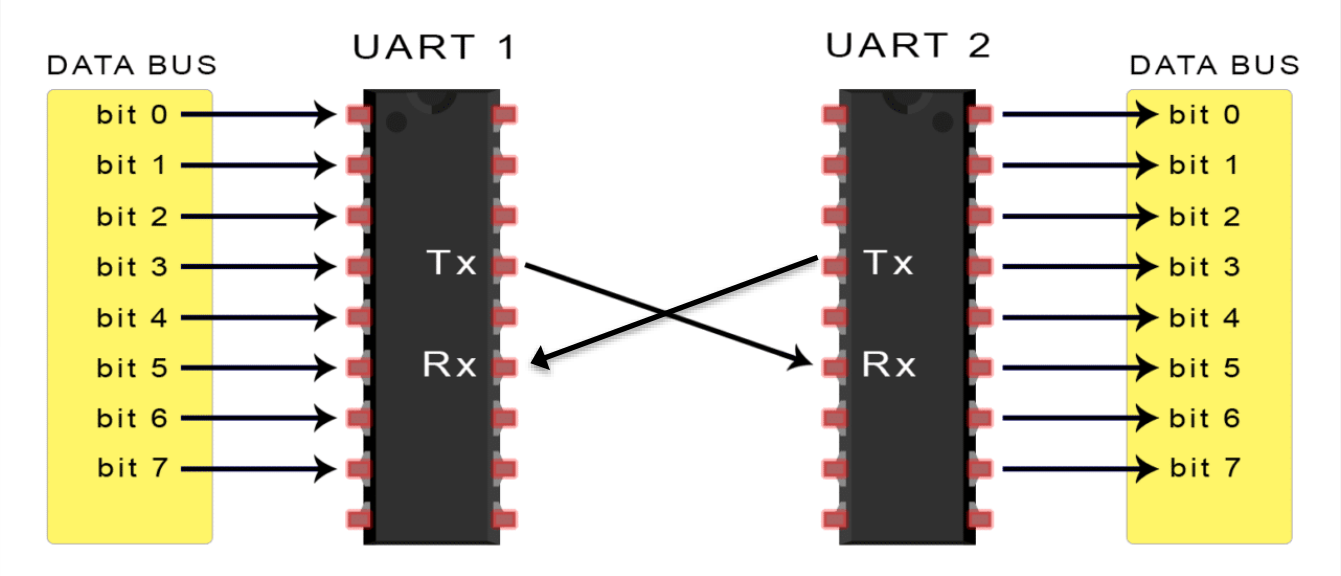
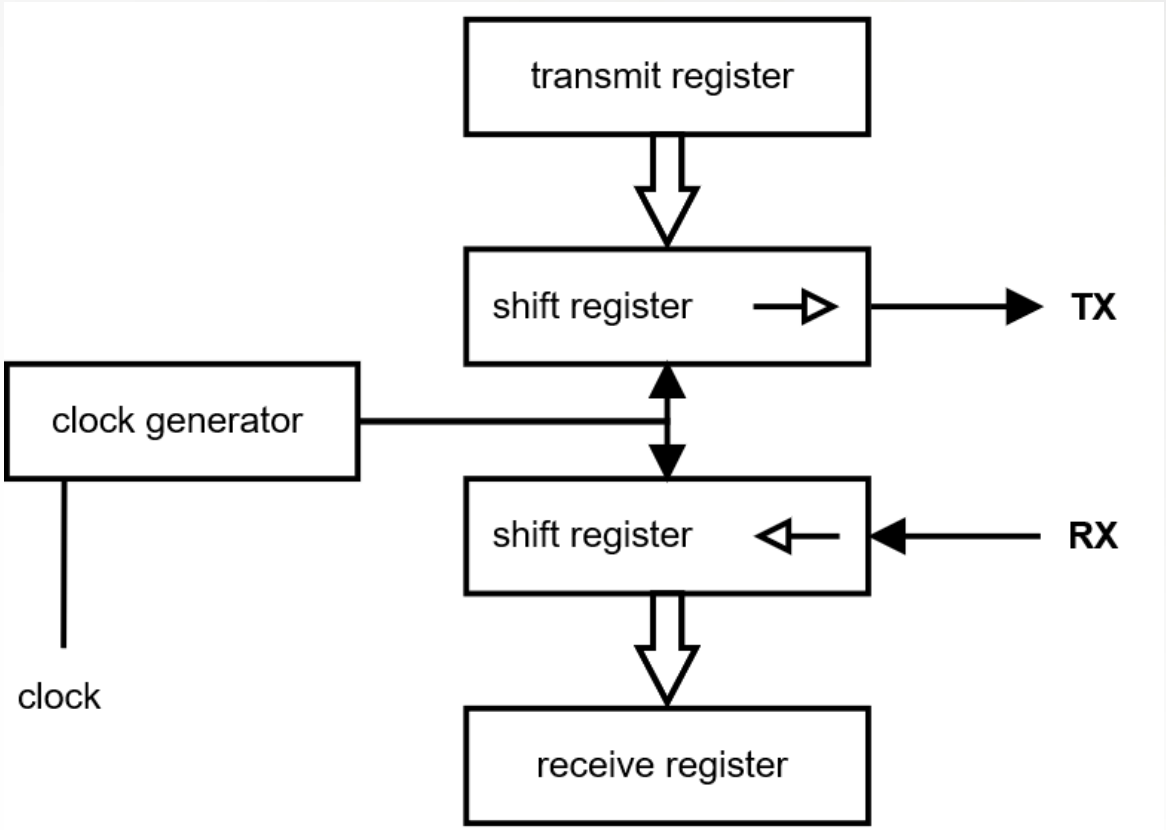
Assignment 4

- Implement an UART entity in VHDL
- Use different processes for receiver and transmitter
- Use an 8x faster clock for sampling (optional)
- Simulate in ModelSim each functionality (receiver and transmitter)
- For simplicity, the clock synthesizer is optional

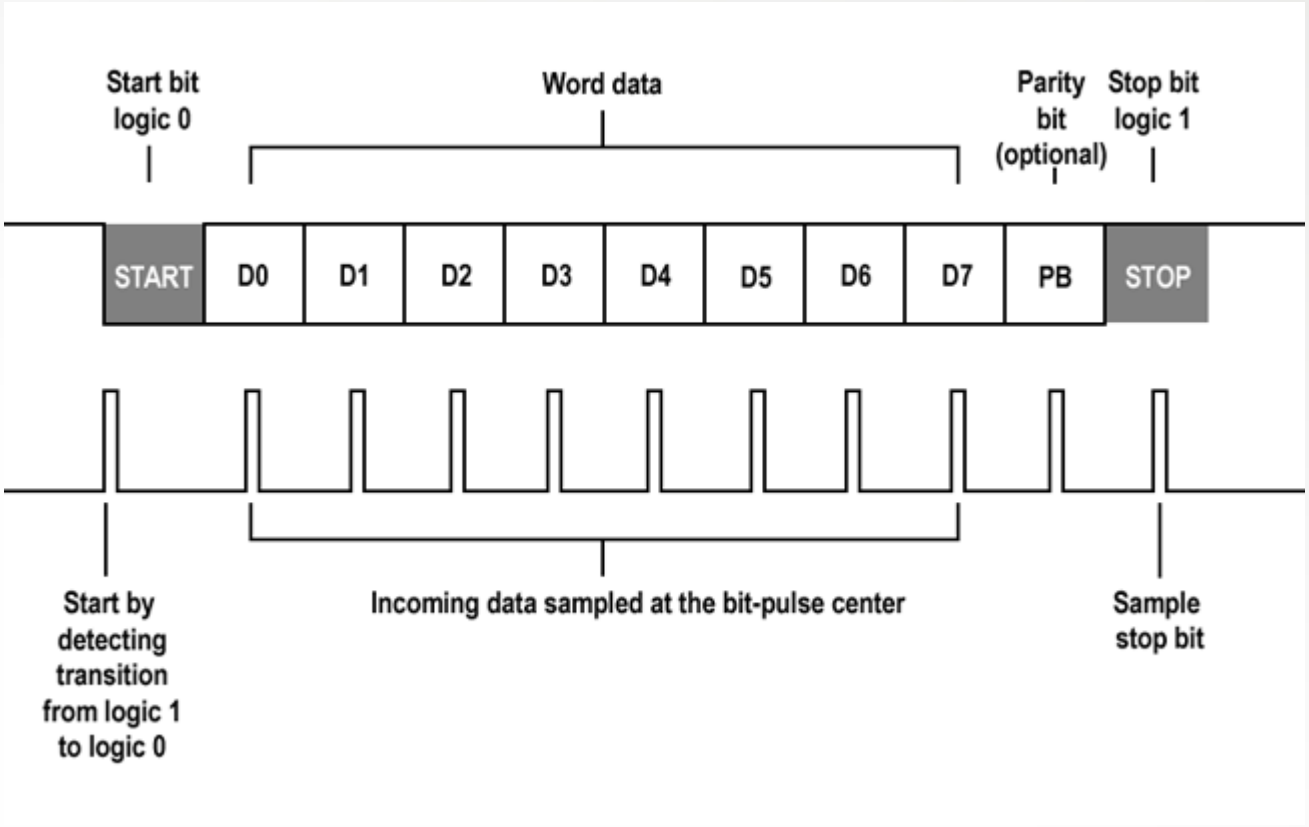
UART
universal asynchronous receiver-transmitter



UART
universal asynchronous receiver-transmitter



UART
universal asynchronous receiver-transmitter



UART

universal asynchronous receiver-transmitter