Reconfigurable Systems

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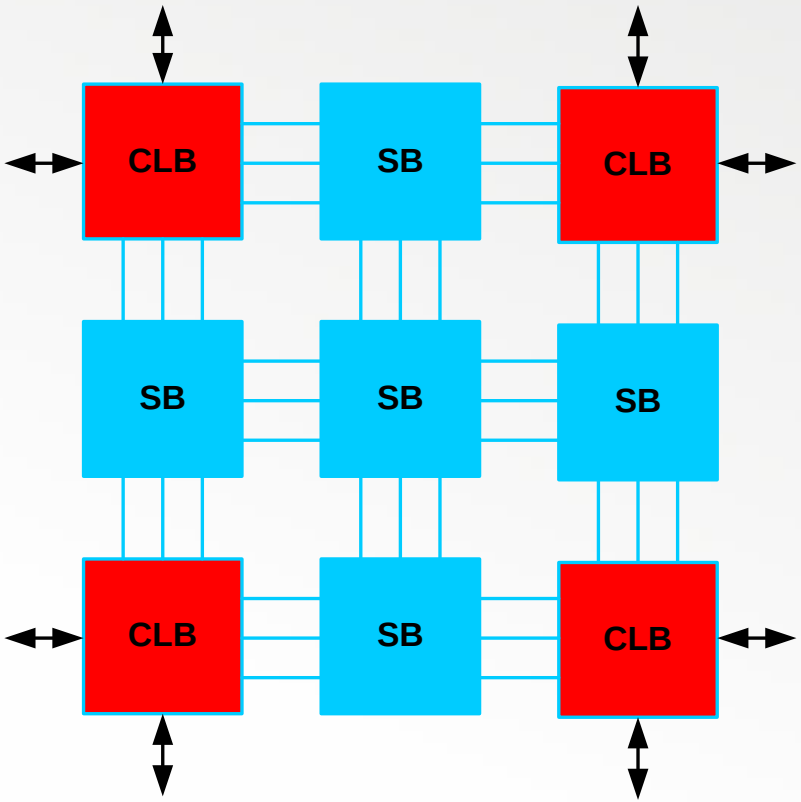
FPGA Principles

- A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be configured by the user to emulate any digital circuit as long as there are enough resources
- An FPGA can be seen as an array of Configurable Logic Blocks (CLBs) connected through programmable interconnect (Switch Boxes)

FPGA structure

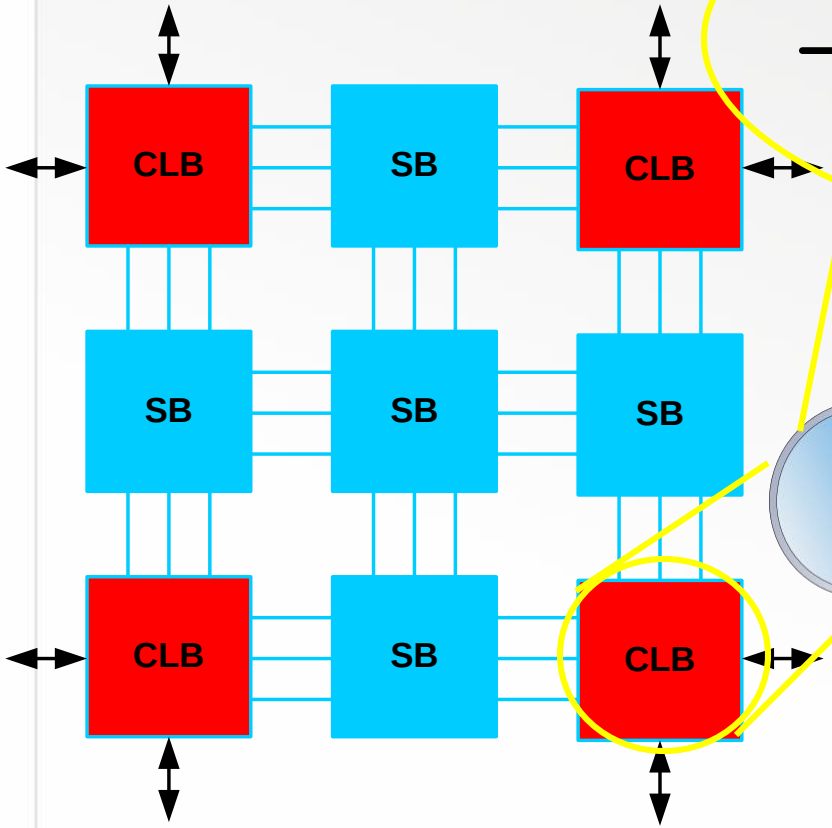


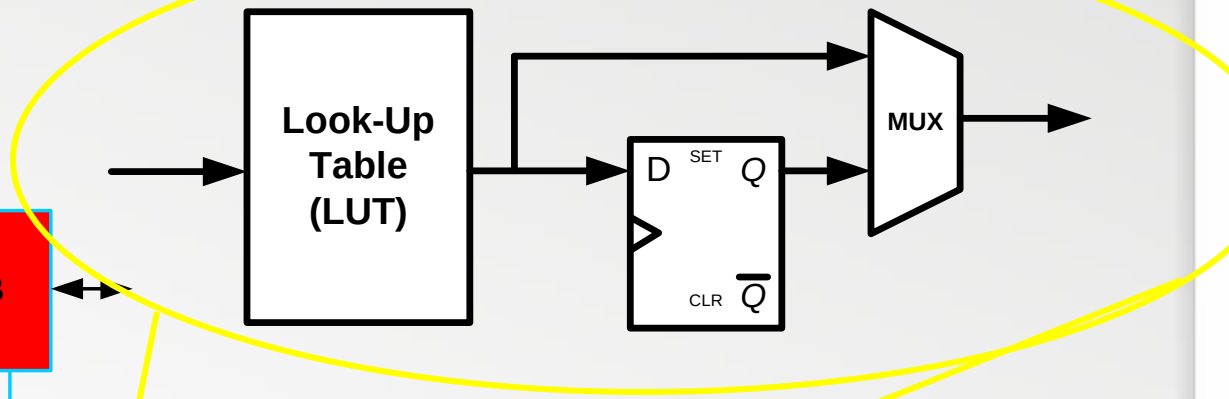
Configurable Logic Blocks

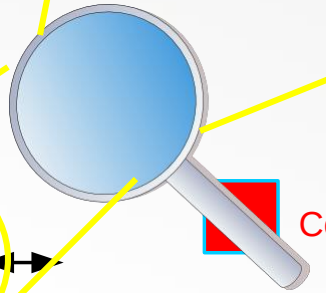
Interconnection Network

I/O Signals (Pins)

Simplified CLB Structure





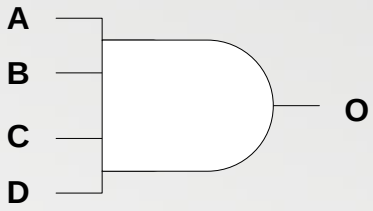


Configurable Logic Blocks

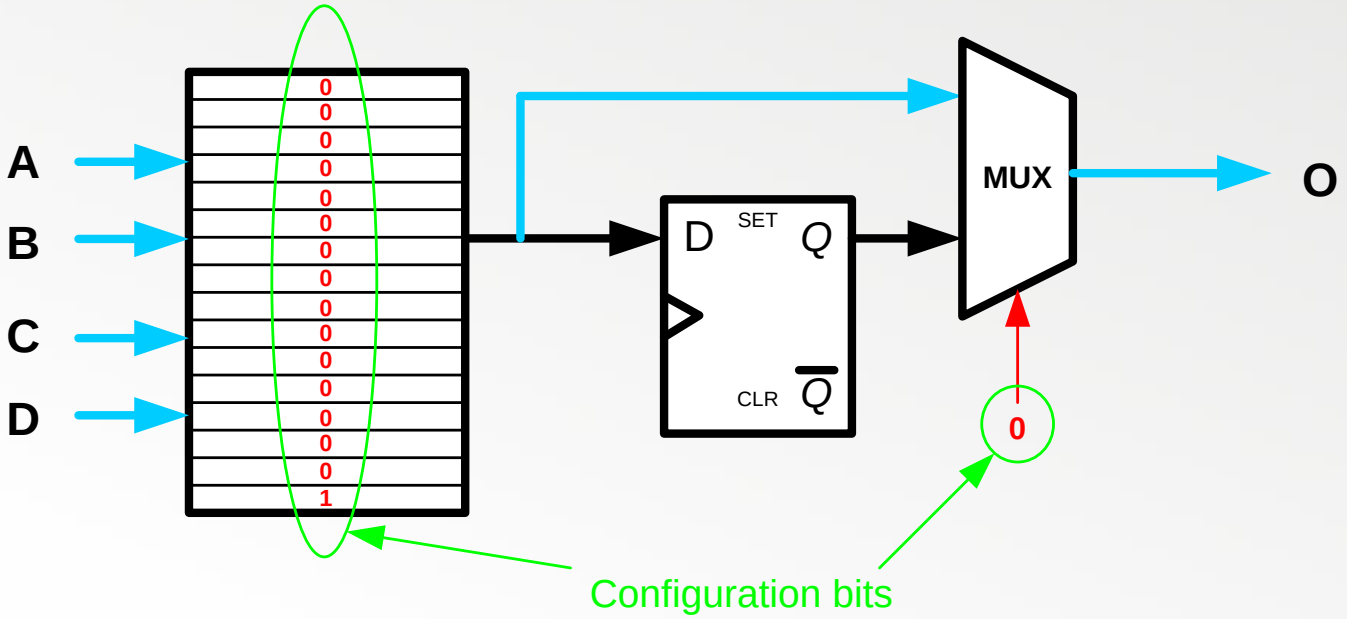
Interconnection Network

I/O Signals (Pins)

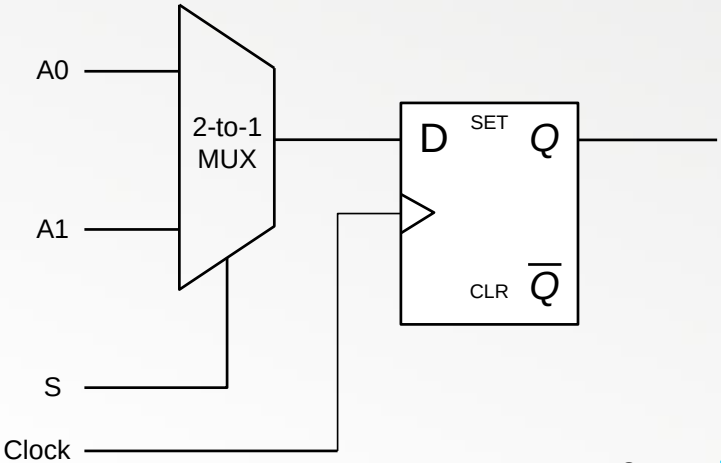
Example: 4-input AND gate



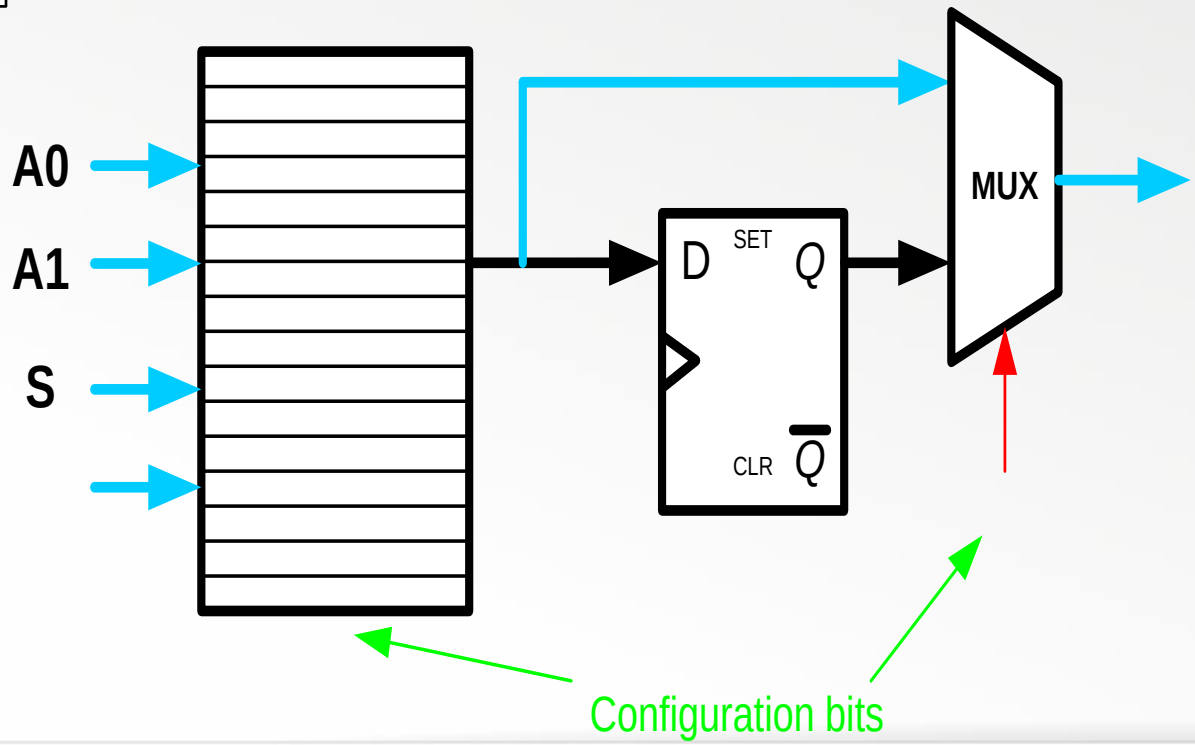
A	B	C	D	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



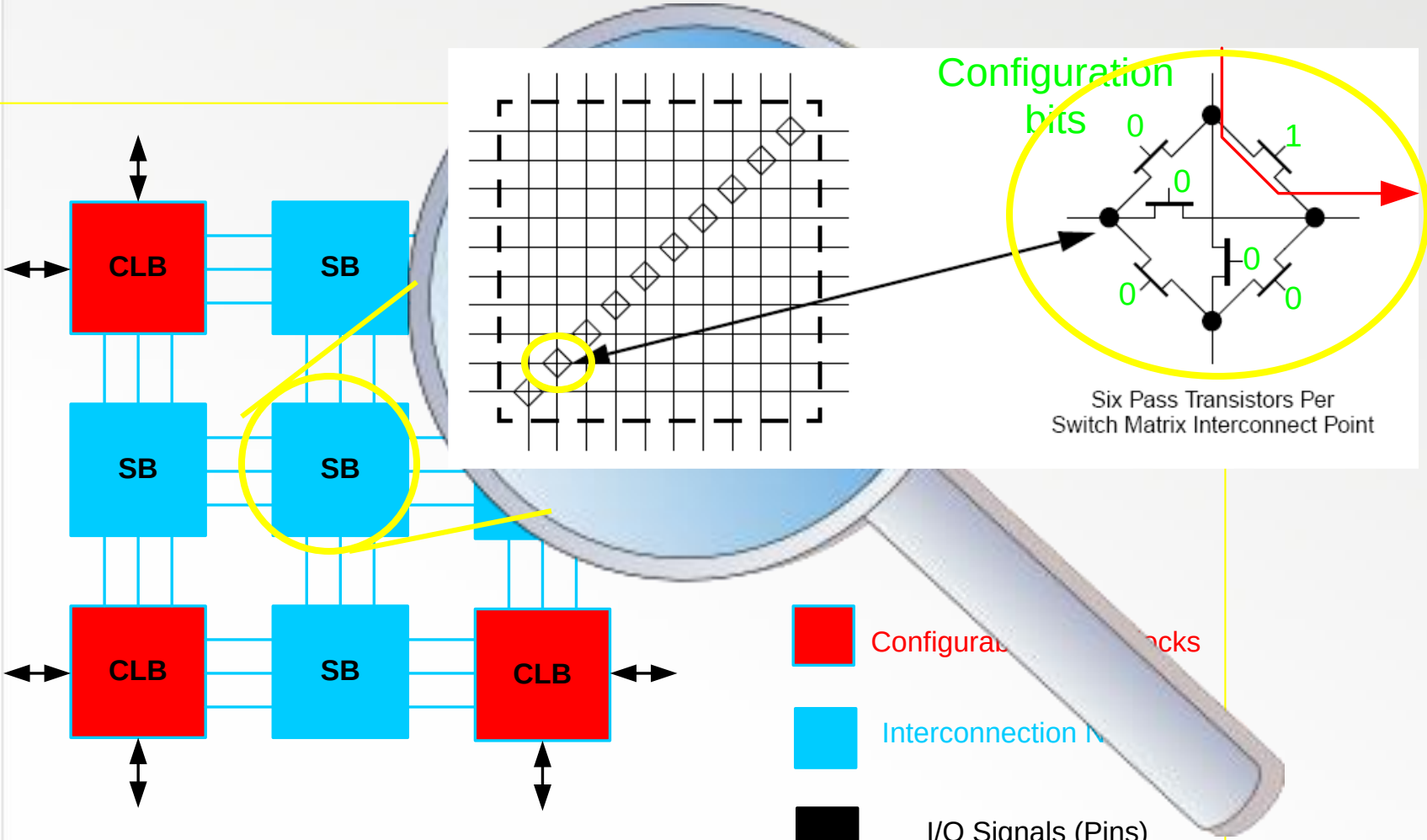
Example 2: Find the configuration bits for the following circuit



A0	A1	S	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

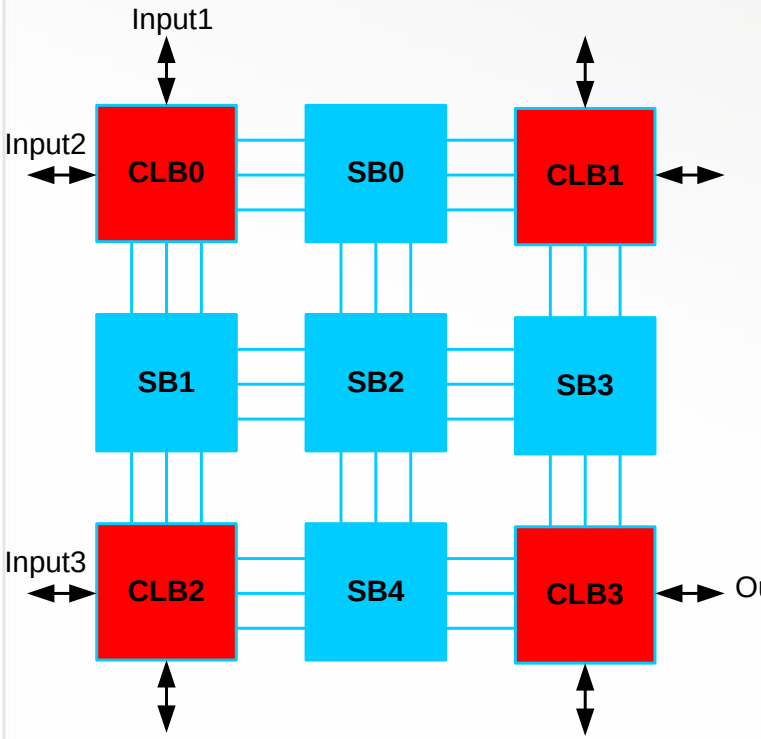


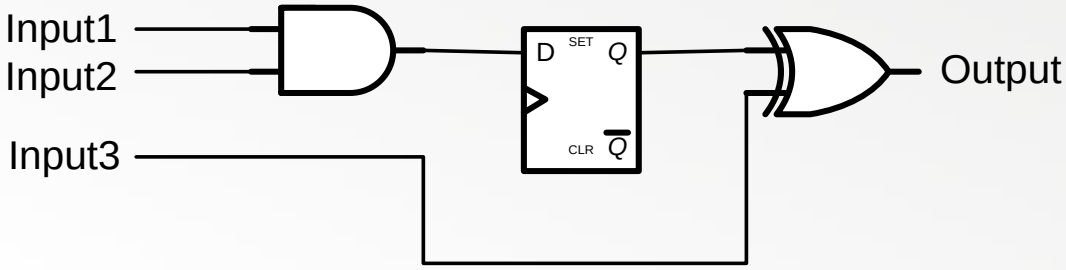
Interconnection Network



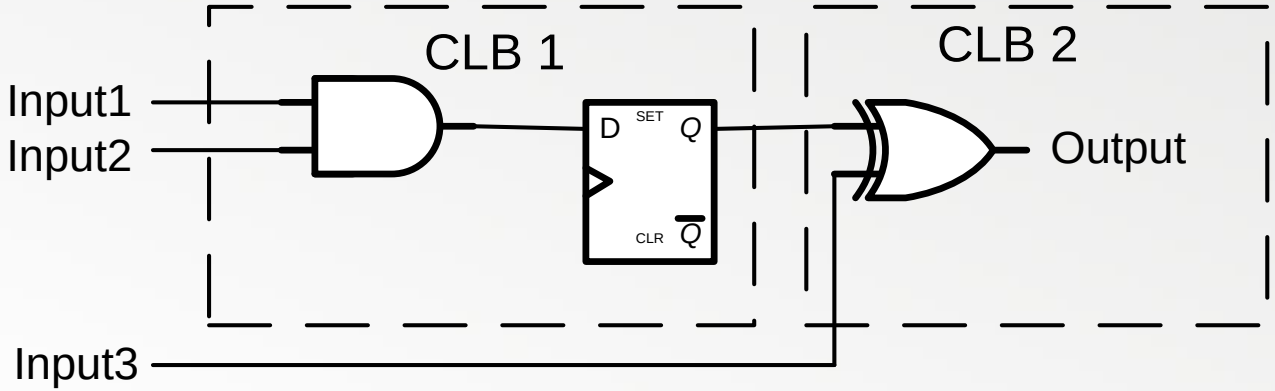
Example 3

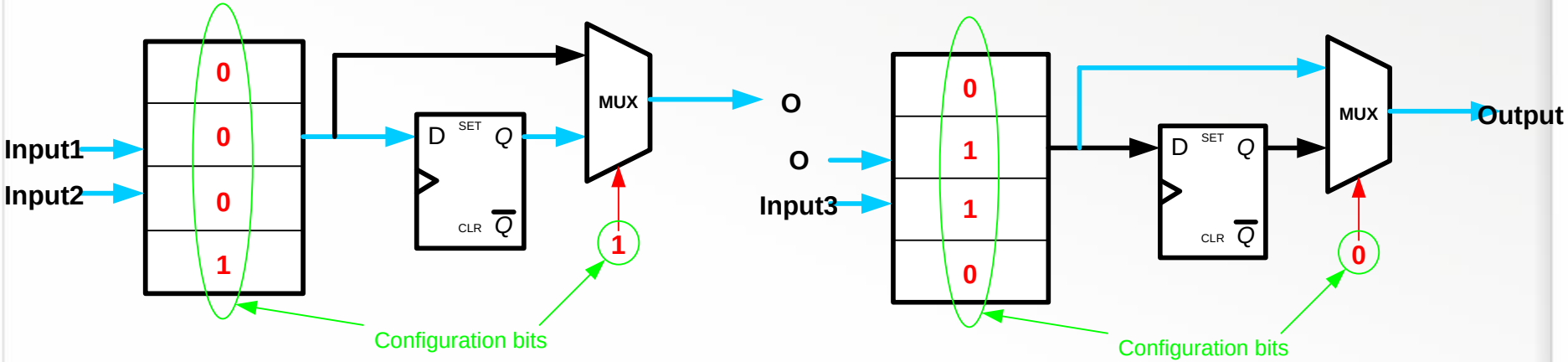
- Determine the configuration bits for the following circuit implementation in a 2x2 FPGA, with I/O constraints as shown in the following figure. Assume 2-input LUTs in each CLB.



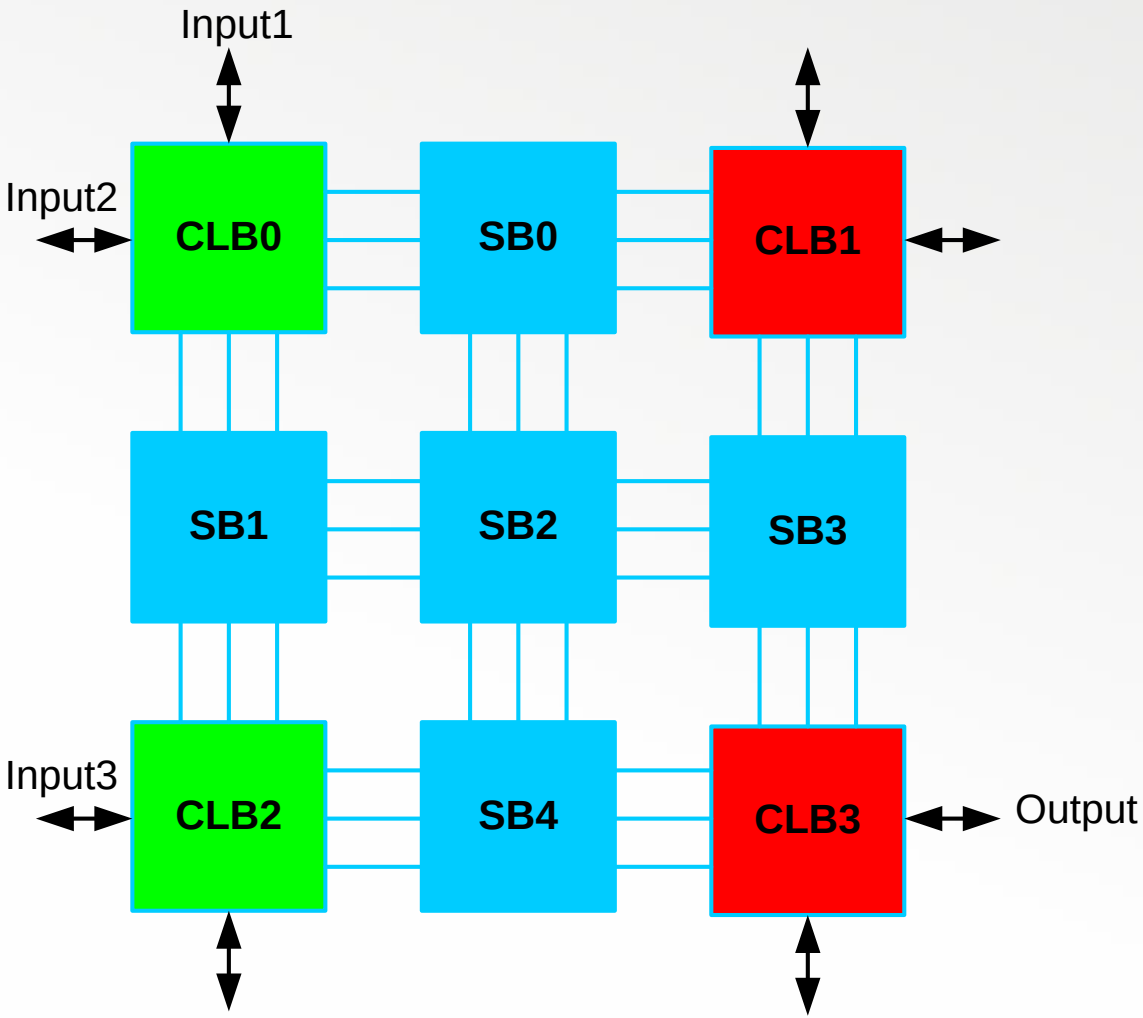


CLBs required

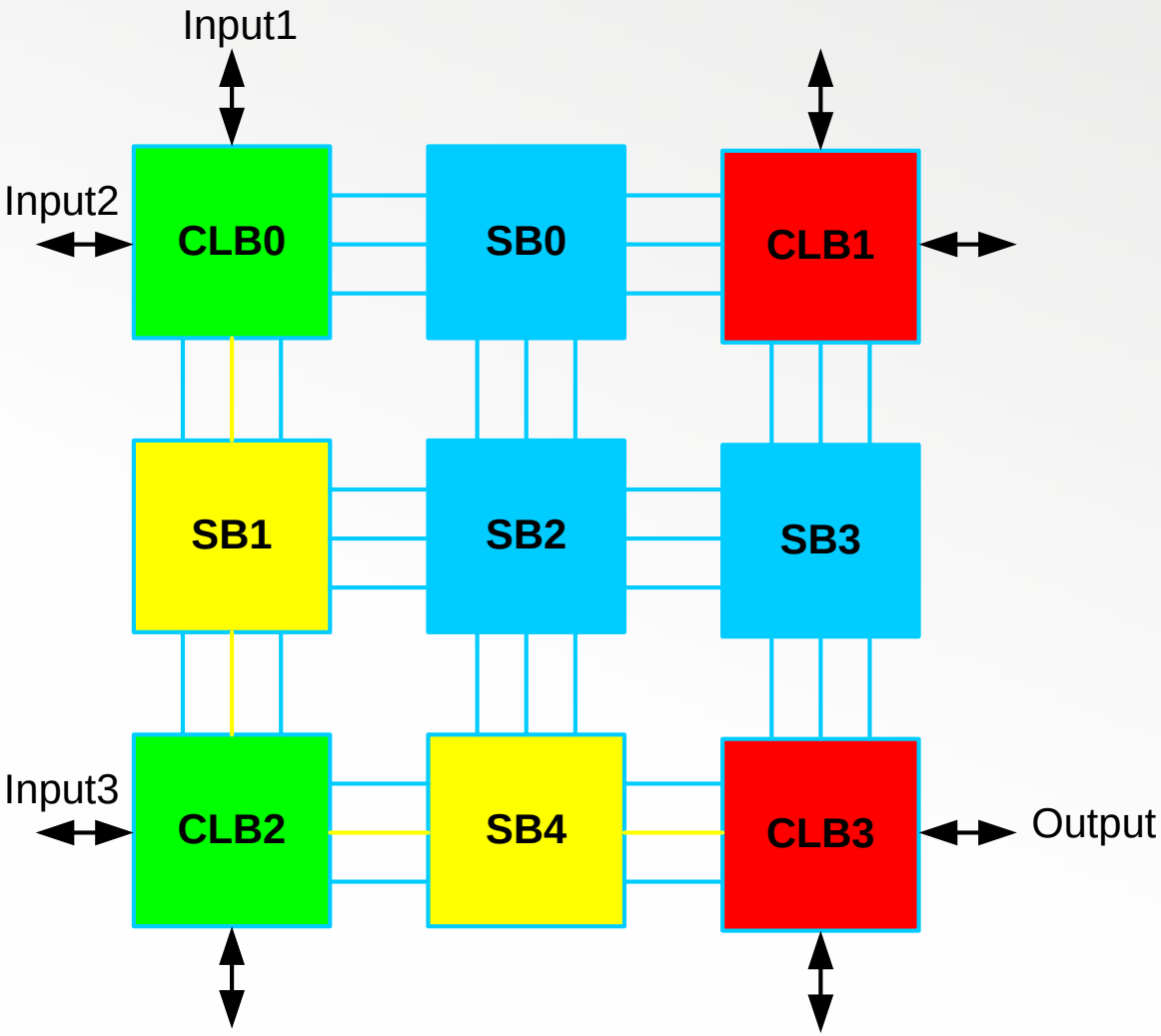




Placement: Select CLBs

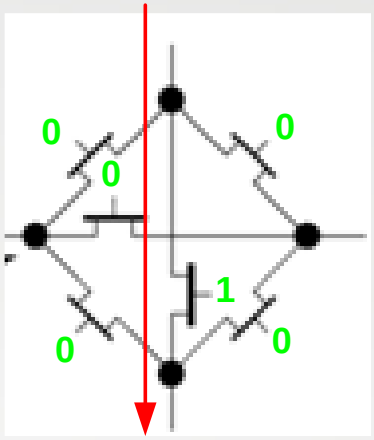


Routing: Select path



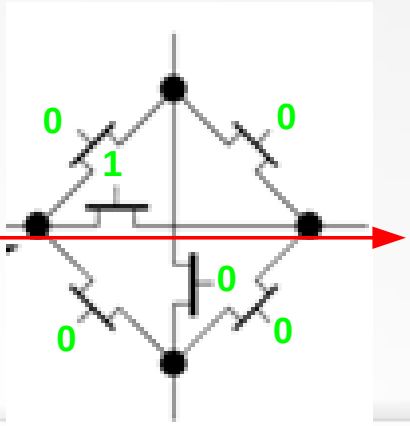
SB1

Configuration bits



SB4

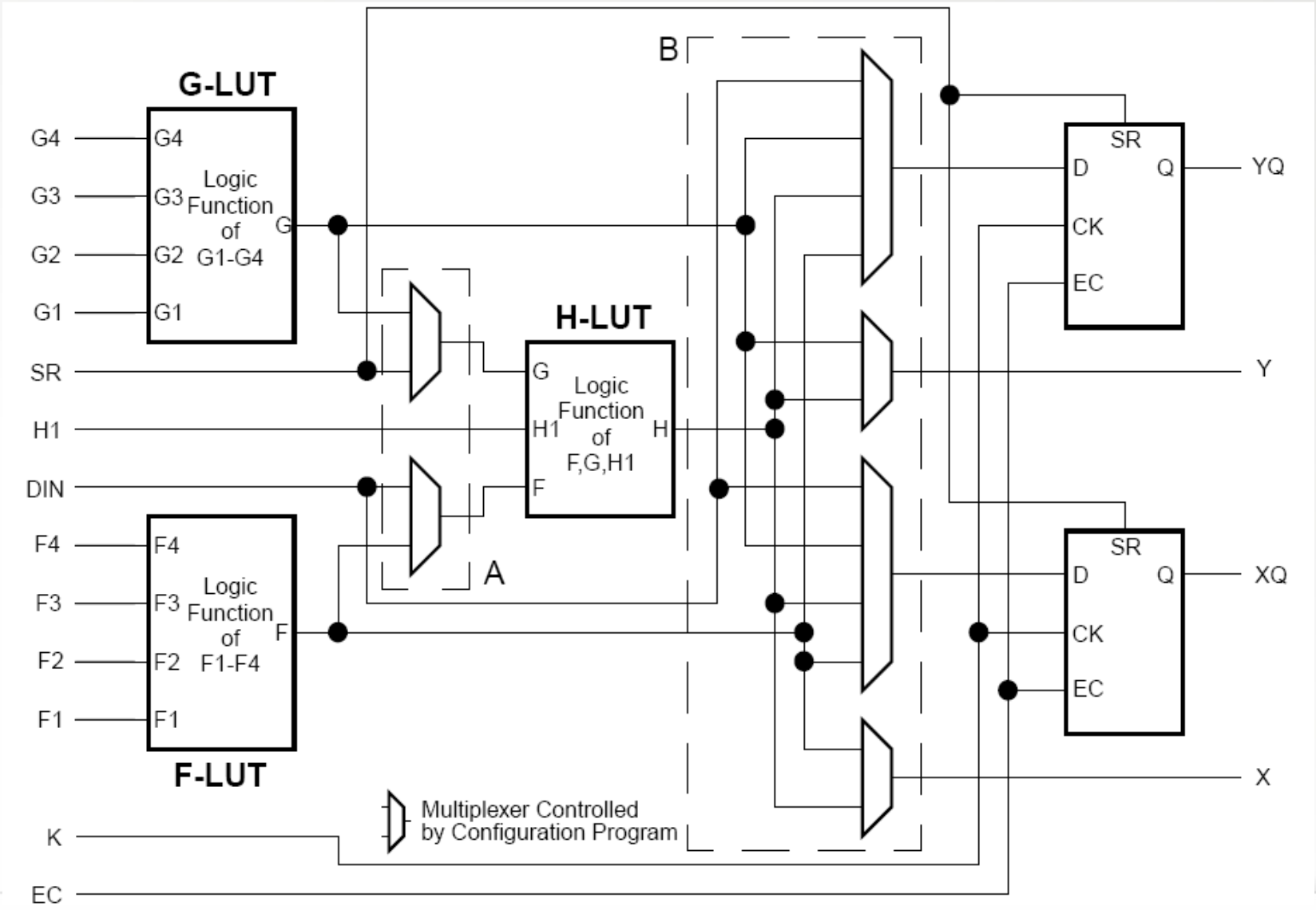
Configuration bits



Configuration Bitstream

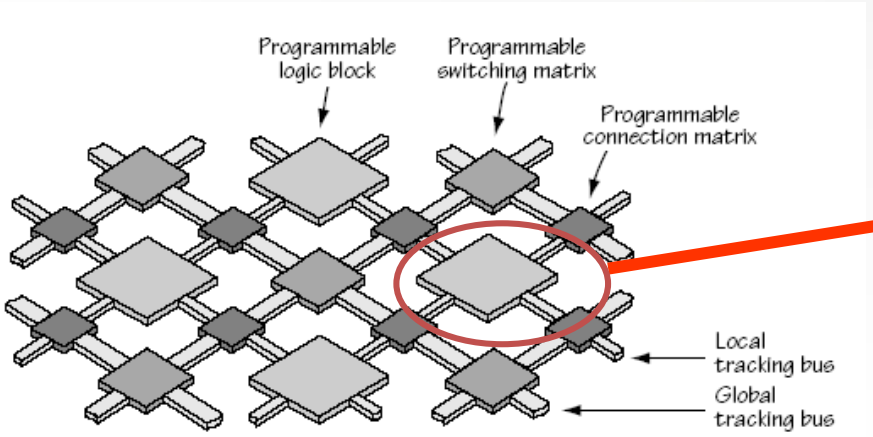
- The configuration bitstream must include ALL CLBs and SBs, even unused ones
- CLB0: 00011
- CLB1: 01100
- CLB2: XXXXX
- CLB3: ?????
- SB0: 000000
- SB1: 000010
- SB2: 000000
- SB3: 000000
- SB4: 000001

Realistic FPGA CLB: Xilinx

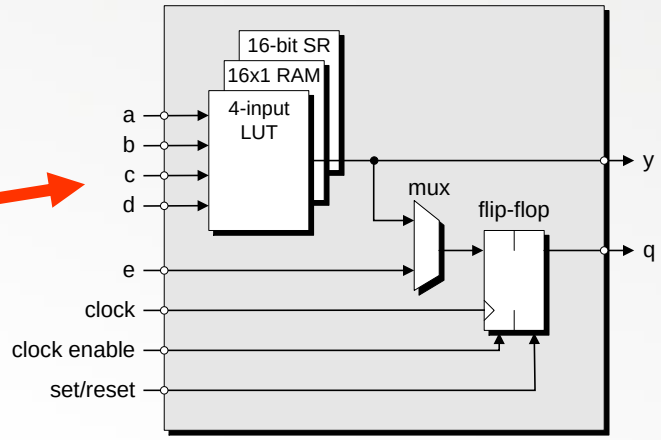


Logic Blocks

- Logic Functions implemented in Look Up Table LUTs.
- Flip-Flops. Registers. Clocked Storage elements.
- Multiplexers (select 1 of N inputs)



FPGA Fabric



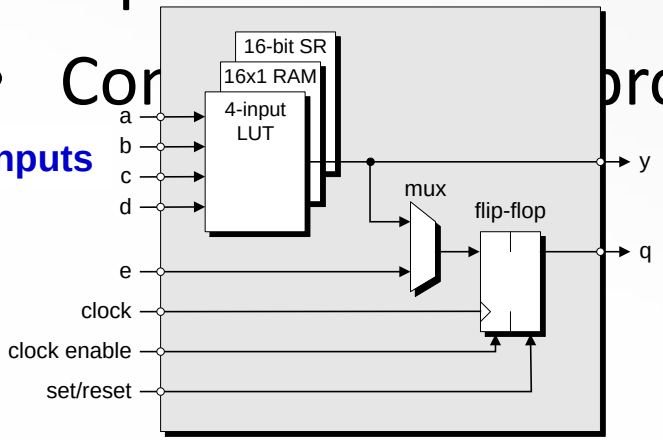
Logic Block

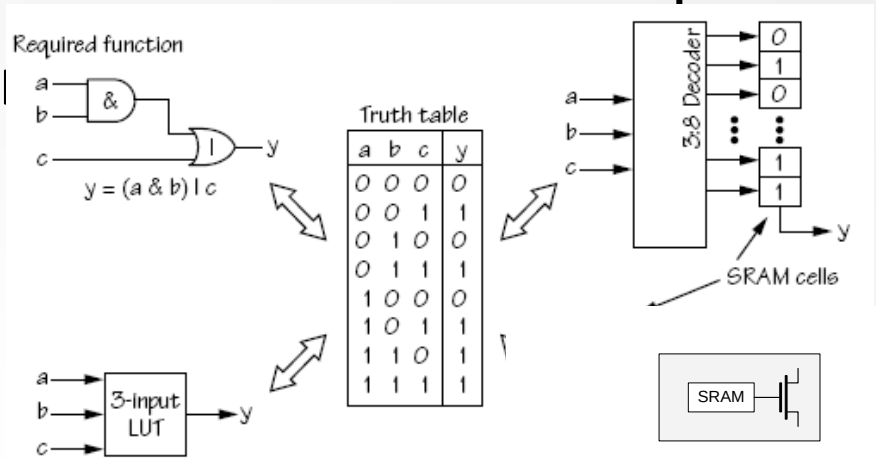
Look Up Tables LUTs

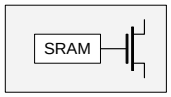
- LUT contains Memory Cells to implement small logic functions
- Each cell holds ‘0’ or ‘1’ .
- Programmed with outputs of Truth Table
- Inputs select content of one [illegible] output
- Cor[illegible]progra[illegible]

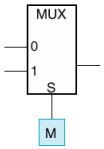
3 Inputs LUT -> 8 Memory Cells

3 – 6 Inputs







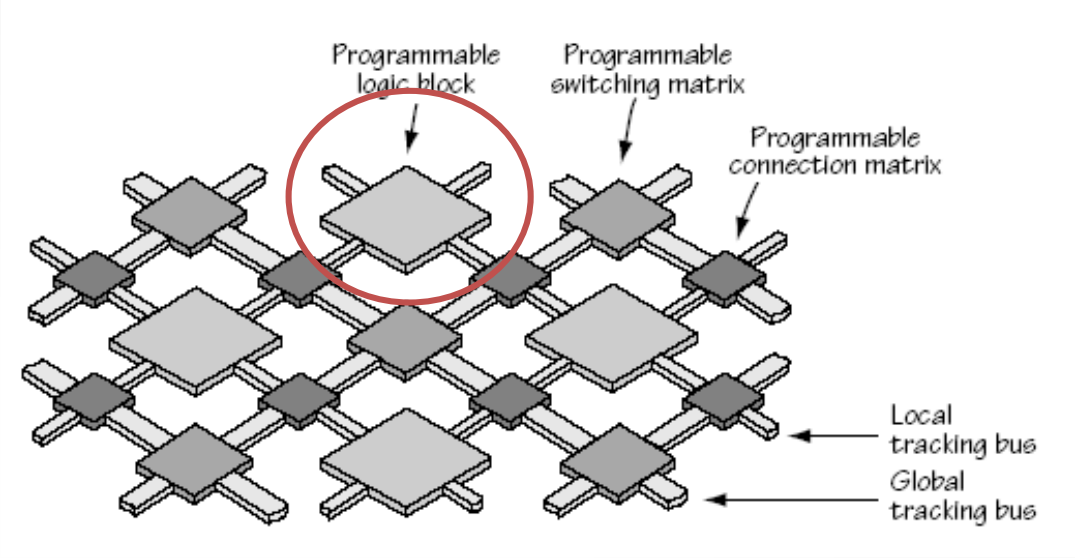


Multiplexer MUX

Static Random Access Memory
SRAM cells

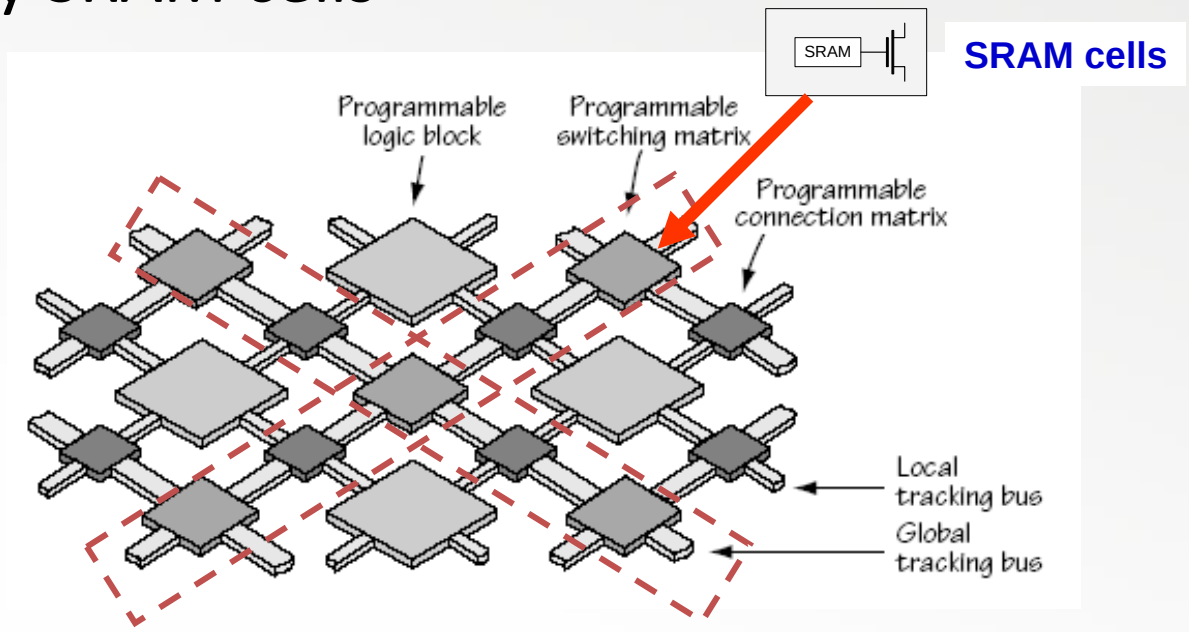
Logic Blocks

- Larger Logic Functions built up by connecting many Logic Blocks together



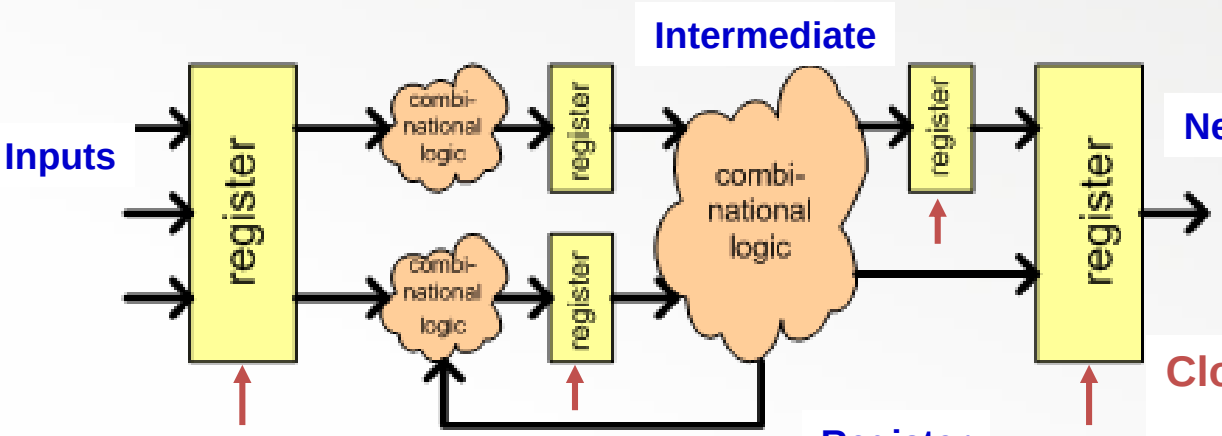
Logic Blocks

- Larger Logic Functions built up by connecting many Logic Blocks together
- Determined by SRAM cells



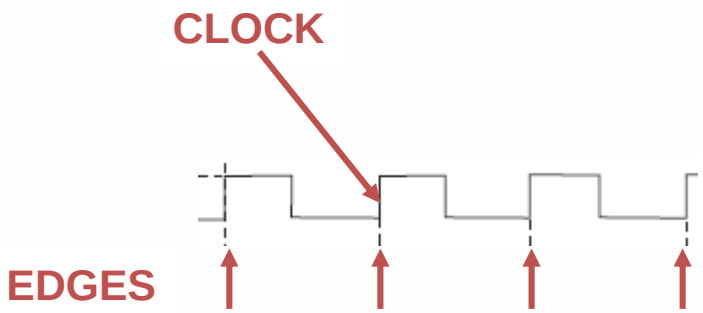
Sequential Circuits

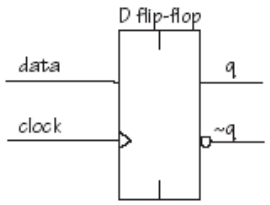
- Combinational Logic (Larger circuits difficult to predict)
- Synchronous Logic driven by a CLOCK
- Registers, Flip Flops (Memory)



Clock Rate determines speed

Comb Logic Must meet Timing
=> Predictable circuits



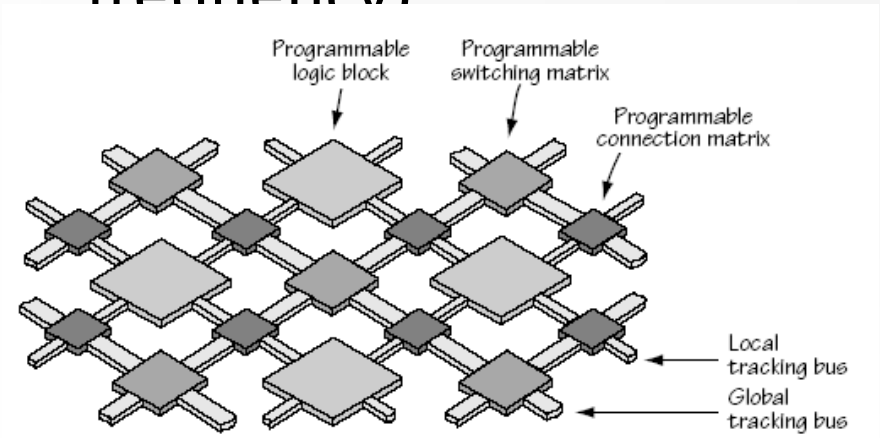


Register

Shift Registers,
Pipelines,
Finite State Machines

Clocked Logic

- Registers on outputs. CLOCKED storage elements.
- Synchronous FPGA Logic Design, Pipelined Logic.
- FPGA Fabric Pulse from Global Clock (e.g. LHC BX frequency)



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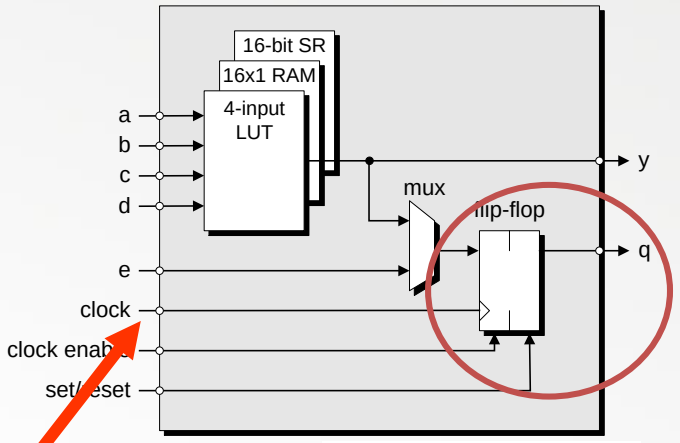
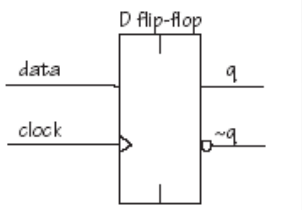




Special Routing for Clocks

Clock from Outside world (eg LHC bunch frequency)

Field Programmable Gate Arrays - FPGA

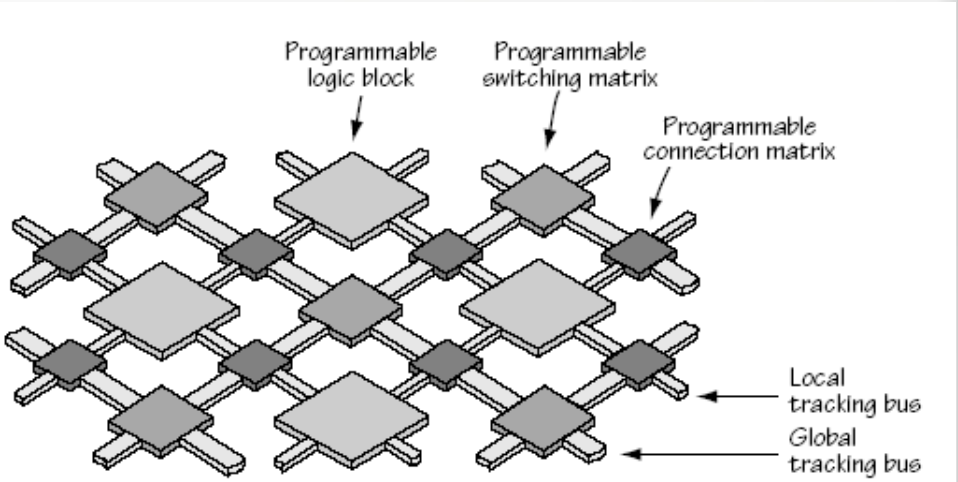
- Field Programmable Gate Array
  - 'Simple' Programmable Logic Blocks
  - Massive Fabric of Programmable Interconnects
  - Standard CMOS Integrated Circuit fabrication process as for SRAM memory chips (Moore's Law)
  - "Hard blocks" for complex high speed fu

Huge Density of Logic Bloc

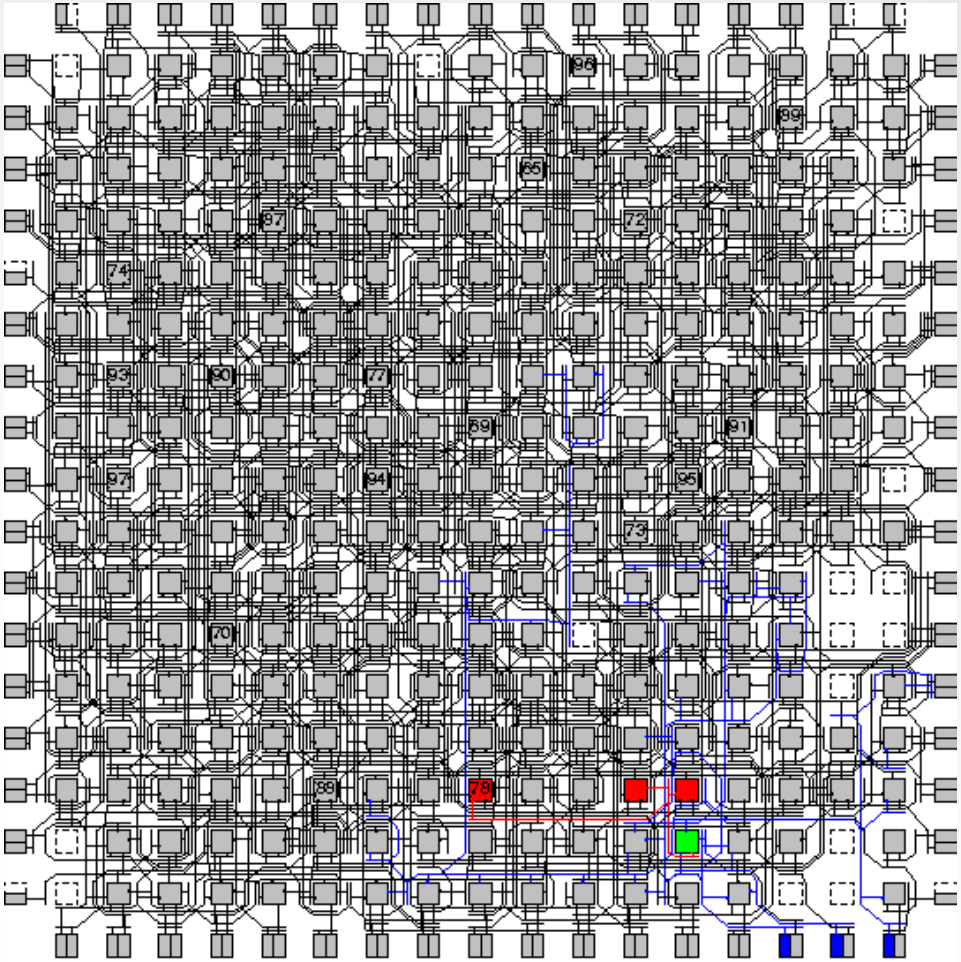
1,000 … 100,000's

in a 'Sea' of Interconnects

FPGA Architecture



Field Programmable Gate Arrays - FPGA



Routing succeeded with a channel width factor of 7.

FPGA EDA Tools

- Must provide a design environment based on digital design concepts and components (gates, flip-flops, MUXs, etc.)
- Must hide the complexities of placement, routing and bitstream generation from the user. Manual placement, routing and bitstream generation is infeasible for practical FPGA array sizes and circuit complexities.