Reconfigurable Computing

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Assignment 1

- Implement in VHDL a sequence detector
- Inputs will be the Clock, Reset and Sequence_In, all digital signals; Outputs will be only one, the Sequence_Detection digital signal
- Use a Finite-State-Machine (FSM) to implement the Architecture part of the system
- When a sequence of “100101” is entered in the input Sequence_in signal, the output should be activated during one clock, otherwise output should be zero

Assignment 1

- Clock is always running and analyzing inputs
- Inputs are always arriving at the speed of the clock
- The FSM should be a Moore FSM type (the output changes only when state changes)
- The work in the assignment should begin with the state diagram for the FSM, specifying the number of states, the sequence according with the input, and the output of each state.

Example of a State Diagram for sequence "1001"