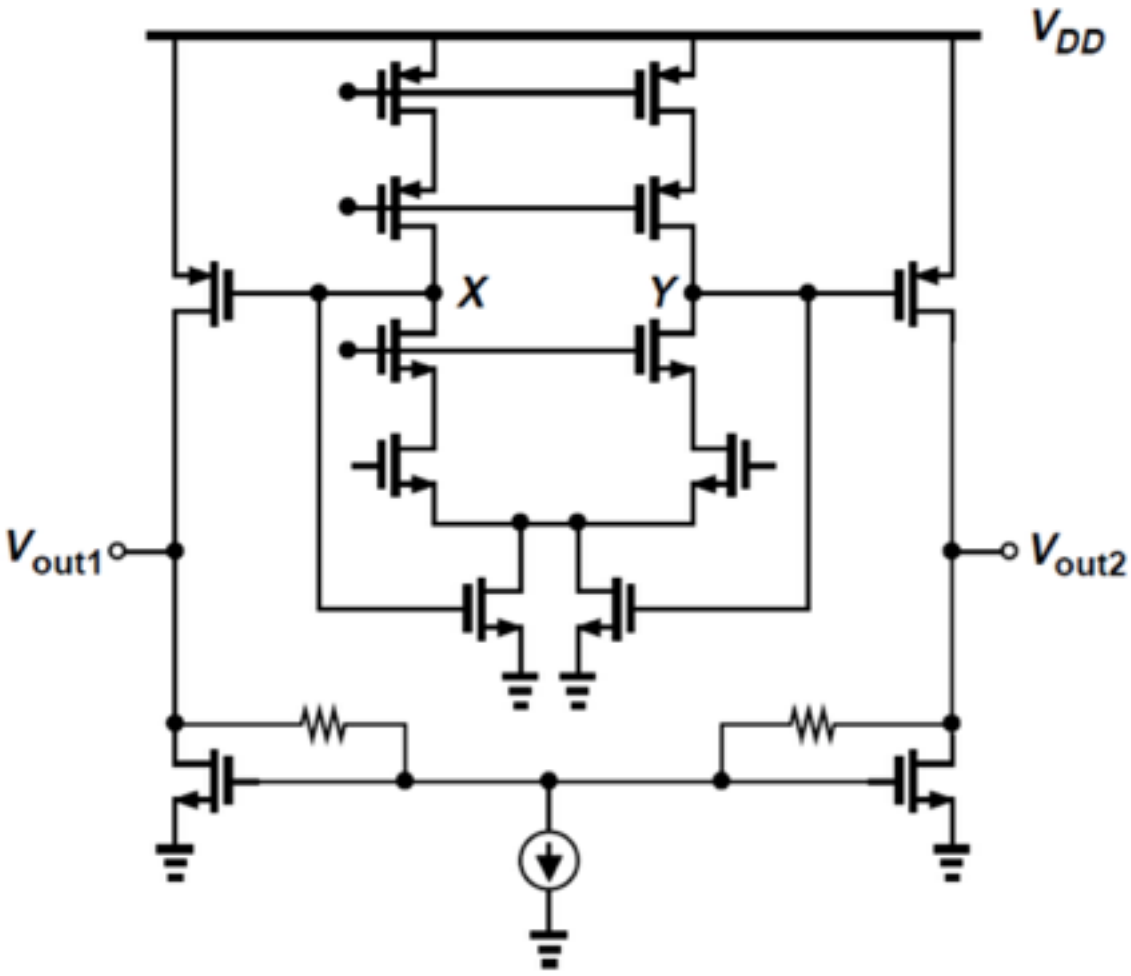
AIC final report

學號：b03901022
系級：　　電機三
姓名：　　卓伯鴻

1. Common-feedback Circuit & Design Procedure:

(1) 共模回授電路(Common-feedback Circuit):
電路設計圖如下：



我使用的共模回授(Common-mode Feedback)方式是採取將第一級(first-stage)的共模輸出(common-mode output)去回授給第一級的偏壓(bias voltage)，也就是上圖中，操控第一級最下兩個電晶體的閘極電壓(gate voltage)的電路形式。再者，第二級的回授則是使用了兩個電阻(resistor)，使得到其平均值作為第二級最下兩個電晶體自身的偏壓(bias voltage)。

(2) 設計理念(Design Procedure):
spice電路設計圖如下：

```
**opamp.sp
.subckt opamp VDD GND Vb1 Vb2 Vb3 Vcm Vin Vip Von Vop
*params
.param M12 = 0.51
.param M34 = 5.75
.param M56 = 6
.param M78 = 4.8
.param M90 = 35
.param Mab = 6.25
.param Mcd = 1.5

.param W_I = 1.2u
.param L_I = 0.9u

*stage 1
M7  1   Vb3 VDD VDD P_18 W= W_I L= L_I M= M78
M8  2   Vb3 VDD VDD P_18 W= W_I L= L_I M= M78
M5  5   Vb2 1   1   P_18 W= W_I L= L_I M= M56
M6  6   Vb2 2   2   P_18 W= W_I L= L_I M= M56
M3  5   Vb1 3   3   N_18 W= W_I L= L_I M= M34
M4  6   Vb1 4   4   N_18 W= W_I L= L_I M= M34
M1  3   Vin 7   7   N_18 W= W_I L= L_I M= M12
M2  4   Vip 7   7   N_18 W= W_I L= L_I M= M12
*CMFB
M13 7   5   GND GND N_18 W= W_I L= L_I M= Mcd
M14 7   6   GND GND N_18 W= W_I L= L_I M= Mcd
*stage2
M9  Von 5   VDD VDD P_18 W= W_I L= L_I M= M90
M10 Vop 6   VDD VDD P_18 W= W_I L= L_I M= M90
M11 Von 8   GND GND N_18 W= W_I L= L_I M= Mab
M12 Vop 8   GND GND N_18 W= W_I L= L_I M= Mab
*passive components
R1  8 Von 500K
R2  8 Vop 500K

.ends
```

我的電路設計理念是，第一步，先訂一個標準的NMOS與PMOS的W和L長度，也就是每一個NMOS與PMOS電晶體都具有相同的長度及寬度，並先進行模擬，再確認這個設計圖是正確連接之後，觀察隔個節點(node:1~7)的電壓以及各個線路的電流狀況，來進行每對電晶體的偏壓(bias voltage)評估。第二步，再評估完各組電晶體的偏壓(bias voltage)值之後，調整各個電晶體的W和L關係來使得電晶體都可以工作在合理的工作區段，也就是飽和區段(saturation region)，而作為回授電路的電晶體則工作在深度三極管區(deep triode region, also known as linear region)。第三步，就是逐一調整每個電晶體的M值，利用電路中的「交易」(trade-off)使電路在各方面都達到足夠的效能。

2. Simulation Results

預期達到效能：

Open loop gain	>3000
Single supply voltage	1.5V
Load	2pF
Output differential swing	1.5V
Unity-Gain-bandwidth	>10MHz
Phase margin	>60 deg.
Slew rate	>10V/us
Closed-loop gain	>=2
Power	<2mW

Table I

電路模擬結果：
(1)testbench.ma0

```
gain            phase_margin     unit_gain_freq   power
temper          alter#
  94.1351         61.9830          4.152e+07        4.238e-04
  25.0000       1
```

(2)Slew_rate.mt0

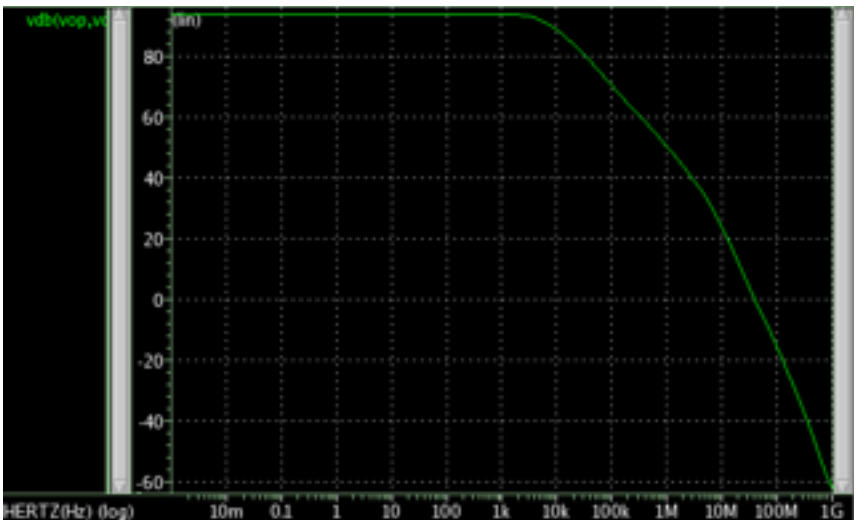
```
rise_time       fall_time        slew_rate_rise   slew_rate_fall
temper          alter#
 6.729e-09       7.970e-09         11.8883          10.0371
  25.0000       1
```

結果整理表格：

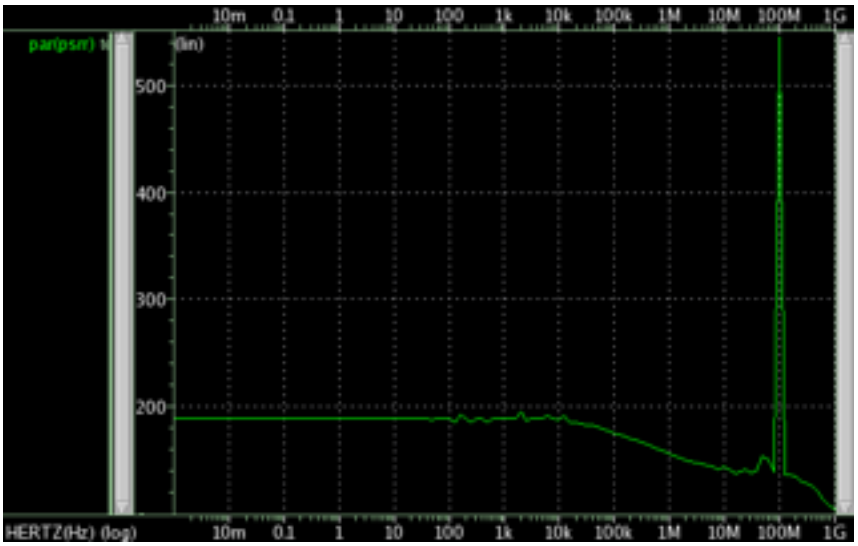
Open loop gain	94.1351(dB)
Single supply voltage	1.5V
Load	2pF
Output differential swing	1.5V
Unity-Gain-bandwidth	4.152e+07(Hz)
Phase Margin	61.9830(deg)
Slew rate	11.8883 / 10.0371 (V/us)
Closed-loop Gain	
Power	4.238e-04(W)

3. Other Simulation Plots

(1) Bode Plot



(2) the power supply rejection ratio



(3) Slew_rate