SAE International

SURFACE VEHICLE RECOMMENDED PRACTICE

SAE J1939-11 SEP2012

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Superseding J1939-11 SEP2005

Physical Layer, 250 Kbps, Twisted Shielded Pair

RATIONALE

Document is being revised to accommodate new OBD regulations which require a 5-meter stub for scan tool connection. Optional split backbone termination has been added. The format has been updated and several other clarifications have been made as part of a 5-year review.

FOREWORD

The set of SAE J1939 Recommended Practice documents define a high speed ISO 11898 CAN protocol based communications network that can support real-time closed loop control functions, simple information exchanges, and diagnostic data exchanges between Electronic Control Units (ECUs) physically distributed throughout the vehicle.

The SAE J1939 communications network is developed for use in heavy-duty environments and suitable for use in horizontally integrated vehicle industries. The physical layer aspects of SAE J1939 reflect its design goal for use in heavy-duty environments. Horizontally integrated vehicles involve the integration of different combinations of loose package components, such as engines and transmissions, which are sourced from many different component suppliers. The SAE J1939 common communication architecture strives to offer an open interconnect system that allows the ECUs associated with different component manufacturers to communicate with each other.

The SAE J1939 communications network is intended for light-duty, medium-duty, and heavy-duty vehicles used on-road or off-road, and for appropriate stationary applications which use vehicle derived components (e.g. generator sets). Vehicles of interest include, but are not limited to, on-highway and off-highway trucks and their trailers, construction equipment, and agricultural equipment and implements.

This set of SAE Recommended Practices has been developed by the SAE Truck and Bus Control and Communications Network Committee of the SAE Truck and Bus Electrical and Electronics Steering Committee. The SAE J1939 communications network is defined using a collection of individual SAE J1939 documents based upon the layers of the Open System Interconnect (OSI) model for computer communications architecture. These SAE J1939 documents are intended as a guide toward standard practice and are subject to change to keep pace with experience and technical advances.

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1. SCOPE

This document defines a physical layer having a robust immunity to EMI and physical properties suitable for harsh environments.

These SAE Recommended Practices are intended for light- and heavy-duty vehicles on- or off-road as well as appropriate stationary applications which use vehicle derived components (e.g., generator sets). Vehicles of interest include but are not limited to: on- and off-highway trucks and their trailers; construction equipment; and agricultural equipment and implements.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1113-13 Electromagnetic Compatibility Measurement Procedure for Vehicle Components--Part 13: Immunity to Electrostatic Discharge

SAE J1128 Low Voltage Primary Cable

SAE J1939 Serial Control and Communications Heavy Duty Vehicle Network - Top Level Document

SAE J1939-13 Off-Board Diagnostic Connector

SAE AS85485 Cable, Electric, Filter Line, Radio Frequency Absorptive

2.1.2 ISO Publication

Available from American National Standards Institute, 25 West 43rd Street, New York, NY 10036-8002, Tel: 212-642-4900, www.ansi.org.

ISO 11898-2 Road vehicles -- Controller area network (CAN) -- Part 2: High-speed medium access unit.

ISO 11898-5 Road vehicles -- Controller area network (CAN) -- Part 5: High-speed medium access unit with low-power Mode

ISO 6722-1 Road vehicles -- 60 V and 600 V single-core cables -- Part 1: Dimensions, test methods and requirements for copper conductor cables

3. NETWORK PHYSICAL DESCRIPTION

3.1 Physical Layer

The physical layer is a realization of an electrical connection of a number of ECUs (Electronic Control Units) to a network. The total number of ECUs will be limited by electrical loads on the bus line. This maximum number of ECUs is fixed to 30, on a given segment, due to the definition of the electrical parameters given in the present specification

3.2 Physical Media

This document defines a physical median of shielded twisted pair. These 2 wires have a characteristic impedance of 120 Ω and are symmetrically driven with respect to the electrical currents. The designations of the individual wires are CAN_H and CAN_L. The names of the corresponding pins of the ECUs are also denoted by CAN_H and CAN_L, respectively. The third connection for the termination of the shield is denoted by CAN_SHLD.

3.3 Differential Voltage

The voltages of CAN_H and CAN_L relative to ground of each individual ECU are denoted by V_{CAN_H} and V_{CAN_L}. The differential voltage between V_{CAN_H} and V_{CAN_L} is defined by Equation 1:

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad \text{(Eq. 1)}$$

3.4 Bus Levels

The bus lines can have one of the two logical states, recessive or dominant (see Figure 1). In the recessive state, V_{CAN_H} and V_{CAN_L} are fixed to a mean voltage level. V_{diff} is approximately zero on a terminated bus. The recessive state is transmitted during bus idle or a recessive bit.

The dominant state is represented by a differential voltage greater than a minimum threshold. The dominant state overwrites the recessive state and is transmitted during a dominant bit.

3.5 Bus Levels During Arbitration

A dominant and recessive bit imposed on the bus lines during a given bit time by two different ECUs will result in a dominant bit.

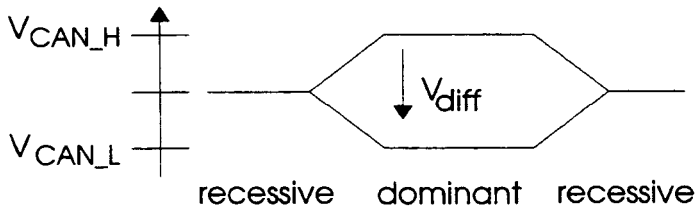


FIGURE 1 - PHYSICAL BIT REPRESENTATION

3.6 Common Mode Bus Voltage Range

The common mode bus voltage is defined as the boundary voltage levels of CAN_H and CAN_L, measured with respect to the individual ground of each ECU, for which proper operation is guaranteed when all ECUs are connected to the bus line.

3.7 Bus Termination

The bus line is electrically terminated at each end with a load resistor denoted by R_L (see Figure 2). Type I ECUs shall not contain the bus termination resistor R_L. Type II ECUs shall contain the bus termination resistor or split termination, and if used shall be located only at one or both ends of a network. Type II ECUs shall be clearly marked as specified in Section 5.2.5. (Also see 5.2.3 for resistor characteristics.)

3.8 Internal Resistance

The internal resistance, R_{in}, of an ECU is defined as the resistance between CAN_H (or CAN_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).

3.9 Differential Internal Resistance

The differential internal resistance, R_{diff}, is defined as the resistance between CAN_H and CAN_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).

3.10 Internal Capacitance

The internal capacitance, C_{in}, of an ECU is defined as the capacitance between CAN_H (or CAN_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).

3.11 Differential Internal Capacitance

The differential internal capacitance, C_{diff}, of an ECU is defined as the capacitance between CAN_H and CAN_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).

3.12 Bit Time

The bit time, t_B, is defined as the duration of one bit (see Figure 5). Bus management functions executed within this bit time, such as ECU synchronization behavior, network transmission delay compensation, and sample point positioning, are defined by the programmable bit timing logic of the CAN protocol IC (Integrated Circuit). The bit time for this document is 4 µs corresponding to 250 Kbit/s.

Various names for the bit segments are used by suppliers of CAN protocol ICs and it is possible that two bit segments are defined as one.

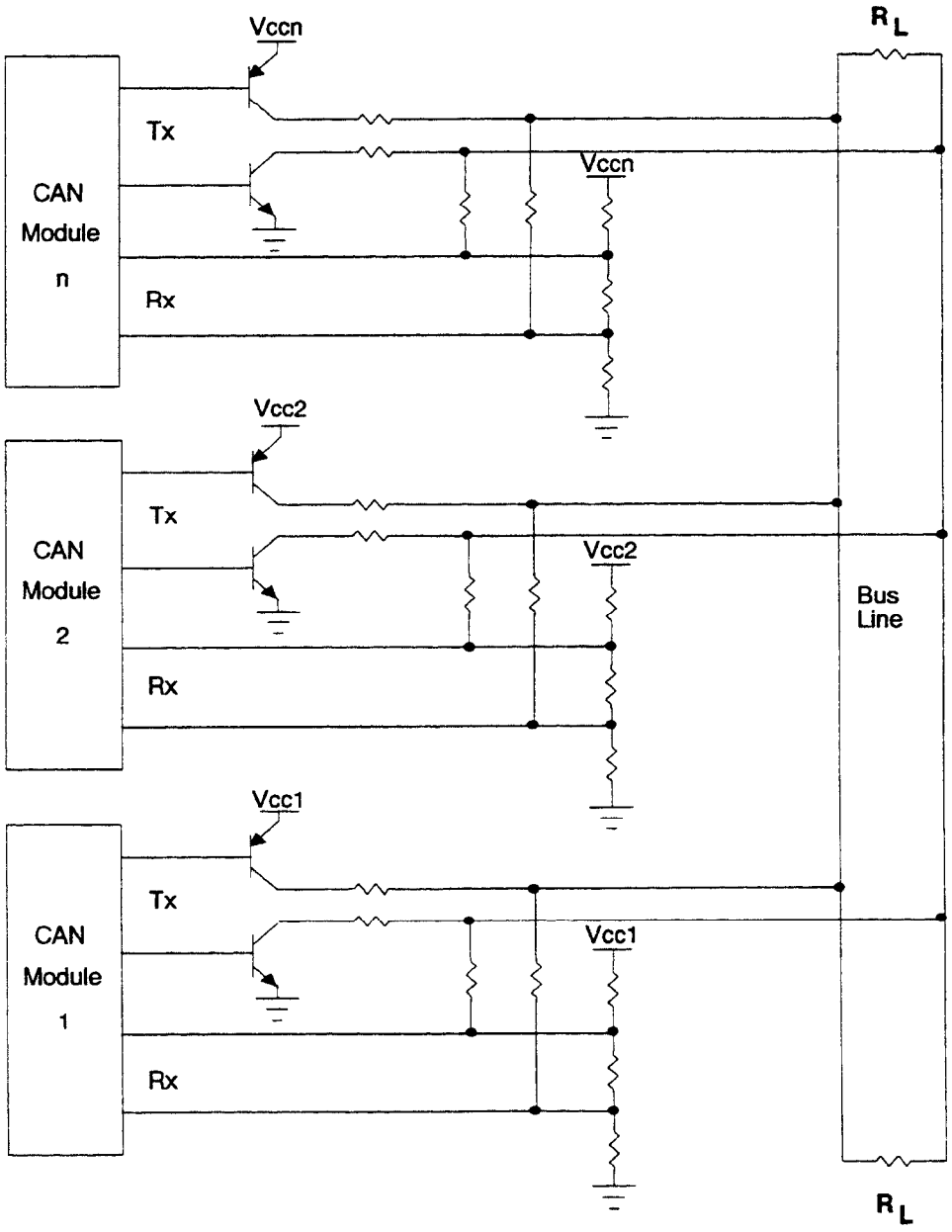


FIGURE 2 - PHYSICAL LAYER FUNCTIONAL

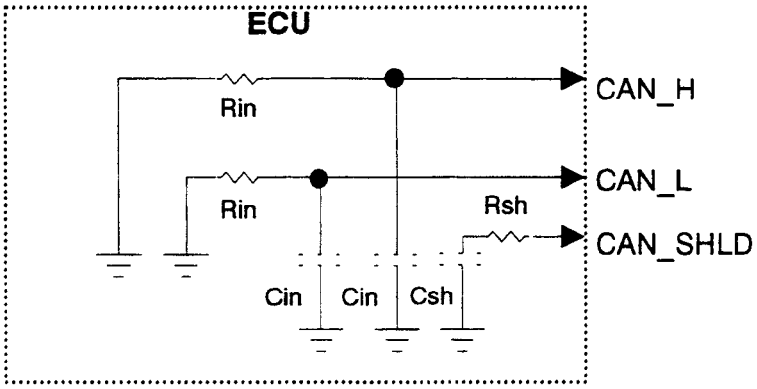


FIGURE 3 - ILLUSTRATION OF INTERNAL CAPACITANCE AND RESISTANCE OF AN ECU IN THE RECESSIVE STATE

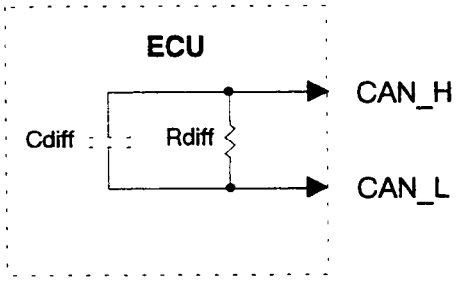


FIGURE 4 - ILLUSTRATION OF DIFFERENTIAL INTERNAL CAPACITANCE AND RESISTANCE OF AN ECU IN THE RECESSIVE STATE

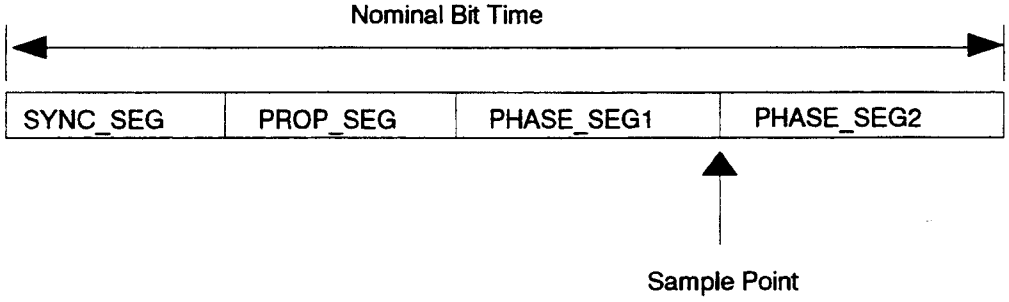


FIGURE 5 - PARTITION OF THE BIT

a. SYNC SEG - This part of the bit time is used to synchronize the various ECUs on the bus. An edge is expected within this bit segment.

b. PROP SEG - This part of the bit time is used to compensate for the physical delay times within the network. These delay times are caused by the propagation time of the bus line and the internal delay time of the ECUs.

c. PHASE SEG1, PHASE SEG2 - These Phase-Buffer-Segments are used to compensate for phase-errors and can be lengthened or shortened by resynchronization.

d. Sample-Point - The Sample-Point is the point of time at which the bus level is read and interpreted as the value of that respective bit. Its location is at the end of PHASE_SEG1.

3.13 Internal Delay Time

The internal delay time of an ECU, t_{ECU}, is defined as the sum of all asynchronous delays that occur along the transmission and reception path of the individual ECUs, relative to the bit timing logic unit of the protocol IC. For more details, see Figure 6.

a. Synchronization - Hard Synchronization and Resynchronization are the two forms of synchronization. They obey the following rules:

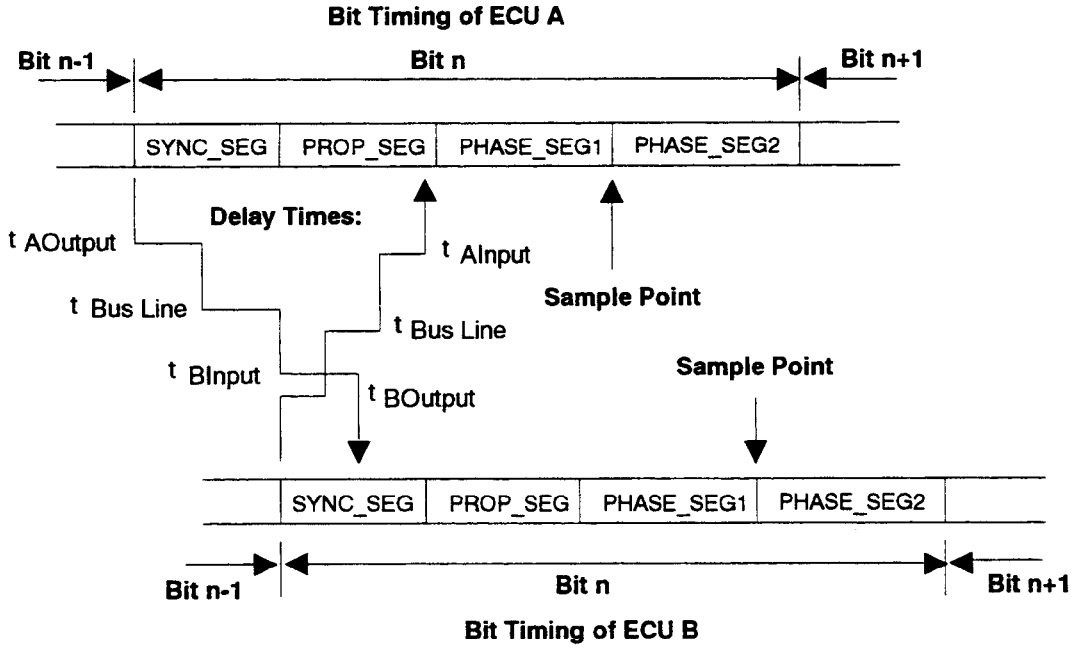
    1. Only one Synchronization within one bit time is allowed.

    2. An edge will be used for Synchronization only if the value detected at the previous Sample Point (previously read bus value) differs from the bus value immediately after the edge.

    3. Hard Synchronization is performed during said edge whenever there is a ‘recessive’ to ‘dominant’ edge.

    4. All other ‘recessive’ to ‘dominant’ edges fulfilling rules 1 and 2 will be used for Resynchronization with the exception that a transmitter will not perform Resynchronization as a result of a ‘recessive’ to ‘dominant’ edge with a positive Phase Error if only ‘recessive’ to ‘dominant’ edges are used for Resynchronization.

b. Synchronization Jump Width (SJW) - As a result of Synchronization PHASE_SEG1 may be lengthened or PHASE_SEG2 may be shortened. The amount of lengthening or shortening of the Phase Buffer bit Segments has an upper bound given by the Synchronization Jump Width. The Synchronization Jump Width is less than or equal to PHASE_SEG1.



Notes:

1) The sum of output and input ECU delays, with ECU disconnected from the bus relative to the bit timing logic is critical. The important characteristic parameter of an ECU is (see 3.12)

$$t\_ECU = t\_Output + t\_Input \quad [Where \_ = ECU (A,B...)]$$

2) For proper arbitration, the following condition must be met:

$$t_A ECU + t_B ECU + 2 * t_{Bus\ line} <= t_{PROP\_SEG} + (t_{PHASE\_SEG1} - t_{SJW})$$

SYNC_SEG is not taken into account as it is possible that this segment is lost if there is a phase shift between modules.

t_{SJW} is part of PHASE_SEG1 to compensate phase-errors. It is subtracted from the available time as it is possible that a spike may cause a missynchronization with a phase shift of t_{SJW}.

That means the leading transmitting bit timing logic with respect to synchronization of ECU A must be able to know the correct bus level of bit n at the sample point. The tolerable values of t_{ECU} strongly depends on the bit rate and line length of the bus and of the possible bit timing as shown by the arbitration condition.

3) The acceptable crystal tolerances of the protocol ICs and the potential for missynchronization is determined by PHASE_SEG1 and 2.

FIGURE 6 - TIME RELATIONSHIP BETWEEN BIT TIMING LOGIC OF ECU A AND B DURING ARBITRATION

3.14 CAN Bit Timing Requirements

It is necessary to ensure that a reliable network can be constructed with components from multiple suppliers. Without any bit timing restrictions, different devices may not be able to properly receive and interpret valid messages. Under certain network conditions it may also be possible for a particular device to have unfair access to the network. In addition, it makes network management (system diagnostics) much more difficult. CAN chip suppliers also recommend that all devices on a given network be programmed with the same bit timing values.

All CAN ICs divide the bit time into smaller sections defined as tq (time quantum). For most CAN ICs 1 tq = 250 ns (with a 16 MHz clock) (determined by oscillator frequency and baud rate prescaler).

Therefore specific values for the bit timing registers need to be defined to ensure that a reliable network exists for all nodes based on the best tradeoffs between propagation delay and clock tolerance. Note that there are some differences in bit segment definition between manufacturers of CAN devices.

It is recommended that a tq be selected which permits the sample point (see Figure 5) to be located as close to but not later than 7/8 of a bit time (0.875x4uS = 3.5uS). This provides the best tradeoff between propagation delay and clock tolerance.

The following values are recommended for typical controller ICs running at standard clock frequencies. At other frequencies, different values may have to be selected to maintain the sample point as close as possible but not later than the preferred time.

16 MHz
sample point = 0.875 tb
tq=250 ns (16 tq/bit)
tsync=250 ns (1 tq)
TSEG1 = 3.25 µs (13 tq)
TSEG2 = 500 ns (2 tq)

20 MHz
sample point = 0.85 tb
tq = 200 ns (20 tq/bit)
tsync = 200 ns (1 tq)
TSEG1 = 3.2 µs (16 tq)
TSEG2 = 600 ns (3 tq)

SJW = 1 tq (SJW is a part of TSEG1 and TSEG2)
Total Bit Time = TSEG1 + TSEG2 + Tsyncseg = 13 + 2 + 1 = 16 tq = 4 µs
(Example for 16 MHz clock)

PROP_SEG + PHASE_SEG1 = TSEG1
PHASE_SEG2 = TSEG2,
SYNC_SEG = SYNC_SEG

This selection for the bit timing registers generally requires the use of crystal oscillators at all nodes so that the clock tolerance given in Table 1 can be achieved.

TABLE 1 - AC PARAMETERS OF AN ECU DISCONNECTED FROM THE BUS LINE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bit time(1)	t_B	3.998	4.000	4.002	µs	250 Kbps
Internal Delay Time(2)	t_{ECU}	0.0		0.7	µs	
Internal Capacitance(3)	C_{in}	0	50	100	pF	250 Kbps for CAN_H and CAN_L relative to Ground
Differential Internal Capacitance(3)	C_{diff}	0	25	50	pF	
Available Time(4)	t_{avail}	2.5			µs	40 m bus length
Signal Rise, Fall Time(5)	t_R, t_F	200		500	ns	measured from 10% to 90% of the signal
Signal Rise, Fall Time(5)	t_R, t_F	200		500	ns	measured from 10% to 90% of the signal

1. Including initial tolerance, temperature, aging, etc.
2. The value of t_{ECU} has to be guaranteed for a differential voltage of V_{diff} = 1.0 V for a transition from recessive to dominant and of V_{diff} = 0.5 V for a transition from dominant to recessive. With the bit timing from the example of note 1, a CAN-Interface delay of 500 ns is possible (controller not included) with a reserve of about 300 ns. This allows slower slopes (R1 in Figure A.1) and input filtering. It is recommended to use this feature due to EMC.
   The minimal internal delay time may be zero. The maximum tolerable value is determined by the bit timing and the bus delay time.
3. In addition to the internal capacitance restrictions a bus connection should also have an inductance as low as possible. The minimum values of C_{in} and C_{diff} may be 0, the maximum tolerable values are determined by the bit timing and the network topology parameters l and d (see Table 8). Proper functionality is guaranteed if occurring cable resonant waves do not suppress the dominant differential voltage level below V_{diff} = 1 V and do not increase the recessive differential voltage level above V_{diff} = 0.5 V at each individual ECU (see Tables 3 and 4).
4. The available time results from the bit timing unit of the protocol IC. For example, this time in most controller ICs corresponds to TSEG1. Due to mis-synchronization it is possible to lose the length of SJW. So the available time (t_{avail}) with one mis-synchronization is TSEG1-SJW ms. A tq time of 250 ns and SJW = 1 tq, TSEG1 = 13 tq, TSEG2 = 2tq results in t_{avail} = 3.00 µs.
5. The load on the ECU for the purpose of this parameter should be 60 Ω between CAN_H and CAN_L in parallel with 200 pf of capacitance

4. FUNCTIONAL DESCRIPTION

As shown in Figure 2, the linear bus line is terminated with a load resistor R_L on each end. These resistors suppress reflections.

The bus is in the recessive state if the bus transmitters of all ECUs on the bus are switched off. In this case, the mean bus voltage is generated by the passive biasing circuit in all ECUs on the bus. In Figure 2 this is realized by the resistor network that defines the reference for the receive operation.

A dominant bit is sent to the bus line if the bus driver circuit of at least one unit is switched on. This induces a current flow through the terminating resistors, and consequently, a differential voltage between the two wires. The dominant and recessive states are passed by a resistor network which transforms the differential voltages of the bus line to corresponding recessive and dominant voltage levels at the comparator input of the receiving circuitry for detection.

5. ELECTRICAL SPECIFICATION

5.1 Electrical Data

The parameter specifications in these tables must be fulfilled throughout the operating temperature range of every ECU. These parameters allow up to a maximum of 30 ECUs to be connected to a given bus segment.

5.1.1 Electronic Control Unit

The limits given in the Tables 1 to 4, apply to the CAN_H and CAN_L pins of each ECU, with the ECU disconnected from the bus line (see Section 6).

TABLE 2 - LIMITS OF V_{CAN_H} AND V_{CAN_L} OF AN ECU DISCONNECTED FROM THE BUS LINE FOR NOMINAL BATTERY VOLTAGES OF 12 V AND 24 V

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Max. Voltage	V_{CAN_H}	–3.0		16.0	V	nominal battery voltage
	V_{CAN_L}	–3.0		16.0	V	12 V
Max. Voltage	V_{CAN_H}	–3.0		32.0	V	nominal battery voltage
	V_{CAN_L}	–3.0		32.0	V	24 V

5.1.1.1 Absolute Maximum Ratings

The limits given in Table 2 are the absolute maximum DC voltages which can be connected to the bus lines without damage to transceiver circuits. Although the link is not guaranteed to operate at these conditions, there is no time limit (operating CAN ICs will go “error passive” after a period of time).

5.1.1.2 DC Parameters

Tables 3 and 4 define the DC parameters for the recessive and dominant states, respectively, of an ECU disconnected from the bus.

TABLE 3 - DC PARAMETERS FOR THE RECESSIVE STATE OF AN ECU DISCONNECTED FROM THE BUS LINE - RECESSIVE STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Voltage Output Behavior	V_{CAN_H}	2.0	2.5	3.0	V	no load
	V_{CAN_L}	2.0	2.5	3.0	V	
Differential Voltage Output Behavior	V_{diff_or}	–1200		50	mV	no load
Differential Internal Resistance	R_{diff}	10		100	kΩ	no load
Internal Resistance(1)	R_{in}	5		15	kΩ	no load
Input Range	V_{diff}	–1.0		0.5	V	(2) (3) (4)

1. In order to generate symmetrical waveforms and minimize EMI radiation, R_{in} of CAN_H and CAN_L should have almost the same value. The deviation has to be less than 5% relative to each other.
2. The equivalent of the two terminating resistors in parallel (60 Ω) is connected between CAN_H and CAN_L.
3. Reception must be ensured within the common mode voltage range defined in Table 5 and Table 6, respectively.
4. Although V_{diff} < –1.0 V is only possible during fault conditions it should be interpreted as recessive.

TABLE 4 - DC PARAMETERS FOR THE DOMINANT STATE OF AN ECU DISCONNECTED FROM THE BUS LINE - DOMINANT STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Voltage Output Behavior	V_{CAN_H}	3.0	3.5	5.0	V	(1)
	V_{CAN_L}	0.0	1.5	2.0	V	
Differential Voltage Output Behavior	V_{diff_ld}	1.5	2.0	3.0	V	(1)
Input Range	V_{diff}	1.0		5.0	V	(1) (2)

1. The equivalent of the two terminating resistors in parallel (60 Ω) is connected between CAN_H and CAN_L.
2. Reception must be ensured within the common mode voltage range defined in Tables 5 and 6, respectively.

TABLE 5 - BUS VOLTAGE PARAMETERS FOR THE RECESSIVE STATE WITH ALL ECUS CONNECTED TO THE BUS LINE - RECESSIVE STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage on the bus line	V_{CAN_H}	0.1	2.5	4.5	V	measured with respect to
	V_{CAN_L}	0.1	2.5	4.5		ground of each ECU
Differential Bus Voltage(1)	V_{diff}	–400	0	12	mV	measured at each ECU connected to the bus line

1. The differential bus voltage is determined by the output behavior of all ECUs during the recessive state. Therefore, V_{diff} is approximately zero (see Table 3). The minimum value is determined by the requirement that a single transmitter must be able to represent a dominant bit by a minimum value of V_{diff} = 1.2 V.

TABLE 6 - BUS VOLTAGE PARAMETERS FOR THE DOMINANT STATE WITH ALL ECUS CONNECTED TO THE BUS LINE - DOMINANT STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage on Bus(1)	V_{CAN_H}		3.5	7.0	V	measured with respect to ground of each ECU
	V_{CAN_L}	−2.0	1.5			
Differential Bus Voltage(2)	V_{diff}	1.2	2.0	3.0	V	Measured at each ECU connected to the bus line
				5.0	V	during arbitration

1. The minimum value of V_{CAN_H} is determined by the minimum value of V_{CAN_L} plus the minimum value of V_{diff}. The maximum value of V_{CAN_L} is determined by the maximum value of V_{CAN_H} minus the value of V_{diff}.
2. The bus load increases as ECUs are added to the network, due to R_{diff}. Consequently, V_{diff} decreases. The minimum value of V_{diff} determines the number of ECUs allowed on the bus. The maximum value of V_{diff} is defined by the upper limit during arbitration. This maximum value of V_{diff} for single operation must not exceed 3 V.

5.1.1.3 AC Parameters

Table 1 defines the AC Parameter requirements of the ECUs.

5.1.2 Bus Voltages - Operational

The parameters specified in Tables 5 and 6 apply when all ECUs (between 2 and 30) are connected to a correctly terminated bus line. The maximum allowable ground offset between any ECUs on the bus is 2 V. The voltage extremes associated with this offset would occur in the dominant state (see Table 6).

5.1.3 Electrostatic Discharge (ESD)

CAN_H and CAN_L should be tested while disconnected from the bus line according to SAE J1113/13 for ESD using 15 kV.

5.1.4 Example Physical Layer Circuits

There are many physical layer circuits which meet the requirements of this recommended practice. Example implementations are shown in Appendix A.

5.2 Physical Media Parameters

The following sections describe the characteristics of the cable, termination, and topology of the network. (See Table 7.)

5.2.1 Bus Line

The bus line consists of a CAN_H, CAN_L and CAN_SHLD conductors. The CAN_H should be yellow in color while the CAN_L should be green. In addition, the cable must meet the minimum requirements in Table 7.

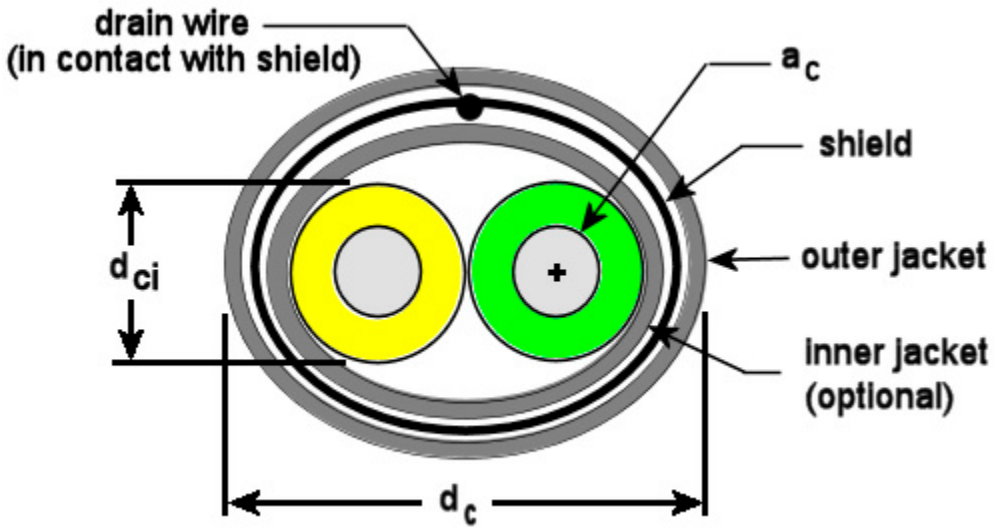


FIGURE 7 - CABLE CROSS-SECTION

TABLE 7 - PHYSICAL MEDIA PARAMETERS FOR TWISTED SHIELDED CABLE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Impedance	Z	108	120	132	Ω	Three meter sample length measured at 1 Mhz between the two sig. wires, with shield grounded, using open/short method.
Lay Length[6]		28	39	50	mm	(0.45 to 0.91 twists per 25.4 mm
Specific Resistance	r_b	0	25	50	mΩ/m	measured at 20 °C [1]
Specific Line Delay	t_p		5.0		ns/m	67% Vp[2]
Specific Capacitance	c_b	0	40	75	pF/m	Between conductors
	c_s	0	70	110	pF/m	Conductor to shield
Cable size						
0.5mm^2 Conductor (20 AWG)	a_c	0.508			mm^2	[3] [4]
Wire insulation dia.	d_{ci}	2.23		3.05	mm	
Cable diameter	d_c	6.0		8.5	mm	
0.8mm^2 Conductor (18 AWG)	a_c	0.760			mm^2	[3] [4]
Wire insulation dia.	d_{ci}	2.5		3.5	mm	
Cable diameter	d_c	8.5		11.0	mm	
Shield Effectiveness			200	225	mΩ/m	Surface transfer impedance up to 1 MHz Test method per SAE AS85485
Temperature Range	C	–40		+125	°C	Heat aging: 3000 hours per ISO 6722, Test with a mandrel 4-5x diameter of cable.[5]
Cable Bend Radius	r	4xdia of cable			mm	90 degree bend radius without cable performance or physical degradation

1. The differential voltage on the bus line seen by a receiving ECU depends on the line resistance between it and the transmitting ECU. Therefore, the total resistance of the signal wires is limited by the bus level parameters of each ECU.
2. The minimum delay time between two points of the bus line may be zero. The maximum value is determined by the bit time and the delay times of the transmitting and receiving circuitry.
3. Other conductor sizes available. Component insulation dimensions may be larger than those specified in SAE J1128. Design engineers should ensure compatibility between cables, connectors and contacts
4. Meet performance requirements of SAE J1128 for types GXL or SXL (includes drain wire where applicable)
5. 125°C or per OEM specification
6. Maximum untwisted wire at connector is 50 mm.

5.2.2 Topology

Figures 8A through 8C show the different wiring topologies with different combinations of network terminations. The figures contain ECU 1, ECU 2, ECU n-1 and ECU n, which are Type I ECUs. ECU A and ECU B in Figures 8B and 8C are Type II ECUs.

The wiring topology of this network should be as close as possible to a linear structure in order to avoid cable reflections. In practice, it may be necessary to connect short cable stubs to a main backbone cable, as shown in the Figure 8A. To minimize standing waves, nodes should not be equally spaced on the network and cable stub lengths, dimension S in Figures 8A through 8C, should not all be the same length. The dimensional requirements of the network are shown in Table 8.

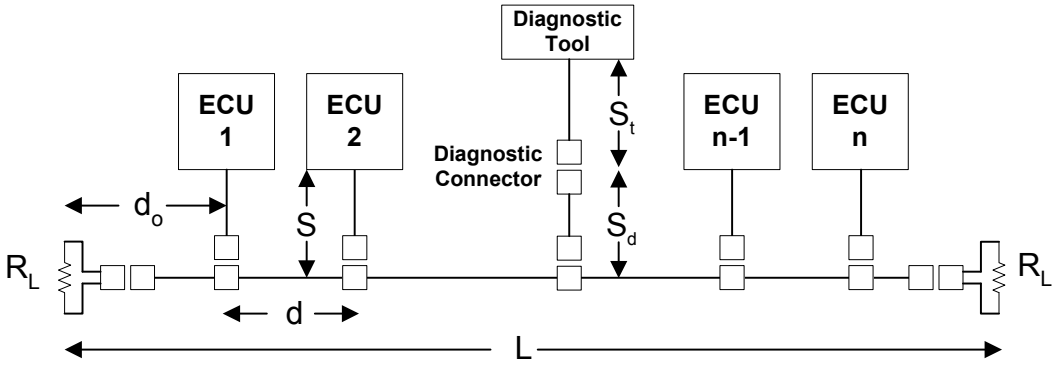


FIGURE 8A - NETWORK TOPOLOGY (TYPE I ECUS ONLY)

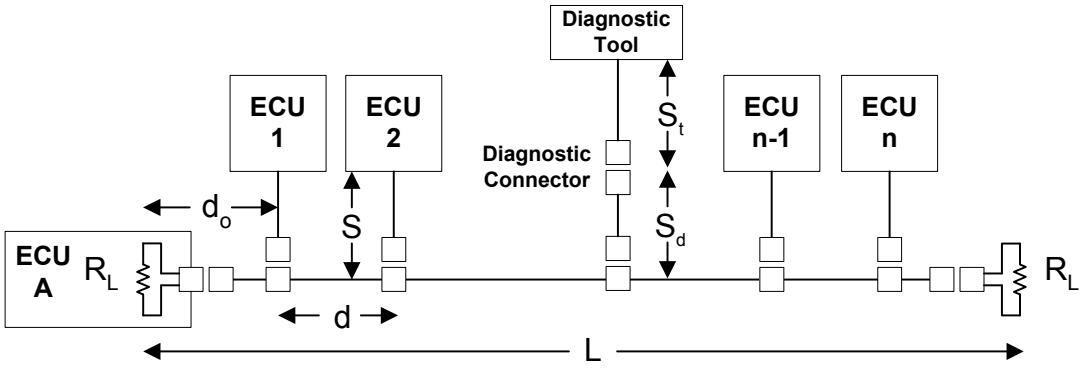


FIGURE 8B - WIRING NETWORK TOPOLOGY (ONE TYPE II ECU INSTALLED)

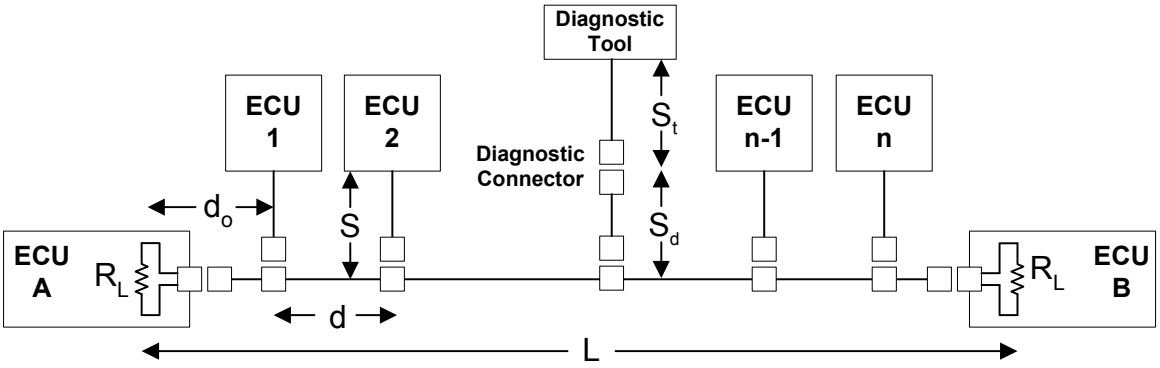


FIGURE 8C - WIRING NETWORK TOPOLOGY (TWO TYPE II ECUS INSTALLED)

TABLE 8 - NETWORK TOPOLOGY PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Length	L	0		40	m	not including cable stubs
Node Stub Length(1)	S	0		1	m	
Diagnostic Stub Length	S_d	0		0.66	m	
Diagnostic Tool Cable Length	S_t	0		5	m	
Stub Distance	d	0.1		40	m	The distance between stubs on the backbone
Stub Distance from R_L	d_0	0			m	R_L may be located within an ECU, but the ECU shall be marked as a Type II ECU

5.2.3 Terminating Resistor

Each end of the main ‘backbone’ of the linear bus must be terminated with an appropriate resistance to provide correct termination of the CAN_H and CAN_L conductors. This termination resistance should be connected between the CAN_H and CAN_L conductors. The termination resistance should meet the characteristics specified in Table 9.

TABLE 9 - TERMINATING RESISTOR PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Resistance	R_L	110	120	130	Ω	minimum power dissipation 400 mW(1)

1. Assumes a short of 16V to V_{CAN_H}

5.2.4 Split termination of backbone

One or both ends of the backbone may be terminated with split termination in which R_L is divided into two well matching resistors. (See Figure A3.) In order to achieve good electro-magnetic emission performance, it is recommended not to exceed ±1 % tolerance between the two identical resistors of the split termination locally. Reference ISO 11898-5.

The center tap between the resistors should be connected to ground through a 4.7 nF capacitor, C_L.

5.2.5 Shield Termination

The shield should be terminated by a wire conductor and directly grounded at only one point.

General guidelines (in order of importance) for direct termination of the shield are:

1. Connect to the point of least electrical noise
2. Use the lowest impedance connection possible
3. The closest connection to the center of the network should be used.

It is the responsibility of the vehicle manufacturer to identify the shield termination implementation.

Each node on the bus should also provide a shield ground; however, this connection of the CAN_SHLD conductor should be by a series resistor and capacitor to the best ground connection within the node. Recommended values are R = 1 Ω and C = 0.68 μF. (See Figure A1.)

5.2.6 ECU Type I and Type II Markings

An ECU that does not contain an internal Load Resistor (R_L) shall be designated as a Type I ECU and does not require a marking. An ECU that contains an internal R_L shall be designated as a Type II ECU. The Type II ECU shall have a unique marking on the outside housing to easily determine the internal R_L feature.

5.3 Connector Specifications

Two types of connectors are shown that are capable of implementing all aspects of the network. An ECU may be connected with either a hard splice (Appendix C) or connector. If a connector is to be used to connect an ECU to the 'backbone' of the network, it is called the Stub Connector and is designated “A” in Figure 9. The ‘backbone’ connector is shown in Figure 10. The connector used to connect the termination resistor to the ends of the 'backbone' cable or to pass through structural boundaries, such as cab bulkheads, or to extend the ends of the 'backbone' is called the ‘Through Connector’ and is designated “B” in Figure 9. The ‘Through Connector’ is shown in Figure 11.

These two connectors are very similar in design, with different keying structures to eliminate the possibility of connecting the network in a method that would be detrimental to proper communications. The connectors shall provide for the electrical connections of CAN_H, CAN_L, and drain wire CAN_SHLD.

An example of the use of this connector concept is shown in Figure 9.

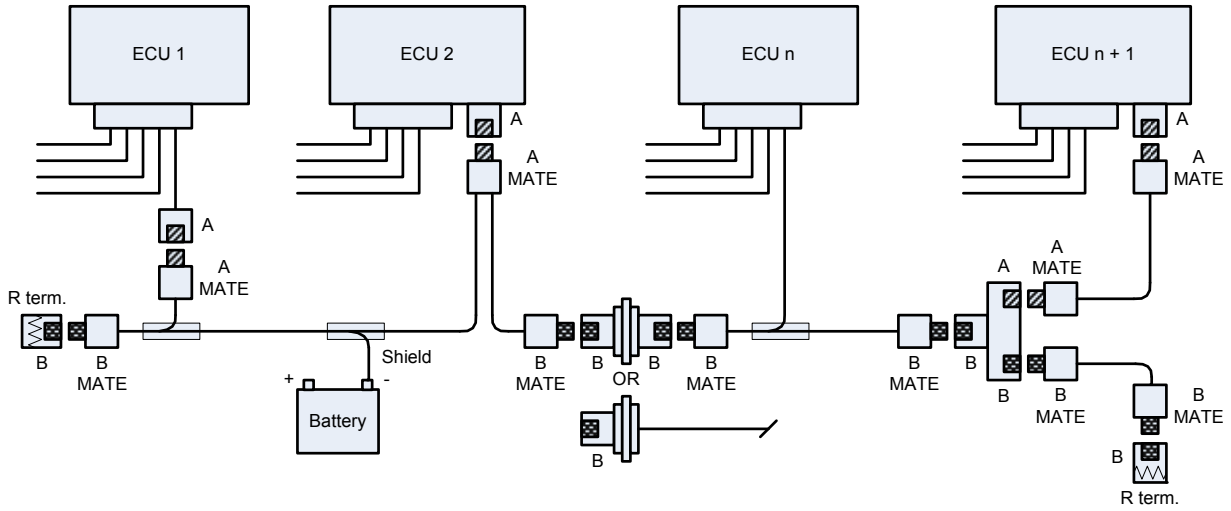


FIGURE 9 - AN EXAMPLE OF NETWORK CONNECTOR USAGE

5.3.1 Connector Electrical Performance Requirements

The connectors and their associated terminals shall meet the electrical requirements specified in Table 10.

TABLE 10 - CONNECTOR PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage[1]	V_{CAN_H}			16	V	nominal VBAT=12 V
	V_{CAN_L}			32	V	nominal VBAT=24 V
Current	I	0	25	80	mA	
Peak Current	I_p			500	mA	Time restriction: $101t_B$ [1]
Characteristic Impedance	Z_c	100	120	140	Ω	
Transmission Frequency	f	25			Mhz	
Contact Resistance[2]	R_T			10	mΩ	

1. Bus fault.
2. The differential voltage on the bus line seen by a receiving ECU depends on the line resistance between this and the transmitting ECU. Therefore, the transmission resistance of the signal wires is limited by the bus level parameters at each ECU.

5.3.2 Connector Mechanical Requirements

If connectors are used, these connectors should have locking, polarizing, and retention devices that meet the requirements of the specific application. These connectors should also incorporate environmental protection appropriate for the application. The dimensional characteristics of the Stub and Through connectors are shown in Figures 10 and 11, respectively.

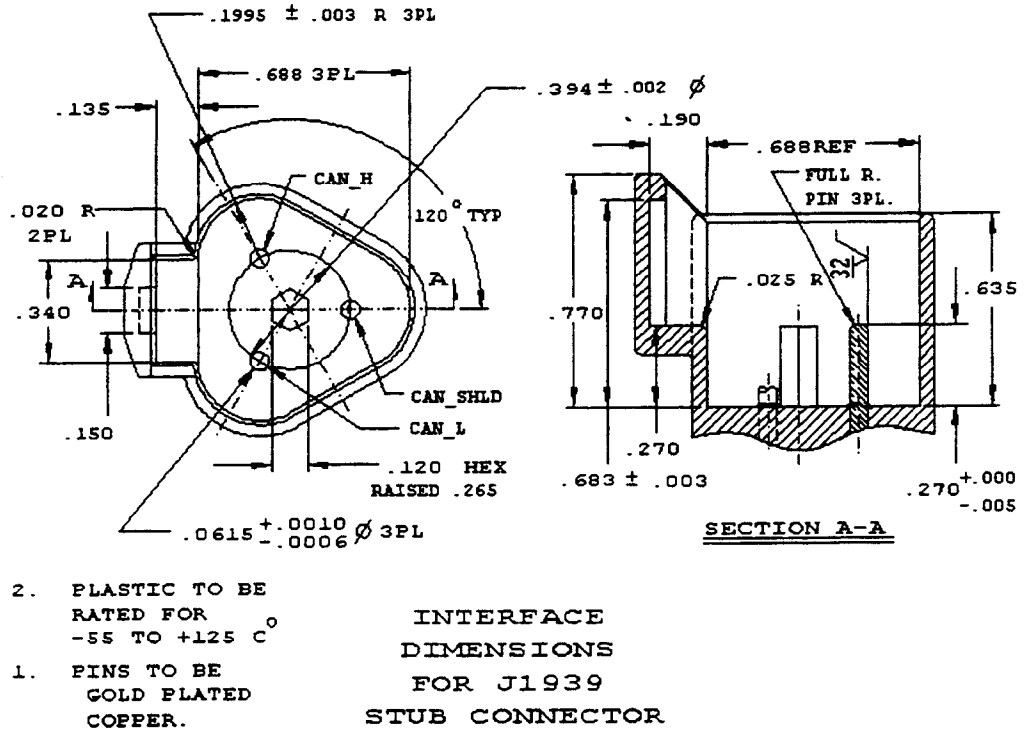


FIGURE 10 - STUB CONNECTOR (WITH MALE KEY) DIMENSIONAL REQUIREMENTS (A)

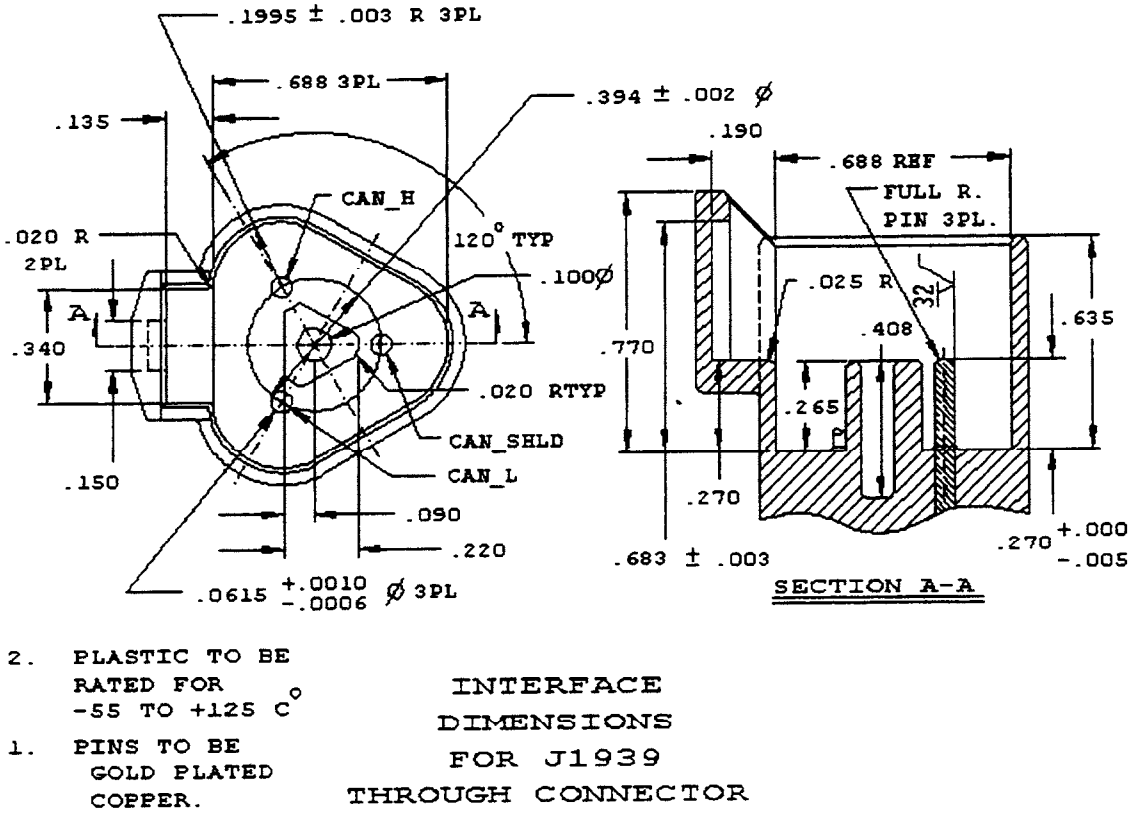


FIGURE 11 - THROUGH CONNECTOR (WITH FEMALE KEY) DIMENSIONAL REQUIREMENTS (B)

6. CONFORMANCE TESTS

The following figures and formulas show, in principle, how the parameters specified in Section 5.1 should be verified by component manufacturers. While there are many requirements of the physical layer, this section defines a portion of Transceiver compliance tests. Note that the ground connection is not the same as CAN_SHLD. The measurement ground reference should be the ECU ground.

6.1 Recessive Output of the ECUs

The recessive output voltage can be measured as shown in Figure 12.

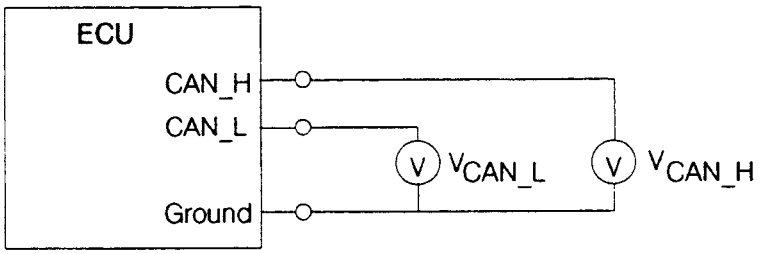


FIGURE 12 - MEASUREMENT OF V_{CAN_H} AND V_{CAN_L} DURING THE BUS IDLE STATE

V_{CAN_H} and V_{CAN_L} are measured unloaded while the bus is idle. V_{diff} is then determined by

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad \text{(Eq. 2)}$$

Table 3 defines the limits during the recessive state.

NOTE: V_{CAN_H} and V_{CAN_L} is measured with no load such that the worst case would be observed for the maximum recessive condition.

6.2 Internal Resistance of CAN_H and CAN_L

The internal resistance, R_{in}, of CAN_H and CAN_L can be measured as shown in Figure 13.

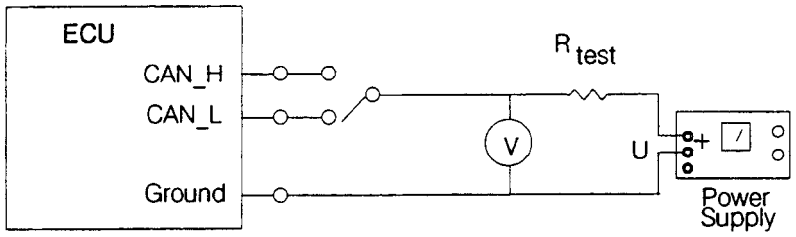


FIGURE 13 - MEASUREMENT OF R_{IN} WHILE THE ECU PROTOCOL IC IS SET TO BUS IDLE

R_{in} of CAN_H and CAN_L is determined for U = 0 V and U = 5 V, respectively, with R_{test} = 5 kΩ. R_{in} of CAN_H and CAN_L is then calculated by

$$R_{in} = R_{test} \frac{V_{CAN\_H,L} - V}{V - U} \quad \text{(Eq. 3)}$$

where:

V_{CAN_H} and V_{CAN_L} are the open circuit voltages according to Figure 12. R_{in} is defined for the recessive state by Table 3, including Note 4, for DC - Parameters.

6.3 Internal Differential Resistance

The internal differential resistance R_{diff} can be measured as shown in Figure 14.

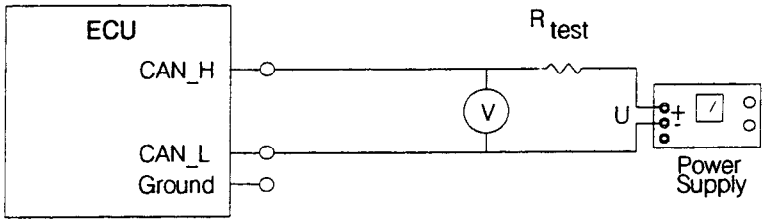


FIGURE 14 - MEASUREMENT OF R_{DIFF} WHILE THE ECU PROTOCOL IC IS SET TO BUS IDLE

R_{diff} is determined for U = 5 V and R_{test} = 10 kΩ during bus idle as shown in Equation 4:

$$R_{diff} = R_{test} \frac{(V_{diff} - V)}{V - U} \quad \text{(Eq. 4)}$$

where:

V_{diff} is the differential open circuit voltage according to 6.1.

6.4 Recessive Input Threshold of an ECU

The recessive input threshold can be verified over the common mode range as shown in Figure 15.

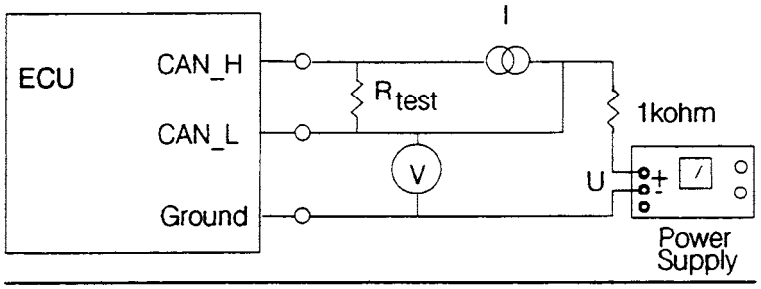


FIGURE 15 - TESTING THE INPUT THRESHOLD FOR RECESSIVE BIT DETECTION

Current I is adjusted to a value which develops 0.5 V (the upper limit for detecting a recessive bit during the recessive state) across R_{test} with R_{test} = 60 Ω (Bus Line Load Equivalent Resistance). In addition, U is set to two suitable values that produce V = –2 V and V = 6 V during bus idle. Under these conditions, the ECU must not stop transmitting. This indicates that every transmitted recessive bit is still detected as recessive by the protocol IC of the ECU. The level of the dominant bits is nearly independent of U.

NOTE: The 6 V value is used instead of 7 V since the maximum threshold for receiving a recessive bit is 0.5 V per Table 2.

6.5 Dominant Output of an ECU

The dominant output of an ECU can be measured as shown in Figure 16.

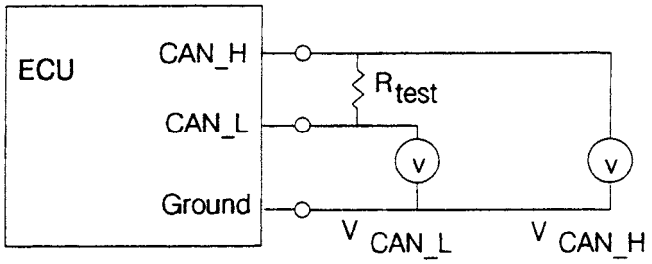


FIGURE 16 - MEASUREMENT OF V_{CAN_H} AND V_{CAN_L} WHILE THE ECU SENDS A DOMINANT BIT

V_{CAN_H} and V_{CAN_L} are measured during a dominant bit transmission. R_{test} is set to 60 Ω. The corresponding value of V_{diff} is given by

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad \text{(Eq. 5)}$$

Note that the dominant state voltages of an ECU disconnected from the bus are defined in Table 4.

6.6 Dominant Input Threshold of an ECU

The dominant input threshold of an ECU can be verified over the common mode range as shown in Figure 17.

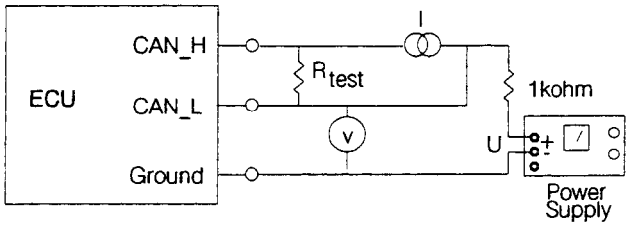


FIGURE 17 - TESTING THE INPUT THRESHOLD FOR DOMINANT BIT DETECTION

Current I is adjusted to a value which induces, with R_{test} = 60 Ω (Bus Line Load Equivalent Resistance), the upper threshold of 1 V required to detect a dominant bit during the recessive state. In addition, U is set to two values that produce V = −2 V and V = 6 V during bus idle. Under these conditions, the ECU must stop transmitting the message which demonstrates that arbitration has been acknowledged. This indicates that every transmitted recessive bit is detected as dominant by the protocol IC of the ECU. The level of dominant bits is nearly independent of U.

NOTE: The 6 V value is used instead of 7 V since the maximum threshold for receiving a dominant bit is 1 V per Table 4.

6.7 Internal Delay Time

The internal delay time of an ECU can be measured as shown in Figure 18.

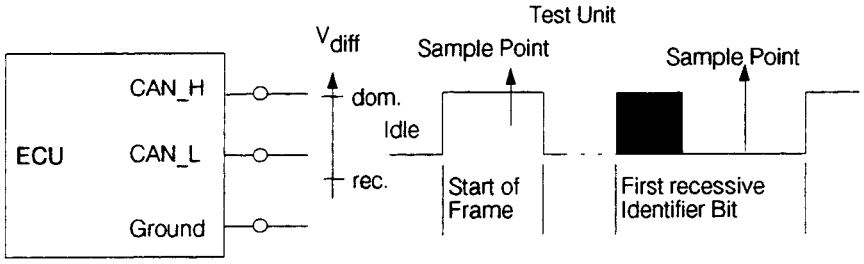


FIGURE 18 - MEASUREMENT OF THE INTERNAL DELAY TIME T_{ECU} BY PARTLY OVERWRITING THE FIRST RECESSIVE IDENTIFIER BIT (SHADED AREA) BY A DOMINANT LEVEL UNTIL THE ARBITRATION IS LOST

The test unit shown in Figure 18 synchronizes itself to the start of frame bit transmitted by the protocol IC of the ECU. Upon detection of the first recessive identifier bit, the test unit partly overwrites this recessive bit for a time t_{overw} by a dominant level (shaded area in Figure 18). This overwriting is increased until the protocol IC of the ECU loses arbitration and stops transmitting. If this situation is reached, the available part of the bit time t_{avail} for delay time compensation is just exhausted (see also Figures 5 and 6 and Table 7). Then t_{ECU} is calculated by Equation 6.

$$t_{ECU} = t_{avail} - t_{overw} \quad \text{(Eq. 6)}$$

where:

t_{avail} is known from the bit timing unit of the protocol IC and t_{overw} is known from the test unit.

The dominant and recessive voltage levels are set by the test unit to the corresponding threshold voltages for reception. This means that the dominant overwriting level is 1 V, and the recessive level is 0.5 V. This ensures a uniquely defined relationship between voltage levels and internal delay time.

7. DISCUSSION OF BUS FAULTS

a. Possible Failures—During normal operation, several bus failures can occur that may influence operation. These failures and the resulting network behavior are specified subsequently.

7.1 Loss of Connection to Network

If a node becomes disconnected from the network, the remaining nodes shall continue communication.

7.2 Node Power or Ground Loss

If a node loses power, or if it is in a low voltage condition, the network is not loaded down, and the remaining nodes shall continue communication.

If a node loses ground, the network shall not be biased up. The remaining nodes shall continue communication.

7.3 Unconnected Shield

In case the shield loses connection at one node, communication is possible but electromagnetic interference increases. Common mode voltages can be induced between the shield and the wires.

7.4 Open and Short Failures

In principle, failures are detectable if there is a significant message destruction rate, as interpreted by the electronic control units. Some external events that may cause failures are shown in Figure 19 and are discussed as follows:

a. Case 1: CAN_H is Interrupted—Data communication between nodes on opposite sides of an interruption is not possible. Data communication between nodes on the same side of an interruption may be possible, but with reduced signal-to-noise ratio.

b. Case 2: CAN_L is Interrupted—Data communication between nodes on opposite sides of an interruption is not possible. Data communication between nodes on the same side of an interruption may be possible, but with reduced signal-to-noise ratio.

c. Case 3: CAN_H is Shorted to VBat—Data communication is not possible if VBat is greater than the maximum allowed common mode bus voltage.

d. Case 4: CAN_L is Shorted to GND—Data communication is possible, because the bus voltages are within the allowed common mode voltage range. Signal-to-noise ratio is reduced and radiation is increased. The electromagnetic immunity is decreased.

e. Case 5: CAN_H is Shorted to GND—Data communication is not possible.

f. Case 6: CAN_L is Shorted to VBat—Data communication is not possible.

g. Case 7: CAN_H is Shorted to CAN_L—Data communication is not possible.

h. Case 8: Both Bus Lines are Interrupted at the Same Location—Data communication between nodes on opposite sides of an interruption is not possible. Data communication between nodes on the same side of an interruption may be possible, but with reduced signal-to-noise ratio.

I. Case 9: Loss of Termination Resistor—Data communication via the bus may be possible, but with reduced signal-to-noise ratio.

j. Case 10: Topology Parameter Violations (i.e., Bus Length, Cable Stub Length, Node Distribution)—Data communication via the bus may be possible, but with reduced signal-to-noise ratio.

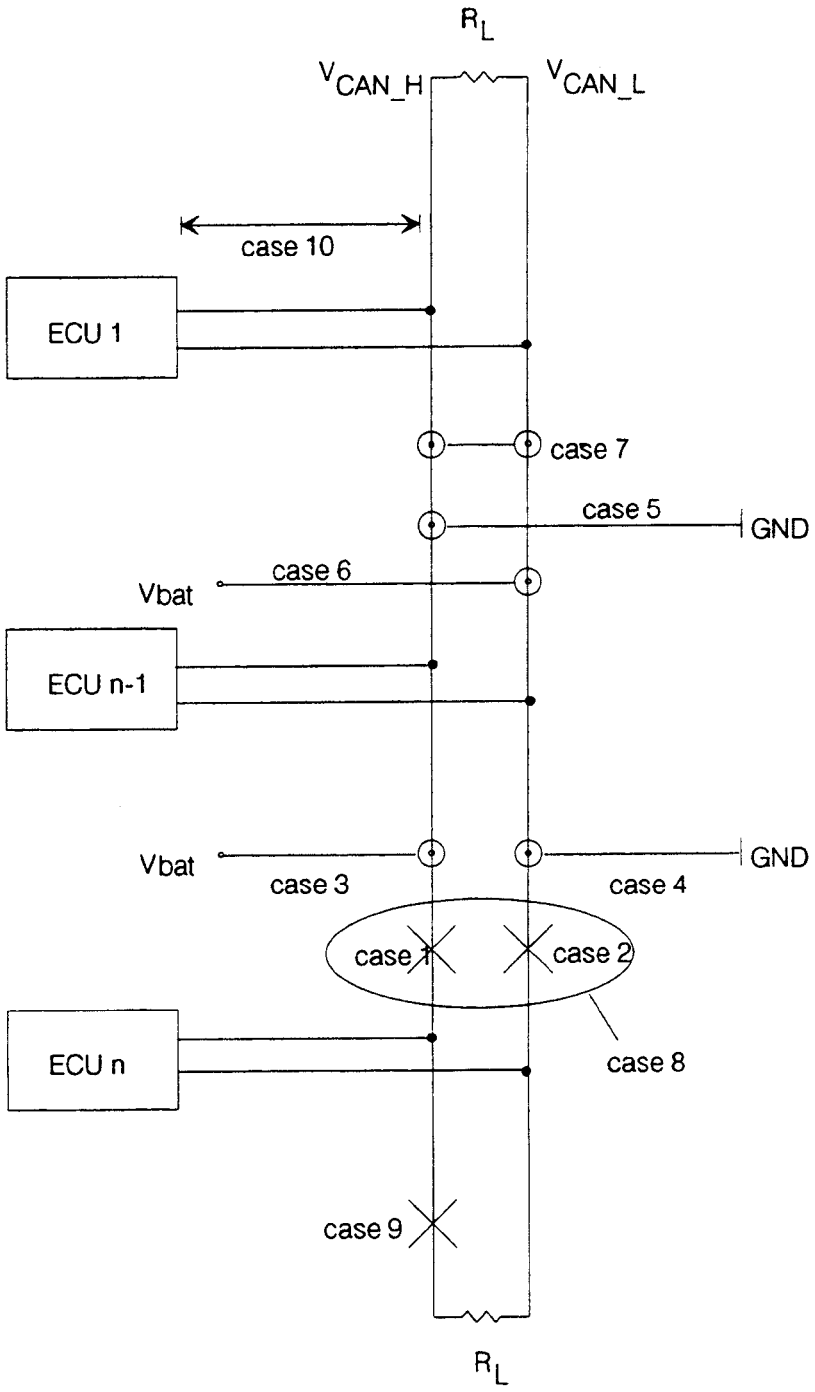


FIGURE 19 - POSSIBLE FAILURES DUE TO EXTERNAL EVENTS

8. NOTES

8.1 Marginal Indicia

A change bar (l) located in the left margin is for the convenience of the user in locating areas where technical revisions, not editorial changes, have been made to the previous issue of this document. An (R) symbol to the left of the document title indicates a complete revision of the document, including technical revisions. Change bars and (R) are not used in original publications, nor in documents that contain editorial changes only.

PREPARED BY THE SAE TRUCK AND BUS CONTROL AND COMMUNICATIONS NETWORK COMMITTEE OF THE SAE TRUCK AND BUS ELECTRICAL AND ELECTRONIC STEERING COMMITTEE

APPENDIX A- EXAMPLE CIRCUITS

A.1 EXAMPLE PHYSICAL LAYER CIRCUITS

This circuit provides a solution utilizing surface mount components and an integrated circuit CAN transceiver, U1. Capacitor C1 provides power supply decoupling for U1 and is typically between 0.01 UF and 0.1 UF. Resistor R1 determines the slope (rise and fall times) of CAN_H and CAN_L while the IC is transmitting. The VREF output, pin 5 of U1, provides a voltage of approximately VCC/2.

L1 is used to reduce the amount of high-frequency microprocessor switching noise coupled on the bus. Testing has shown this component to reduce radiated emissions over the test range of 10 KHz to 200 MHz, but particularly below 30 MHz. While this component improves radiated emissions performance, its use is not essential to meeting the requirements of SAE J1939-11 and therefore not required. The radiated emissions performance of ECU must be addressed on an individual basis.

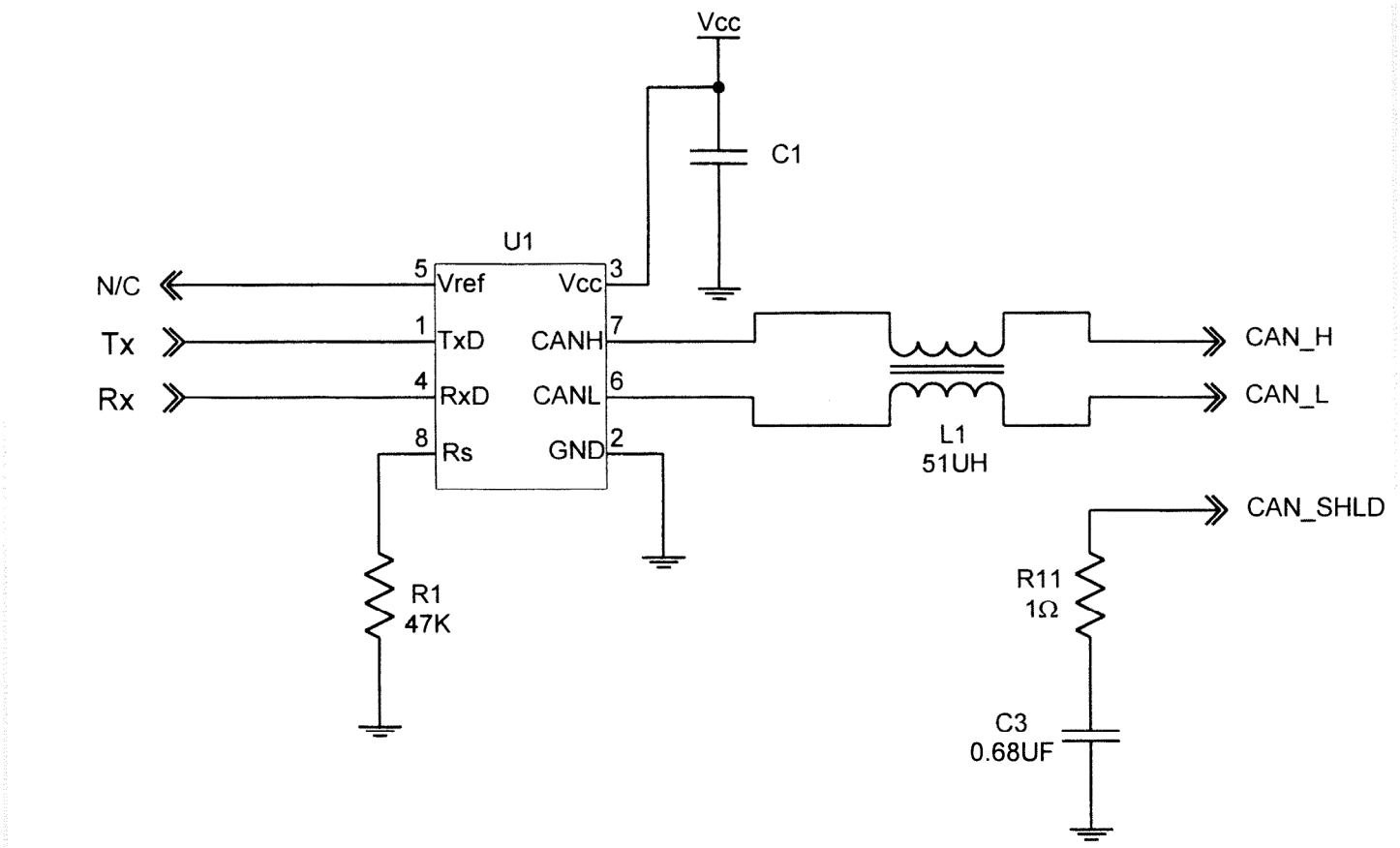


FIGURE A1 - EXAMPLE PHYSICAL LAYER CIRCUIT

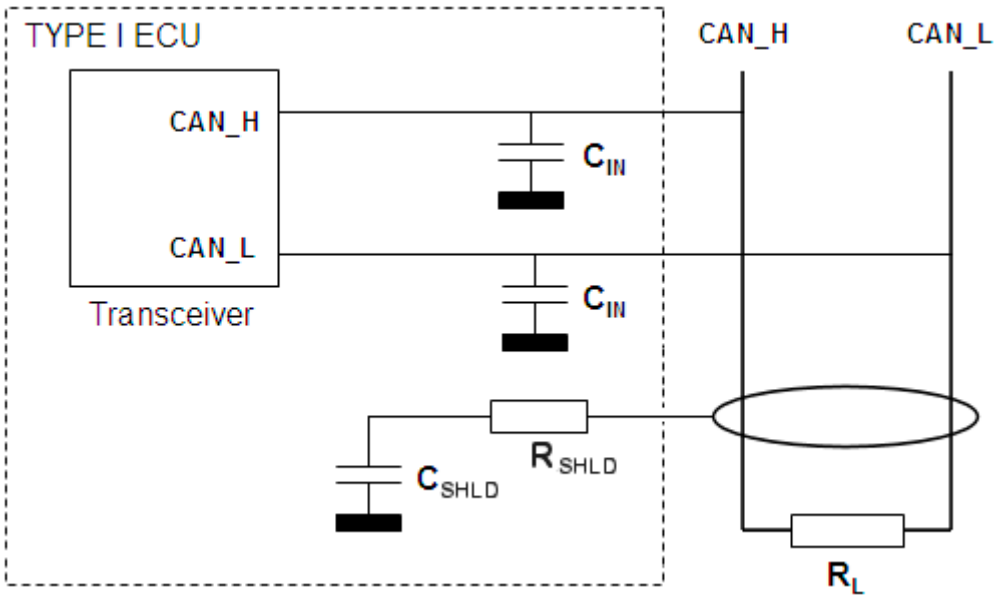


FIGURE A2 – CIRCUIT WITH EXTERNAL BACKBONE TERMINATION

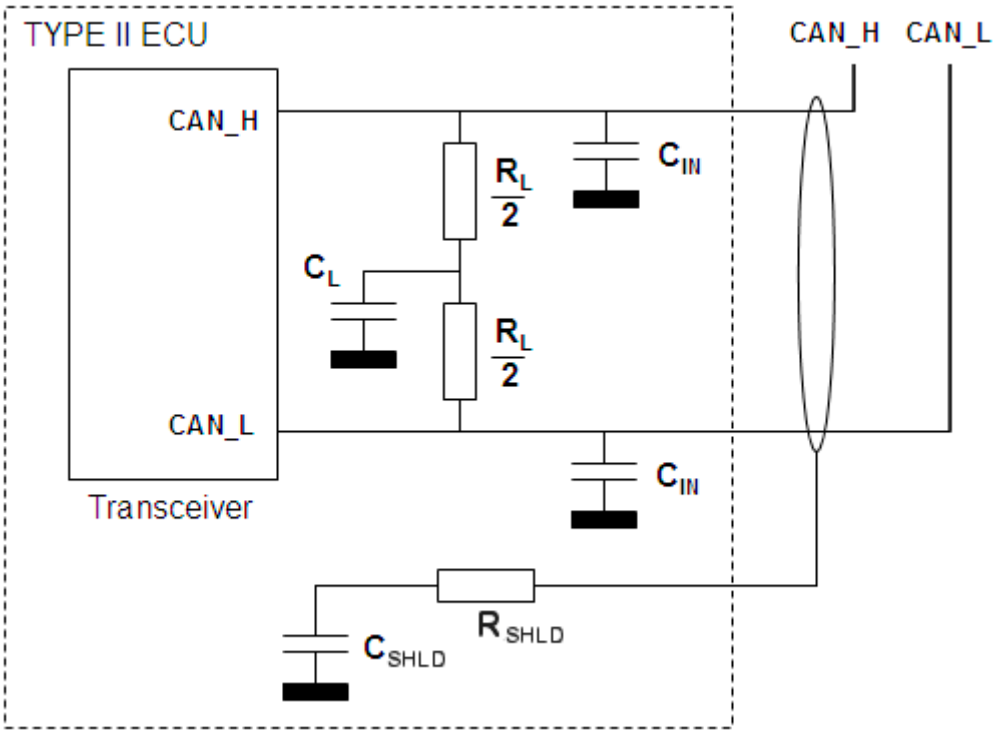


FIGURE A3 – CIRCUIT WITH INTERNAL BACKBONE SPLIT TERMINATION

APPENDIX B - RECOMMENDED CABLE TERMINATION PROCEDURE

B.1 RECOMMENDED CABLE TERMINATION PROCEDURE

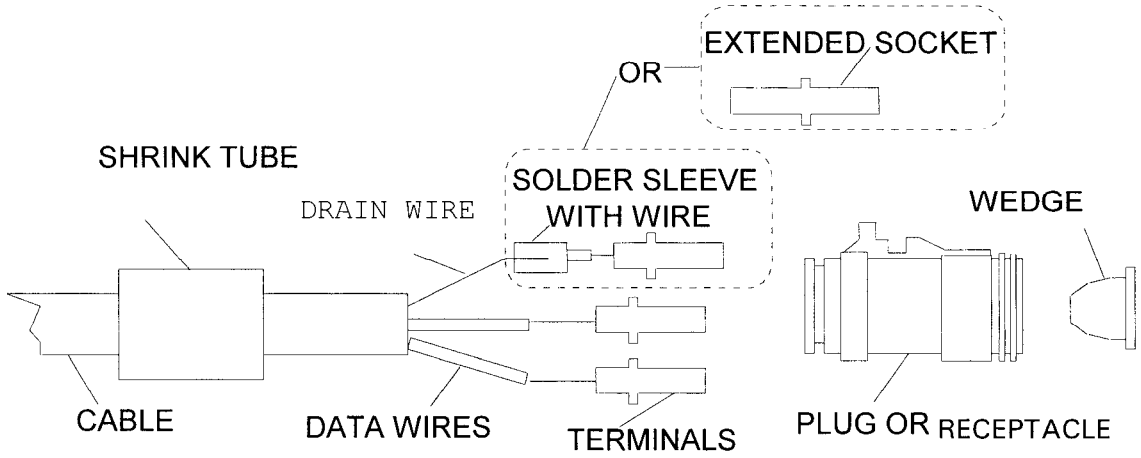


FIGURE B1 - CABLE TERMINATION

1. Remove cable outer jacket approximately 40 to 100 mm. Maintain wire twist so that the untwisted length is no more than 50 mm from the wire seals in the finished connection. However, enough wire should be left untwisted to avoid deformation of the connector seals.

2. Remove foil shield from exposed wires to within 2 mm of cable jacket.

3. Strip insulation from data wires 7 mm ± 0.8 mm.

4. Attach adhesive filled solder sleeve and wire to drain wire per manufacturer's recommendation OR attach extended wire barrel socket contact to the drain wire.

5. For the solder sleeve option, cut wire on solder sleeve to a length of 25 mm and strip the insulation on that wire 7 mm ± 0.8 mm.

6. Crimp the appropriate terminal on each data wire and the solder sleeve wire OR extended socket per manufacturers recommendation.

7. Slide adhesive filled shrink tube over cable end.

8. Install terminals into connector body per manufacturer's instructions. Isopropyl alcohol may be used to aid in assembly.

9. Install wedge in front of connector body per manufacturer's instructions.

10 For outer jacket removal greater than 40 mm, apply the replacement EMC shielding material per the manufacturer's recommendation.

11. Apply shrink tube to end of connector body per manufacturer's recommendation.

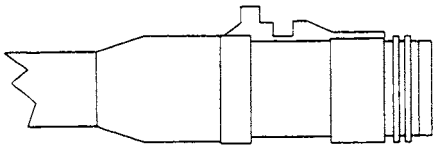


FIGURE B2 - FINISHED ASSEMBLY

APPENDIX C- RECOMMENDED CABLE SPLICE PROCEDURE

C.1 RECOMMENDED CABLE SPLICE PROCEDURE

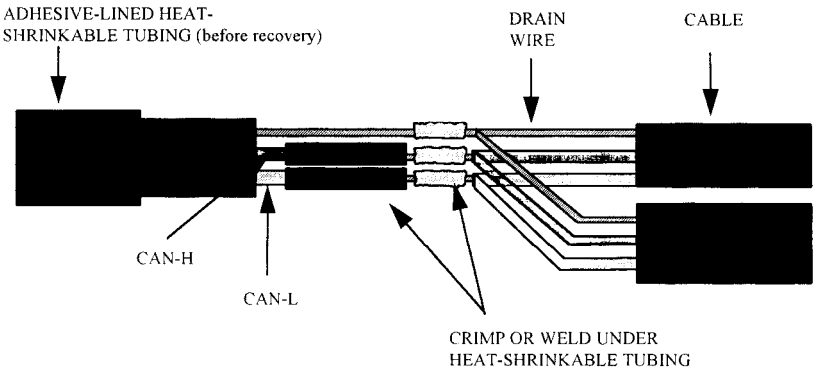


FIGURE C1 - CABLE SPLICE[1]

1. Cut the end of the cable cleanly. Measure back 40 mm to 100 mm and mark the cable jacket. Remove this section of cable jacket and foil shield.
2. Measure back approximately 6 mm on the drain wire and cut it.
3. Remove approximately 6 mm of insulation on the data wire CAN-H.
4. Measure back approximately 21 mm on data wire CAN-L and cut it. Remove approximately 6 mm of insulation.
5. Repeat steps 1 through 4 for the other two cables that will be spliced but REVERSE the order of steps 3 and 4 for CAN-H and CAN-L[2].
6. Slide the two pieces of insulating heat-shrinkable tubing over the CAN-H and CAN-L data wires.
7. Slide the one piece of adhesive-lined heat-shrinkable tubing onto the cable.
8. Install crimp (or weld) the three drain wires together, the three CAN-H data wires together, and the three CAN-L data wires together.
9. Solder the connections if desired.
10. Center the insulating heat-shrinkable tubing over the two crimped or welded data wire splices and install the tubing per the manufacturer's recommendation.

---

[1] Shielding material not shown.
[2] The overall length of the assembly is minimized by offsetting the crimps.

11. Apply the replacement EMC shielding material per the manufacturer's recommendation.

12. Center the adhesive-lined heat-shrinkable tubing over the assembly and apply per manufacturer's recommendation.

FIGURE C2 - SEALED CABLE SPLICE-FINISHED ASSEMBLY

APPENDIX D- RECOMMENDED CABLE REPAIR PROCEDURE

D.1 RECOMMENDED CABLE REPAIR PROCEDURE

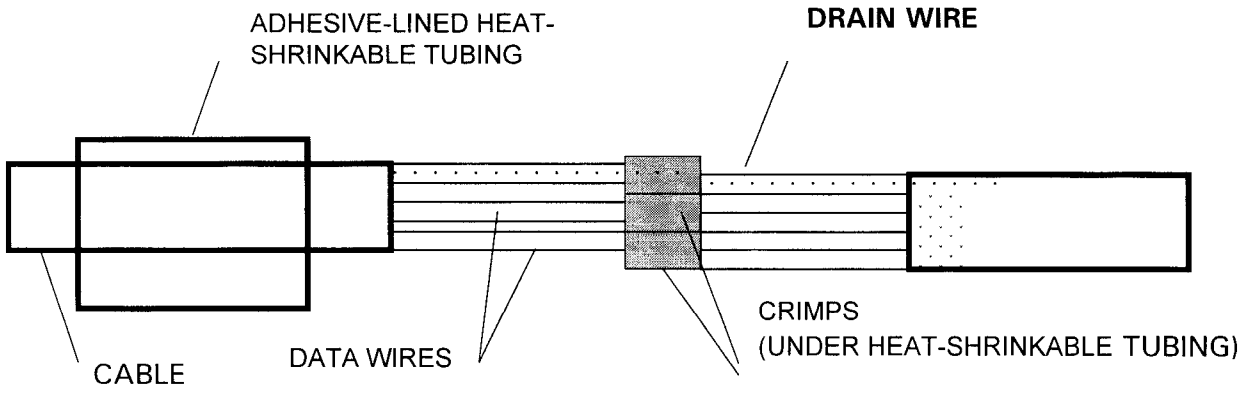


FIGURE D1 - CABLE REPAIR[3]

1. Cut the end of the cables cleanly. Measure back 40 mm to 100 mm and mark the cable jacket. Remove this section of cable jacket.
2. Strip the insulation of both data wires back approximately 6 mm.
3. Repeat this procedure for the other cable.
4. Install one end of a crimp on each of the data wires and drain wire on either cable.
5. Slide the (2) pieces of insulating heat-shrinkable tubing over the crimps and onto the data wires.
6. Slide the (1) piece of adhesive-lined heat-shrinkable tubing onto the cable.

   Insert the wires from the other cable into the appropriate crimp and install the crimp, maintaining polarity (CAN-H, CAN-L).
7. Center the insulating heat-shrinkable tubing over the two crimps and install the tubing per the manufacturer's recommendation.
8. Apply the replacement EMC shielding material per the manufacturer's recommendation.

   Center the adhesive-lined heat-shrinkable tubing over the assembly and apply per manufacturer's recommendation.

FIGURE D2 - CABLE SPLICE-FINISHED ASSEMBLY

[3] Shielding material not shown.