DSD Final Checkpoint Scores

1. Baseline

(1) Area: (um^2)

截圖: Total cell area = 245036.661605

```
    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1836
Number of nets:                         19467
Number of cells:                        18118
Number of combinational cells:          13986
Number of sequential cells:              4121
Number of macros/black boxes:               0
Number of buf/inv:                       4009
Number of references:                       8

Combinational area:             131351.600835
Buf/Inv area:                    25065.505862
Noncombinational area:          113685.060770
Macro/Black Box area:                0.000000
Net Interconnect area:         2342072.052460

Total cell area:                245036.661605
Total area:                    2587108.714064

Hierarchical area distribution
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                                Global cell area          Local cell area
                                ----------------  ------------------------------
Hierarchical cell               Absolute  Percent Combi-    Noncombi-   Black-
                                Total     Total   national  national    boxes   Design
------------------------------  --------  ------- --------  ----------  ------  --------------
CHIP                            245036.6616 100.0  1340.9460      0.0000  0.0000  CHIP
D_cache                          74712.7576  30.5 37451.4334  37261.3242  0.0000  D_cache
I_cache                          63579.5107  25.9 26552.4276  37027.0830  0.0000  I_cache
i_RISCV                         105403.4473  43.0 49935.8107  39396.6535  0.0000  RISCV_Pipeline
i_RISCV/alu_u                    14864.1318   6.1 14864.1318      0.0000  0.0000  ALU
i_RISCV/cpr                       1206.8514   0.5  1206.8514      0.0000  0.0000  comparator
------------------------------  --------  ------- --------  ----------  ------  --------------
Total                                             131351.6008 113685.0608 0.0000
```

(2) Total Simulation Time of given noHazard testbench: (ns)

截圖: 1088.490 ns

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

*Verdi* Loading libsscore_vcs202206.so
FSDB Dumper for VCS, Release Verdi_T-2022.06, Linux x86_64/64bit, 05/29/2022
(C) 1996 - 2022 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
------------------------- Simulation FINISH !! -------------------------
======================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

======================================================================
$finish called from file "Final_tb.v", line 222.
$finish at simulation time             1088490
          V C S   S i m u l a t i o n   R e p o r t
Time: 1088490 ps
CPU Time:      1.550 seconds;       Data structure size:   4.6Mb
Wed May 28 22:09:40 2025
CPU time: 4.192 seconds to compile + 1.654 seconds to elab + 1.172 seconds to link + 1.607 seconds in simulation
```

(3) Total Simulation Time of given hasHazard testbench: (ns)

截圖: 9187.490 ns

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

*Verdi* Loading libsscore_vcs202206.so
FSDB Dumper for VCS, Release Verdi_T-2022.06, Linux x86_64/64bit, 05/29/2022
(C) 1996 - 2022 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
------------------------- Simulation FINISH !! -------------------------
======================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

======================================================================
$finish called from file "Final_tb.v", line 222.
$finish at simulation time              9187490
           V C S   S i m u l a t i o n   R e p o r t
Time: 9187490 ps
CPU Time:      9.000 seconds;       Data structure size:   4.6Mb
Wed May 28 22:09:20 2025
CPU time: 4.615 seconds to compile + 1.495 seconds to elab + 1.022 seconds to link + 9.061 seconds in simulation
```

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)
3.49 ns

```
1  // this is a test bench feeds initial instruction and data
2  // the processor output is not verified
3
4  `timescale 1 ns/10 ps
5
6  `define CYCLE 3.49 // You can modify your clock frequency
7  `define MAX_CYCLES 10000000 // Max cycle count to stop the simulaiton. You can modify it
8
9  `define SDFFILE   "./Netlist/CHIP_syn.sdf"  // Modify your SDF file name
```