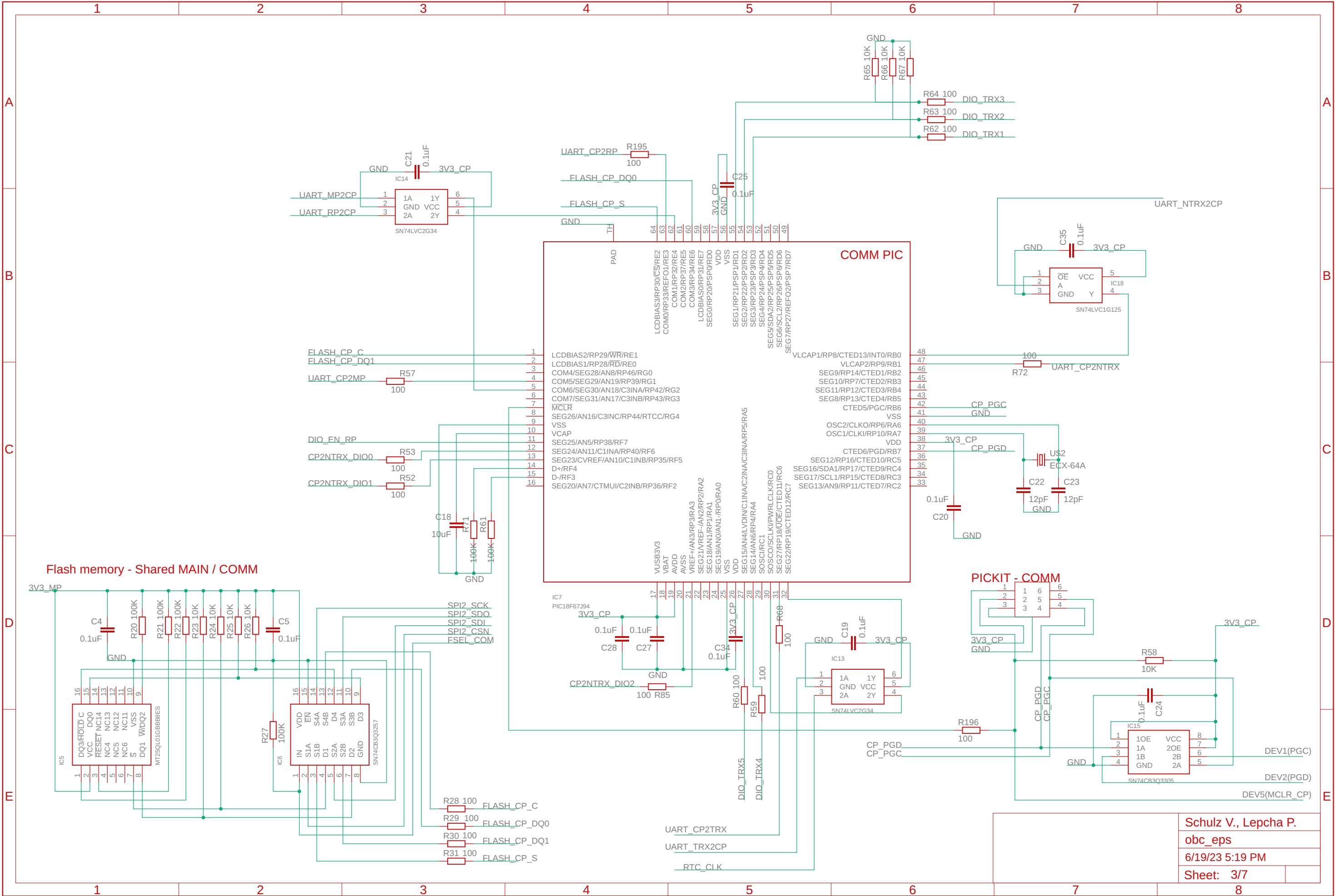


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OBC</div><div>JP3</div><table><tr><td>DEV1(PGC)</td><td>1</td><td>2</td><td>2</td><td>DEV2(PGD)</td></tr><tr><td>OBC_GPIO_3</td><td>3</td><td>3</td><td>4</td><td>DEV4(MCLR_RP)</td></tr><tr><td>DEV5(MCLR_CP)</td><td>5</td><td>5</td><td>6</td><td>DEV6(MCLR_MP)</td></tr><tr><td>UART_TRX2CP</td><td>7</td><td>7</td><td>8</td><td>UART_CP2TRX</td></tr><tr><td>OBC_GPIO_0</td><td>9</td><td>9</td><td>10</td><td>OBC_GPIO_1</td></tr><tr><td>OBC_GPIO_2</td><td>11</td><td>11</td><td>12</td><td>DEV12(MCLR_SP)</td></tr><tr><td>GND</td><td>13</td><td>14</td><td>14</td><td>GND</td></tr><tr><td>5V0</td><td>15</td><td>13</td><td>16</td><td>5V0</td></tr><tr><td>UART_MP2DBG</td><td>17</td><td>15</td><td>16</td><td>UART_DBG2MP</td></tr><tr><td>UART_MP2FAB</td><td>19</td><td>17</td><td>18</td><td>UART_FAB2MP</td></tr><tr><td>OBC_GPIO_4</td><td>21</td><td>19</td><td>20</td><td>OBC_GPIO_5</td></tr><tr><td>UNREG1</td><td>23</td><td>21</td><td>22</td><td>UNREG1</td></tr><tr><td>3V3_2</td><td>25</td><td>23</td><td>24</td><td>3V3_2</td></tr><tr><td>OBC_GPIO_6</td><td>27</td><td>25</td><td>26</td><td>OBC_GPIO_7</td></tr><tr><td>RAW_POWER</td><td>29</td><td>27</td><td>28</td><td>RAW_POWER</td></tr><tr><td>SPI_CSn_FM2MSN</td><td>31</td><td>29</td><td>30</td><td>SPI_SDO_FM2MSN</td></tr><tr><td>SPI_SDI_FM2MSN</td><td>33</td><td>31</td><td>32</td><td>SPI_SCK_FM2MSN</td></tr><tr><td>UNREG2</td><td>35</td><td>33</td><td>34</td><td>UNREG2</td></tr><tr><td>OBC_GPIO_8</td><td>37</td><td>35</td><td>36</td><td>CP2NTRX_DIO2</td></tr><tr><td>KILL_OBC</td><td>39</td><td>37</td><td>38</td><td>UART_CP2NTRX</td></tr><tr><td>UART_NTRX2CP</td><td>41</td><td>39</td><td>40</td><td>CP2NTRX_DIO0</td></tr><tr><td>CP2NTRX_DIO1</td><td>43</td><td>41</td><td>42</td><td>DIO_TRX1</td></tr><tr><td>DIO_TRX2</td><td>45</td><td>43</td><td>44</td><td>DIO_TRX3</td></tr><tr><td>DIO_TRX4</td><td>47</td><td>45</td><td>46</td><td>DIO_TRX5</td></tr><tr><td>3V3_1</td><td>49</td><td>47</td><td>48</td><td>3V3_1</td></tr><tr><td></td><td>49</td><td>49</td><td>50</td><td></td></tr></table><div>A3B-50PA-2DS(71)</div></div><div><table><tr><th>BIRDS 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Name	BIRDS Name	DEV1(PGC)	DEV1(PGC)	CPLD_IO_OBC12		DEV5(MCLR_CP)	DEV5(MCLR_CP)	UART_TRX2CP	UART_TRX2CP	DIO_OBC0	DIO_OBC0	DIO_OBC2	DIO_OBC2	GND_SYS	GND_SYS	5V0	5V0	UART_MP2DBG	UART_TX_EXT	UART_MP2FAB	UART_MP2FAB	CPLD_IO_OBC08	CPLD_IO_OBC08	UNREG1	UNREG1	3V3-2	3V3-2	CPLD_IO_OBC10	CPLD_IO_OBC10	RAW_POWER	RAW_POWER	SPI_CSn_FM2MSN	SPI_CSn_FM2MSN	SPI_SDI_FM2MSN	SPI_SDI_FM2MSN	UNREG2	UNREG2	CPLD_IO_OBC16	CPLD_IO_OBC16	KILL_OBC	KILL_OBC	DIO_TRX7		DIO_TRX0	DIO_TRX0	DIO_TRX2	DIO_TRX2	DIO_TRX4	DIO_TRX4	3V3-1	3V3-1	DEV1(PGC)	1	2	2	DEV2(PGD)	OBC_GPIO_3	3	3	4	DEV4(MCLR_RP)	DEV5(MCLR_CP)	5	5	6	DEV6(MCLR_MP)	UART_TRX2CP	7	7	8	UART_CP2TRX	OBC_GPIO_0	9	9	10	OBC_GPIO_1	OBC_GPIO_2	11	11	12	DEV12(MCLR_SP)	GND	13	14	14	GND	5V0	15	13	16	5V0	UART_MP2DBG	17	15	16	UART_DBG2MP	UART_MP2FAB	19	17	18	UART_FAB2MP	OBC_GPIO_4	21	19	20	OBC_GPIO_5	UNREG1	23	21	22	UNREG1	3V3_2	25	23	24	3V3_2	OBC_GPIO_6	27	25	26	OBC_GPIO_7	RAW_POWER	29	27	28	RAW_POWER	SPI_CSn_FM2MSN	31	29	30	SPI_SDO_FM2MSN	SPI_SDI_FM2MSN	33	31	32	SPI_SCK_FM2MSN	UNREG2	35	33	34	UNREG2	OBC_GPIO_8	37	35	36	CP2NTRX_DIO2	KILL_OBC	39	37	38	UART_CP2NTRX	UART_NTRX2CP	41	39	40	CP2NTRX_DIO0	CP2NTRX_DIO1	43	41	42	DIO_TRX1	DIO_TRX2	45	43	44	DIO_TRX3	DIO_TRX4	47	45	46	DIO_TRX5	3V3_1	49	47	48	3V3_1		49	49	50		BIRDS Name	KITSUNE Name	DEV2(PGD)	DEV2(PGD)	DEV4(MCLR_RP)	DEV4(MCLR_RP)	DEV6(MCLR_MP)	DEV6(MCLR_MP)	UART_CP2TRX	UART_CP2TRX	DIO_OBC1	DIO_OBC1	DIO_OBC3	DIO_OBC3	GND_SYS	GND_SYS	5V0	5V0	UART_RX_EXT	UART_DBG2MP	UART_FAB2MP	UART_FAB2MP	CPLD_IO_OBC09	CPLD_IO_OBC09	UNREG1	UNREG1	3V3-2	3V3-2	CPLD_IO_OBC11	CPLD_IO_OBC11	RAW_POWER	RAW_POWER	SPI_SDO_FM2MSN	SPI_SDO_FM2MSN	SPI_SCK_FM2MSN	SPI_SCK_FM2MSN	UNREG2	UNREG2	CPLD_IO_OBC17	CPLD_IO_OBC17		DIO_TRX6	CPLD_IO_OBC18	CPLD_IO_OBC18	DIO_TRX1	DIO_TRX1	DIO_TRX3	DIO_TRX3	DIO_TRX5	DIO_TRX5	3V3-1	3V3-1	C
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