Report Generated by Test Manager

Title: **Horloge_Interne_Test**
Author: **Khalid Bouzrhaiba**
Date: **12-Aug-2024 17:22:50**

Test Environment

Platform: PCWIN64
MATLAB: (R2023a)

Summary

Name	Outcome	Duration (Seconds)
Results: 2024-Aug-12 17:21:03	10 ✓	35.588
Horloge_interne_v3	10 ✓	34.864
Horloge_interne_v3/Horloge_Interne	✓	3.744
Horloge_interne_v3_Harness	✓	3.744
Horloge_interne_v3/Horloge_Interne/Changes_Interval	✓	2.231
CHANGES	✓	2.232
Horloge_interne_v3/Horloge_Interne/Day_adjustment/CD_when_Month//Year_overflows	✓	2.38
CD_6	✓	2.381
Horloge_interne_v3/Horloge_Interne/Day_adjustment/Subsystem2	✓	2.807
CD_5	✓	2.806
Horloge_interne_v3/Horloge_Interne/Hour_adjustment	✓	1.714
CHANGED_HOUR2	✓	1.714
Horloge_interne_v3/Horloge_Interne/Last_Day_of_Month	✓	1.86
Last_Day_Month_scenario2	✓	1.859
Horloge_interne_v3/Horloge_Interne/Leap_Year	✓	2.046
Leap_scenario1	✓	2.045
Horloge_interne_v3/Horloge_Interne/MATLAB Function1	✓	4.513
CYN_remD2	✓	4.512
Horloge_interne_v3/Horloge_Interne/MN_from_DN	✓	3.116

AM_2	✓	3.116
Horloge_interne_v3/Horloge_Interne/H_var_State1	✓	2.232
DN_LDY_V1	✓	2.232

Results: 2024-Aug-12 17:21:03

Result Type: Result Set
Parent: None
Start Time: 12-Aug-2024 17:21:04
End Time: 12-Aug-2024 17:21:40
Outcome: Total: 10, Passed: 10

Aggregated Coverage Results

Analyzed Model	Sim Mode	Complexity	Decision	Condition	MCDC	Execution
Horloge_interne_v3/Horloge_Interne	Normal	49	100%	100%	100%	100%
Horloge_interne_v3/Horloge_Interne/Changes_Interval	Normal	4	100%	100%	--	100%
Horloge_interne_v3/Horloge_Interne/Day_adjustment/CD_when_Month//Year_overflows	Normal	0	--	--	--	--
Horloge_interne_v3/Horloge_Interne/Hour_adjustment	Normal	4	100%	--	--	100%
Horloge_interne_v3/Horloge_Interne/Day_adjustment/Subsystem2	Normal	0	--	--	--	100%
Horloge_interne_v3/Horloge_Interne/Last_Day_of_Month	Normal	2	100%	--	--	100%
Horloge_interne_v3/Horloge_Interne/Leap_Year	Normal	2	100%	100%	100%	100%
Horloge_interne_v3/Horloge_Interne/MATLAB Function1	Normal	7	100%	100%	100%	--
Horloge_interne_v3/Horloge_Interne/MN_from_DN	Normal	13	100%	100%	100%	100%
Horloge_interne_v3/Horloge_Interne/H_var_State1	Normal	5	100%	100%	--	100%

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Horloge_interne_v3

Test Result Information

Result Type: Test File Result
Parent: Results: 2024-Aug-12 17:21:03

Start Time:	12-Aug-2024 17:21:04
End Time:	12-Aug-2024 17:21:39
Outcome:	Total: 10, Passed: 10

Test Suite Information

Name:	Horloge_interne_v3

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Horloge_interne_v3/Horloge_Interne

Test Result Information

Result Type:	Test Suite Result
Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:04
End Time:	12-Aug-2024 17:21:08
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne

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Horloge_interne_v3_Harness

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne
Start Time:	12-Aug-2024 17:21:04
End Time:	12-Aug-2024 17:21:08
Outcome:	Passed

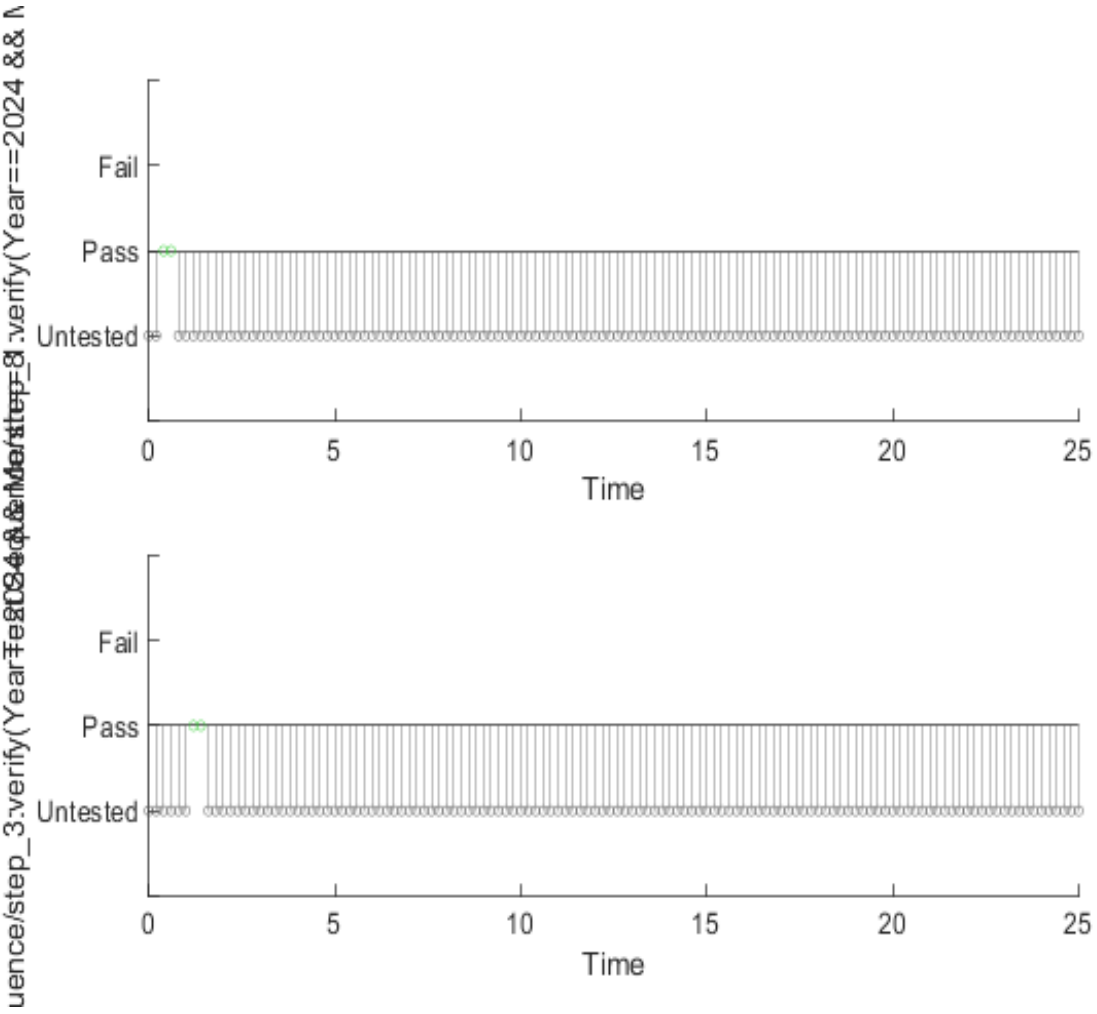
Test Case Information

Name:	Horloge_interne_v3_Harness
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(Year==2024 && Month==8 && Day==1 && Hour==9 && Minute==1)	Link
Test Sequence/step_3:verify(Year==2024 && Month==8 && Day==2 && Hour==4 && Minute==1)	Link
Test Sequence/step_5:verify(Year==2024 && Month==8 && Day==5 && Hour==13 && Minute==1)	Link
Test Sequence/step_7:verify(Year==2024 && Month==8 && Day==31 && Hour==23 && Minute==1)	Link
Test Sequence/step_9:verify(Year==2024 && Month==9 && Day==1 && Hour==0 && Minute==1)	Link
Test Sequence/step_11:verify(Year==2024 && Month==10 && Day==23 && Hour==17 && Minute==1)	Link
Test Sequence/step_13:verify(Year==2024 && Month==3 && Day==20 && Hour==5 && Minute==1)	Link
Test Sequence/step_15:verify(Year==2025 && Month==1 && Day==1 && Hour==0 && Minute==1)	Link
Test Sequence/step_17:verify(Year==2025 && Month==2 && Day==28 && Hour==23 && Minute==1)	Link
Test Sequence/step_19:verify(Year==2025 && Month==3 && Day==1 && Hour==0 && Minute==1)	Link
Test Sequence/step_21:verify(Year==2138 && Month==8 && Day==31 && Hour==1 && Minute==1)	Link
Test Sequence/step_23:verify(Year==2025 && Month==1 && Day==1 && Hour==1 && Minute==1)	Link
Test Sequence/step_25:verify(Year==2024 && Month==2 && Day==11 && Hour==17 && Minute==1)	Link
Test Sequence/step_27:verify(Year==2024 && Month==3 && Day==3 && Hour==13 && Minute==1)	Link
Test Sequence/step_29:verify(Year==2024 && Month==4 && Day==14 && Hour==5 && Minute==1)	Link
Test Sequence/step_31:verify(Year==2024 && Month==5 && Day==25 && Hour==21 && Minute==1)	Link
Test Sequence/step_33:verify(Year==2024 && Month==6 && Day==15 && Hour==17 && Minute==1)	Link
Test Sequence/step_35:verify(Year==2024 && Month==7 && Day==27 && Hour==9 && Minute==1)	Link
Test Sequence/step_37:verify(Year==2024 && Month==9 && Day==7 && Hour==1 && Minute==1)	Link
Test Sequence/step_39:verify(Year==2024 && Month==10 && Day==18 && Hour==17 && Minute==1)	Link
Test Sequence/step_41:verify(Year==2024 && Month==11 && Day==29 && Hour==9 && Minute==1)	Link
Test Sequence/step_43:verify(Year==2024 && Month==12 && Day==20 && Hour==5 && Minute==1)	Link
Test Sequence/step_45:verify(Year==2101 && Month==1 && Day==11 && Hour==1 && Minute==1)	Link
Test Sequence/step_47:verify(Year==2025 && Month==8 && Day==1 && Hour==9 && Minute==1)	Link
Test Sequence/step_49:verify(Year==2024&& Month==1 && Day==1 && Hour==9 && Minute==1)	Link
Test Sequence/step_51:verify(Year==2024 && Month==2 && Day==1 && Hour==9 && Minute==1)	Link
Test Sequence/step_53:verify(Year==2025 && Month==2 && Day==1 && Hour==9 && Minute==1)	Link

Name
Test Sequence/step_1:verify(Year==2024 && Month==8 && Day==1 && Hour==9 && Minute==1)
Test Sequence/step_3:verify(Year==2024 && Month==8 && Day==2 && Hour==4 && Minute==1)



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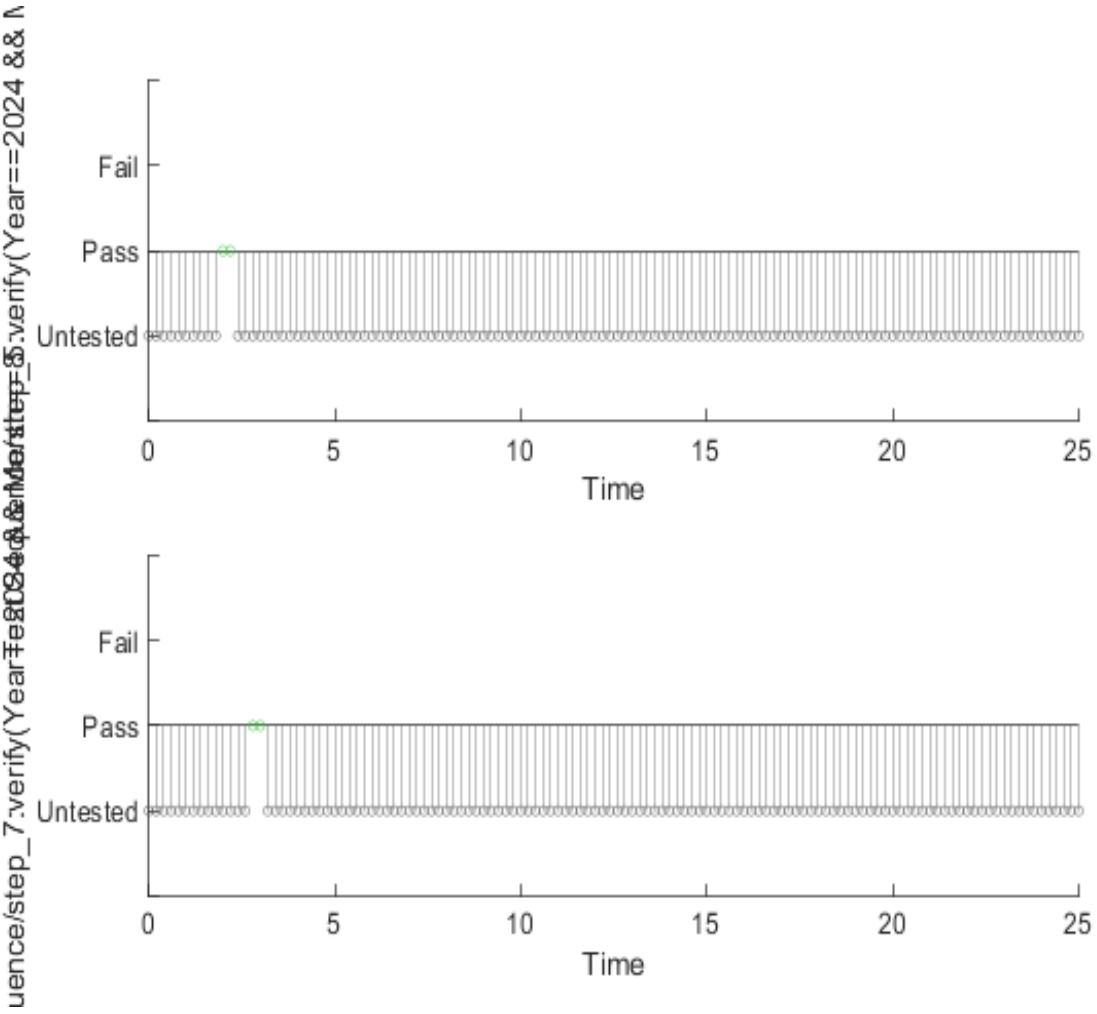
Name
Test Sequence/step_5:verify(Year==2024 && Month==8 && Day==5 && Hour==13 && Minute==1)
Test Sequence/step_7:verify(Year==2024 && Month==8 && Day==31 && Hour==23 && Minute==1)



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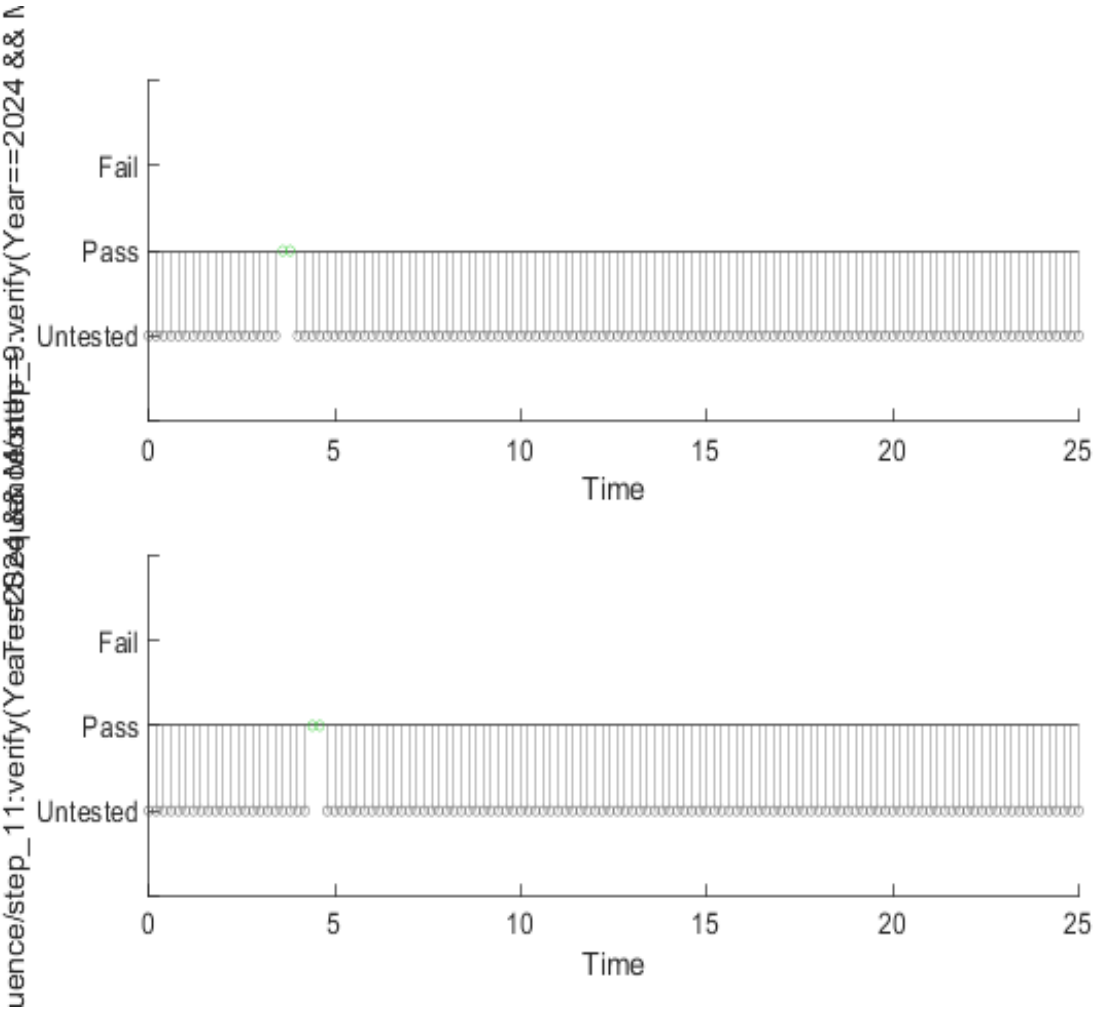
Name
Test Sequence/step_9:verify(Year==2024 && Month==9 && Day==1 && Hour==0 && Minute==1)
Test Sequence/step_11:verify(Year==2024 && Month==10 && Day==23 && Hour==17 && Minute==1)



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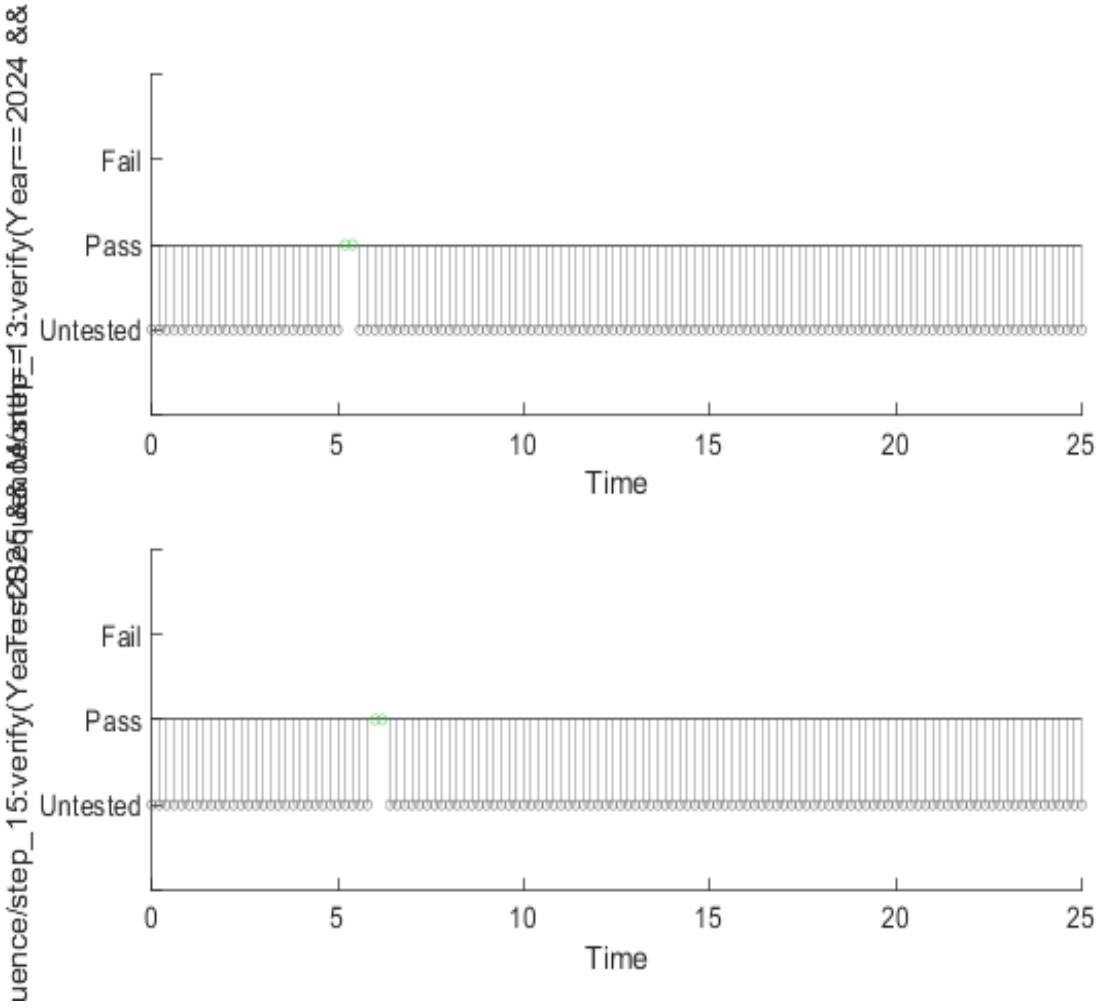
Name
Test Sequence/step_13:verify(Year==2024 && Month==3 && Day==20 && Hour==5 && Minute==1)
Test Sequence/step_15:verify(Year==2025 && Month==1 && Day==1 && Hour==0 && Minute==1)



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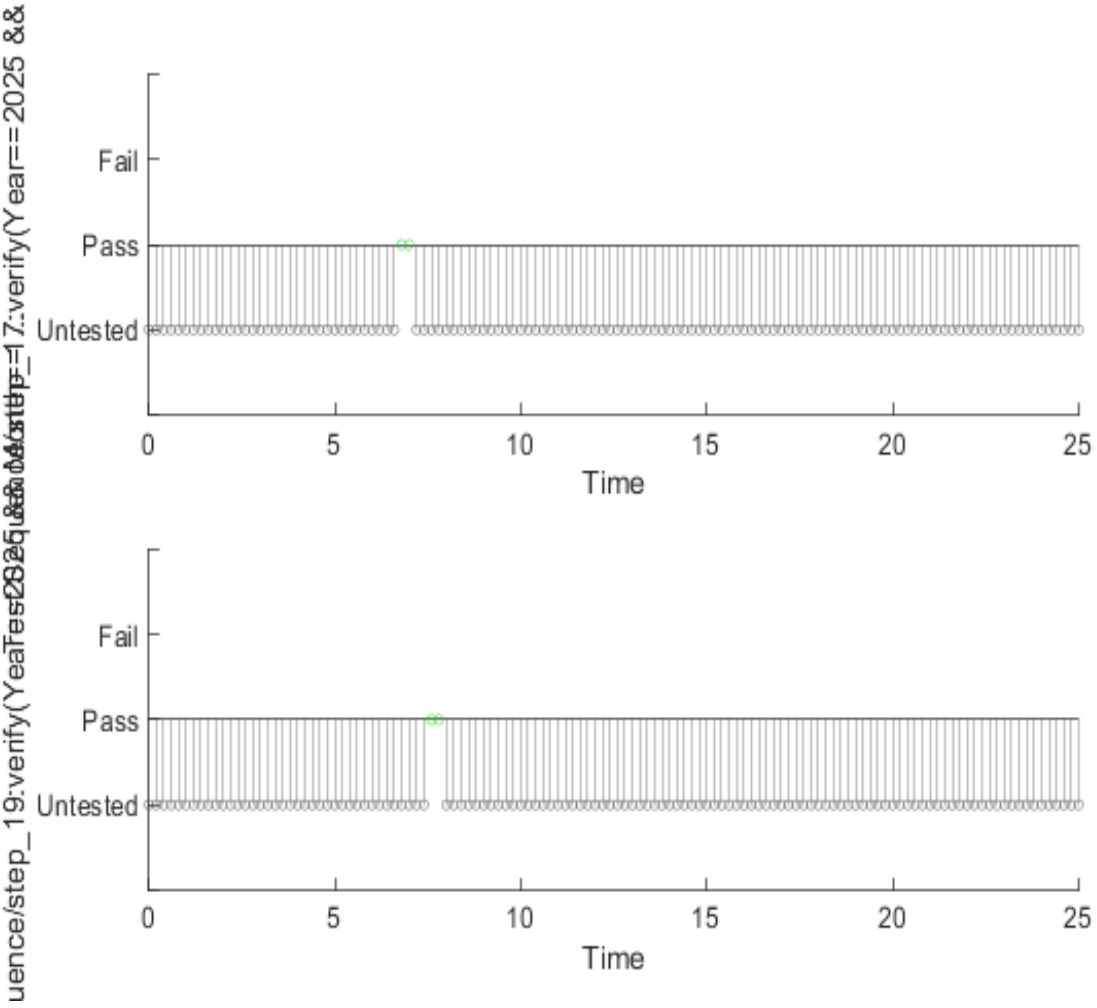
Name
Test Sequence/step_17:verify(Year==2025 && Month==2 && Day==28 && Hour==23 && Minute==1)
Test Sequence/step_19:verify(Year==2025 && Month==3 && Day==1 && Hour==0 && Minute==1)



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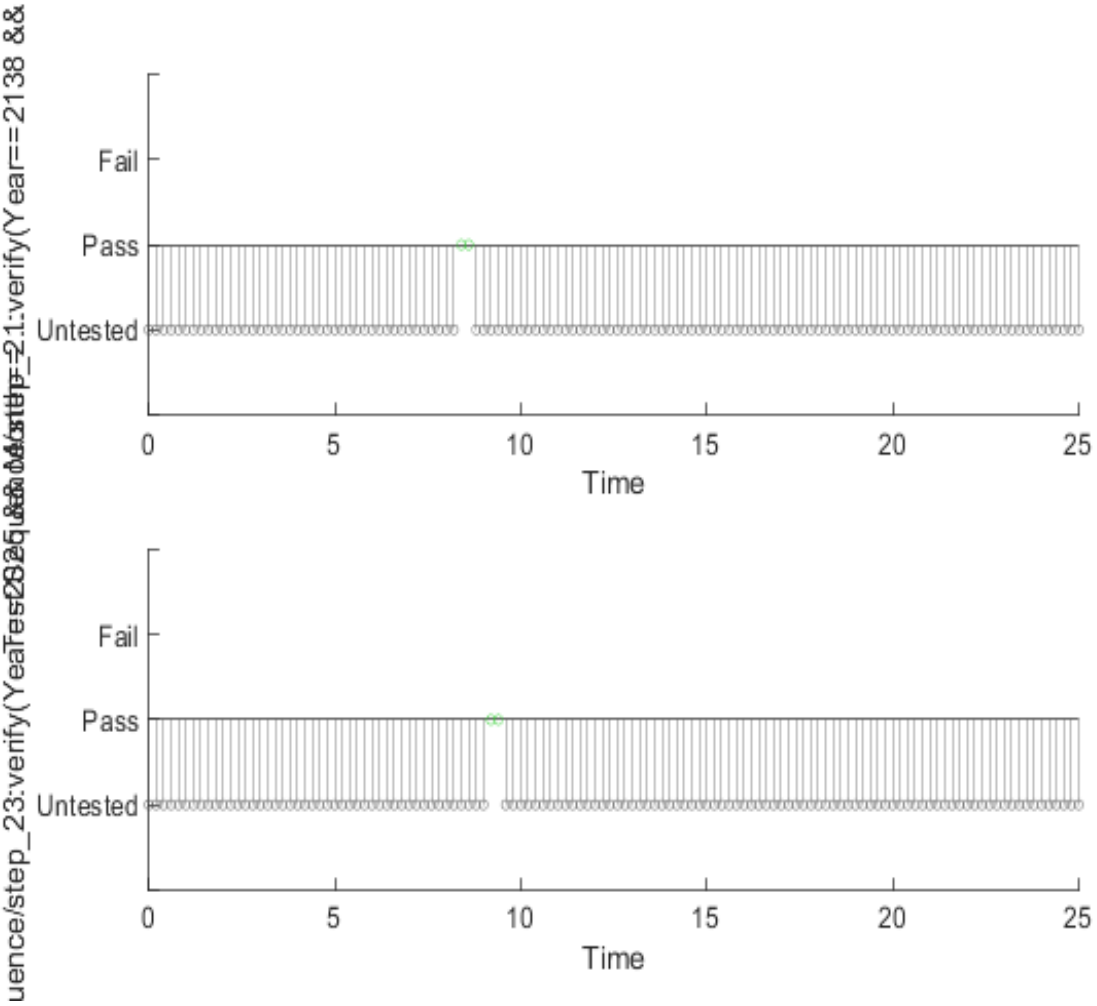
Name
Test Sequence/step_21:verify(Year==2138 && Month==8 && Day==31 && Hour==1 && Minute==1)
Test Sequence/step_23:verify(Year==2025 && Month==1 && Day==1 && Hour==1 && Minute==1)



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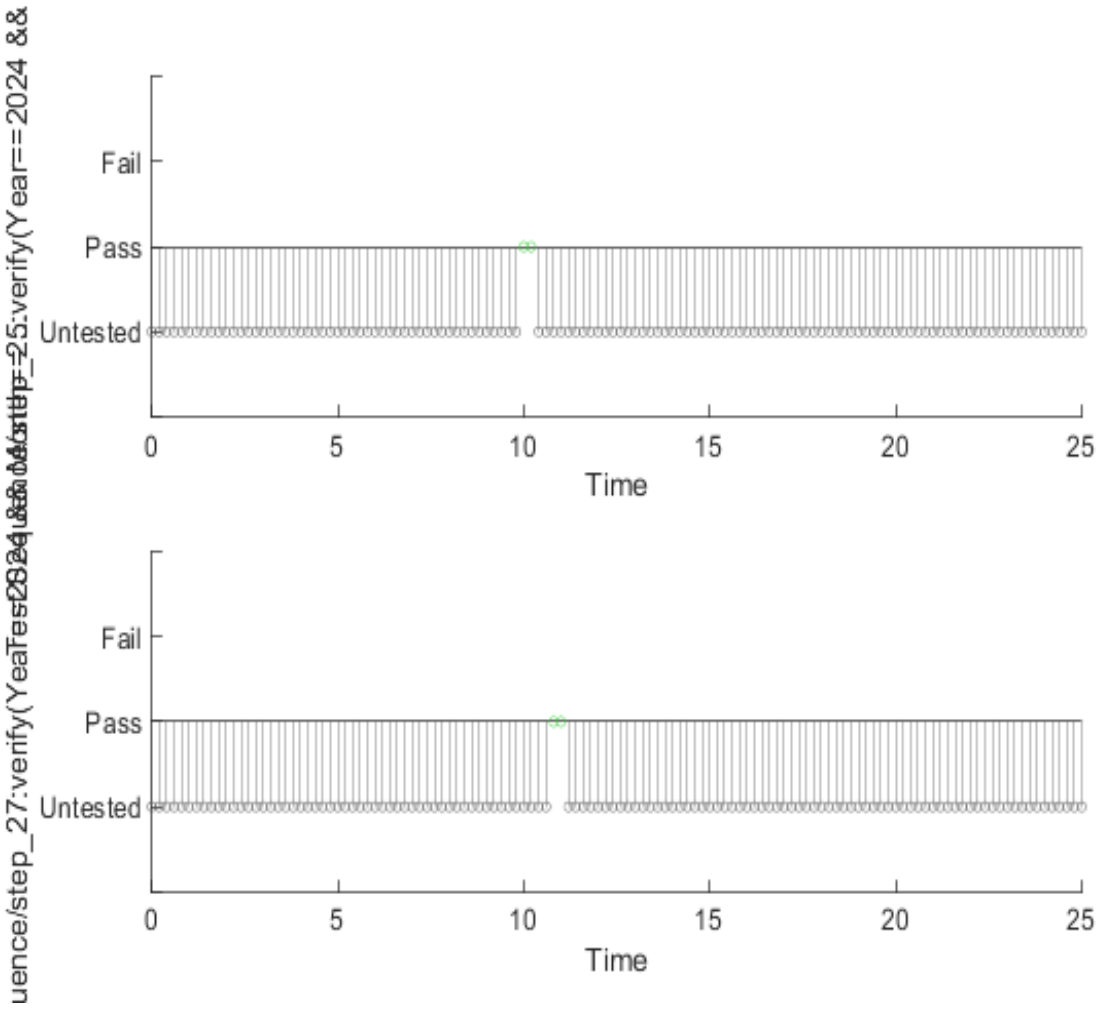
Name
Test Sequence/step_25:verify(Year==2024 && Month==2 && Day==11 && Hour==17 && Minute==1)
Test Sequence/step_27:verify(Year==2024 && Month==3 && Day==3 && Hour==13 && Minute==1)



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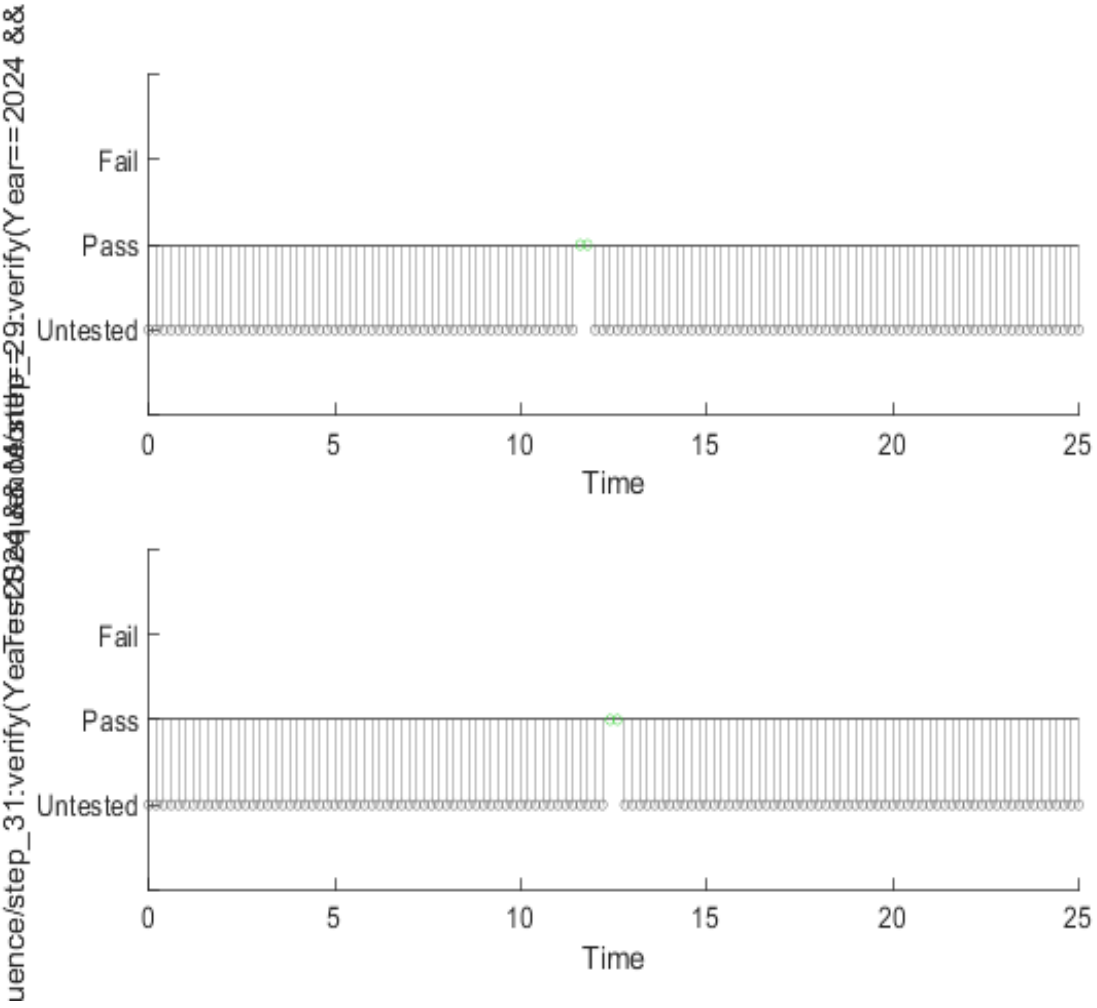
Name
Test Sequence/step_29:verify(Year==2024 && Month==4 && Day==14 && Hour==5 && Minute==1)
Test Sequence/step_31:verify(Year==2024 && Month==5 && Day==25 && Hour==21 && Minute==1)



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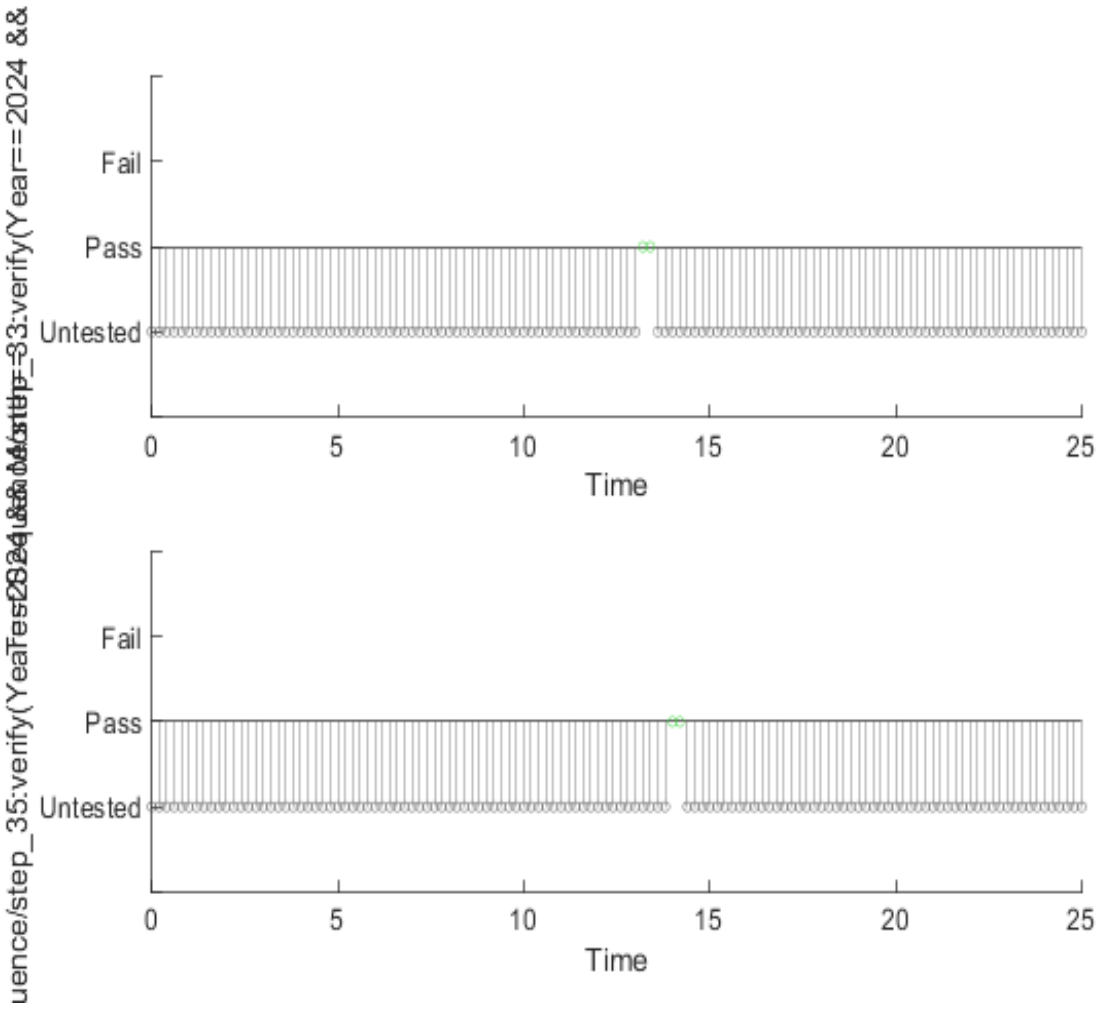
Name
Test Sequence/step_33:verify(Year==2024 && Month==6 && Day==15 && Hour==17 && Minute==1)
Test Sequence/step_35:verify(Year==2024 && Month==7 && Day==27 && Hour==9 && Minute==1)



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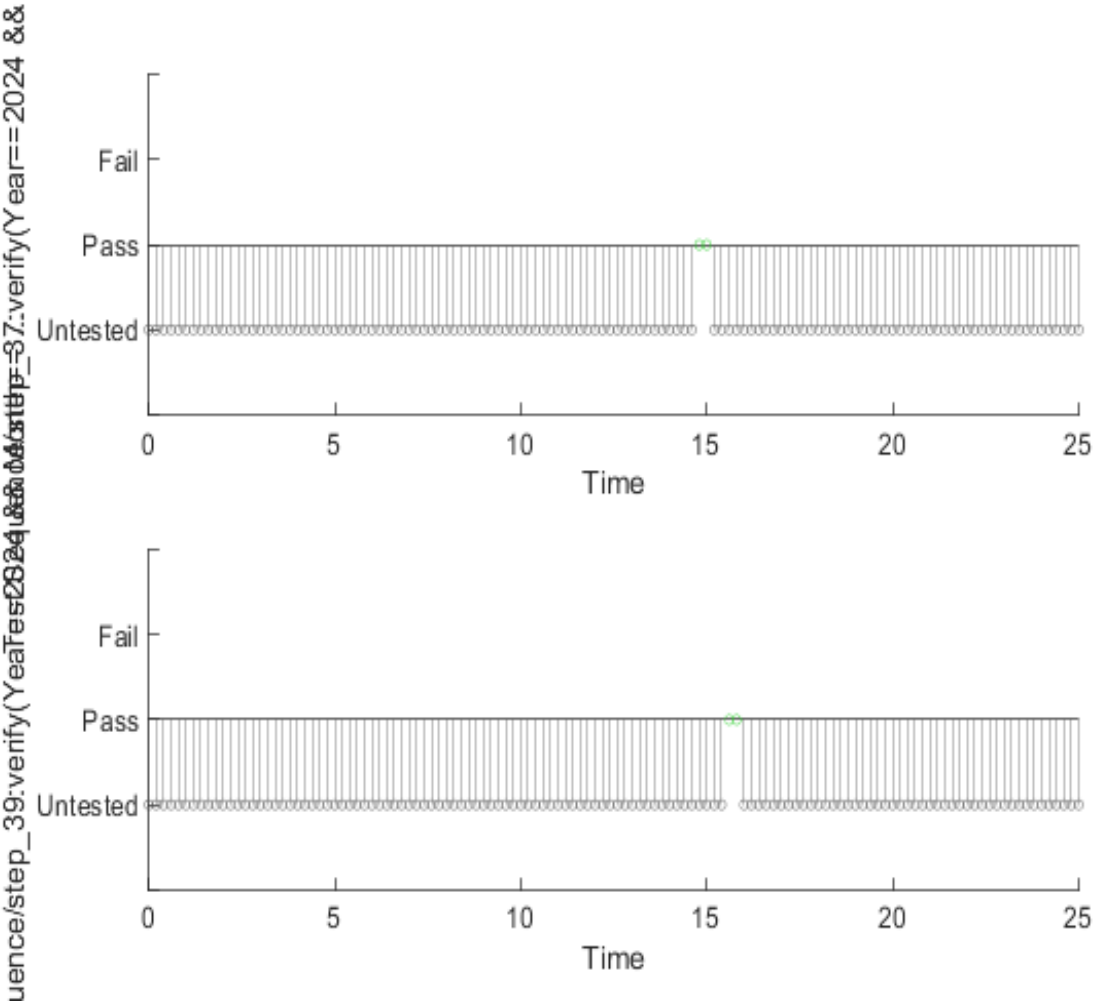
Name
Test Sequence/step_37:verify(Year==2024 && Month==9 && Day==7 && Hour==1 && Minute==1)
Test Sequence/step_39:verify(Year==2024 && Month==10 && Day==18 && Hour==17 && Minute==1)



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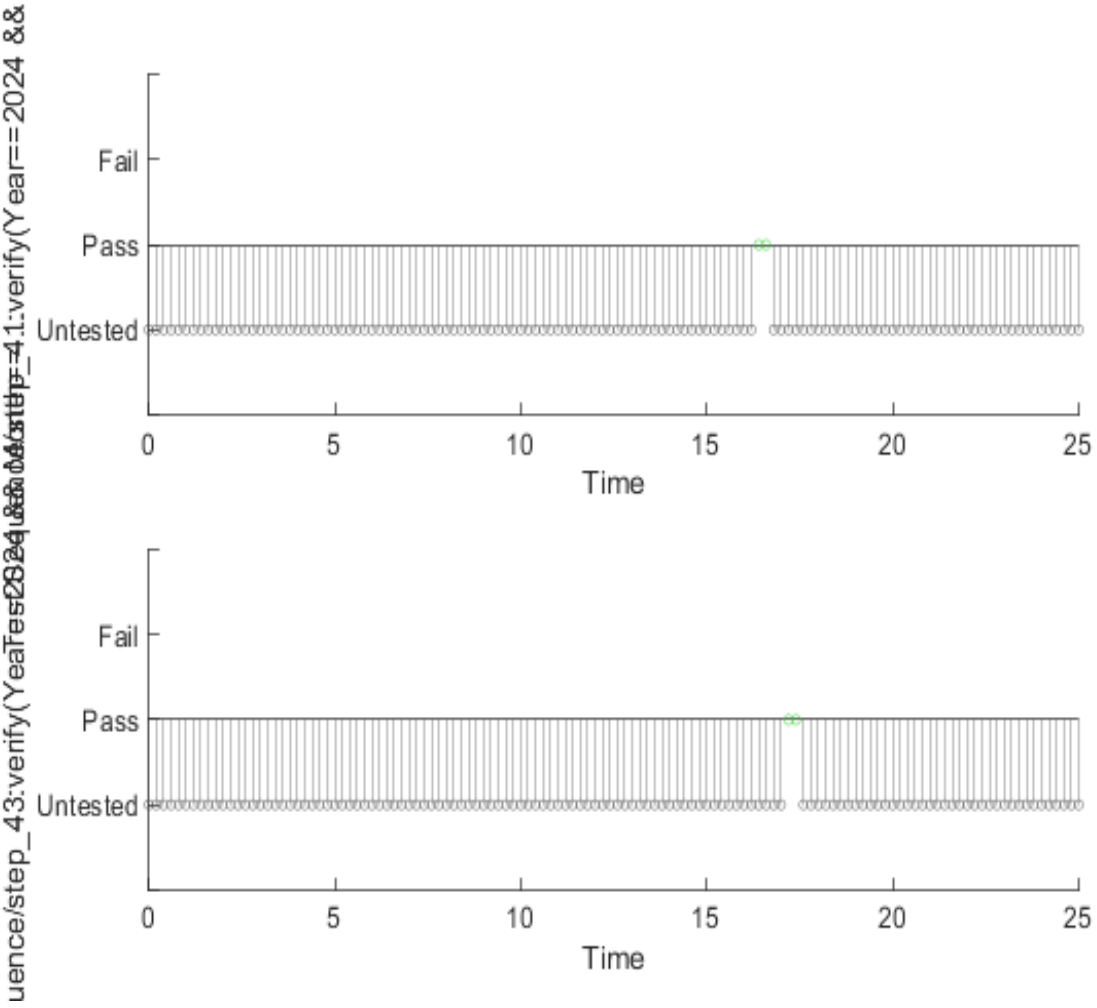
Name
Test Sequence/step_41:verify(Year==2024 && Month==11 && Day==29 && Hour==9 && Minute==1)
Test Sequence/step_43:verify(Year==2024 && Month==12 && Day==20 && Hour==5 && Minute==1)



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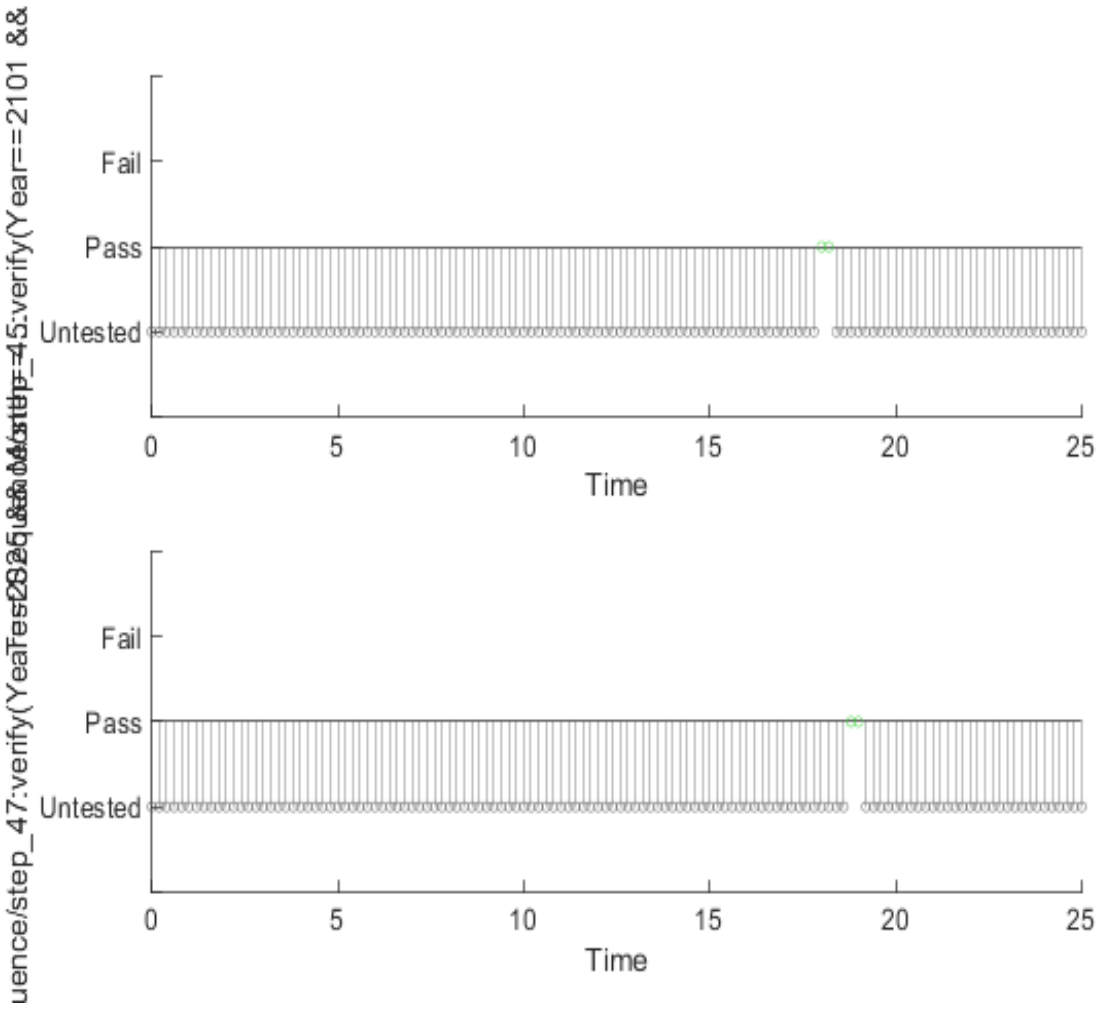
Name
Test Sequence/step_45:verify(Year==2101 && Month==1 && Day==11 && Hour==1 && Minute==1)
Test Sequence/step_47:verify(Year==2025 && Month==8 && Day==1 && Hour==9 && Minute==1)



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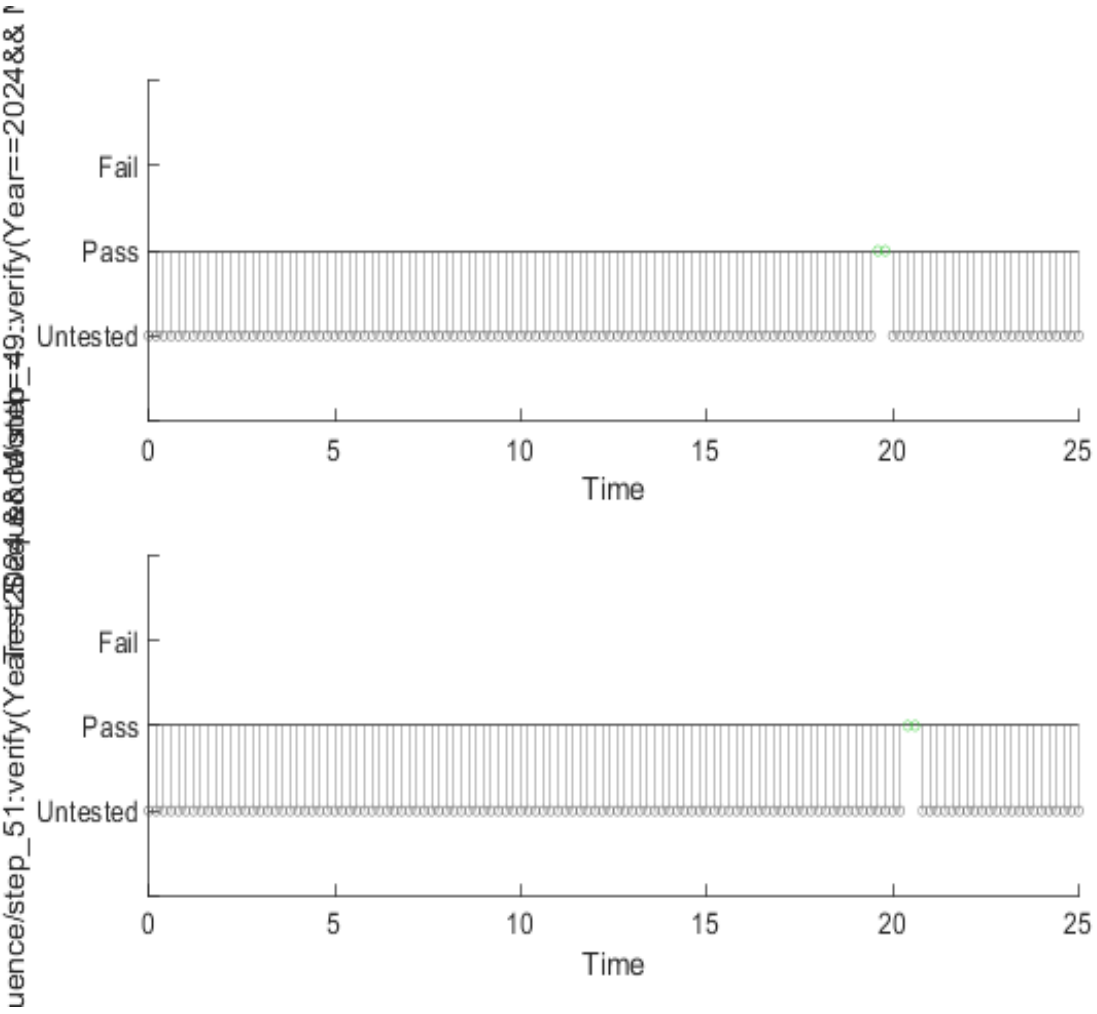
Name
Test Sequence/step_49:verify(Year==2024&& Month==1 && Day==1 && Hour==9 && Minute==1)
Test Sequence/step_51:verify(Year==2024 && Month==2 && Day==1 && Hour==9 && Minute==1)



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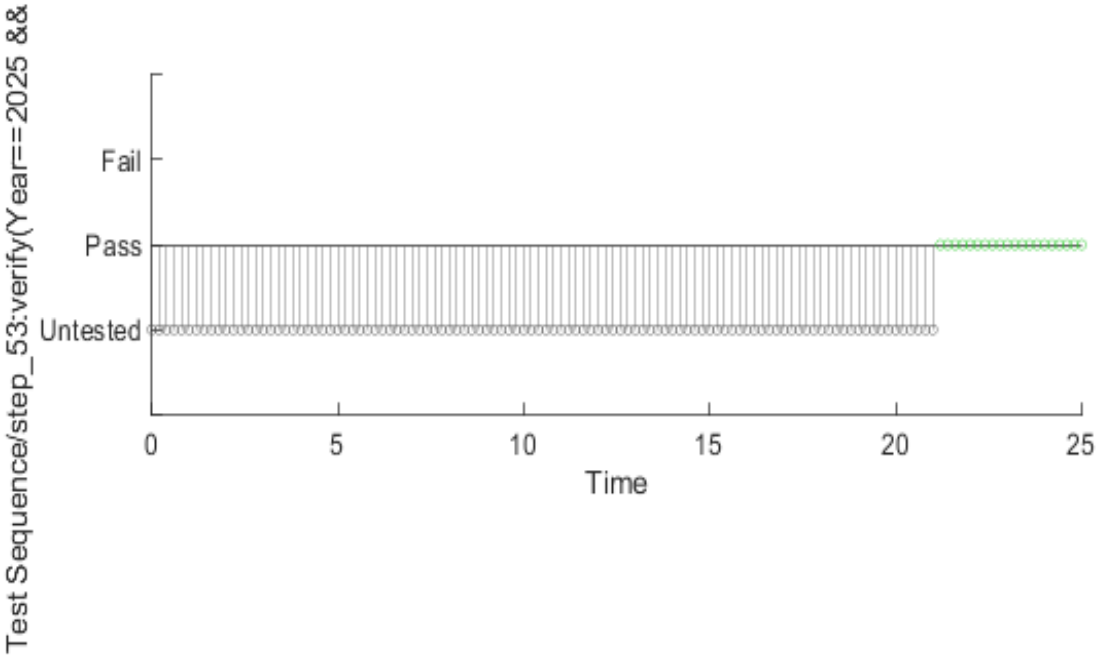
Name
Test Sequence/step_53:verify(Year==2025 && Month==2 && Day==1 && Hour==9 && Minute==1)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	Horloge_interne_v3_Harness
Harness Owner:	Horloge_interne_v3/Horloge_Interne
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	25
Checksum:	2656447006 2138775566 1399288097 391726634
Simulink Version:	10.7
Model Version:	1.9
Model Author:	Khalid-B
Date:	Mon Aug 12 16:49:55 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:04
Simulation Stop Time:	2024-08-12 17:21:07
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ Changes_Interval

Test Result Information

Result Type:	Test Suite Result
Parent:	Horloge_interne_v3

Start Time: 12-Aug-2024 17:21:10
End Time: 12-Aug-2024 17:21:12
Outcome: Total: 1, Passed: 1

Test Suite Information

Name: Horloge_interne_v3/Horloge_Interne/Changes_Interval

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CHANGES

Test Result Information

Result Type: Test Case Result
Parent: Horloge_interne_v3/Horloge_Interne/Changes_Interval
Start Time: 12-Aug-2024 17:21:10
End Time: 12-Aug-2024 17:21:12
Outcome: Passed

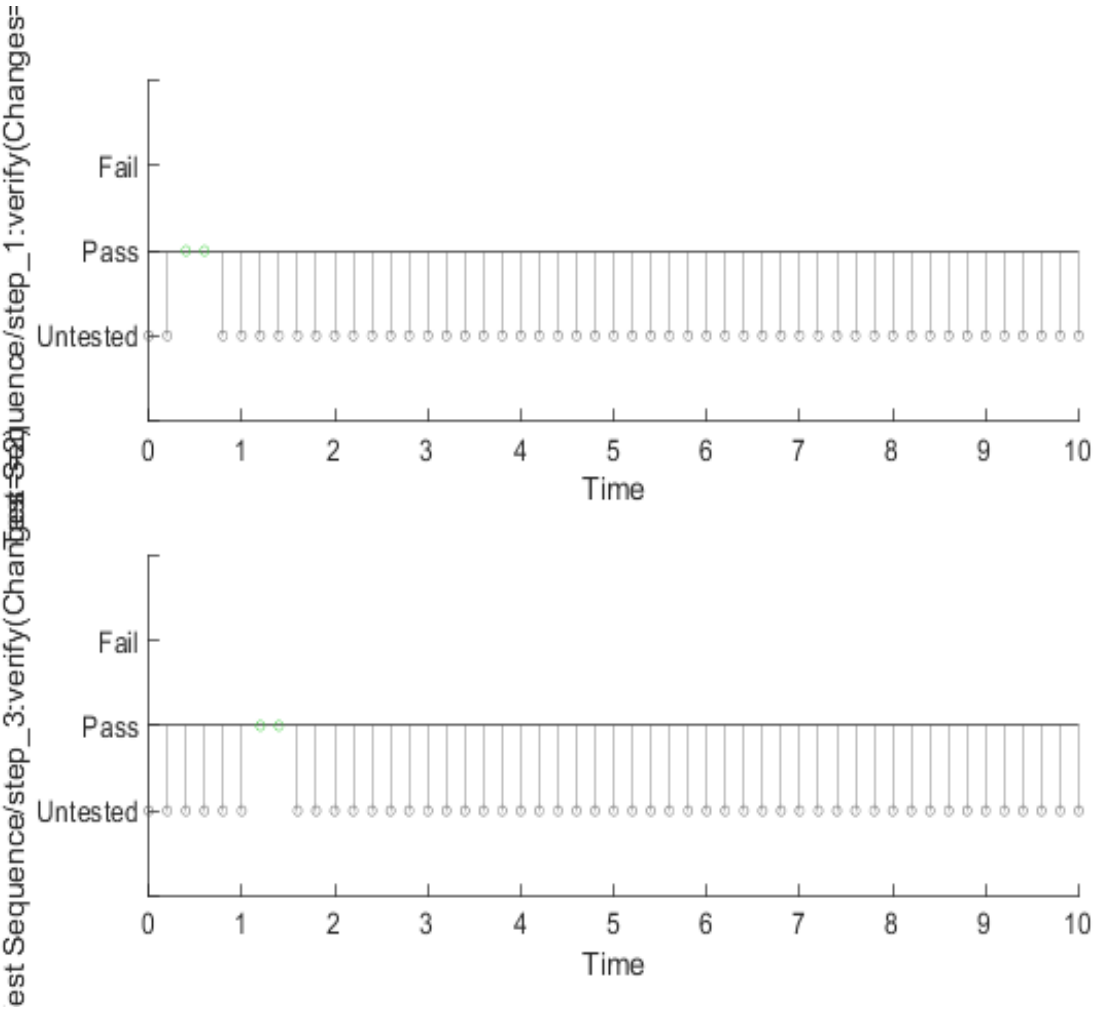
Test Case Information

Name: CHANGES
Type: Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(Changes==1)	Link
Test Sequence/step_3:verify(Changes==2)	Link
Test Sequence/step_5:verify(Changes==3)	Link
Test Sequence/step_7:verify(Changes==4)	Link

Name
Test Sequence/step_1:verify(Changes==1)
Test Sequence/step_3:verify(Changes==2)



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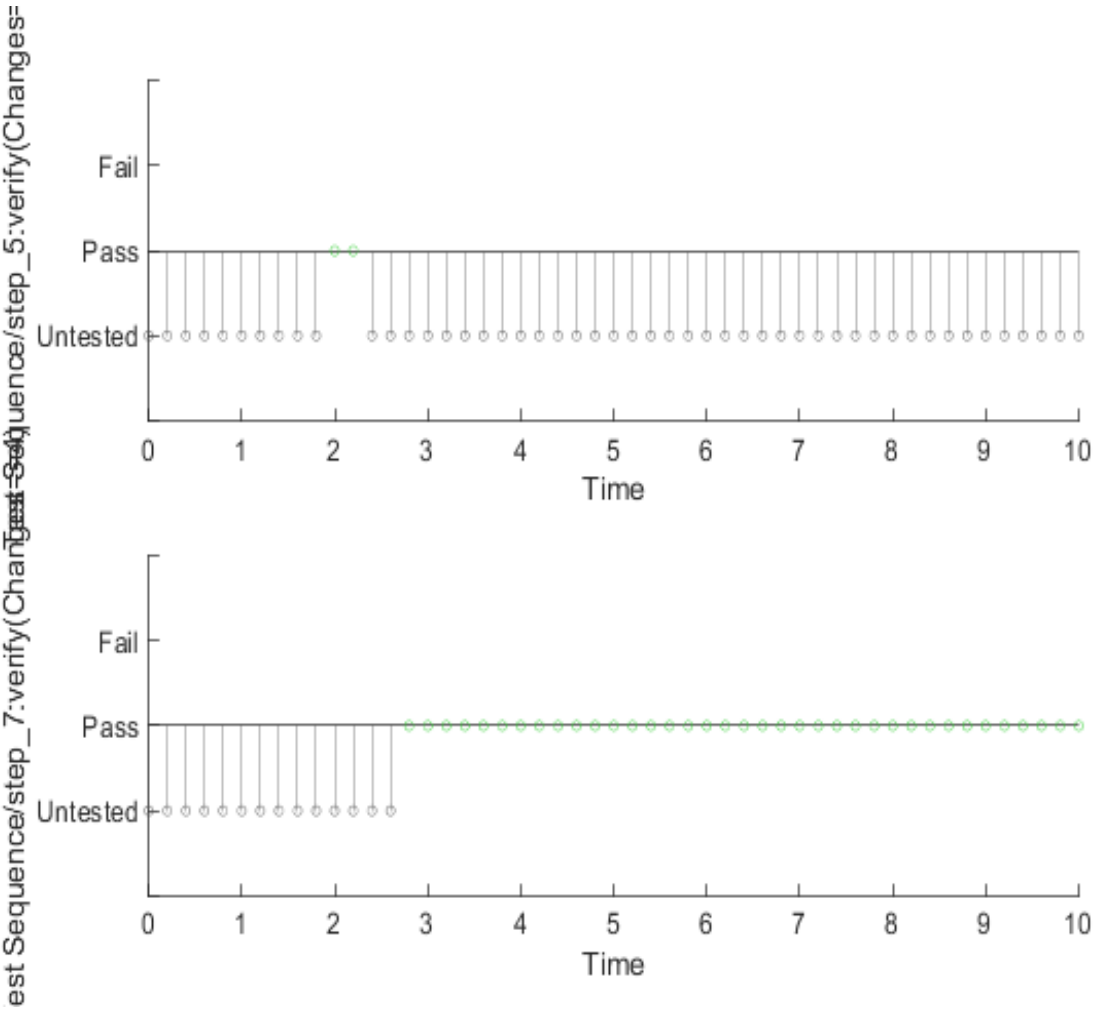
Name
Test Sequence/step_5:verify(Changes==3)
Test Sequence/step_7:verify(Changes==4)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	CHANGES
Harness Owner:	Horloge_interne_v3/Horloge_Interne/ Changes_Interval
Release:	Current

Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	1528038129 2405889979 2876292762 1225159822
Simulink Version:	10.7
Model Version:	1.4
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:43 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:10
Simulation Stop Time:	2024-08-12 17:21:12
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ Day_adjustment/CD_when_Month// Year_overflows

Test Result Information

Result Type:	Test Suite Result
Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:13
End Time:	12-Aug-2024 17:21:15
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/ Day_adjustment/CD_when_Month// Year_overflows

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CD_6

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/ Day_adjustment/CD_when_Month// Year_overflows
Start Time:	12-Aug-2024 17:21:13
End Time:	12-Aug-2024 17:21:15
Outcome:	Passed

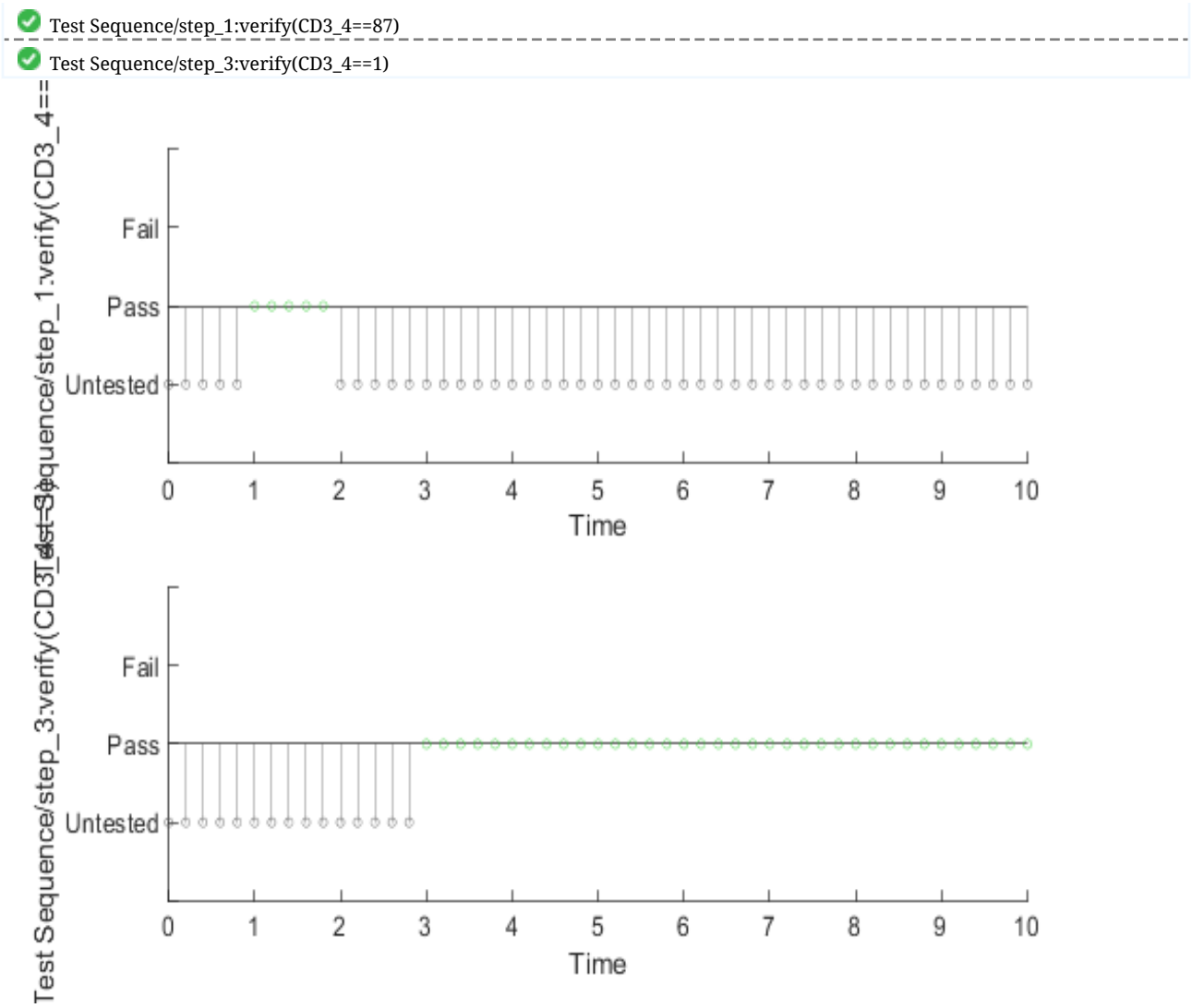
Test Case Information

Name:	CD_6
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(CD3_4==87)	Link
Test Sequence/step_3:verify(CD3_4==1)	Link

Name



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	CD_6

Harness Owner:	Horloge_interne_v3/Horloge_Interne/ Day_adjustment/CD_when_Month// Year_overflows
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	4174866680 603902661 864138931 2435204343
Simulink Version:	10.7
Model Version:	1.14
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:44 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:13
Simulation Stop Time:	2024-08-12 17:21:15
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ Day_adjustment/Subsystem2

Test Result Information

Result Type:	Test Suite Result
Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:16
End Time:	12-Aug-2024 17:21:19
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/ Day_adjustment/Subsystem2

Back to Report Summary

CD_5

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/ Day_adjustment/Subsystem2
Start Time:	12-Aug-2024 17:21:16
End Time:	12-Aug-2024 17:21:19
Outcome:	Passed

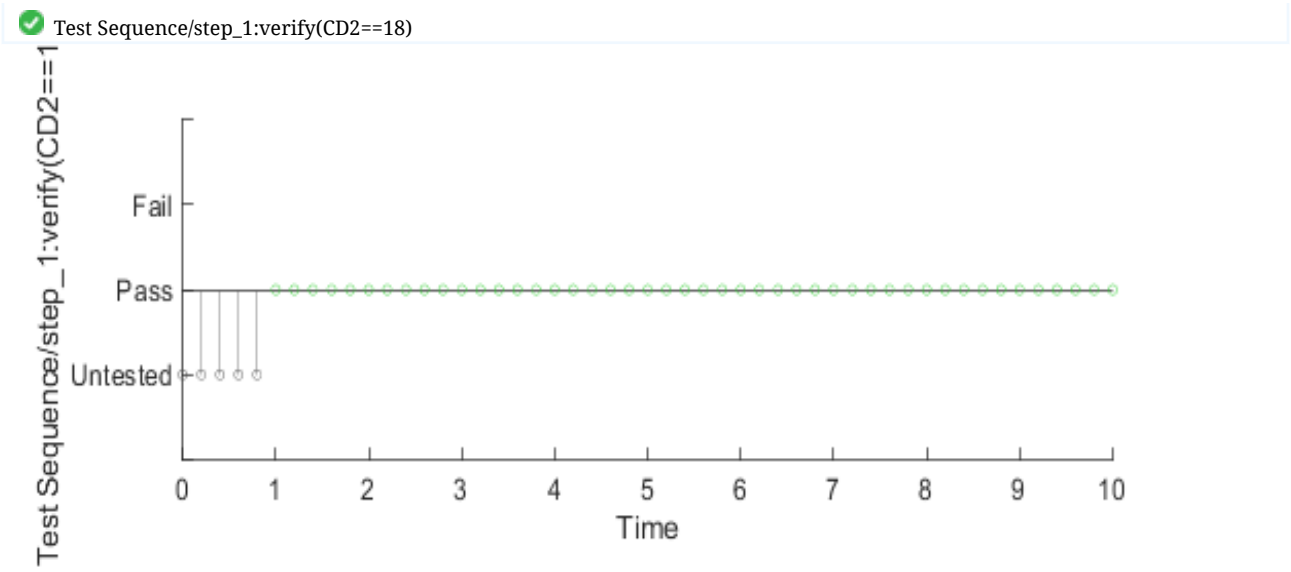
Test Case Information

Name:	CD_5
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(CD2==18)	Link

Name



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	CD_5
Harness Owner:	Horloge_interne_v3/Horloge_Interne/ Day_adjustment/Subsystem2

Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	972147553 3734940968 2161296706 3759945467
Simulink Version:	10.7
Model Version:	1.13
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:44 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:17
Simulation Stop Time:	2024-08-12 17:21:18
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ Hour_adjustment

Test Result Information

Result Type:	Test Suite Result
Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:20
End Time:	12-Aug-2024 17:21:22
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/ Hour_adjustment

Back to Report Summary

CHANGED_HOUR2

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/ Hour_adjustment
Start Time:	12-Aug-2024 17:21:20
End Time:	12-Aug-2024 17:21:22
Outcome:	Passed

Test Case Information

Name:	CHANGED_HOUR2
Type:	Baseline Test

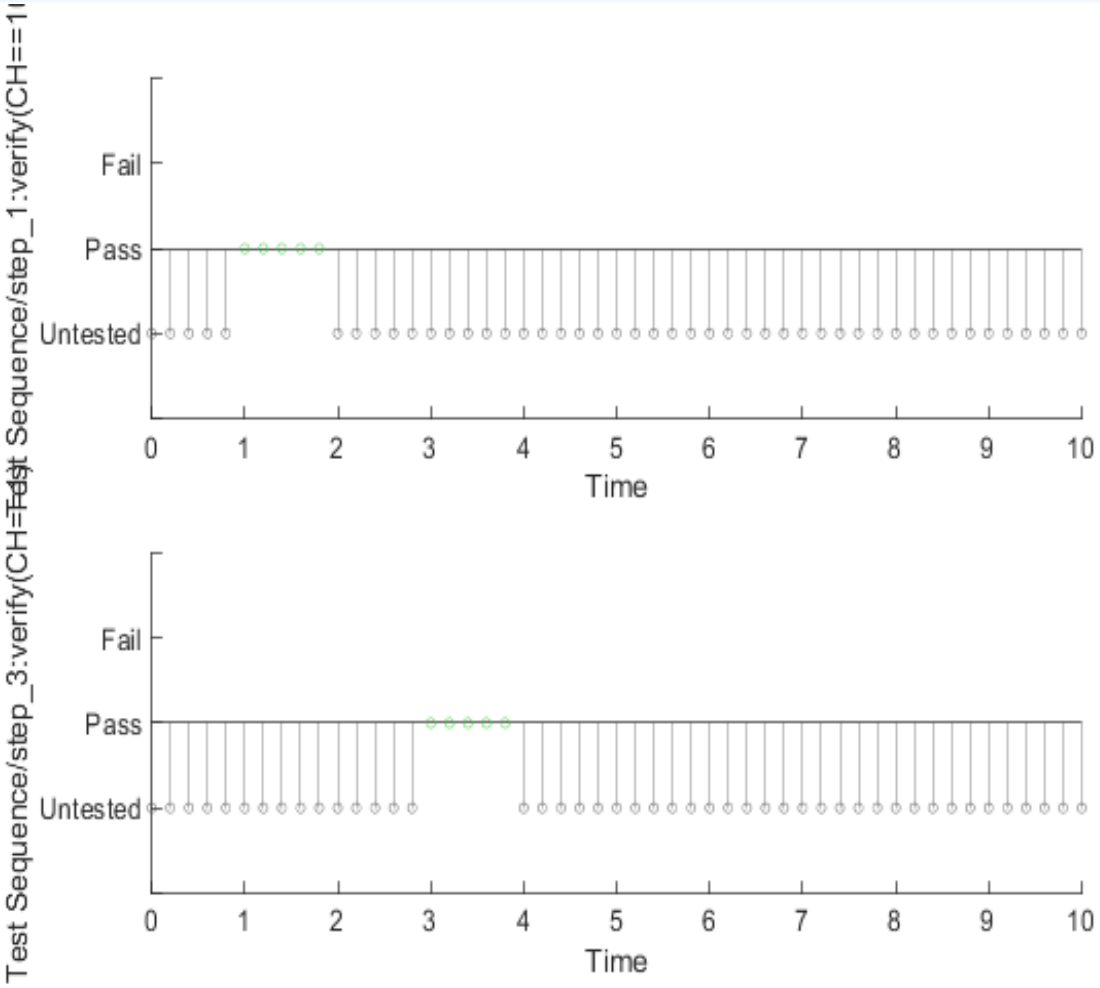
Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(CH==10)	Link
Test Sequence/step_3:verify(CH==1)	Link
Test Sequence/step_5:verify(CH==16)	Link
Test Sequence/step_7:verify(CH==16)	Link

Name

Test Sequence/step_1:verify(CH==10)

Test Sequence/step_3:verify(CH==1)



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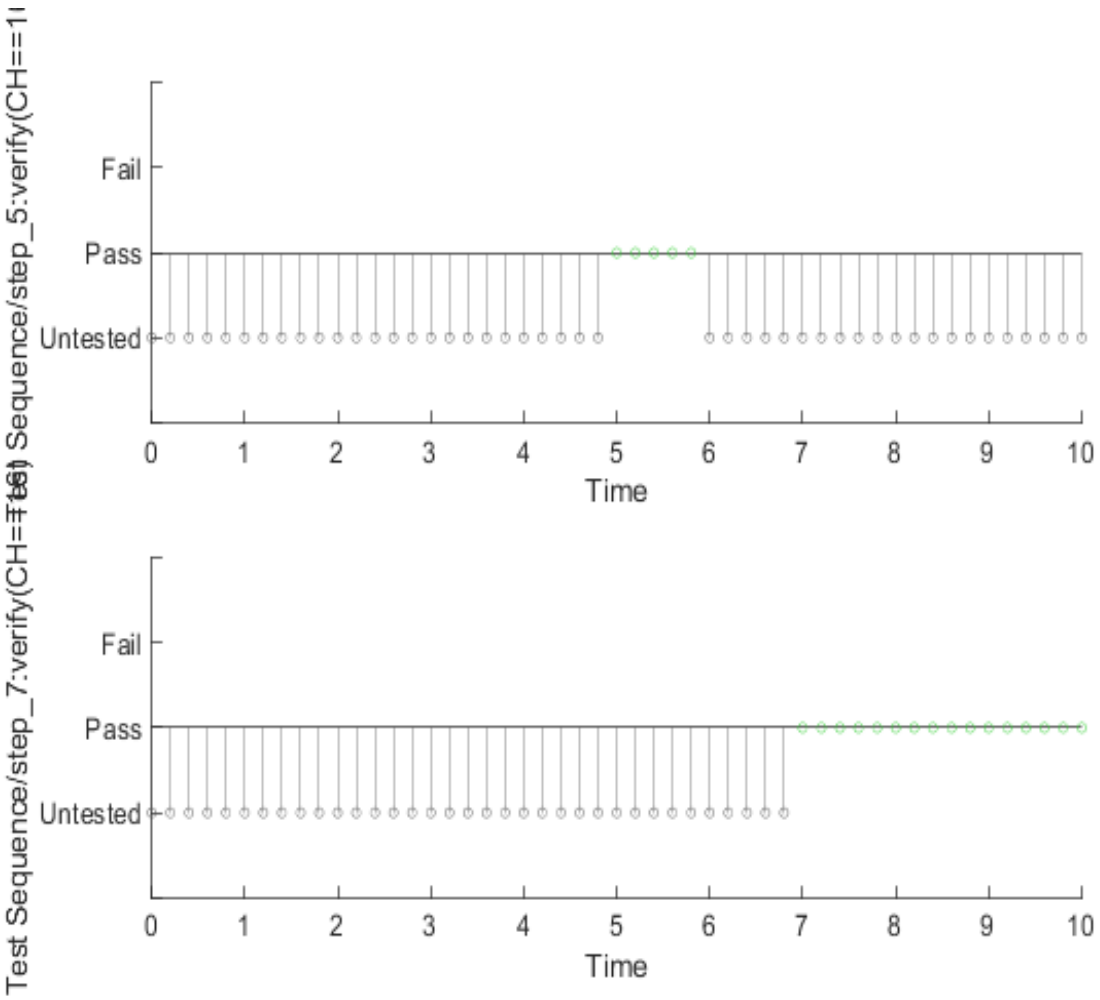
Name
Test Sequence/step_5:verify(CH==16)
Test Sequence/step_7:verify(CH==16)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	CHANGED_HOUR2
Harness Owner:	Horloge_interne_v3/Horloge_Interne/ Hour_adjustment
Release:	Current

Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	1935193750 3850173969 1068277957 3781451612
Simulink Version:	10.7
Model Version:	1.15
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:44 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:20
Simulation Stop Time:	2024-08-12 17:21:21
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ Last_Day_of_Month

Test Result Information

Result Type: Test Suite Result

Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:22
End Time:	12-Aug-2024 17:21:24
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/ Last_Day_of_Month

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Last_Day_Month_scenario2

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/ Last_Day_of_Month
Start Time:	12-Aug-2024 17:21:22
End Time:	12-Aug-2024 17:21:24
Outcome:	Passed

Test Case Information

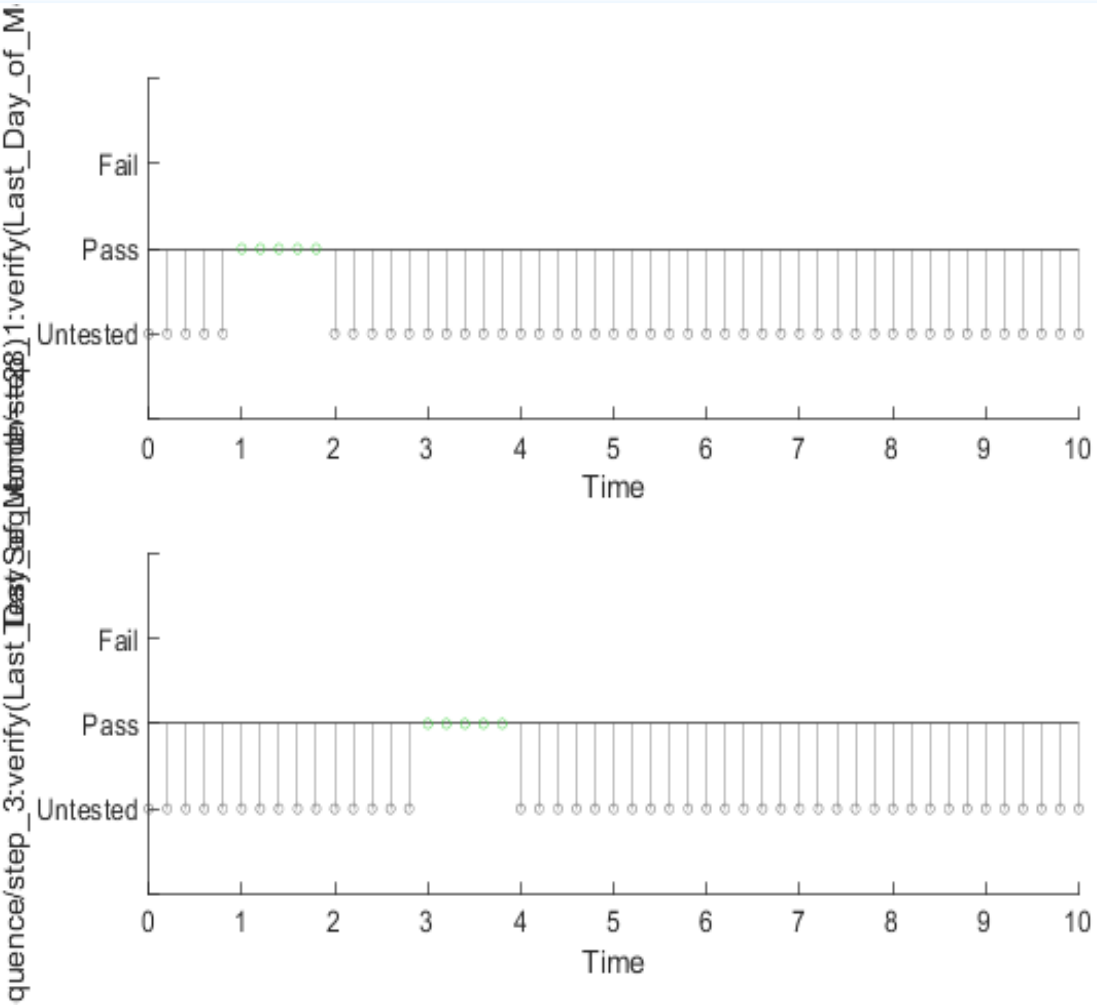
Name:	Last_Day_Month_scenario2
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(Last_Day_of_Month==29)	Link
Test Sequence/step_3:verify(Last_Day_of_Month==28)	Link
Test Sequence/step_5:verify(Last_Day_of_Month==31)	Link
Test Sequence/step_7:verify(Last_Day_of_Month==30)	Link

Name
Test Sequence/step_1:verify(Last_Day_of_Month==29)

Test Sequence/step_3:verify(Last_Day_of_Month==28)



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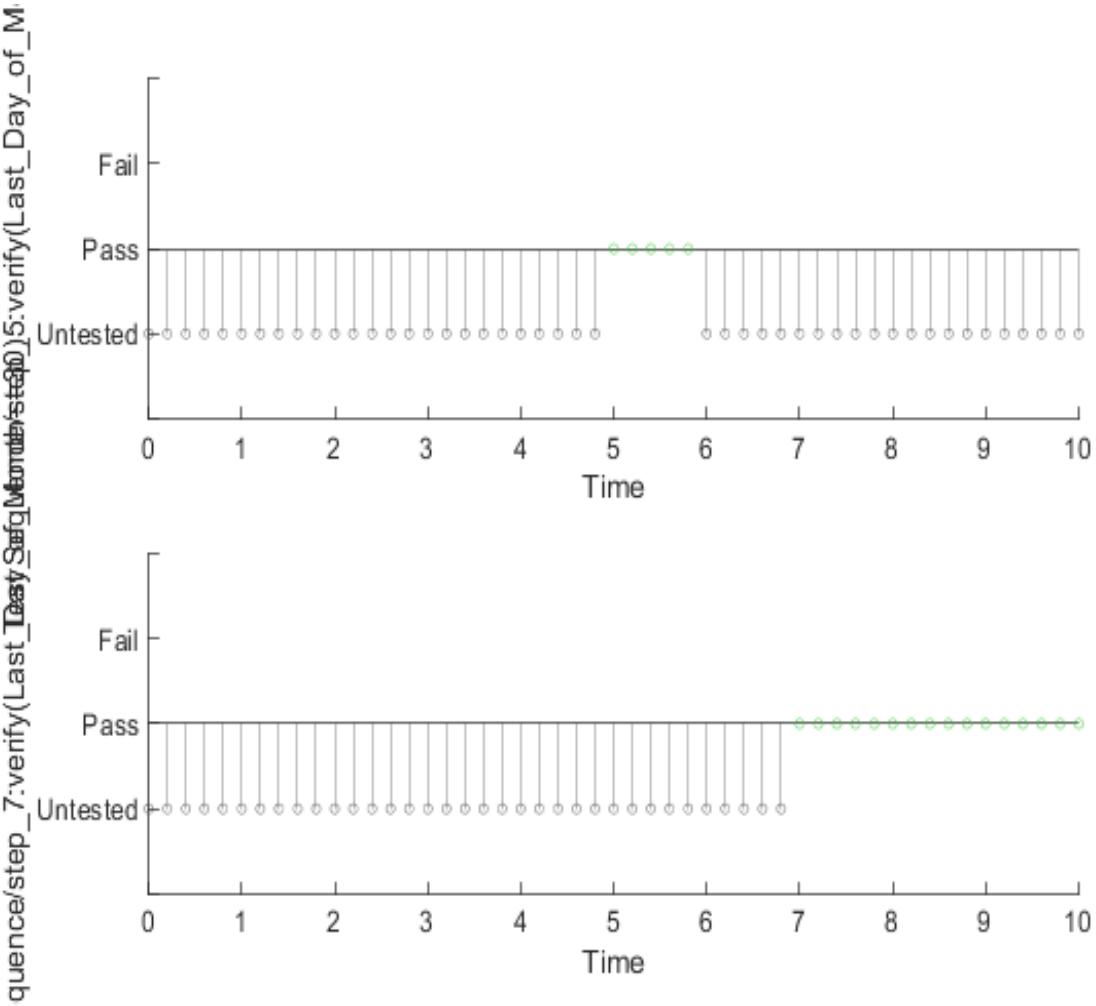
Name
Test Sequence/step_5:verify(Last_Day_of_Month==31)
Test Sequence/step_7:verify(Last_Day_of_Month==30)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	Last_Day_Month_scenario2
Harness Owner:	Horloge_interne_v3/Horloge_Interne/ Last_Day_of_Month
Release:	Current

Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	4284381204 4208318777 745706502 2875428380
Simulink Version:	10.7
Model Version:	1.14
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:44 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:22
Simulation Stop Time:	2024-08-12 17:21:24
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ Leap_Year

Test Result Information

Result Type: Test Suite Result

Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:25
End Time:	12-Aug-2024 17:21:27
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/Leap_Year

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Leap_scenario1

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/Leap_Year
Start Time:	12-Aug-2024 17:21:25
End Time:	12-Aug-2024 17:21:27
Outcome:	Passed

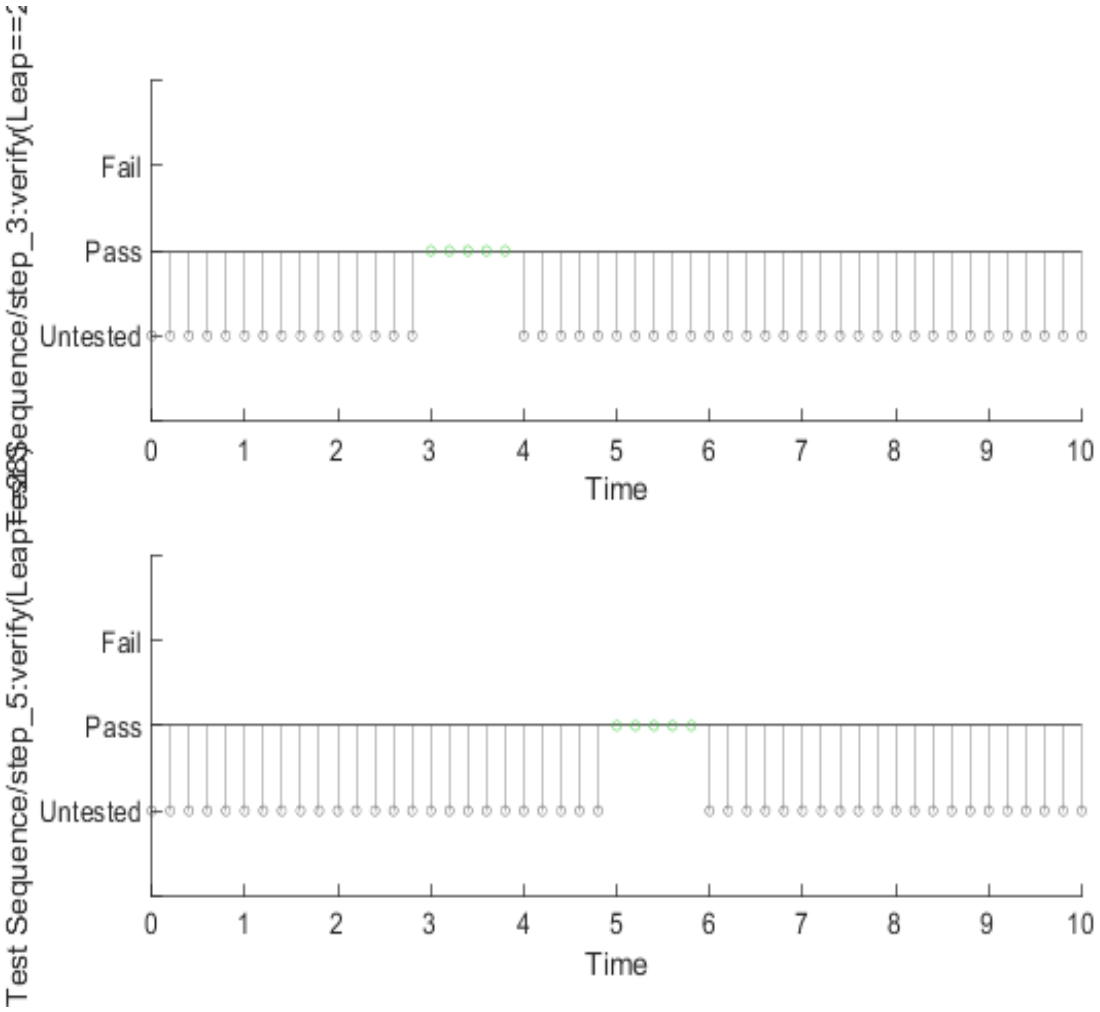
Test Case Information

Name:	Leap_scenario1
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_3:verify(Leap==29)	Link
Test Sequence/step_5:verify(Leap==28)	Link
Test Sequence/step_7:verify(Leap==29)	Link

Name
Test Sequence/step_3:verify(Leap==29)
Test Sequence/step_5:verify(Leap==28)



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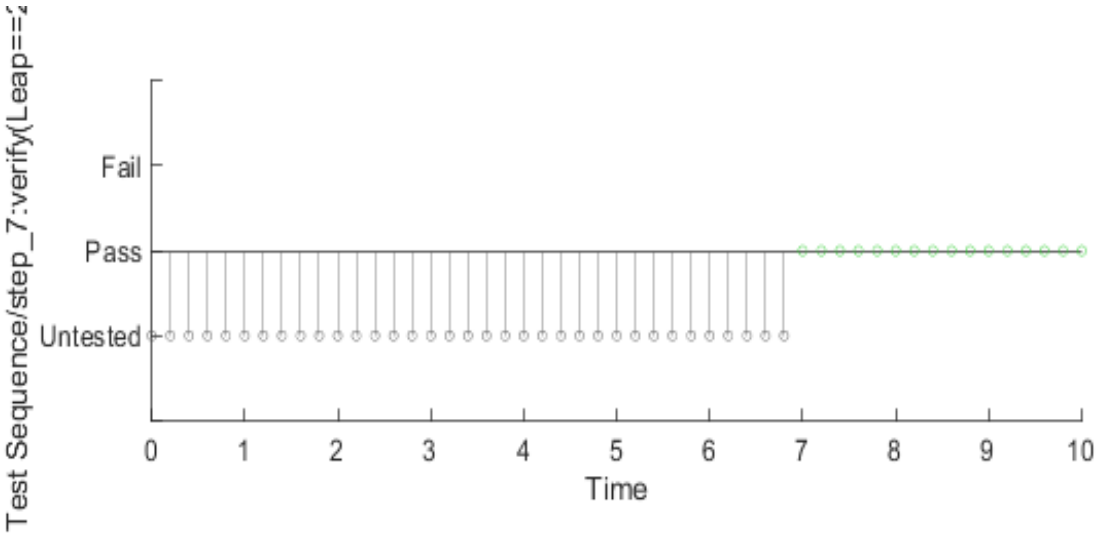
Name
Test Sequence/step_7:verify(Leap==29)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	Leap_scenario1
Harness Owner:	Horloge_interne_v3/Horloge_Interne/Leap_Year
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	144916322 1516373151 4249223224 3939431754
Simulink Version:	10.7
Model Version:	1.13
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:44 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:25
Simulation Stop Time:	2024-08-12 17:21:26
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ MATLAB Function1

Test Result Information

Result Type:	Test Suite Result
Parent:	Horloge_interne_v3

Start Time: 12-Aug-2024 17:21:27
End Time: 12-Aug-2024 17:21:32
Outcome: Total: 1, Passed: 1

Test Suite Information

Name: Horloge_interne_v3/Horloge_Interne/MATLAB Function1

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CYN_remD2

Test Result Information

Result Type: Test Case Result
Parent: Horloge_interne_v3/Horloge_Interne/MATLAB Function1
Start Time: 12-Aug-2024 17:21:27
End Time: 12-Aug-2024 17:21:32
Outcome: Passed

Test Case Information

Name: CYN_remD2
Type: Baseline Test

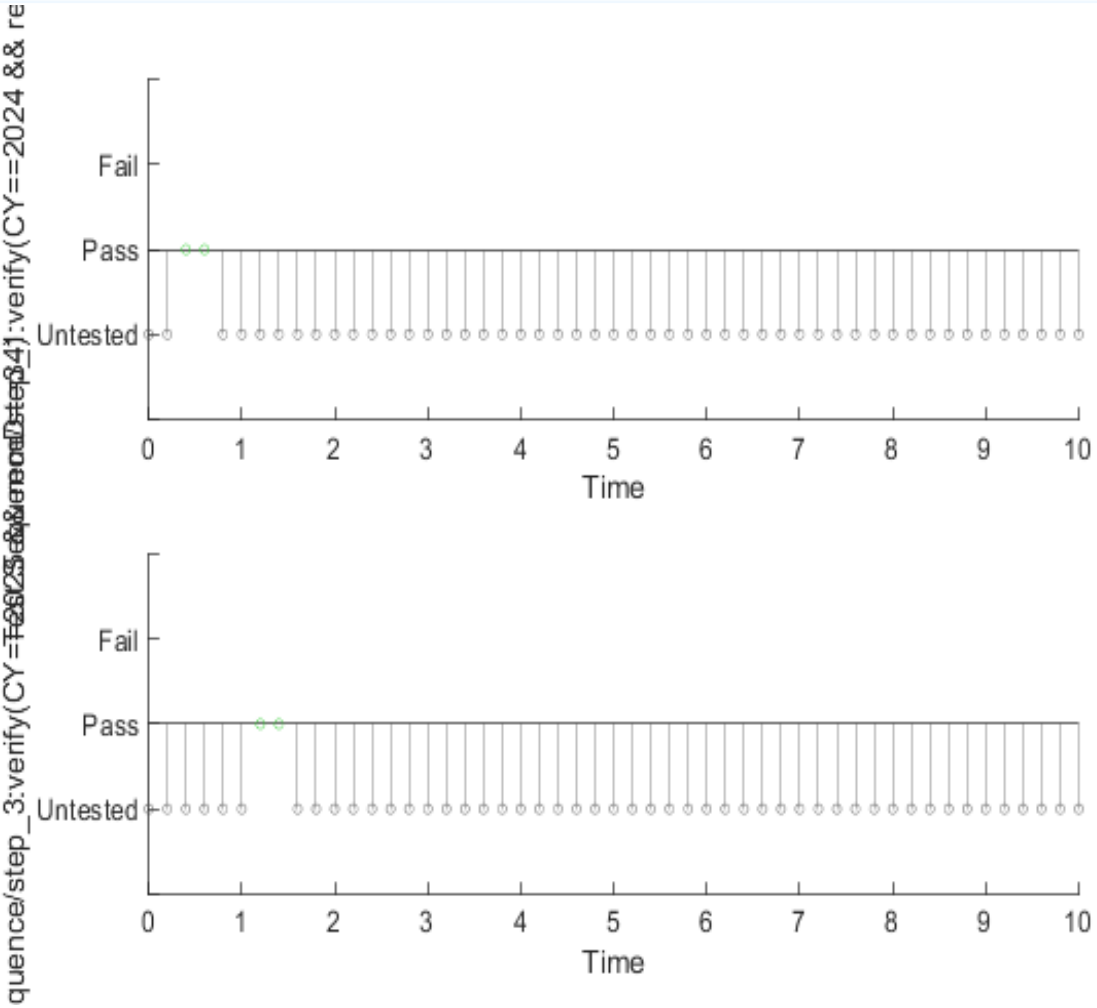
Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(CY==2024 && remD==100)	Link
Test Sequence/step_3:verify(CY==2025 && remD==34)	Link
Test Sequence/step_5:verify(CY==2025 && remD==100)	Link
Test Sequence/step_7:verify(CY==2026 && remD==35)	Link
Test Sequence/step_9:verify(CY==2100 && remD==100)	Link
Test Sequence/step_11:verify(CY==2101 && remD==35)	Link

Name

Test Sequence/step_1:verify(CY==2024 && remD==100)

Test Sequence/step_3:verify(CY==2025 && remD==34)



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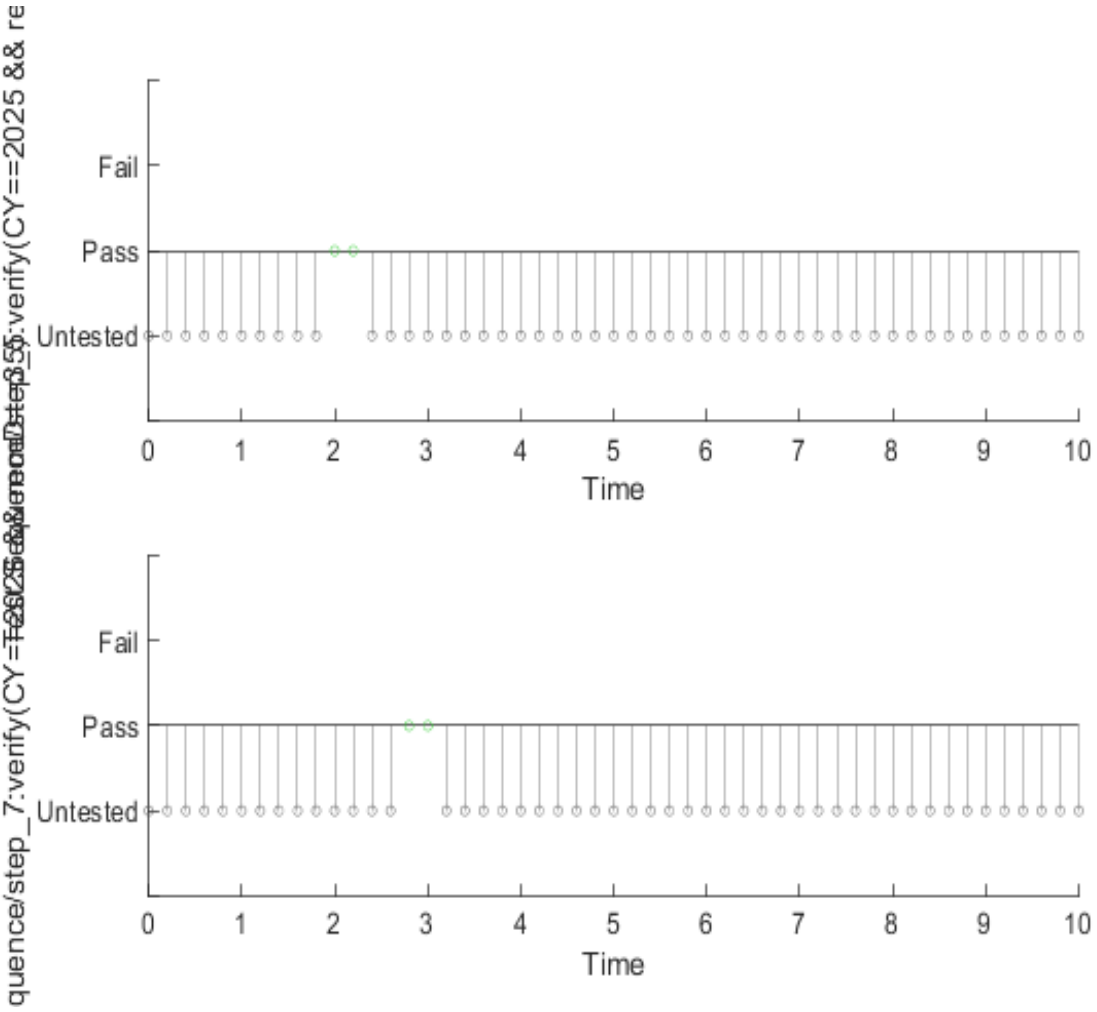
Name
Test Sequence/step_5:verify(CY==2025 && remD==100)
Test Sequence/step_7:verify(CY==2026 && remD==35)



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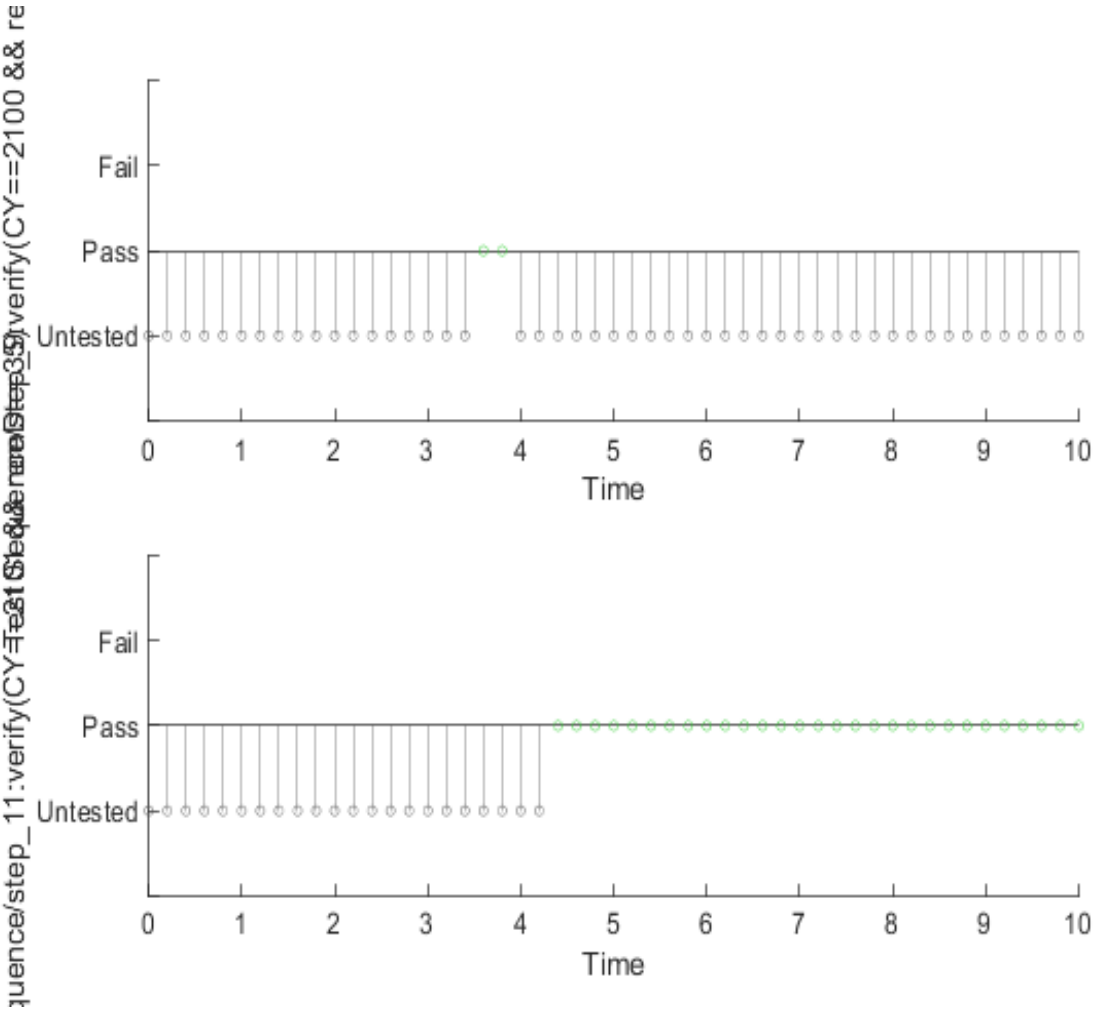
Name
Test Sequence/step_9:verify(CY==2100 && remD==100)
Test Sequence/step_11:verify(CY==2101 && remD==35)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	CYN_remD2
Harness Owner:	Horloge_interne_v3/Horloge_Interne/MATLAB Function1
Release:	Current

Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	1761183483 852994869 4142329056 2274541223
Simulink Version:	10.7
Model Version:	1.18
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:45 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:27
Simulation Stop Time:	2024-08-12 17:21:31
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ MN_from_DN

Test Result Information

Result Type: Test Suite Result

Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:33
End Time:	12-Aug-2024 17:21:36
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/ MN_from_DN

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AM_2

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/ MN_from_DN
Start Time:	12-Aug-2024 17:21:33
End Time:	12-Aug-2024 17:21:36
Outcome:	Passed

Test Case Information

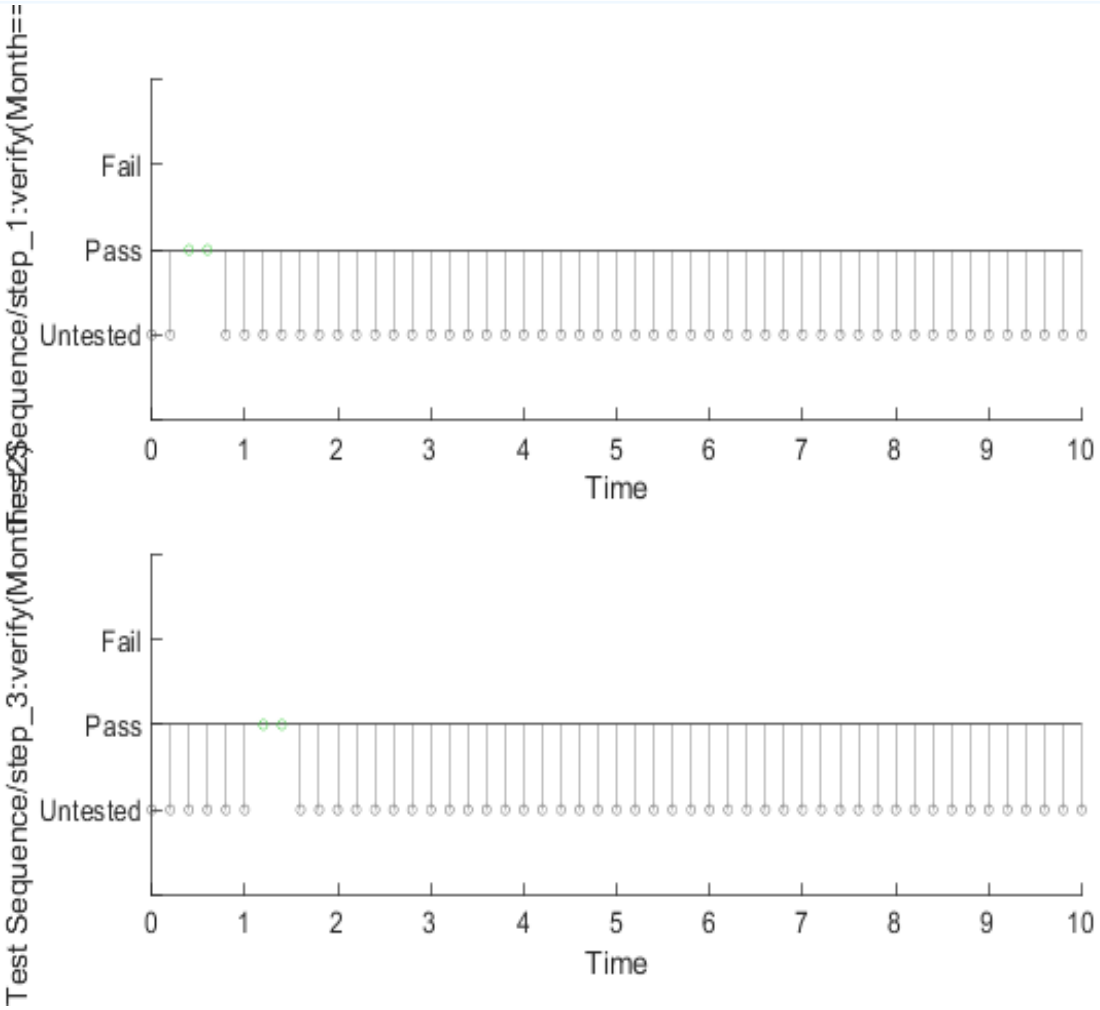
Name:	AM_2
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(Month==1)	Link
Test Sequence/step_3:verify(Month==2)	Link
Test Sequence/step_5:verify(Month==2)	Link
Test Sequence/step_7:verify(Month==3)	Link
Test Sequence/step_9:verify(Month==4)	Link
Test Sequence/step_11:verify(Month==5)	Link
Test Sequence/step_13:verify(Month==6)	Link
Test Sequence/step_15:verify(Month==7)	Link

Test Sequence/step_17:verify(Month==8)	Link
Test Sequence/step_19:verify(Month==9)	Link
Test Sequence/step_21:verify(Month==10)	Link
Test Sequence/step_23:verify(Month==11)	Link
Test Sequence/step_25:verify(Month==12)	Link

Name
Test Sequence/step_1:verify(Month==1)
Test Sequence/step_3:verify(Month==2)



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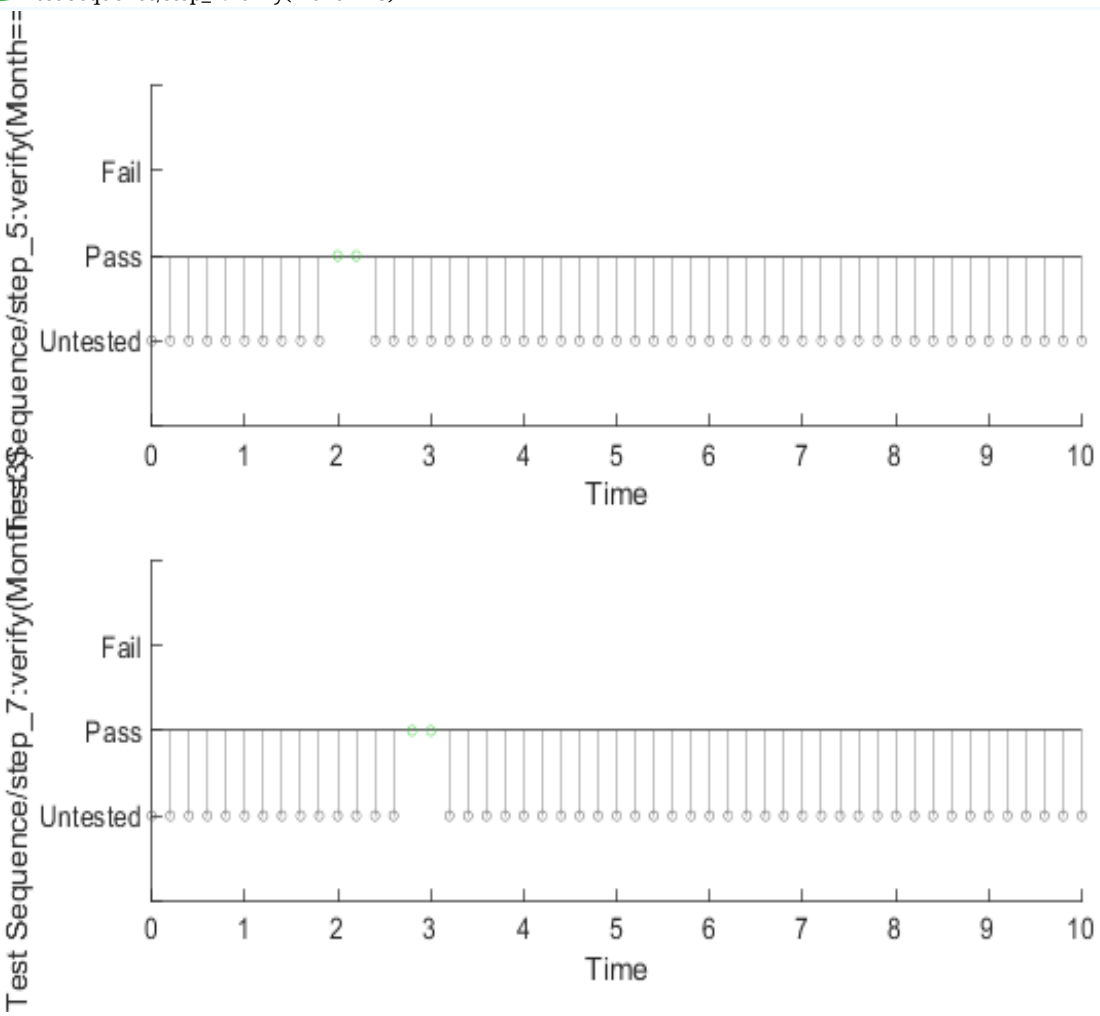
Name
Test Sequence/step_5:verify(Month==2)
Test Sequence/step_7:verify(Month==3)



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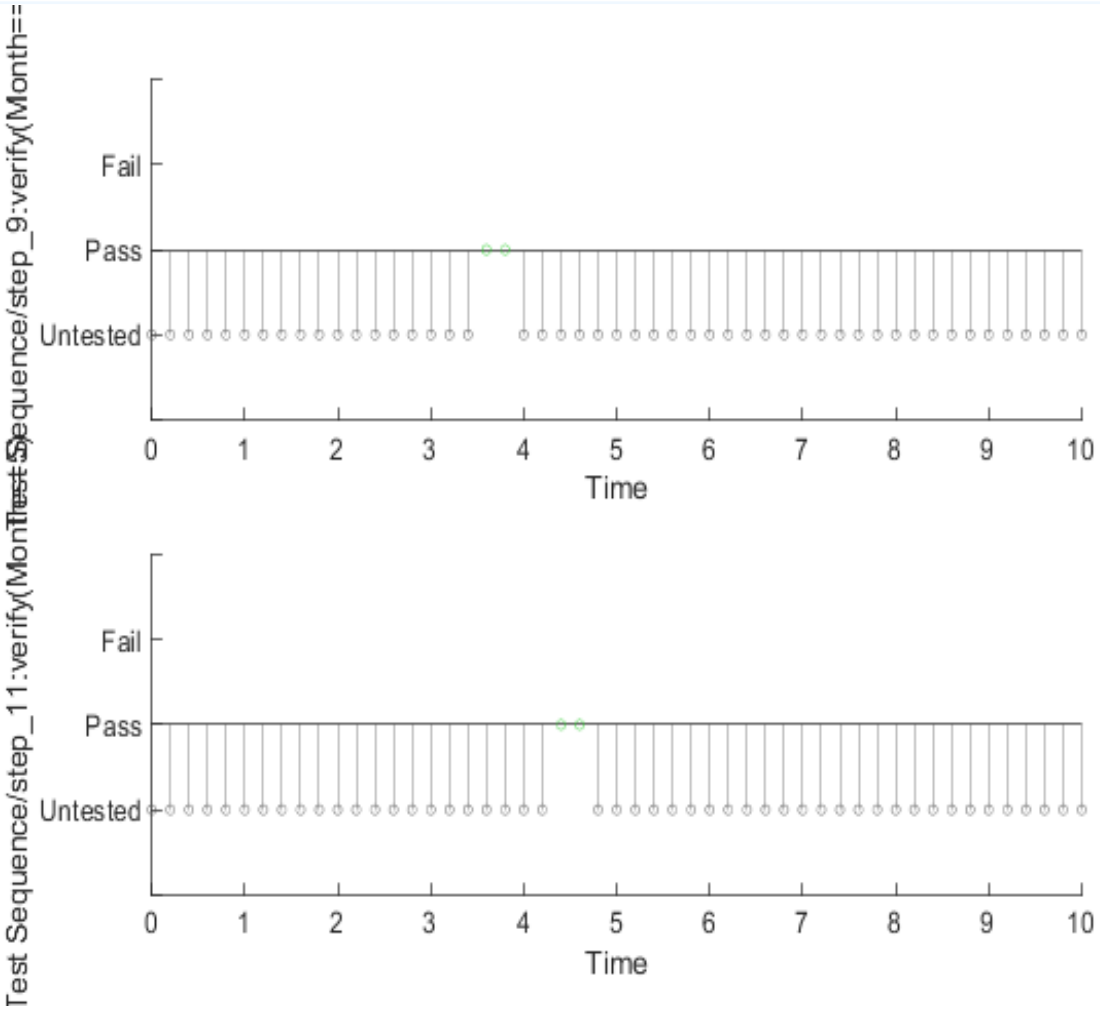
Name
Test Sequence/step_9:verify(Month==4)

Test Sequence/step_11:verify(Month==5)



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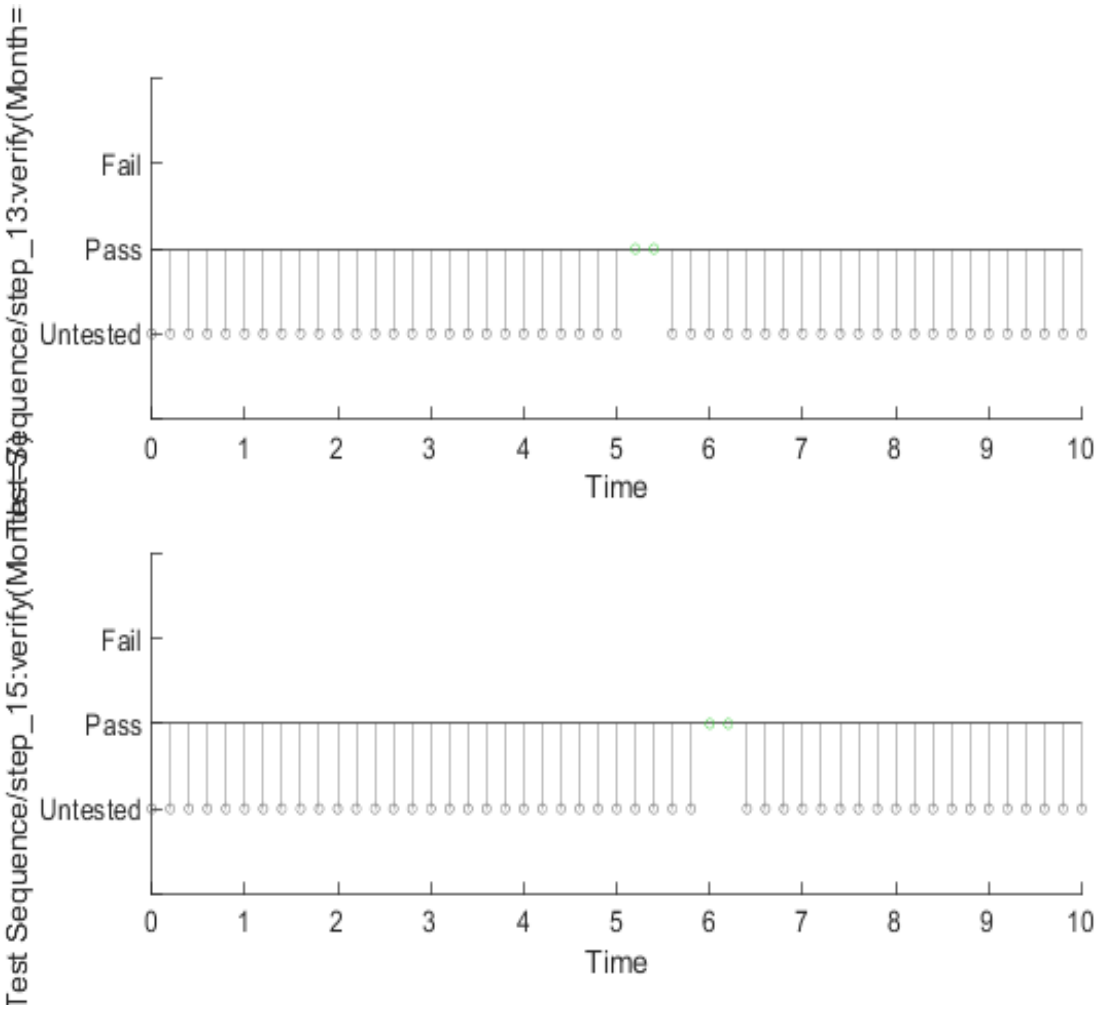
Name
Test Sequence/step_13:verify(Month==6)
Test Sequence/step_15:verify(Month==7)



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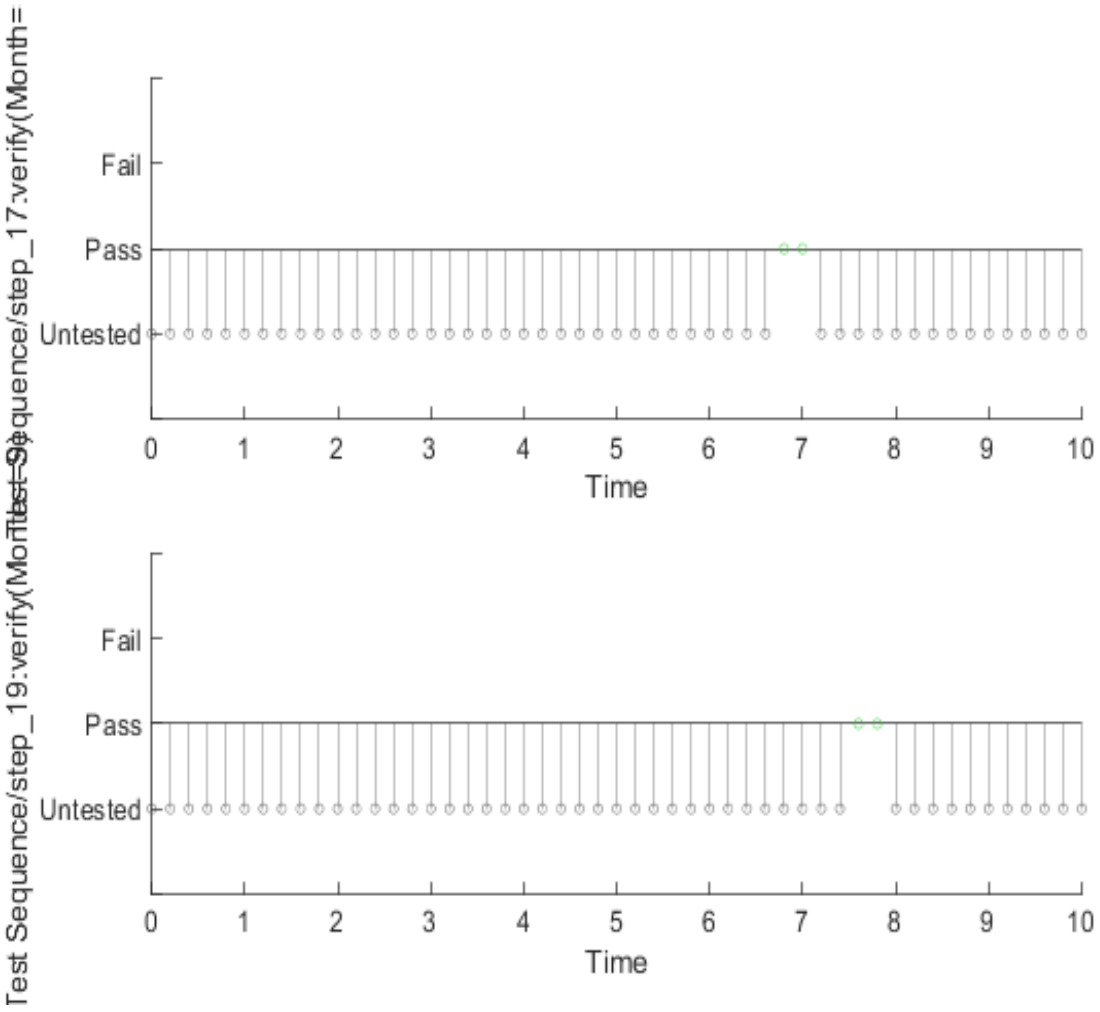
Name
Test Sequence/step_17:verify(Month==8)
Test Sequence/step_19:verify(Month==9)



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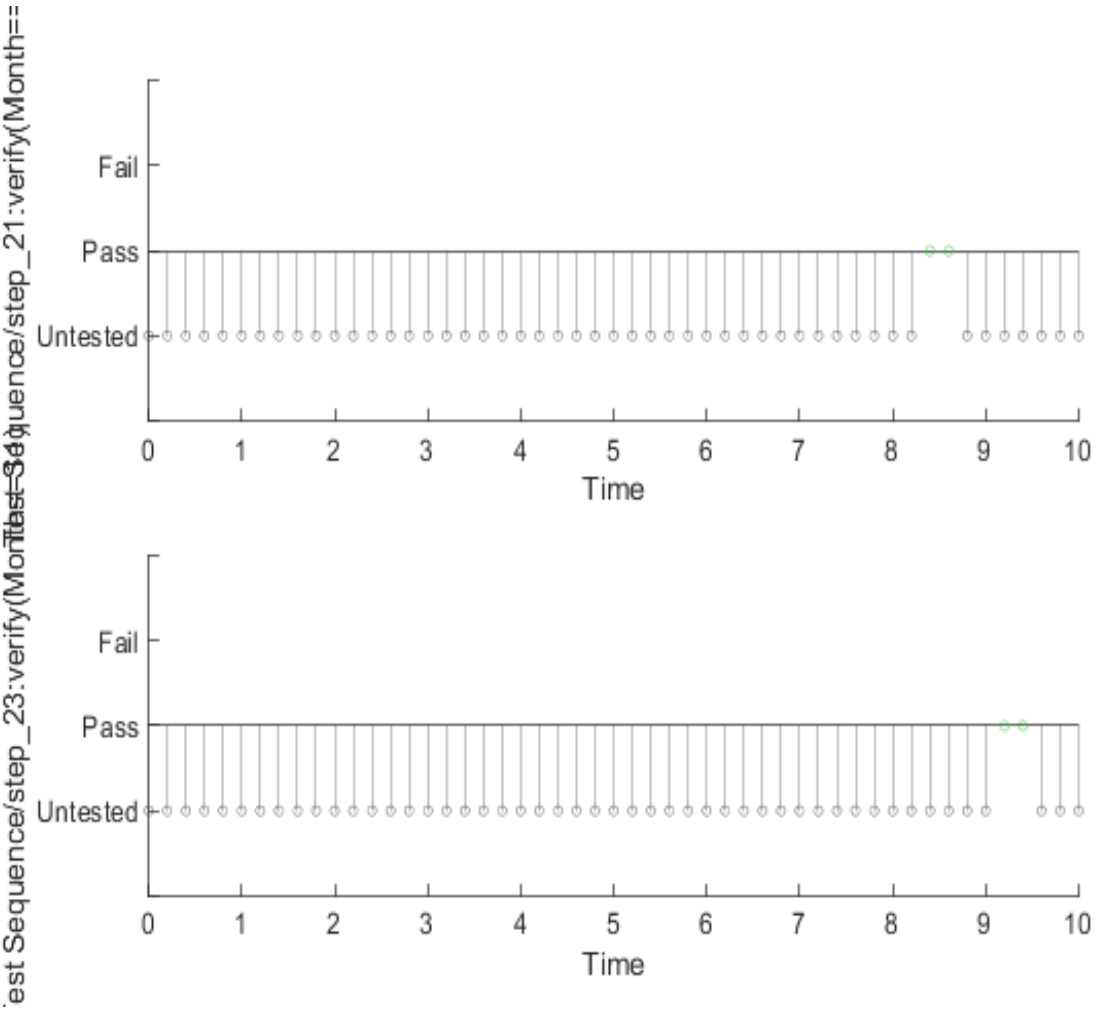
Name
Test Sequence/step_21:verify(Month==10)
Test Sequence/step_23:verify(Month==11)



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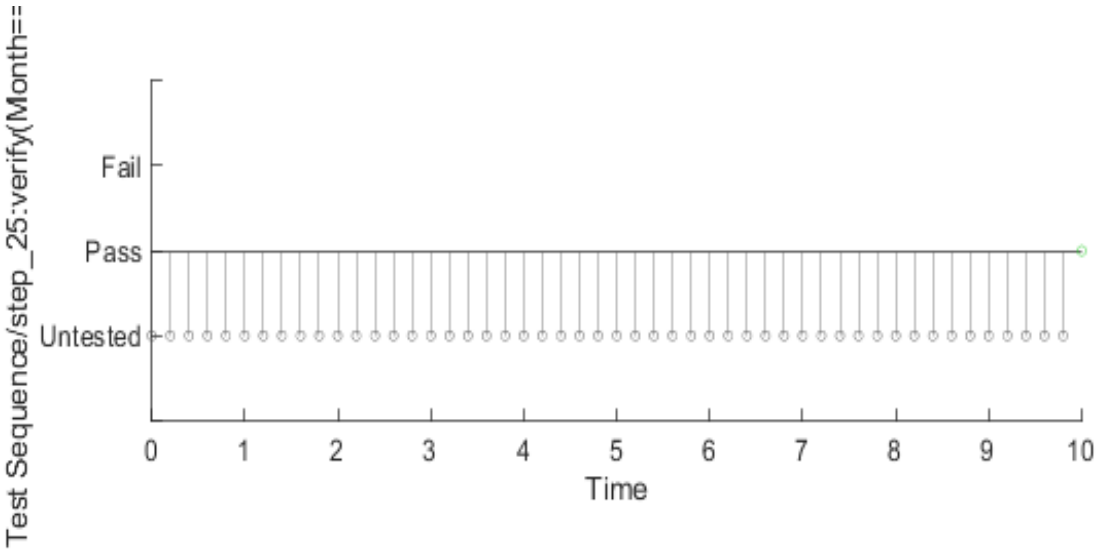
Name
Test Sequence/step_25:verify(Month==12)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	AM_2
Harness Owner:	Horloge_interne_v3/Horloge_Interne/ MN_from_DN
Release:	Current

Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	3257757266 13761782 2089818698 3011459932
Simulink Version:	10.7
Model Version:	1.15
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:45 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:33
Simulation Stop Time:	2024-08-12 17:21:35
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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Horloge_interne_v3/Horloge_Interne/ H_var_State1

Test Result Information

Result Type: Test Suite Result

Parent:	Horloge_interne_v3
Start Time:	12-Aug-2024 17:21:37
End Time:	12-Aug-2024 17:21:39
Outcome:	Total: 1, Passed: 1

Test Suite Information

Name:	Horloge_interne_v3/Horloge_Interne/ H_var_State1

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DN_LDY_V1

Test Result Information

Result Type:	Test Case Result
Parent:	Horloge_interne_v3/Horloge_Interne/ H_var_State1
Start Time:	12-Aug-2024 17:21:37
End Time:	12-Aug-2024 17:21:39
Outcome:	Passed

Test Case Information

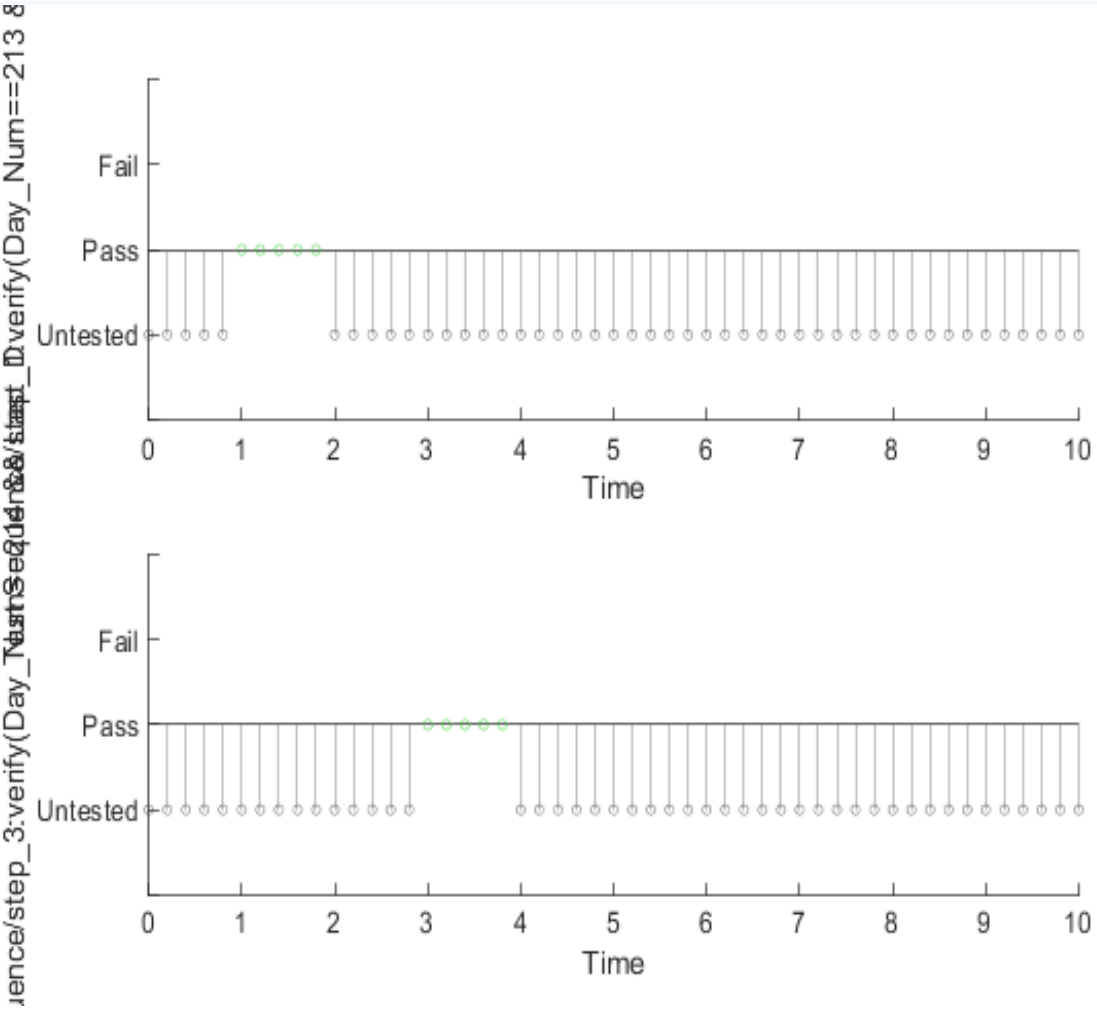
Name:	DN_LDY_V1
Type:	Baseline Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(Day_Num==213 && Last_Day_of_Year==365)	Link
Test Sequence/step_3:verify(Day_Num==214 && Last_Day_of_Year==366)	Link
Test Sequence/step_5:verify(Day_Num==1 && Last_Day_of_Year==365)	Link
Test Sequence/step_7:verify(Day_Num==32 && Last_Day_of_Year==366)	Link

Name
Test Sequence/step_1:verify(Day_Num==213 && Last_Day_of_Year==365)

Test Sequence/step_3:verify(Day_Num==214 && Last_Day_of_Year==366)



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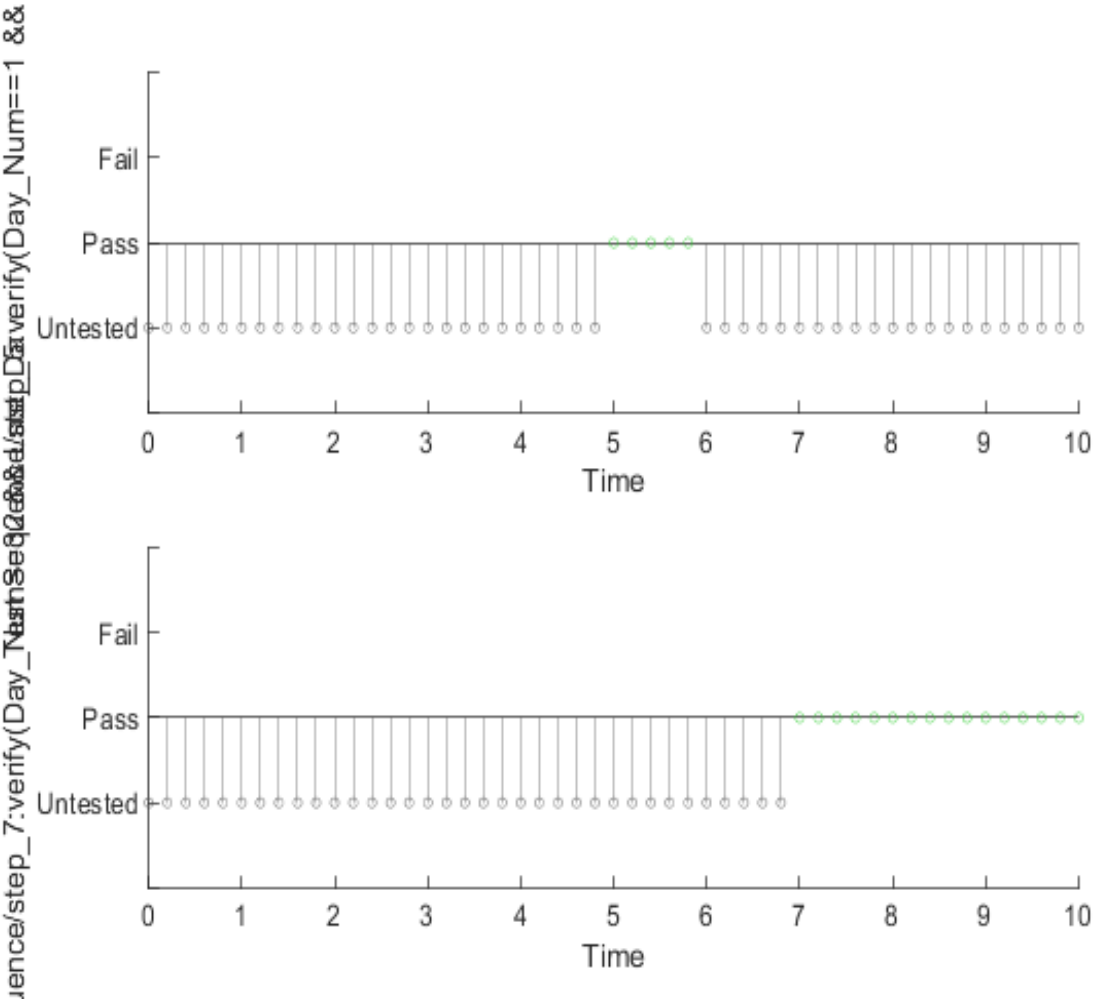
Name
Test Sequence/step_5:verify(Day_Num==1 && Last_Day_of_Year==365)
Test Sequence/step_7:verify(Day_Num==32 && Last_Day_of_Year==366)



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Simulation

System Under Test Information

Model:	Horloge_interne_v3
Harness:	DN_LDY_V1
Harness Owner:	Horloge_interne_v3/Horloge_Interne/ H_var_State1
Release:	Current

Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	2302935330 1379156285 364311402 378052790
Simulink Version:	10.7
Model Version:	1.15
Model Author:	Khalid-B
Date:	Mon Aug 12 14:34:46 2024
User ID:	Khalid-B
Model Path:	C:\Users\Khalid-B\Desktop\matlab\Alten\newnew\Horloge_interne_v3\Horloge_interne_v3.slx
Machine Name:	KHALID
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2024-08-12 17:21:37
Simulation Stop Time:	2024-08-12 17:21:39
Platform:	PCWIN64

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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