INF1001 – Introduction to Computing (Quiz)

Quiz 1.1

Question 1 (1 point)

What does the word synchronous digital circuits refers to?

- ◯ Requires software to work.
- ◯ Requires inputs to work.
- ◯ Requires clock to work.
- ◯ Requires power to work.

Question 2 (1 point)

How many permutations are there for a 5-bit binary number?

- ◯ 32
- ◯ 4
- ◯ 64
- ◯ 16

Question 3 (1 point)

What is the difference between a positive logic versus a negative logic for digital circuit?

- ◯ Positive logic uses high voltage to represent binary 1 and low voltage to represent binary 0 while negative does the reverse.
- ◯ Positive logic uses high voltage to represent binary 0 and low voltage to represent binary 1 while negative does the reverse.
- ◯ Positive logic uses high current to represent binary 0 and low current to represent binary 1 while negative does the reverse.
- ◯ Positive logic uses high current to represent binary 1 and low current to represent binary 0 while negative does the reverse.

Question 4 (1 point)

In computer, convert 1.25KB to bytes.

[ ]

Question 5 (1 point)

Given a 16-bit binary number 1100 1010 0101 0110, identify the value for bit 9 and bit 8.

[ ]

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Quiz 1.2

Question 1 (1 point)

What happen when sampling is performed below Nyquist rate?

- ◯ Aliasing will occur.
- ◯ Excess data will be produced.
- ◯ Over sampling will occur.
- ◯ The signal remain to be an analog signal.

Question 2 (1 point)

Given a sampling frequency of 1.5 GHz, what is the maximum frequency of a signal that it can capable of digitalising without signal loss.

[ ]

Question 3 (1 point)

What is the purpose of quantisation?

- ◯ Convert a discrete digital value to analog.
- ◯ Convert an analog sample to a discrete digital value.
- ◯ Determine the sampling frequency required.
- ◯ Determine the number of samples required.

Question 4 (1 point)

Which component performs quantisation?

[ ]

Question 5 (1 point)

Which of the following would you consider to be the biggest disadvantage of digital signal representation?

- ◯ Larger storage space required.
- ◯ Digital data are easily copied, hence requires additional data protection.
- ◯ Digital signal are easily reproducible.
- ◯ Digital signal has inherent lost information due to sampling and quantisation.

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Quiz 1.3

Question 1 (1 point)

When you use an analog to digital converter with 20-bit resolution, how many levels will each sample be represented?

Question 2 (1 point)

When an audio signal is sampled at 20KHz at 16-bit resolution at stereo (2 channels for left and right channel) quality, what is the file size that you will expect for a 5 minutes recording?

Question 3 (1 point)

Given a minimum period for a signal is 1.5 ns, what is the most appropriate sampling frequency.

- 1.4 GHz
- 1.3 GHz
- 1.4 MHz
- 1.3GHz

Question 4 (1 point)

What is the main trade-off when you sampling at much higher frequency beyond Nyquist rate?

- Larger file size
- Smaller file size
- Higher resolution data
- Lower resolution data

Question 5 (1 point)

When a signal sample ranging between -10V to +10V is converted to a digital signal using an 8-bit ADC, what is the quantisation noise?

- 78mV
- 39mV
- 1.25V
- 2.5V

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Quiz 1.4

Question 1 (1 point)

In a typical computer, when a programmer declare a variable integer, where is this stored?

Question 2 (1 point)

A Von Neumann computer contains 3 key components, they are:

- [ ] Memory
- [ ] CPU
- [ ] I/O
- [ ] ALU
- [ ] System Busses

Question 3 (1 point)

Computer and mobile devices have RAM that are usually volatile, what does this mean?

- ◯ The content of the RAM are duplicated after power off.
- ◯ The content of the RAM are retained after power off.
- ◯ The content of the RAM are transferred after power off.
- ◯ The content of the RAM are lost after power off.

Question 4 (1 point)

The central processing unit or CPU contains register, control unit and _____?

Question 5 (1 point)

The program execution cycle is usually described as a 3 stage process, which is the correct sequence during execution?

- ◯ Fetch, Decode, Execute
- ◯ Fetch, Execute, Decode
- ◯ Decode, Fetch, Execute
- ◯ Execute, Decode, Fetch

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Quiz 1.5

Question 1 (1 point)

Which of the following is NOT a task of an operating system (OS).

- ◯ Scheduling of tasks to execute.
- ◯ Control and manage hardware resources
- ◯ Control how much RAM can be installed on a computer hardware.
- ◯ Manage access control for different users.

Question 2 (1 point)

Which computer bus is bidirectional?

- ◯ Address
- ◯ Data
- ◯ Control
- ◯ None of the above

Question 3 (1 point)

Given a memory chip with 16-bit data bus and 31-bit address bus, what is the capacity of the memory?

[ ]

Question 4 (1 point)

Arrange the following memory in increasing order of their access time with (1) being the fastest.

- [ ] External harddisk
- [ ] CPU registers
- [ ] Cache memory
- [ ] Main memory (e.g. RAM)
- [ ] Secondary memory

Question 5 (1 point)

Which are the follow are correct when describing about virtual machine (VM) and container?

- ☐ VM support multiple OS while container usually support single OS.
- ☐ Multiple applications are able to run on both VM and Container.
- ☐ Container has a lower overhead than VM.
- ☐ Container support multiple OS while VM usually support single OS.
- ☐ VM has a lower overhead than container.

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Quiz 2.1

Question 1 (1 point)

Manually convert decimal number 55 to 8-bit binary.

Question 2 (1 point)

For a 6-bit unsigned binary number, what is the range of decimal numbers it is able to represent?

- 0 to +64
- 0 to +32
- 0 to +31
- 0 to +63

Question 3 (1 point)

Given a variable to store a random data that can range from 0 to +65536, what is the most appropriate number of bits required for the variable?

- 16-bit
- 18-bit
- 15-bit
- 17-bit

Question 4 (1 point)

For a 3-bit binary number, which is the correct counting sequence from 0 to 7.

- 000, 010, 001, 011, 100, 110, 101, 111
- 000, 001, 011, 010, 100, 101, 111, 110
- 000, 001, 010, 011, 100, 101, 110, 111
- 000, 001, 011, 010, 110, 111, 101, 100

Question 5 (1 point)

For a 5 digit decimal number, what is highest decimal value that it can represent?

INF1001 – Introduction to Computing (Quiz)

Quiz 2.2

Question 1 (1 point)

Which binary number represents a sign-magnitude number with a decimal value of -0?

- ◯ 0000 0000
- ◯ 0111 1111
- ◯ 1111 1111
- ◯ 1000 0000

Question 2 (1 point)

What is the smallest negative decimal number that can be stored in 10-bit 1's complement number?

[ ]

Question 3 (1 point)

Given a 1's complement 8-bit binary number expressed in hexadecimal form as F5, what is it equivalent decimal value?

- ◯ -245
- ◯ -117
- ◯ -10
- ◯ 245

Question 4 (1 point)

Manually convert the following binary number to hexadecimal: 1011 1101 0101 1001

[ ]

Question 5 (1 point)

How is decimal value -255 represented in binary form for sign-magnitude and 1's complement representations?

- ◯ Sign-magnitude = 1111 1111, 1's complement = 0000 0000
- ◯ Sign-magnitude = 1 0000 0000, 1's complement = 0 1111 1111
- ◯ Sign-magnitude = 0 1111 1111, 1's complement = 1 0000 0000
- ◯ Sign-magnitude = 1 1111 1111, 1's complement = 1 0000 0000

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Quiz 2.3

Question 1 (1 point)

Convert decimal value -126 to 2's complement form in 8-bit binary.

Question 2 (1 point)

Convert decimal number +16 to 5-bit binary number?

- ◯ Overflow
- ◯ 1 0000
- ◯ 1 1111
- ◯ 0 1111

Question 3 (1 point)

Given a 2's complement number represented in hexadecimal form as E9, what is the decimal value?

Question 4 (1 point)

Which is (are) the key advantage of 2's complement representation?

- ☐ Equal numbers of positive and negative numbers
- ☐ Only one zero representation
- ☐ Arithmetic operations can be applied directly on positive and negative numbers.
- ☐ Two zeroes representations
- ☐ Larger range of numbers that it is able to represent

Question 5 (1 point)

Without using the calculator, identify which of the following selection (s) is (are) correct for 2's complement representation.

- ☐ Hexadecimal number 82 is a positive number
- ☐ Hexadecimal number 82 is a negative number
- ☐ Binary number 1010 1111 is a negative number
- ☐ Binary number 1010 1111 is a positive number

INF1001 – Introduction to Computing (Quiz)

Quiz 2.4

Question 1 (1 point)

For a 10-bit 2's complement number, what is the range of decimal numbers it can represent?

- ◯ -511 to +512
- ◯ -1023 to +1024
- ◯ -1024 to +1023
- ◯ -512 to +511

Question 2 (1 point)

Given a number 1011, how would you interprets its value?

- ◯ 1011 is a hexadecimal number and its decimal value is 4113
- ◯ 1011 is a decimal value as decimal is the default numbering system
- ◯ 1011 is a binary number and its decimal value is 11
- ◯ 1011 is a 2's complement binary number and its decimal value is -5

Question 3 (1 point)

What is the 8-bit binary value to add two 2's complement binary number A = 1101 0111 and B = 1011 0001?

Question 4 (1 point)

What set of decimal numbers represented in 8-bit 2's complement representations will result in an overflow when added together.

- ☐ A = -85, B = -44
- ☐ A = -117, B = -11
- ☐ A = 125, B = 45
- ☐ A = 127, B = -56

Question 5 (1 point)

Manually convert 2's complement 8-bit number represented in hexadecimal 9A to decimal.

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Quiz 2.5

Question 1 (1 point)

For a 12-bit 2's complement number 98A, which is the signed extended 16-bit number expressed in hexadecimal form?

Question 2 (1 point)

Given a 16-bit signed magnitude binary number represented in hexadecimal form as 807D, what is the truncated 8-bit equivalent value.

- ◯ 83
- ◯ 7D
- ◯ 80
- ◯ FD

Question 3 (1 point)

Given a decimal number -25, what is the respective sign-magnitude, 1's complement and 2's complement value in hexadecimal form?

- ◯ sign-magnitude = E7, 1's complement = E7, 2's complement = E7
- ◯ sign-magnitude = 99, 1's complement = E6, 2's complement = E7
- ◯ sign-magnitude = 99, 1's complement = E7, 2's complement = E7
- ◯ sign-magnitude = E6, 1's complement = 99, 2's complement = E7
- ◯ sign-magnitude = E7, 1's complement = E6, 2's complement = E7

Question 4 (1 point)

Manually perform the following binary subtraction: 0110 0110 - 1110 1000

Question 5 (1 point)

Which of the following could potentially result in an overflow

- ☐ (+ve) - (+ve)
- ☐ (-ve) - (-ve)
- ☐ (+ve) - (-ve)
- ☐ (-ve) - (+ve)

Question 6 (1 point)

When performing addition for of 12-bit 2's complement number, what does the result of bit 12 indicates?

- ◯ Overflow
- ◯ Borrow
- ◯ Carry
- ◯ Negative

INF1001 – Introduction to Computing (Quiz)

Quiz 2.6

Question 1 (1 point)

For a 1's complement binary number 1011 0111, what is the signed-extended 16-bit value?

- ◯ 1000 0000 0011 0111
- ◯ 1111 1111 1011 0111
- ◯ 1111 1111 0011 0111
- ◯ 1000 0000 1011 0111

Question 2 (1 point)

When two n-bit numbers are added together, how many bits is the length of the sum?

- ◯ (n + 2) bits
- ◯ (n + 1) bits
- ◯ (2 x n) bits
- ◯ (n) bits

Question 3 (1 point)

Which pair(s) of 8-bit 2's complement arithmetic will not result in overflow nor carry?

- ☐ -52 + -77
- ☐ 52 + 76
- ☐ 52 + 77
- ☐ -52 + -76

Question 4 (1 point)

Given two 8-bit 2's complement binary numbers 1100 0110 and 1000 0100, express the result of the binary addition as a 12-bit number.

Question 5 (1 point)

An unsigned number FE24 is to be sign-extended to a 32-bit number, what is the hexadecimal value?

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Quiz 2.7

Question 1 (1 point)

Using a calculator, perform the following arithmetic operation: F4 + 8A

- 007E
- 7E
- FF7E
- 807E

Question 2 (1 point)

Given a calculator uses 16-bit to represent binary numbers, what is the largest positive number it can represent?

- 65536
- 32768
- 32767
- 65535

Question 3 (1 point)

Using a calculator, what is the results for adding these two 2's complement binary numbers: 1010 1111 0001 1010 0000 and 1100 1011. Express you answer in decimal.

- 717419
- -331413
- 717163
- -331157

Question 4 (1 point)

Using a calculator, add F25 and E4B. Express the answer in decimal.

Question 5 (1 point)

Using a calculator, convert decimal -25564 to 16-bit binary.

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Quiz 2.8

Question 1 (1 point)

Given a fractional binary number 10110.0011, what is the decimal value?

Question 2 (1 point)

Express decimal number 32.75 as fractional binary form

Question 3 (1 point)

When a decimal number 0.64 is expressed in binary with 5-bit precision, which binary representation give the least amount of error?

- 0.10011
- 0.11001
- 0.10111
- 0.10100

Question 4 (1 point)

In 32-bit IEEE754 floating point representation, which of the following statement is correct?

- 1 sign bit, 7 mantissa bit, 24 exponent bit
- 1 sign bit, 8 exponent bit, 23 mantissa bit
- 1 sign bit, 8 mantissa bit, 23 exponent bit
- 1 sign bit, 7 exponent bit, 24 mantissa bit

Question 5 (1 point)

Which is the most significant drawback of fractional representation using binary number?

- Different bit length is required
- Arithmetic operation is more complex
- Conversion process is tedious and need to be performed manually
- Error could be present when representing decimal number in binary

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Quiz 2.9

Question 1 (1 point)

What is the 32-bit value in hexadecimal for IEEE754 to represent 0.0.

Question 2 (1 point)

What is the exponent value for the IEEE754 32-bit binary value C200 8000?

- 194
- -62
- 132
- -124

Question 3 (1 point)

Given a 32-bit IEE 754 floating point number represented in hexadecimal form as C200 8000, manually compute its floating point value.

Question 4 (1 point)

From the 32-bit binary number representing IEEE754 floating point number, which bit determine the sign of the floating point number?

- Bit 0
- Bit 31
- Bit 1
- Bit 30

Question 5 (1 point)

Using the floating point calculator (www.h-schmidt.net/FloatConverter/IEEE754.html), which pair of floating point number(s) will result in the same 32-bit binary representation?

- [ ] 999999.9999 and 999999.999
- [ ] 100.001 and 100.01
- [ ] 1000000.001 and 1000000.01
- [ ] 1.0000000000001 and 1.00000000001

INF1001 – Introduction to Computing (Quiz)

Quiz 2.10

Question 1 (1 point)

Which of the following is (are) valid 2-bit gray code sequence?

- [ ] 00, 01, 11, 10
- [ ] 01, 11, 10, 00
- [ ] 00, 01, 10, 11
- [ ] 11, 00, 01, 10

Question 2 (1 point)

With reference to the ASCII table, what is the character string for these ASCII code 49 6E 46 31 30 30 31?

Question 3 (1 point)

Given a Binary Code Decimal (BCD) code 1001 0111 0101, what is the decimal value?

Question 4 (1 point)

In Binary Coded Decimal (BCD), what is the BCD result when these two BCD numbers are added together: 1001 0111 + 0001 0101?

- ◯ 1011 0010
- ◯ 0001 0001 1100
- ◯ 1010 1100
- ◯ 0001 0001 0010

Question 5 (1 point)

The following is a partial 3-bit gray code sequence, identify the missing 3-bit value in blank: 011, 010, ___, 111, 101, ...

- ◯ 001
- ◯ 110
- ◯ 000
- ◯ 100

INF1001 – Introduction to Computing (Quiz)

Quiz 2.11

Question 1 (1 point)

Given a 7-bit binary data 101 0111, what is the 8-bit data when an even parity bit is added to the MSB of the data?

Question 2 (1 point)

An ISP (Internet Service Provider) offers fiber broadband connection with a speed of 1 Gbps. How long will it take to down a data file with a size of 150 GB?

- ◯ 1200 seconds
- ◯ 150 seconds
- ◯ 120
- ◯ 1500 seconds

Question 3 (1 point)

Given a 4 characters string of 8-bit data (92, DD, 8C, 62) where 7-bit are encoded using ASCII and the LSB is an odd parity bit, which character is erroneous?

Question 4 (1 point)

Which of the following technology uses serial communication?

- ☐ Bluetooth
- ☐ USB
- ☐ Wi-Fi
- ☐ 5G

Question 5 (1 point)

What is the biggest challenge when transmitting data in parallel?

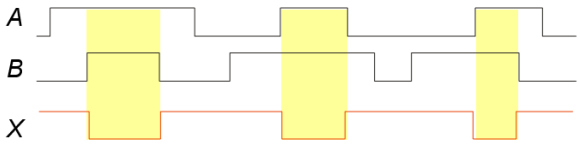
- ◯ Data arrived at destination out of sync
- ◯ Data communication only requires a single wire
- ◯ Data communication is only possible for long distance
- ◯ Data arrived at destination too quickly

INF1001 – Introduction to Computing (Quiz)

Quiz 3.1

Question 1 (1 point)

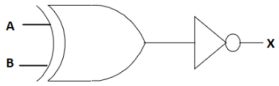
A 2-input gate produces the output shown (X represents the output.) This is a



- ◯ OR gate
- ◯ NAND gate
- ◯ NOR gate
- ◯ AND gate

Question 2 (1 point)

What is the truth table output for the corresponding logic circuit?

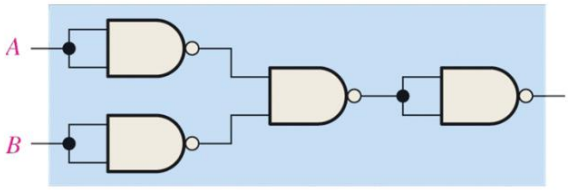


A B	X
0 0	
0 1	
1 0	
1 1	

- ◯ 1 0 0 1
- ◯ 0 1 1 0
- ◯ 0 0 1 1
- ◯ 0 1 1 1

Question 3 (1 point)

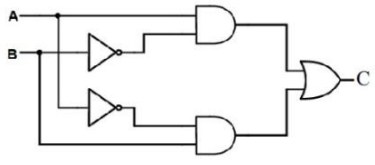
The circuit shown is equivalent to an



- ◯ none of the above
- ◯ XOR gate
- ◯ AND gate
- ◯ OR gate

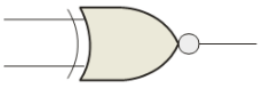
Question 4 (1 point)

Identify the logic gate for the following circuit.



Question 5 (1 point)

What is the gate represented by the following symbol?



INF1001 – Introduction to Computing (Quiz)

Quiz 3.2

Question 1 (1 point)

Which of the following boolean algebra is incorrect?

- X + ~X = 1
- X.X = 0
- X.~X = 0
- X.1 = X

Question 2 (1 point)

Simplify the boolean equation:

$$A.\overline{B} + A(\overline{B+C}) + B(\overline{B+C})$$

- $\overline{A}.B$
- $\overline{A}.C$
- $A.\overline{B}$
- $A.\overline{C}$

Question 3 (1 point)

Simply the following boolean equation: (X + Y).(X + ~Y)

Question 4 (1 point)

Using De Morgan theorem, what of the following is NOT equivalent to

$$\overline{A.\overline{B} + C.\overline{D}}$$

- $(\overline{A} + B).(\overline{C} + D)$
- $\overline{(A.\overline{B}).(\overline{C.\overline{D}})}$
- $(A + \overline{B}).(C + \overline{D})$
- $(\overline{A}.\overline{C} + \overline{A}.D + B.\overline{C} + B.D)$

Question 5 (1 point)

Simply the following boolean equation: (x + y).(x + z)

INF1001 – Introduction to Computing (Quiz)

Quiz 3.3

Question 1 (1 point)

How many inputs (I) and outputs (O) can one combinational circuit has?

- I = as many as required, O = 1
- I = 1, O = as many as required
- I = 1, O = 1
- I = as many as required, O = as many as required

Question 2 (1 point)

In a combinatorial circuit with 4-input express in canonical form as:

$$f(A,B,C,D) = \sum m(1,5,13)$$

Which is the correct logic equation for the circuit.

- f = A.B.C.~D + A.~B.C.~D + ~A.B.~C.~D
- f = ~A.~B.~C.D + ~A.B.~C.D + ~A.B.~C.~D
- f = ~A.~B.~C.D + A.~B.C.~D + A.~B.C.D
- f = ~A.~B.~C.D + ~A.B.~C.D + A.B.~C.D

Question 3 (1 point)

Given a 3-input product term as X.~Y.Z, what is the corresponding sum term?

- ~X + Y + ~Z
- X + ~Y + Z
- X + Y + Z
- ~X + ~Y + ~Z

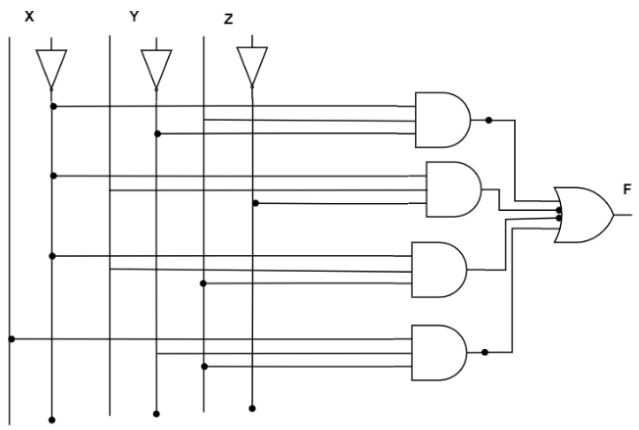
Question 4 (1 point)

Identify one maxterm from the following truth table, indicate the index in your answer.

Index	A	B	C	g
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

Question 5 (1 point)

In the following logic circuit, how many product terms can you identify?



INF1001 – Introduction to Computing (Quiz)

Quiz 3.4

Question 1 (1 point)

Simplify the following boolean equation: Z = A.(1 + B + ~C + ~Y)

Question 2 (1 point)

Given a combinatorial circuit has 3 inputs has 6 product terms when expressed in SOP form, how many sum terms do you expect when it is expressed in POS form?

Question 3 (1 point)

For a 2-input POS boolean equation Z = (A + B).(A + ~B), which is the corresponding SOP equation?

- ◯ Z = A.B
- ◯ Z = ~A.B + A.B
- ◯ Z = A.~B + A.B
- ◯ Z = A.B + ~A.~B

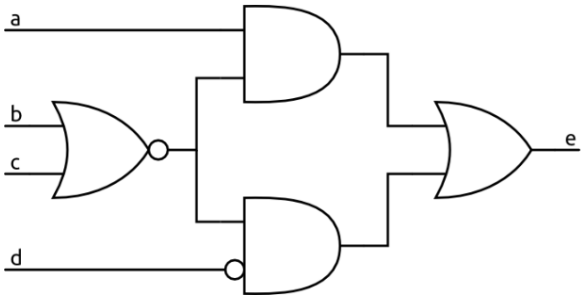
Question 4 (1 point)

Which of the following regarding don't care conditions are correct?

- ☐ Don't care refers to input combinations that never occurs.
- ☐ Output conditions are required to be 0 for these input combinations.
- ☐ Output conditions are can either be 1 or 0 for these input combinations.
- ☐ Output conditions are required to be 1 for these input combinations.

Question 5 (1 point)

Which is the correct logic equation representing the following circuit?



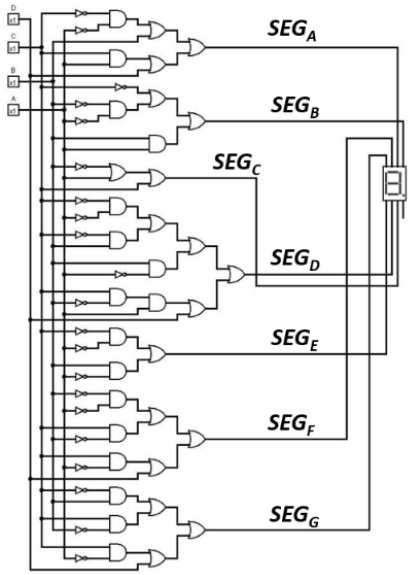
- ◯ e = a.(~b + c) + ~d.(~b + c)
- ◯ e = a.~(b + c) + d.~(b + c)
- ◯ e = a.~(b + c) + ~d.~(b + c)
- ◯ e = a + ~(b + c) + ~d + ~(b + c)

INF1001 – Introduction to Computing (Quiz)

Quiz 3.5

Question 1 (1 point)

For the following 7-segment decoder circuit, what is the boolean equation for segment E?



- ◯ A.~C + ~A.~B
- ◯ ~A.~C + ~A.B
- ◯ ~A.C + ~A.~B
- ◯ ~A.~C + A.~B

Question 2 (1 point)

For a 7-segment display, enter the 7 binary bits (e.g. 000 0000) that will display digit 4 given that the 7-bit are arranged in segment *abcdefg*.

Question 3 (1 point)

Simplify a 2-input boolean equation Z = A + ~A.B

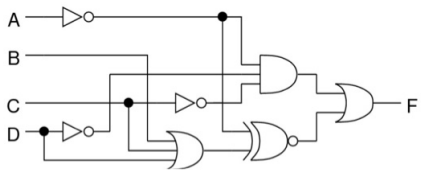
Question 4 (1 point)

What is the impact of having a combinatorial circuit with more logic gates.

- ☐ The circuit will likely take longer to compute an operation.
- ☐ The circuit will occupy less space and hence smaller.
- ☐ The circuit will consume more power.
- ☐ The circuit will likely run faster.

Question 5 (1 point)

For the following circuit, determine these 4 performance matrices. Number of gates (g), number of gat inputs literals (gi), maximum path length (mpl) and maximum fan-in (mfi).



- ◯ g = 4, gi = 10, mpl = 3, mfi = 2
- ◯ g = 7, gi = 13, mpl = 3, mfi = 3
- ◯ g = 4, gi = 13, mpl = 3, mfi = 3
- ◯ g = 7, gi = 10, mpl = 2, mfi = 3

INF1001 – Introduction to Computing (Quiz)

Quiz 4.1

Question 1 (1 point)

For a half adder circuit, which are the conditions for the sum output to be set to 1?

- [ ] A = 1, B = 1
- [ ] A = 0, B = 1
- [ ] A = 1, B = 0
- [ ] A = 0, B = 0

Question 2 (1 point)

Determine the two entries (highlighted in red) in the truth table of a full adder as shown below.

A_i	B_i	C_i	S_i	C_{i+1}
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

- ◯ $S_i = 0, C_{i+1} = 1$
- ◯ $S_i = 1, C_{i+1} = 0$
- ◯ $S_i = 1, C_{i+1} = 1$
- ◯ $S_i = 0, C_{i+1} = 0$

Question 3 (1 point)

For a single-bit full adder circuit, how many input combinations will result in both sum and carry out to be set to 1?

Question 4 (1 point)

Indicate the index (row) that is incorrect for the following truth table for a full adder.

Index	A_i	B_i	C_i	S_i	C_{i+1}
0	0	0	0	**0**	**0**
1	0	0	1	**1**	**0**
2	0	1	0	**0**	**1**
3	0	1	1	**0**	**1**
4	1	0	0	**1**	**0**
5	1	0	1	**1**	**0**
6	1	1	0	**0**	**1**
7	1	1	1	**1**	**1**

- [ ] 1
- [ ] 7
- [ ] 5
- [ ] 6
- [ ] 3
- [ ] 2
- [ ] 4
- [ ] 0

Question 5 (1 point)

Consider the use of multiple single-bit full adder circuits, how many gates will be required to build a 64-bit ripple adder?

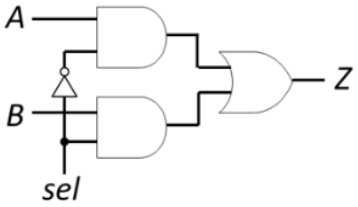
INF1001 – Introduction to Computing (Quiz)

Quiz 4.2

Question 1 (1 point)

List the two missing entries in the truth table for a 2-to-1 multiplexer as shown below. Indicate your answer as (X1 X2) with X1 being the upper entry.

A	B	sel	Z
×	0	1	0
×	1	1	
0	×	0	
1	×	0	1



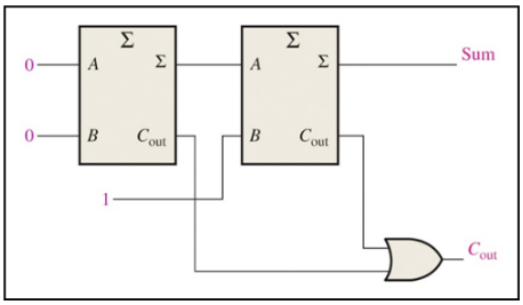
Question 2 (1 point)

For a 4-bit ripple adder, which pair of inputs will take the longest time to compute?

- A=0000 & B=0000
- A=0001 & B=0001
- A=0011 & B=0001
- A=0000 & B=0001

Question 3 (1 point)

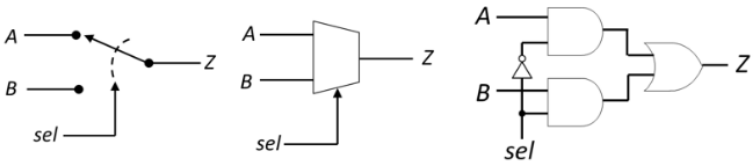
For the full-adder shown, assume the input bits are as shown with A = 0, B = 0, Cin = 1. The Sum and Cout will be



- Sum = 0, Cout = 0
- Sum = 0, Cout = 1
- Sum = 1, Cout = 1
- Sum = 1, Cout = 0

Question 4 (1 point)

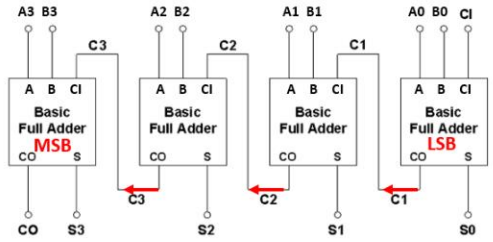
The following show 3 circuits of a 2-to-1 multiplexer, under what conditions will output Z=B?



- sel = B
- sel = 0
- sel = A
- sel = 1

Question 5 (1 point)

For the following 4-bit adder, given A=0110 and S=1000, which is a possible value for B?

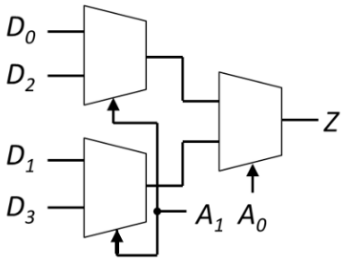


INF1001 – Introduction to Computing (Quiz)

Quiz 4.3

Question 1 (1 point)

For the following 4-to-1 multiplexer, what are the A1 and A0 to enable output Z to select D_1? Indicate your answer as (A1 A0).

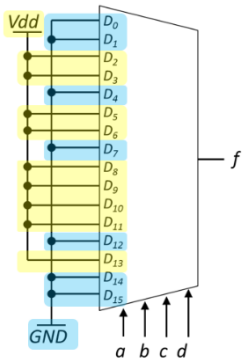


Question 2 (1 point)

For the implementation of boolean function using multiplexer, where should the input be connected to if the product term is a don't care?

$$f(a,b,c,d) = \sum m(2,3,5,6,8,9,10,11,13)$$

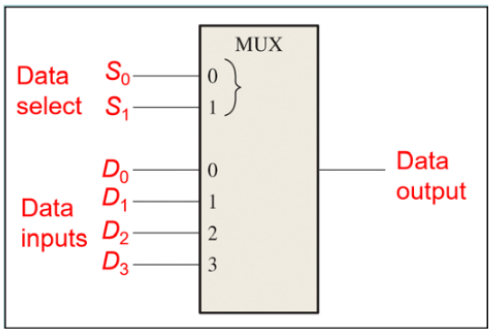
D	a b c d	f
D_0	0 0 0 0	0
D_1	0 0 0 1	0
D_2	0 0 1 0	1
D_3	0 0 1 1	1
D_4	0 1 0 0	0
D_5	0 1 0 1	1
D_6	0 1 1 0	1
D_7	0 1 1 1	0
D_8	1 0 0 0	1
D_9	1 0 0 1	1
D_{10}	1 0 1 0	1
D_{11}	1 0 1 1	1
D_{12}	1 1 0 0	0
D_{13}	1 1 0 1	1
D_{14}	1 1 1 0	0
D_{15}	1 1 1 1	0



- Can only connect to GND
- Can only connect to VDD
- Can only connect to don't care
- Connect either to VDD or GND

Question 3 (1 point)

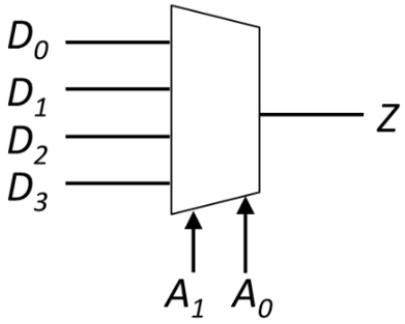
If the data select lines of the MUX are S_1S_0 = 11, the output will be



- HIGH
- Equal to D_0
- LOW
- Equal to D_3

Question 4 (1 point)

A 4-to-1 multiplexer is used to implement a logic equation: Z=A.~B. What should input A & B be connected to?



- Connect A to D1 and B to D0.
- Connect A to A1 and B to A0.
- Connect A to D3 and B to D4.
- Connect A to D0 and B to D1.

Question 5 (1 point)

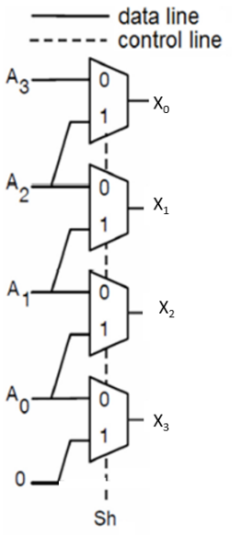
For a 64-to-1 multiplexer, how many select inputs do you expect?

INF1001 – Introduction to Computing (Quiz)

Quiz 4.4

Question 1 (1 point)

For the following circuit, what is the output (expressed in X3X2X1X0) when A3..0 = 0101 and Sh = 0?



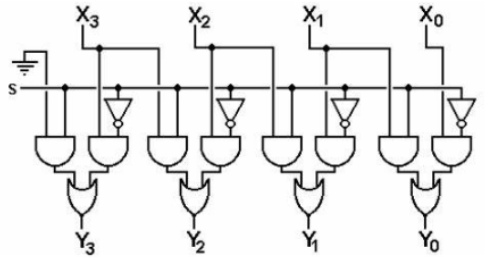
Question 2 (1 point)

What is the key limitation to use a shifter circuit to perform arithmetic multiplication (or division)?

- It requires more logic gates compared to using an arithmetic multiplier (or divisor).
- It is slower compared to using an arithmetic multiplier (or divisor).
- It can only perform multiplication (or division) in multiple of 2.
- It can only be done for limit number of bits.

Question 3 (1 point)

Given X3-0 = 0110, what is the output when S=1?



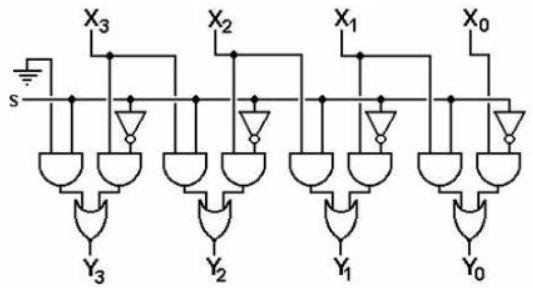
- Y3-0 = 1001
- Y3-0 = 0011
- Y3-0 = 1100
- Y3-0 = 0110

Question 4 (1 point)

Express decimal value 24 in 8-bit binary, perform a logically shift 2-bit to the left, what is the answer in decimal?

Question 5 (1 point)

Given a 4-bit circuit shown below, what is the function of this circuit?



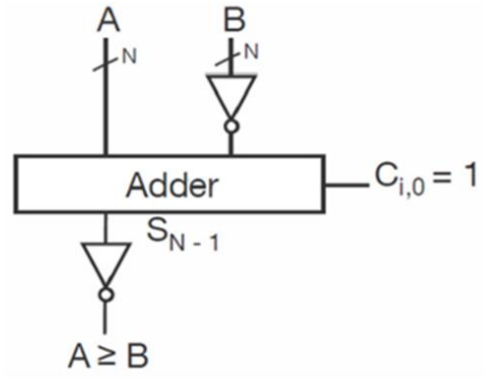
- 1's complement
- Logical shift right
- Logical shift left
- 2's complement

INF1001 – Introduction to Computing (Quiz)

Quiz 4.5

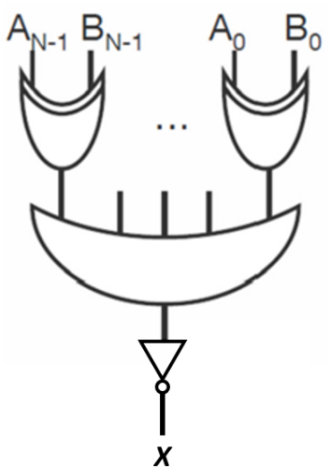
Question 1 (1 point)

In the following circuit, given N=8-bit, what does S_7 indicates?



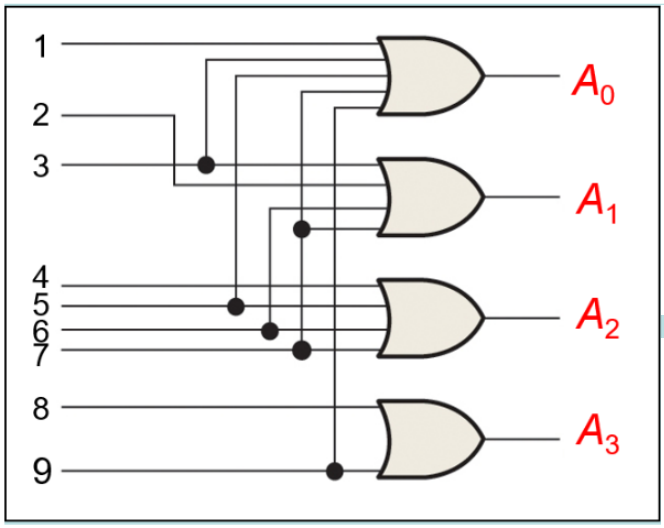
Question 2 (1 point)

A comparator circuit is as shown below, what does output X indicates?



Question 3 (1 point)

The decimal-to-binary encoder shown does not have a zero input. This is because



- when zero is the input, all lines should be LOW
- another encoder is used for zero
- none of the above
- zero will produce illegal logic level

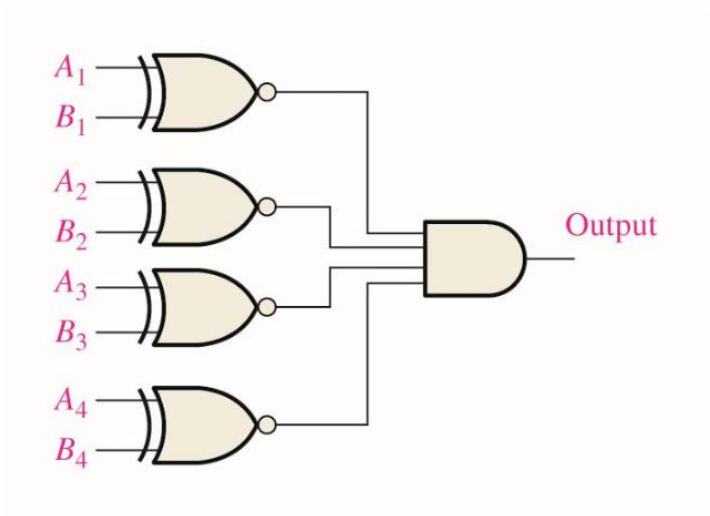
Question 4 (1 point)

If you expand two 4-bit comparators to accept two 8-bit numbers, the output of the lower-order comparator is

- equal to the final output
- connected to the output of the higher-order comparator
- not used
- connected to the cascading inputs of the higher-order comparator

Question 5 (1 point)

The output will be LOW if



- A > B
- A = B
- A < B
- A != B

INF1001 – Introduction to Computing (Quiz)

Quiz 4.6

Question 1 (1 point)

How many transistors are required to build a 2-input XOR gate?

Question 2 (1 point)

Which statements (s) about FPGA and ASIC are correct?

- [ ] ASIC consumes lesser power and occupy less chip area compared to FPGA.
- [ ] FPGA are easily reprogrammable compared to ASIC.
- [ ] FPGA is higher in terms of cost compared to ASIC at low volume.
- [ ] ASIC is simpler to design compared to FPGA.

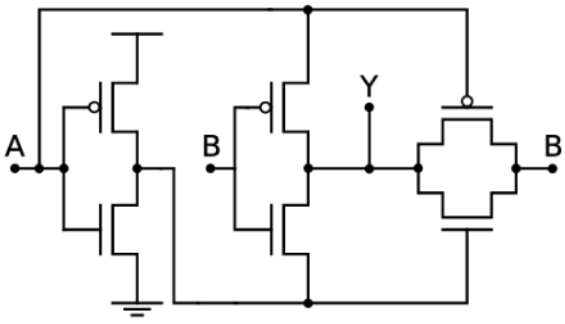
Question 3 (1 point)

When you multiply two n-bit numbers together, what is the maximum width of the result?

- ◯ (2n+1) bit
- ◯ (n + 1) bit
- ◯ (2n) bit
- ◯ (n^2) bit

Question 4 (1 point)

Which logic gate does this circuit represents?



- ◯ XOR
- ◯ XNOR
- ◯ NOR
- ◯ NAND

Question 5 (1 point)

When we refer to the state of the art semiconductor manufacturing technology in terms of nanometer (e.g. 5nm), what are we referring to with respect to the transistor?

INF1001 – Introduction to Computing (Quiz)

Quiz 4.7

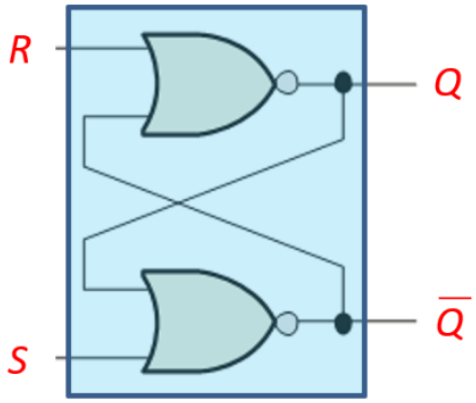
Question 1 (1 point)

S=R=1 is considered a NOT ALLOWED state for an SR latch, what do you think will happen to the SR latch when S and R are set to 1 concurrently?

- ◯ It will explode.
- ◯ Content will be cleared to 0.
- ◯ Content cannot be determined.
- ◯ Content will be set to 1

Question 2 (1 point)

For an SR latch as shown below where S=R=0 and Q=1, what will happen when S is change from 0 to 1 (R remains at 0)?



Question 3 (1 point)

In an active-LOW SR latch, which is the inputs for S and R to change the content of the latch to 1?

- ◯ S=1, R=1
- ◯ S=0, R=0
- ◯ S=1, R=0
- ◯ S=0, R=1

Question 4 (1 point)

Given the current content of an SR latch is 1, how do you clear the content to change it to 0 instead?

Question 5 (1 point)

For an SR latch, which signal indicates the content store inside the latch?

- ◯ R
- ◯ Q
- ◯ Q-bar
- ◯ S

INF1001 – Introduction to Computing (Quiz)

Quiz 4.8

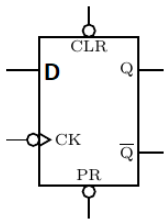
Question 1 (1 point)

The output of a D latch will not change if

- ◯ D is LOW
- ◯ the current content is LOW
- ◯ Enable is not active
- ◯ all of the above

Question 2 (1 point)

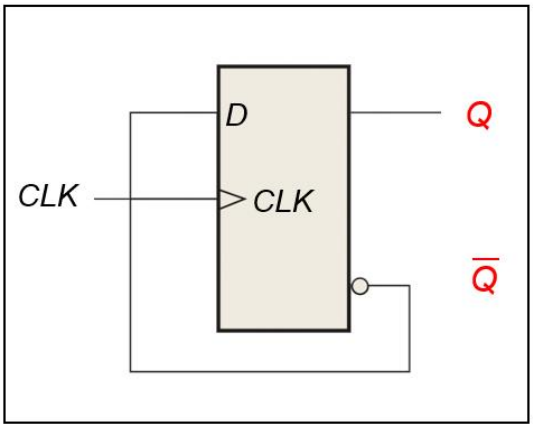
For a D flip-flop with asynchronous active-LOW CLR and PR, what happen to the content Q when the following are asserted: CLR=1 and PR=0?



- ◯ Q will be toggled.
- ◯ Q will remain the same.
- ◯ Q goes to 0.
- ◯ Q goes to 1.

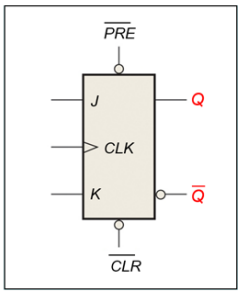
Question 3 (1 point)

The D flip-flop shown will _____on the next clock pulse.



Question 4 (1 point)

How many asynchronous inputs does the J-K flip-flop below have?



Question 5 (1 point)

For an active-LOW JK flip-flop, what happen to its content when both J & K inputs are '0'?

- ◯ Content will toggle it state.
- ◯ Content will be set to 1.
- ◯ Content will be cleared to 0.
- ◯ Content will remain the same as previous state.

INF1001 – Introduction to Computing (Quiz)

Quiz 4.9

Question 1 (1 point)

As extracted from the datasheet of a D-type flip flop HCD4013 from ST (www.st.com/resource/en/datasheet/hcf4013.pdf), only the minimum and typical data setup time are given. What do you think is the maximum setup time?

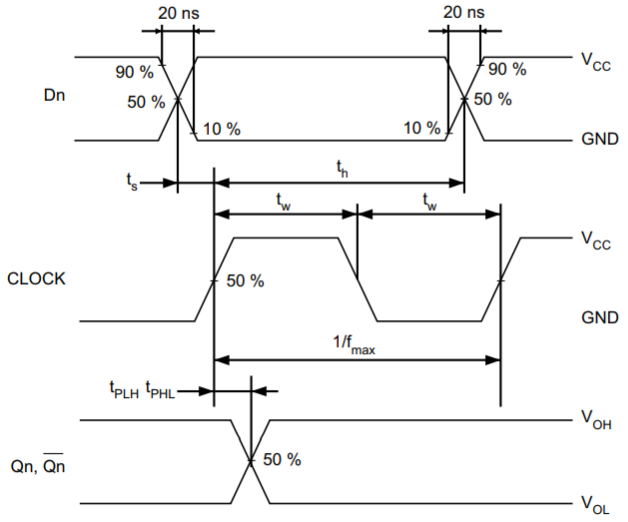
Table 7. Dynamic electrical characteristics
(T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 kΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test condition	Value(1)			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_s	Data setup time	5	40	20		ns
		10	20	10		
		15	15	7		

- ◯ Unlimited
- ◯ Indeterministic
- ◯ Clock period - t_h
- ◯ Same as typical time

Question 2 (1 point)

As extracted from the datasheet of a D-type flip flop HCD4013 from ST (www.st.com/resource/en/datasheet/hcf4013.pdf), what does t_h refers to?



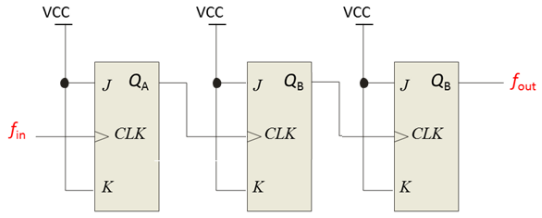
Question 3 (1 point)

For a D flip-flop device, what happen when the setup or hold time are not met according to the timing requirements specified in the datasheet?

- ◯ Output will be set to 0.
- ◯ Output will be set to 1.
- ◯ Output is indeterministic.
- ◯ Output will toggle its value.

Question 4 (1 point)

For the following circuit, given f_{in} is 400 MHz, what is the frequency f_{out} ?



Question 5 (1 point)

Which component inside a CPU are synchronous circuit?

- ☐ Adder unit
- ☐ Memory
- ☐ Arithmetic Logic Unit (ALU)
- ☐ Control Unit