Bisrat Asefaw CSS 422 (Hardware) Prof. Yang

Homework Problem Set #4

Note:

Submit each circuit file separately, with a meaningful name for each file! Do not Zip!

- 1. Consider the logic gate circuit shown below (5 points)
 - 1. (2 points) Derive a Boolean equation for the output X. You don't need to simplify this equation, but feel free to try!

$$(\overline{(A \oplus C)} + \overline{B})\overline{((B+D)\overline{B})}$$

2. (3 points) Draw a truth table for the circuit.

	\mathbf{A}	В	C	D	X
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
A	1	0	1	0	0
В	1	0	1	1	0
C	1	1	0	0	1
D	1	1	0	1	1
\mathbf{E}	1	1	1	0	0
${f F}$	1	1	1	1	0

3. (14 points) Design a combinational circuit system.

Design a combinational circuit with three inputs x,y,z, and three outputs A,B,C. When the binary inputs is 0,1,2, or 3, the binary output is two greater than the input. When the binary input is 4,5,6, or 7, the binary output is one less than the input.

Please answer all of the following sub-questions.

1) (3 points) x, y, z are inputs and A, B, C are outputs. Draw a truth table for the given function.

X	y	Z	A	В	C
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

2) (3 points) Based on the truth table you draw, build Karnaugh maps for the output A,B,C.

For A	~x~y	~xy	xy	x~y
~Z		1	1	
Z		1	1	1

For B	~x~y	~xy	xy	x~y
~Z	1			1
Z	1		1	

For C	~x~y	~xy	xy	x~y
~Z			1	1
Z	1	1		

3) (3 points) Derive (as simple as possible) Boolean equations for A,B,C using the Karnaugh maps

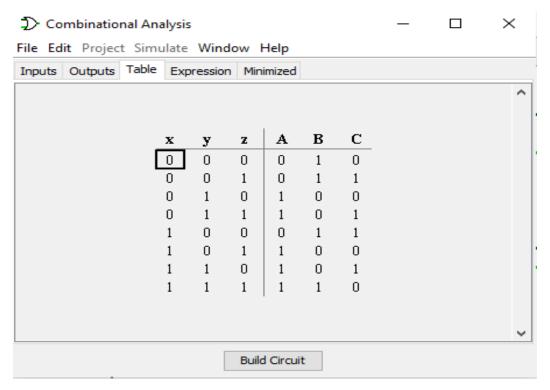
$$\bullet \quad \mathbf{A} = \mathbf{y} + \mathbf{z}\mathbf{x}$$

•
$$\mathbf{B} = \mathbf{x} \mathbf{y} + \mathbf{x} \mathbf{y} \mathbf{z} + \mathbf{x} \mathbf{y} \mathbf{z}$$

•
$$C = \sim xz + x \sim z$$

4) (3 points) Based on the Boolean equations, draw the logical gate diagram (circuit) for this system in Logisim. Save the circuit file and submit it as an individual file!

5) (2 points) Test your circuit with the Logisim simulation and generate the truth table (In logisim, project-->analyze circuit-->table). Copy & past the table in your submission!



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