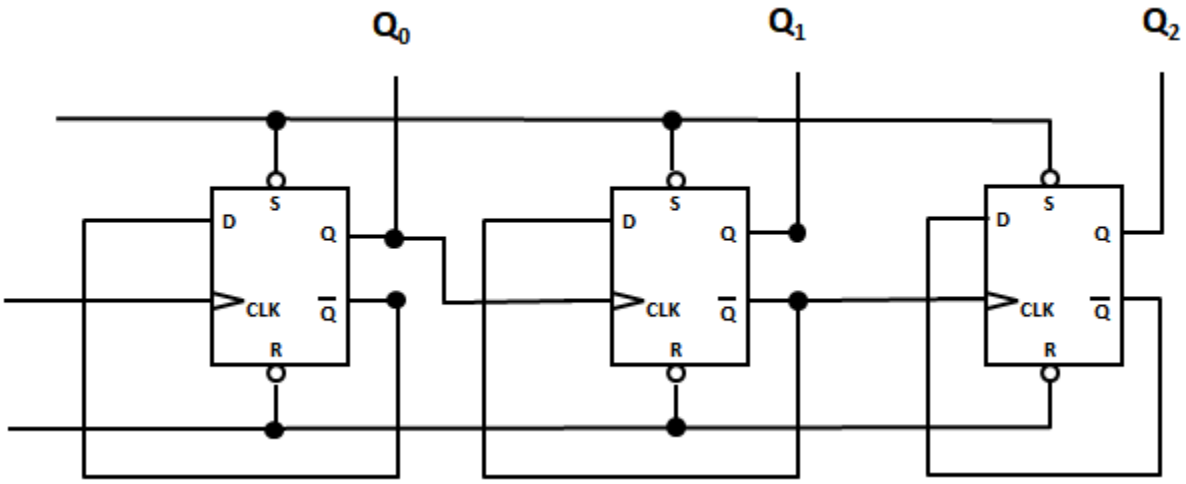
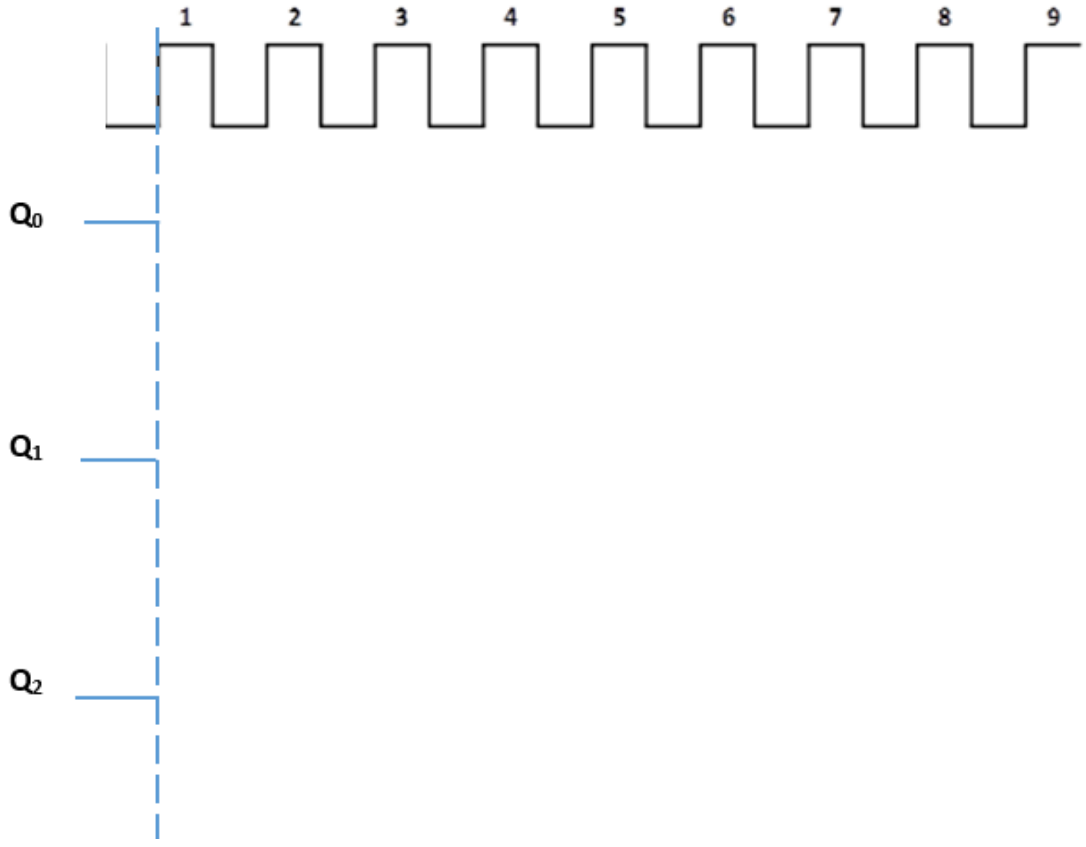
1. **A circuit is shown here.**



You can assume Q_2, Q_1 and Q_0 are set to 0 (logic low) before the first clock rising edge. Q_2, Q_1 and Q_0 will start changing at the first clock rising edge.

(1) Given the circuit in the description, please express the signals of Q_2, Q_1 and Q_0 as the clock signal changes (i.e., the timing graph of Q_2, Q_1 and Q_0). A skeleton of the answer is shown below.



(2) Based on the analysis in the previous question, please draw a state diagram for $Q_2Q_1Q_0$.

2. This is a sequential circuit system with one JK flip-flop, one D flip-flop, and one input signal "W". The output of JK flip-flop is named as A and the output of D flip-flop is named as B. The value of AB is considered a system state. The state (i.e., the value of AB) changes as follows: if W is 1, the state does not change; if W is 0, the state changes in the order of 01, 11, 00, 10, and repeat. Please design such a circuit with the required state changes. Please show the K-map for Ja, Ka, and Db.