CSS 422 Midterm exam Spring, 2017

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(Signed)_____

Number conversion. Show your work.
1.1 Convert 4913 from decimal to base seven.

1.2 Negate 183 decimal, and express the 16 bit twos complement result both in binary and hex.

1.3 Express 23578.5 as a single precision IEEE floating point number. Show your answer in hex.

1.4 Express -23578.5 as a double precision IEEE floating point number. Show your answer in hex.

2.1 Convert the following assembly code to machine code, expressed in hex.

```
    ORG $400
    LEA  $1000,A7

    CLR.L  D4


    MOVE.L  -(A7),D4
```

2.2 Why is each instruction invalid?

```
CLR.W       #$5F5F

MOVE.K   #$3F12,D4

MOVE.W    (A3)+,D8
```

2.3 Before each instruction below in executed, the condition code XNZVC contains %11001, D2 contains $AA557FFE, D7 contains $000000FE. What will be in these 5 bits of CCR after the instruction is executed? Evaluate each instruction individually; they are not meant to be in sequence.

		X	N	Z	V	C
2.3.1	BNE LABEL					
2.3.2	MOVE.W D2,D7					
2.3.3	CLR.B D2					
2.3.4	LEA (4,SP),A0					
2.3.5	CMP.L D2,D7					

3) Rewrite the following C code to M68K assembly language. The first part has been started for you. You are to translate the given code; use of a lookup table is not a correct solution.

```
unsigned char letter;
int value = 0;
/*  get letter from the user */
if (‘0’ <= letter && letter <= ‘9’)   /* '0' = 48;  '9' = 57 */
        value = letter - ‘0’;
else if (‘A’ <= letter && letter <= ‘F’)   /* 'A' = 65 ;  'F' = 70 */
        value = letter -‘A’ + 10;

        ORG $A000
letter   DS  1
value   DC.W 0
        ORG $800
        ...
        MOV.B  letter,D0
```

4.1 Assume that a 68K machine has a four stage pipeline given below, and that each stage executes in one time chunk.

a) Obtain next instruction (IA)
b) Decode the instruction (DC)
c) Fetch operand data (OA)
e) Execute the instruction (EX)

With no pipeline problems, nine instructions will execute in 12 time chunks. How many chunks will the following instructions need? **Identify** the instructions that slow the pipeline.

```
LEA     Peri,A0      A0 points to the memory-mapped peripheral
MOVE.B  D0,(6,A0)    Move the least-significant byte of D0 to the peripheral
ROR.L   #8,D0        Rotate D0 to get the next 8 bits
MOVE.B  D0,(4,A0)    Move the next byte, bits 8 to 15, to the peripheral
ROR.L   #8,D0
MOVE.B  D0,(2,A0)
ROR.L   #8,D0
MOVE.B  D0,(0,A0)
ROR.L   #8,D0        After four rotations D0 is back to its old value
```

4.2 Suppose that processor A runs at 72 MHz with a 5 stage pipeline and processor B runs at 100 MHz with a 3 stage pipeline. With the pipeline working perfectly, which processor has faster throughput?

4.3 At the perfect pipelining limit, what is the performance ratio of the two processors above?

4.4 What is the execution time of an instruction on processor A without pipelining?