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CSS 422 (Hardware)
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Homework Problem Set #3

Q1. Cache and Memory mapping (9 points)

Suppose a byte-addressable memory has a total memory capacity of 2M bytes and the cache consists of 64 blocks, where each block contains 32 bytes.

1. Direct Mapping

  1) Divide the bits into tag, block and offset bits.

- Memory = 2^{21} bytes
- Cache # block = 2^6
- Each block contains = 32 bytes = 2^5 bytes

Tag = 10 bits Block = 6 bits, Offset bits = 5 bits

2) What is the tag, line and offset for the address $123A63, in hexadecimal?

Binary representation: 1001000111 010011 00011
tag: 0x__**247**_____
line: 0x__**13**_____
offset: 0x__0**3**_____

2. Fully Associative Mapping

  1) Divide the bits into tag and offset bits.

  Tag: 16 bits, Offset: 5bits

  2) What is the tag and offset for the address $123A63, in hexadecimal?

Binary representation: 1001000111010011 00011
tag: 0x__**91D3**__
offset: 0x____0**3**_____

3. 4-way set associative mapping

  1) Divide the bits into tag, set and offset bits

    Set = # blocks/n = 64/4 = 16 = 2^4

 Tag: 12 bits, Set: 4 bits, Offset: 5 bits

2) What is the tag, set and offset for the address $123A63, in hexadecimal?

Binary representation: 100100011101 0011 00011

        tag: 0x__91D___
        set: 0x___3_____
        offset: 0x___03_____

Q2. Cache hit and miss (6 points)

Suppose we have a computer that uses a memory with a total memory capacity of 256 bytes. The computer has a 16-byte direct-mapped cache with 4 bytes per block. The computer accesses a number of memory locations throughout the course of running a program. Here is the memory addresses in this exact order: **0x91, 0xA8, 0xA9, 0xAB, 0xAD, 0x93, 0x6E, 0xB9, 0x17, 0xE2, 0x4E, 0x4F, 0x50, and 0xA4.** The cache Tag and Block information has been filled out as shown below.

- Memory 256 byte = 28
- # blocks = 16/4 = 4 = 22
- Offset = 22

Tag = 4 bits   block: 2 bits, offset: 2 bits

Tag (binary)	Block #	offset 0	offset 1	offset 2	offset 3
1110	0				
0001	1				
1011	2				
0110	3				

Address	Tag	Block	Offset	Hit or Miss
91	1001	00	01	Miss
A8	1010	10	00	Miss
A9	1010	10	01	Hit
AB	1010	10	11	Hit
AD	1010	11	01	Miss
93	1001	00	11	Hit
6E	0110	11	10	Miss
B9	1011	10	01	Miss
17	0001	01	11	Hit
E2	1110	00	10	Miss
4E	0100	11	10	Miss
4F	0100	11	11	Hit
50	0101	00	00	Miss

A4	1010	01	00	Miss

1. What is the hit ratio for the entire memory reference sequence (given in bold)?

- **Hist ratio = 5/14 * 100 = 35.7 %**

2. What memory blocks will be in the cache after the last address has been assessed? Please fill in the Tag and Block first. Then, fill the actual address value for each offset location in the corresponding cell.

Tag (binary)	Block #	offset 0	offset 1	offset 2	offset 3
0101	0	50	51	52	53
1010	1	A4	A5	A6	A7
1011	2	B8	B9	BA	BB
0100	3	4C	4D	4E	4F