» Kontron User's Guide «

# ETXexpress®-AI Computer-on-Module (COM)

Version 1.2

If it's embedded, it's Kontron.

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# 1 User Information

## 1.1 About This Document

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## 1.4 Standards

Kontron is certified to ISO 9000 standards.

## 1.5 Warranty

This Kontron product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

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Kontron will not be responsible for any defects or damages to other products not supplied by Kontron that are caused by a faulty Kontron product.

## 1.6 Technical Support

Technicians and engineers from Kontron and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our website at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section for the latest BIOS downloads, Product Change Notifications and additional tools and software. You can also always contact your board supplier for technical support.

# 2 Introduction

## 2.1 The ETXexpress®-AI COM

The Kontron ETXexpress®-AI Computer-on-Module (COM) extends the COM Express™ specification to include a basic form factor (125mmx95mm) module with the commonly used COM Express™ Type 2 connector or new Type 6 connector for use in graphics-intensive applications for the high-end performance sector. The ETXexpress®-AI COM design enables the development of high-performance, customized, energy efficient applications based on the 32-nm Intel® Core™ i7/Core™ i5 processor technology and the Mobile Intel® QM57 Platform Controller Hub. This module also provides the secure development path of an established, future-proof PICMG COM Express™ industry standard.

The Kontron ETXexpress®-AI module processor technology supports an integrated memory controller for up to 8 GBytes of dual-channel DDR3 SODIMM RAM with ECC support (2x 204-pin SODIMM sockets) and integrated 45nm HD graphics with DisplayPort (DP) support. With a comprehensive set of interfaces on the COM Express Type 2 or Type 6 connector, including 1xPCI Express*Gen 2 graphics (PEG), 6xPCI Express x1,4xSATA, 1xPATA (Type 2 only), SDVO/DP/DVI/HDMI (Type 6 only), 8xUSB 2.0, Gigabit Ethernet, dual-channel LVDS, VGA, and Intel® High Definition Audio, this module offers improved computing and graphics performance. These special features make this 125mmx95mm Computer-on-Module a key solution for applications like gaming, digital signage, network/telecommunications, medical technology, automation, and MAG (military, aerospace, government) that require application-specific customization for rapid time-to-market.

All modules in the Kontron ETXexpress® family are compatible with the COM Express™ standard (connector pin-out Type 2 and now the new Type 6) and thus ensure easy interchangeability as well as design scalability and future migration paths.

## 2.2 Naming Clarifications

The COM Express™ standard defines a Computer-On-Module, or COM, with all the components necessary for a bootable host computer, packaged as a super-component. The interfaces provide a smooth transition path from legacy parallel interfaces to Low Voltage Differential Signaling (LVDS) interfaces

including the PCI bus, PCI Express*, Serial ATA (SATA), and parallel ATA (PATA).

» ETXexpress® modules are Kontron COM Express™ modules in the basic form factor (125mm x 95mm)

» microETXexpress® modules are Kontron COM Express™ modules in a compact form factor (95mm x 95mm)

» nanoETXexpress® modules are Kontron COM Express™ compatible modules in an ultra-small form factor that follow pin-out type 1 or type 10 (55mm x 84mm)

## 2.3 Understanding the COM Functionality

All Kontron microETXexpress® and ETXexpress® modules contain two connectors (X1A and X1B), each with two rows. The primary connector rows are Row A and Row B (connector X1A). The secondary connector rows are Row C and Row D (connector X1B). There are a few different orderable SKUs for the EXTexpress-AI module; one for a module that uses COM Express connector Type 2 and another SKU for a version using the new pin-out Type 6 connector. Additional SKUs for ETXexpress-AI modules that support non-ECC memory are also available. Type 6 is a new addition to the PICMG COM Express standard and it is documented in Revision 2.0 of the PICMG specification. The Type 6 pin-out is based on Type 2 and also supports new features on the secondary connector (rows C and D). The key changes are:

» The PCI interface is no longer supported and the pins are used instead for digital display interfaces (DDI) and two additional PCI Express lanes

» The IDE (PATA) parallel interface is no longer supported and the pins are used instead for additional transmit and receive pairs for four USB 3.0 ports. (USB 3.0 is not supported on the ETXexpress-AI module.)

» Three dedicated DDI ports have been added. Ports 1, 2, and 3 can be configured individually for Display Port (DP), HDMI, or DVI and port 1 can also be used for SDV0.

» SDVO is no longer supported on the PEG port. Instead SDVO is multiplexed on DDI port 1.

» Two optional two-wire RS232 serial ports have been added using pins formerly assigned to 12V signals.

The primary connector (Row A and Row B) on the ETXexpress®-AI COM features the following functionality:

» Analog VGA graphics

» LVDS 24-bit dual channel

» Gigabit Ethernet LAN

» Serial ATA (SATA)

» PCI Express*

» SPI Bus

» USB 2.0

» LPC (Low Pin Count) bus

» Watchdog timer

» GPIO

» $I^2C$

» Intel® High Definition Audio (HDA)

The secondary connector (Row C and Row D) supports the following buses and I/O:

» SDVO/DP/DVI/HDMI (Type 6 only)

» DP/DVI/HDMI (Type 6 only)

» PCI Express (Type 6 only)

» PCI 32/33 (Type 2 only)

» Parallel ATA (PATA) via SATA-to-PATA bridge (Type 2 only build option)

NOTE: For full descriptions of the COM Express Type 2 and Type 6 pin-outs, refer to the PICMG documentation that can be obtained from the the PICMG website.

## 2.4 COM Express™ Documentation

This product manual serves as one of three principal references for this COM Express™ module design. It documents the specifications and features of the ETXexpress®-AI COM. The other two references, which are available from your Kontron support representative or from PICMG, include:

» The PICMG COM Express™ Specification, which defines the COM Express™ module form factor, pin-out, and signals. This document can be obtained by filling out the order form on the PIGMG website at http://www.picmg.com .
NOTE: The version that documents the Type 6 connector is Revision 2.0

» The PICMG COM Express™ Design Guide, which serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express™ modules. This guide is on the PICMG website at http://www.picmg.com .

## 2.5 COM Express™ COM Benefits

Basic form factor (125mm x 95 mm) Computer-on-Module Express (COM Express) modules are highly integrated computers. All ETXexpress® modules feature a standardized form factor and a standardized connector layout for a specified set of signals. Each ETXexpress® module is based on the Connector Type 2 pin-out or new Type 6 pin-out of the COM Express™ specification (PICMG COM.0 R2).

This standardization lets designers create a single-system baseboard that can accept present and future COM Express modules.

Kontron ETXexpress® modules include common personal computer (PC) peripheral functions such as:

» Graphics

» USB ports

» Ethernet

» Audio

» IDE/PATA and SATA hard disk drive formats

Baseboard designers can optimize exactly how each of these functions is implemented physically for the intended application by placing connectors precisely where they are needed on a baseboard that is designed for an optimal fit in the system packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in super-component simplifies packaging, eliminates cabling, and significantly reduces system-level total cost of ownership.

A single baseboard design can use a range of COM Express modules. This flexibility enables product differentiation at various price/performance points, and the design of future-proof systems with a built-in upgrade path. The modularity of a COM Express solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express baseboard can work with several successive generations of COM Express modules.

A COM Express baseboard design has many of the advantages of a custom, computer-board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

# 3 Specifications

## 3.1 Functional Specification

### Processor: Intel® Core™ i7 and Core™ i5

» CPU: Intel® Core™ i7-620UE (1.06 GHz)
Intel® Core™ i7-620LE (2.00 GHz)
Intel® Core™ i5-520E (2.40 GHz)
Intel® Core™ i7-610E (2.53.GHz)
Intel® Celeron® P4505 (1.86 GHz)

» Cores: 2 (with HTT)

» Bus Speed: 800/1066 FSB

» Bus/Core Ratio: 11/12

» Cache: L1 cache 24KB data/32 KB instruction
L2 cache up to 4 MBytes, 8-way

» Memory: 2xDDR3 800/1600 MHz SODIMM sockets, up to 8 GBytes, with ECC support
Additional SKUs for modules supporting non-ECC memory

» Graphics PCIe x16 graphics (or 2 x8)
can also be used for an embedded DisplayPort (eDP)

» Features: Hyper-Threading Technology (HTT)

Intel® Virtualization Technology

Execute Disable Bit

Enhanced Intel® Speedstep Technology

Core Sleep States: C0, C1E, C2E, C3, C4E, Intel Deep Power Down State C6

» Instruction Set: 32-bit

» Package: 22mm x 22mm

» Thermal Spec: Operation: 0° to 60°C
Storage: -30° to 85°

NOTE: Intel Deep Power Down State C6 may not be available in the first early field test (EFT) samples.

### Chipset: Mobile Intel® QM57 Platform Controller Hub (PCH)

» Speed: 800/1066 FSB

» USB: 8xUSB 2.0 One USB port with debug capability is mapped to USB Port 0. (This is a new requirement in COM.0 Rev. 2)

» Audio: Intel® High Definition Audio (24 bit/96 kHz)

» PCI Express: 6xPCIe x1 lanes on Type 2, 7xPCIe x1 lanes on Type 6
1xPCIe Gen 2 graphics (PEG) x16 or configurable as 2xPCIe x8 (Type 6)
(2x PCIe x8 on Type 2 also as a custom stuffing option)

» PCI PCI Rev 2.3 @ 32/33 MHz (Type 2 only, not supported on Type 6)

» Package: 37.5mm x 37.5mm

## Integrated Graphics: Intel® Graphics Media Accelerator 4500(Intel® GMA 4500)

The integrated graphics controller contains a refresh of the 5th generation graphics core.

### Features:

» Intel® Dynamic Video Memory Technology support

» Intel® Smart 2D Display Technology (Intel® S2DDT)

» Intel® Clear Video Technology:
- MPEG2 Hardware Acceleration
- WMV9/VC1 Hardware Acceleration
- AVC Hardware Acceleration
- ProcAmp
- Advanced Pixel Adaptive De-interlacing
- Sharpness Enhancement
- De-noise Filter
- High Quality Scaling
- Film Mode Detection (3:2 pull-down) and Correction
- Intel® TV Wizard

» 12 EUs

» Dedicated analog and digital display ports supported through the PCH

## Display Interfaces

» CRT: Resolution up to QXGA (2048x1536)
Resolution up to 1400x1050 analog VGA

» Flat Panel: Dual channel LVDS 24bpp,
resolution up to 1366 x 768 (WXGA), no dithering
or analog VGA

» Digital Display: SDVO/DP/DVI/HDMI (Type 6 only)

## Storage

- » SATA: 4xSerial ATA (SATA) ports supports up to 1.5 Gbit/sec transfer rate SATA-to-PATA bridge (Type 2 only)
- » SATA Features: Boot, RAID0, RAID1, NCQ, Staggered Spinup, Port Multiplier
- » IDE/PATA 1x Parallel ATA (PATA) port (Type 2 only)

## Onboard Devices:

- » Ethernet: Intel® 82577LM PHY (Max TDP 0.727W) uses one PCIe lane
- » Ethernet Features: WakeOnLAN, PXE Lanboot, Time Sync Protocol Indicator, Jumbo Frames
- » TPM: Infineon™ SLB9635TT1 Trusted Platform Module 1.2, onboard (build option)
- » Watchdog Timer: Kontron PIC microcontroller (interfaces to chipset over a watchdog-specific $I^2C$ interface)
- » PCI: 32-bit/33 MHz PCI 2.3 (Type 2 only)
- » Power Management: L0-L3, Device Power Management (D0-D3 hot)
- » AMT AMT 6.0 Active Management Technology
- » Optional: 1xPATA HDD interface (Type 2 only)

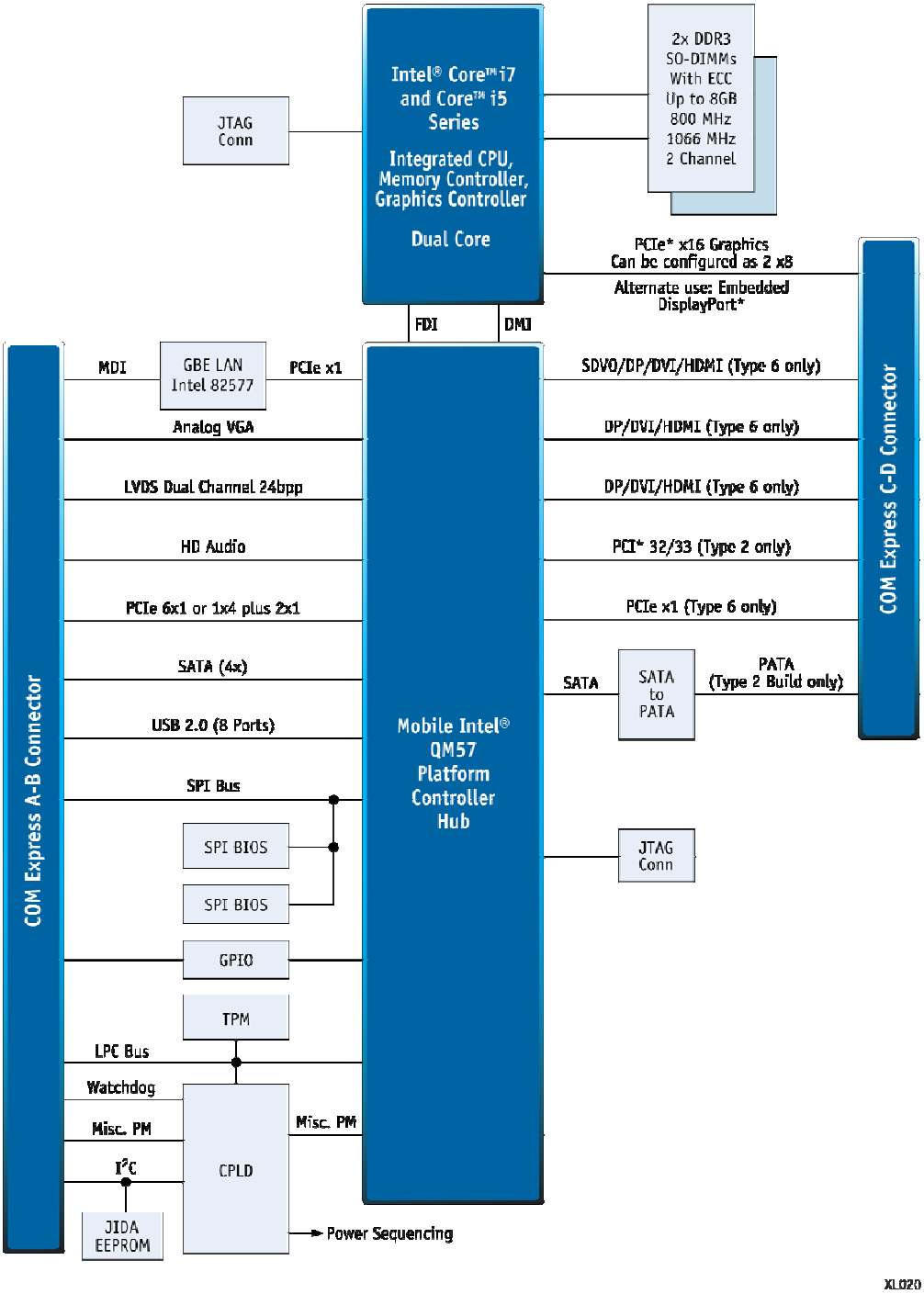
## Additional Interfaces:

- » LPC bus: Yes, to COM Express A-B connector
- » SMBus: Yes, to COM Express A-B connector
- » $I^2C$: Fast $I^2C$ from CPLD
- » GPIO: 8xGPIO, 4 GPI and 4 GPO from PCH
- » SPI Yes, to COM Express A-B connector
- » JIDA: AMI Aptio 4.6.3.5 Core UEFI BIOS
- » K-Station: Yes
- » Bootlogo: Yes
- » MARS: Yes, Charger & Manager Support
- » HWM: Temperature Monitoring for CPU and Board Temperature
- » Passive Cooling: Passive and Critical Trip Point
- » ACPI: ACPI 1.0 / 2.0 / 3.0 with S5 Eco
- » S-States: S0, S3, S4, S5
- » Input Voltage: Single supply support with wide range power supply input, 8V – 18V

## 3.2 Functional Block Diagram

Figure 1 is the ETXexpress®-AI COM block diagram

**Figure 1: ETXexpress®-AI COM Block Diagram**



## 3.3 Mechanical Specifications

### Module Dimensions

» 125 mm x 95 mm ±0.2 mm

#### Height on Top

» Approximately 3.5 mm maximum (without the PCB)

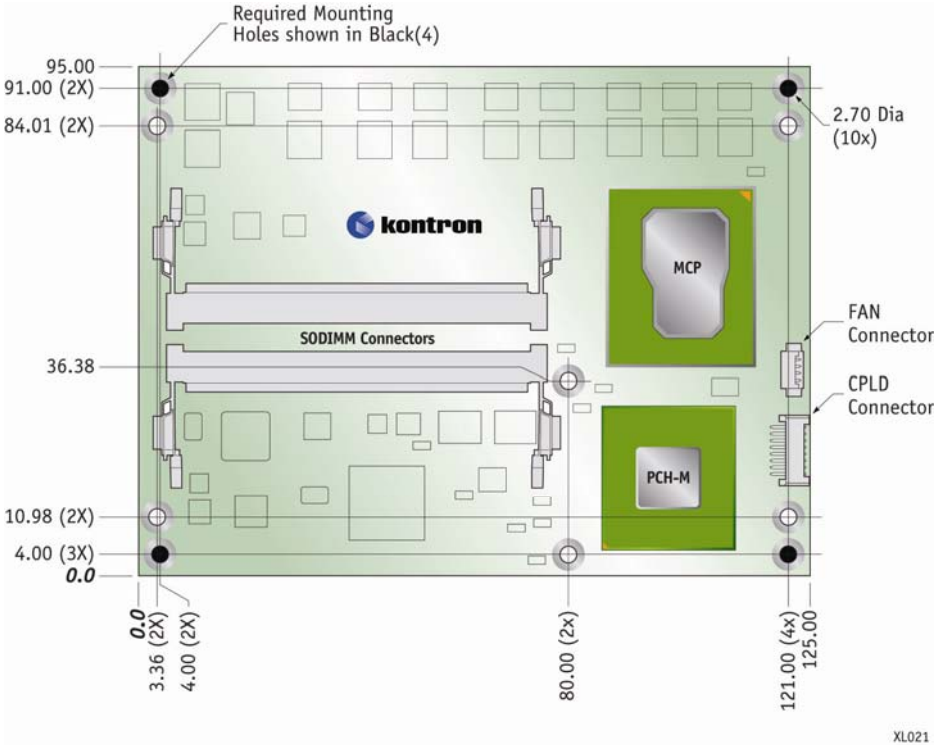
» Height varies depending on whether the optional cooling solution (either a passive heatsink or a heat spreader plate) is installed

#### Height on Bottom

» Approximately 4.06 mm maximum (without the PCB)

Figure 2 is the ETXexpress®-AI COM mechanical drawing

**Figure 2: ETXexpress®-AI COM Mechanical Drawing**




All dimensions are shown in millimeters. The COM Express™ specification says that these holes should be ± 0.25mm [±0.010"], unless otherwise noted. The tolerances for placement of the COM Express connector with respect to the peg holes (dimensions [16.50, 6.00]) should be ± 0.10mm [±0.004. The pads are tied to the PCB ground plane.

# 3.4 Electrical Specifications

## 3.4.1Supply Voltage

» 8 V to 18 V wide range power supply DC in single supply mode (AT)

» 12V + 5VSB ±5% in ATX mode

### Power Supply Risetime

» The input voltages rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There is a smooth and continuous ramp with each DC input voltage from 10% to 90% of its final set-point, as required in the ATX specification

### Supply Voltage Ripple

» Maximum 100 mV peak to peak 0-20MHz

## 3.4.2Supply Current (Windows XP SP3)

The testing performed to capture the supply current data used tested modules mounted on a Kontron evaluation board with a mouse and keyboard connected. The power consumption tests were executed in Windows XP (with SP3) using a tool to stress the CPU at 100% load. The power measurement values were captured after 15 minutes of full load or a stable CPU core temperature of 90°C. To ensure a stable die temperature, a corresponding heatsink was used to hold the temperature under the critical trip point. All boards were equipped with a 2x1024-MB DDR3 SDRAM with ECC. The modules were tested using the maximum CPU frequency. For more detailed information, refer to the "Power Consumption" diagrams on the EMD Customer section of the Kontron website.

**Table 1: Supply Current Test Results**

| Test Description | V_5P0_SBY | V_12P0 | Results |
|---|---|---|---|
| Win XP desktop | 5.045 V (260 mA) | 11.85 V (1.16 A) | 15.06 W |
| Win XP Burn-In Test | 5.042 V (258 mA) | 11.79 V (1.74 A) | 21.82 W |
| Win XP TAT (Max) | 5.040 V (296 mA) | 11.75 V (2.02 A) | 25.23 W |
| S3 WOL disabled | 5.077 V (225 mA) | 0.043 V (0.00 A) | 1.142 W |
| S3 WOL enabled | 5.069 V (276 mA) | 0.043 V (0.00 A) | 1.399 W |
| DOS prompt | 5.043 V (258 mA) | 11.82 V (1.41 A) | 17.97 W |
| Linux KDE desktop | 5.046 V (272 | 11.58 V | 14.69 W |

| | | | |
|---|---|---|---|
| | mA) | (1.15 A) | |
| S5 with Ethernet | 5.084 V (169 mA) | 0.045 V (0.00 A) | 0.859 W |
| Power on inrush current | 5.030 V (291 mA) | 11.80 V (1.66 A) | 21.05 W |

Note: It is difficult to test for all possible applications on the market. There may be an application that draws more power from the CPU than the values measured in the table above. Take this into consideration if you are at the limit of the thermal specification, in which case you should consider improving your thermal solution.

## 3.5 Environmental Specifications

### Temperature

Operating: (with Kontron active heatsink):

» Ambient temperature: 0 to 60°C

» Maximum heat spreader-plate temperature: 0 to 60°C(*)

» Non-operating: -30 to +85°C

NOTE: *The maximum operating temperature with the active heat sink installed is the maximum measurable temperature on any spot on the heat spreader surface. You must maintain the temperature according to the specification above.

### Humidity

» Operating: 10% to 90% (non-condensing)

» Non operating: 5% to 95% (non-condensing)

## 3.6 MTBF

The MTBF is 179,152 hours.

# 4 COM Connectors

The pin-outs for ETXexpress® interface connectors X1A and X1B are documented for convenient reference. See the PICMG COM Express™ Specification on the PICMG website and COM Express™ Design Guide on the Kontron website for detailed, design-level information.

**Figure 3: COM Express Connector Locations**

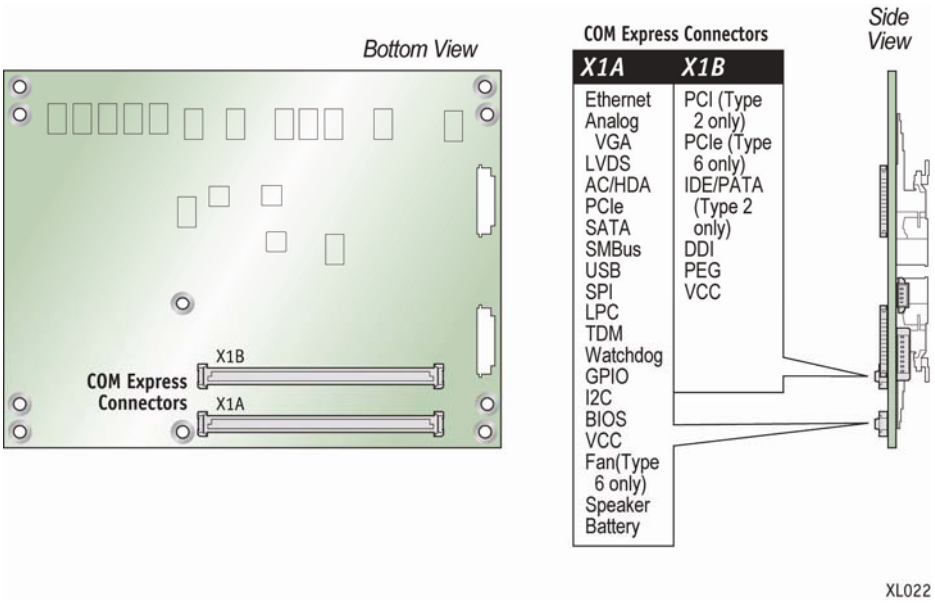



**Table 2: General Signal Description**

| Type | Description |
|---|---|
| I/O-3.3 | Bi-directional 3,3 V IO-Signal |
| I/O-5T | Bi-dir. 3,3V I/O (5V Tolerance) |
| I/O-5 | Bi-directional 5V I/O-Signal |
| I-3.3 | 3,3V Input |
| I/OD | Bi-directional Input/Output Open Drain |
| I-5T | 3,3V Input (5V Tolerance) |
| OA | Output Analog |
| OD | Output Open Drain |
| O-1.8 | 1.8V Output |
| O-3.3 | 3.3V Output |
| O-5 | 5V Output |
| DP-I/O | Differential Pair Input/Output |
| DP-I | Differential Pair Input |
| DP-O | Differential Pair Output |
| PU | Pull-Up Resistor |
| PD | Pull-Down Resistor |
| PWR | Power Connection |

| Type | Description |
|---|---|
| nc | Not connected, signal not available |

Note: To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current and the enclosure of the peripheral device fulfills the fire-protection requirements in IEC/EN60950

## 4.1 COM Express™ Type 2 Pin-Outs

### Table 3: Type 2 Connector X1A - Row A

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A1 | GND (Fixed) | Power Ground | PWR | - | - |
| A2 | GBE0_MDI3- | Ethernet Receive Data- | DP-I | Intel® 82577 | - |
| A3 | GBE0_MDI3+ | Ethernet Receive Data+ | DP-I | Intel® 82577 | - |
| A4 | GBE0_LINK100# | Ethernet Speed LED 100Mbps | O-3.3 | Intel® 82577 | - |
| A5 | GBE0_LINK1000# | Ethernet Speed LED 1000Mbps | O-3.3 | Intel® 82577 | - |
| A6 | GBE0_MDI2- | Ethernet Receive Data- | DP-I | Intel® 82577 | - |
| A7 | GBE0_MDI2+ | Ethernet Receive Data+ | DP-I | Intel® 82577 | - |
| A8 | GBE0_LINK# | LAN Link LED | OD | Intel® 82577 | - |
| A9 | GBE0_MDI1- | Ethernet Receive Data- | DP-I | Intel® 82577 | - |
| A10 | GBE0_MDI1+ | Ethernet Receive Data+ | DP-I | Intel® 82577 | - |
| A11 | GND (Fixed) | Power Ground | PWR | - | - |
| A12 | GBE0_MDI0- | Ethernet Transmit Data- | DP-O | Intel® 82577 | - |
| A13 | GBE0_MDI0+ | Ethernet Transmit Data+ | DP-O | Intel® 82577 | - |
| A14 | GBE0_CTREF | LAN Reference Voltage | O-3.3 | controlled on a power rail | - |
| A15 | SUS_S3# | Indicates Suspend to RAM state | O-3.3 | CPLD I/O | CPLD I/O |
| A16 | SATA0_TX+ | SATA 0 Transmit Data+ | DP-O | | - |
| A17 | SATA0_TX- | SATA 0 Transmit Data- | DP-O | | - |
| A18 | SUS_S4# | Indicates Suspend to Disk state | O-3.3 | CPLD I/O | CPLD I/O |
| A19 | SATA0_RX+ | SATA 0 Receive Data+ | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A20 | SATA0_RX- | SATA 0 Receive Data- | DP-I | | - |
| A21 | GND (Fixed) | Power Ground | PWR | | - |
| A22 | SATA2_TX+ | SATA 2 Transmit Data- | DP-O | | |
| A23 | SATA2_TX- | SATA 2 Transmit Data+ | DP-O | | |
| A24 | SUS_S5# | Indicates Soft Off state | O-3.3 | CPLD I/O | CPLD I/O |
| A25 | SATA2_RX+ | SATA 2 Receive Data+ | Not connected | nc | nc |
| A26 | SATA2_RX- | SATA 2 Receive Data- | Not connected | nc | nc |
| A27 | BATLOW# | Indicates low external battery | I-3.3 | | CPLD I/O |
| A28 | (S)ATA_ACT# | SATA, IDE, SD Activity Indicator | O-3.3 | Buffered Output | |
| A29 | AC/HDA_SYNC | HD Audio Sync | O-3.3 | | |
| A30 | AC/HDA_RST# | HD Audio Reset | O-3.3 | | |
| A31 | GND Fixed) | Power Ground | PWR | - | - |
| A32 | AC/HDA_BITCLK | HD Audio Clock | O-3.3 | | |
| A33 | AC/HDA_SDOUT | HD Audio Data | O-3.3 | | |
| A34 | BIOS_DIS0# | Disable Module BIOS. Enables boot from a BIOS on Baseboard | I-3.3 | | |
| A35 | THRMTRIP# | CPU thermal shutdown indicator | O-3.3 | | |
| A36 | USB6- | USB Data- Port #6 | DP-I/O | | - |
| A37 | USB6+ | USB Data+ Port #6 | DP-I/O | | - |
| A38 | USB_6_7_OC# | USB Overcurrent Pair 6/7 | I-3.3 | | |
| A39 | USB4- | USB Data- Port #4 | DP-I/O | | |
| A40 | USB4+ | USB Data+ Port #4 | DP-I/O | | - |
| A41 | GND (Fixed) | Power Ground | PWR | - | - |
| A42 | USB2- | USB Data- Port #2 | | | |
| A43 | USB2+ | USB Data+ Port #2 | DP-I/O | | |
| A44 | USB_2_3_OC# | USB Overcurrent Pair 2/3 | I-3.3 | | |
| A45 | USB0- | USB Data- Port #0 | DP-I/O | | |
| A46 | USB0+ | USB Data+ Port #0 | DP-I/O | | |
| A47 | VCC_RTC | RTC Power Supply +3V | PWR | - | - |
| A48 | EXCD0_PERST# | PCIe Express Card 0 Reset | O-3.3 | | |
| A49 | EXCD0_CPPE# | PCIe Express Card 0 Request | I-3.3 | | |
| A50 | LPC_SERIRQ | LPC Serial Interrupt Request | IO-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A51 | GND (Fixed) | Power Ground | PWR | - | - |
| A52 | PCIE_TX5+ | PCIe 5 Transmit Data+ | DP-O | | |
| A53 | PCIE_TX5- | PCIe 5 Transmit Data- | DP-O | | |
| A54 | GPI0 | General Purpose Input 0 | I-3.3 | | |
| A55 | PCIE_TX4+ | PCIe 4 Transmit Data+ | DP-O | | |
| A56 | PCIE_TX4- | PCIe 4 Transmit Data- | DP-O | | |
| A57 | GND (Fixed) | Power Ground | PWR | - | - |
| A58 | PCIE_TX3+ | PCIe 3 Transmit Data+ | DP-O | | |
| A59 | PCIE_TX3- | PCIe 3 Transmit Data- | DP-O | | |
| A60 | GND (Fixed) | Power Ground | PWR | - | - |
| A61 | PCIE_TX2+ | PCIe 2 Transmit Data+ | DP-O | | |
| A62 | PCIE_TX2- | PCIe 2 Transmit Data- | DP-O | | |
| A63 | GPI1 | General Purpose Input 1 | I-3.3 | | |
| A64 | PCIE_TX1+ | PCIe 1 Transmit Data+ | DP-O | | |
| A65 | PCIE_TX1- | PCIe 1 Transmit Data- | DP-O | | |
| A66 | GND (Fixed) | Power Ground | PWR | - | - |
| A67 | GPI2 | General Purpose Input 2 | I-3.3 | | |
| A68 | PCIE_TX0+ | PCIe lane #0 Transmit+ | DP-O | | |
| A69 | PCIE_TX0- | PCIe lane #0 Transmit- | DP-O | | |
| A70 | GND (Fixed) | Power Ground | PWR | - | - |
| A71 | LVDS_A0+ | LVDS Channel A (positive) | DP-O | | |
| A72 | LVDS_A0- | LVDS Channel A (negative) | DP-O | | - |
| A73 | LVDS_A1+ | LVDS Channel A (positive) | DP-O | | - |
| A74 | LVDS_A1- | LVDS Channel A (negative) | DP-O | | |
| A75 | LVDS_A2+ | LVDS Channel A (positive) | DP-O | | |
| A76 | LVDS_A2- | LVDS Channel A (negative) | DP-O | | |
| A77 | LVDS_VDD_EN | LVDS Panel Power Controller | O-3.3 | | |
| A78 | LVDS_A3+ | LVDS Channel A (positive) | DP-O | | |
| A79 | LVDS_A3- | LVDS Channel A (negative) | DP-O | | |
| A80 | GND (Fixed) | Power Ground | PWR | - | - |
| A81 | LVDS_A_CK+ | LVDS Channel A Clock+ | DP-O | | |
| A82 | LVDS_A_CK- | LVDS Channel A Clock- | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A83 | LVDS_I2C_CK | LVDS $I^2C$ Clock | IO-3.3 | | |
| A84 | LVDS_I2C_DAT | LVDS $I^2C$ Data | IO-3.3 | | |
| A85 | GPI3 | General Purpose Input 3 | I-3.3 | | |
| A86 | KBD_RST# | Keyboard Reset | I-3.3 | | |
| A87 | KBD_A20GATE | A20 gate | I-3.3 | | |
| A88 | PCIE0_CK_REF+ | PCIe Clock (positive) | DP-O | | |
| A89 | PCIE0_CK_REF- | PCIe Clock (negative) | DP-O | | |
| A90 | GND (Fixed) | Power Ground | PWR | - | - |
| A91 | SPI_Power | Power for off-board SPI flash | O-3.3 | | |
| A92 | SPI_MISO | SPI Master In Slave Out data line | I-3.3 | | |
| A93 | GPO0 | General Purpose Output 0 | O-3.3 | | |
| A94 | SPI_CLK | SPI clock line for off-board SPI | O-3.3 | | |
| A95 | SPI_MOSI | SPI Master Out Slave In data line | O-3.3 | | - |
| A96 | GND | Power Ground | PWR | - | - |
| A97 | TYPE10# | | Not connected | nc | nc |
| A98 | RSVD | Reserved | Not connected | nc | nc |
| A99 | RSVD | Reserved | Not connected | nc | nc |
| A100 | GND (Fixed) | Power Ground | PWR | - | - |
| A101 | RSVD | Reserved | Not connected | nc | nc |
| A102 | RSVD | Reserved | Not connected | nc | nc |
| A103 | RSVD | Reserved | Not connected | nc | nc |
| A104 | VCC_12V | 12V VCC | PWR | - | - |
| A105 | VCC_12V | 12V VCC | PWR | - | - |
| A106 | VCC_12V | 12V VCC | PWR | - | - |
| A107 | VCC_12V | 12V VCC | PWR | - | - |
| A108 | VCC_12V | 12V VCC | PWR | - | - |
| A109 | VCC_12V | 12V VCC | PWR | - | - |
| A110 | GND | Power Ground | PWR | - | - |

## Table 4: Type 2 Connector X1A - Row B

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| B1 | GND (Fixed) | Power Ground | PWR | - | - |
| B2 | GBE0_ACT# | Ethernet Activity LED | Not connected | nc | nc |
| B3 | LPC_FRAME# | LPC Frame Indicator | O-3.3 | | |
| B4 | LPC_AD0 | LPC Address / Data Bus | IO-3.3 | | |
| B5 | LPC_AD1 | LPC Address / Data Bus | IO-3.3 | | |
| B6 | LPC_AD2 | LPC Address / Data Bus | IO-3.3 | | |
| B7 | LPC_AD3 | LPC Address / Data Bus | IO-3.3 | | |
| B8 | LPC_DRQ0# | LPC Serial DMA Request | I-3.3 | | |
| B9 | LPC_DRQ1# | LPC Serial DMA Request | I-3.3 | | |
| B10 | LPC_CLK | LPC Clock | O-3.3 | | |
| B11 | GND (Fixed) | Power Ground | PWR | - | - |
| B12 | PWRBTN# | Power Button Input | I-3.3 | | |
| B13 | SMB_CLK | SMBus Clock | O-3.3 | | |
| B14 | SMB_DAT | SMBus Data | IO-3.3 | | |
| B15 | SMB_ALERT# | SMBus Interrupt | IO-3.3 | | |
| B16 | SATA1_TX+ | SATA 1 Transmit Data+ | DP-O | | |
| B17 | SATA1_TX- | SATA 1 Transmit Data- | DP-O | | |
| B18 | SUS_STAT# | Indicates imminent suspend operation; used to notify LPC devices. | O-3.3 | | |
| B19 | SATA1_RX+ | SATA 1 Receive Data+ | DP-I | | |
| B20 | SATA1_RX- | SATA 1 Receive Data- | DP-I | | |
| B21 | GND (Fixed) | Power Ground | PWR | - | - |
| B22 | SATA3_TX+ | SATA 3 Transmit Data+ | DP-O | | |
| B23 | SATA3_TX- | SATA 3 Transmit Data- | DP-O | | |
| B24 | PWR_OK | Power OK from power supply | I-3.3 | | |
| B25 | SATA3_RX+ | SATA 3 Receive Data+ | DP-I | | |
| B26 | SATA3_RX- | SATA 3 Receive Data- | DP-I | | |
| B27 | WDT | Indicator for Watchdog Timeout | O-3.3 | | |
| B28 | AC/HDA_SDIN2 | Audio CODEC Serial Data In 2 | I-3.3 | | |
| B29 | AC/HDA_SDIN1 | Audio CODEC Serial Data in 1 | I-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| B30 | AC/HDA_SDIN0 | Audio CODEC Serial Data in 0 | I-3.3 | | |
| B31 | GND (Fixed) | Power Ground | PWR | - | - |
| B32 | SPKR | Speaker Interface | O-3.3 | | |
| B33 | I2C_CK | $I^2C$ Clock | IO-3.3 | | |
| B34 | I2C_DAT | $I^2C$ Data | IO-3.3 | | |
| B35 | THRM# | Over Temperature Indicator | I-3.3 | | |
| B36 | USB7- | USB Data- Port #7 ( | DP-I/O | | |
| B37 | USB7+ | USB Data+ Port #7 | DP-I/O | | |
| B38 | USB_4_5_OC# | USB Overcurrent Pair 4/5 | I-3.3 | | |
| B39 | USB5- | USB Data- Port #5 | DP-I/O | | |
| B40 | USB5+ | USB Data+ Port #5 | DP-I/O | | |
| B41 | GND (Fixed) | Power Ground | PWR | - | - |
| B42 | USB3- | USB Data- Port #3 | DP-I/O | | |
| B43 | USB3+ | USB Data+ Port #3 | DP-I/O | | |
| B44 | USB_0_1_OC# | USB Overcurrent Pair 0/1 | I-3.3 | | |
| B45 | USB1- | USB Data- Port #1 | DP-I/O | | |
| B46 | USB1+ | USB Data+ Port #1 | DP-I/O | | |
| B47 | EXCD1_PERST# | PCIe Express Card 1 Reset | O-3.3 | | |
| B48 | EXCD1_CPPE# | PCIe Express Card 1 Request | I-3.3 | | |
| B49 | SYS_RESET# | Reset button input | I-3.3 | | |
| B50 | CB_RESET# | Carrier Board Reset | O-3.3 | | |
| B51 | GND (Fixed) | Power Ground | PWR | - | - |
| B52 | PCIE_RX5+ | PCIe 5 Receive Data+ | DP-I | | |
| B53 | PCIE_RX5- | PCIe 5 Receive Data- | DP-I | | |
| B54 | GPO1 | General Purpose Output 1 | O-3.3 | | |
| B55 | PCIE_RX4+ | PCIe 4 Receive Data+ | DP-I | | |
| B56 | PCIE_RX4- | PCIe 4 Receive Data- | DP-I | | |
| B57 | GPO2 | General Purpose Output 2 | O-3.3 | | |
| B58 | PCIE_RX3+ | PCIe 3 Receive Data+ | DP-I | | |
| B59 | PCIE_RX3- | PCIe 5 Receive Data- | DP-I | | |
| B60 | GND (Fixed) | Power Ground | PWR | - | - |
| B61 | PCIE_RX2+ | PCIe 2 Receive Data+ | DP-I | | |
| B62 | PCIE_RX2- | PCIe 2 Receive Data- | DP-I | | |
| B63 | GPO3 | General Purpose | O-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Output 3 | | | |
| B64 | PCIE_RX1+ | PCIe 1 Receive Data+ | DP-I | | |
| B65 | PCIE_RX1- | PCIe 1 Receive Data- | DP-I | | |
| B66 | WAKE0# | PCI Express Wake Event | I-3.3 | | |
| B67 | WAKE1# | General Purpose Wake Event | I-3.3 | | |
| B68 | PCIE_RX0+ | PCIe lane #0 Receive+ | DP-I | | |
| B69 | PCIE_RX0- | PCIe lane #0 Receive- | DP-I | | |
| B70 | GND (Fixed) | Power Ground | PWR | - | - |
| B71 | LVDS_B0+ | LVDS Channel B (Positive) | DP-O | | |
| B72 | LVDS_B0- | LVDS Channel B (Negative) | DP-O | | |
| B73 | LVDS_B1+ | LVDS Channel B (Positive) | DP-O | | |
| B74 | LVDS_B1- | LVDS Channel B (Negative) | DP-O | | |
| B75 | LVDS_B2+ | LVDS Channel B (Positive) | DP-O | | |
| B76 | LVDS_B2- | LVDS Channel B (Negative) | DP-O | | |
| B77 | LVDS_B3+ | LVDS Channel B (Positive) | DP-O | | |
| B78 | LVDS_B3- | LVDS Channel B (Negative) | DP-O | | |
| B79 | LVDS_BKLT_EN | Backlight Enable | O-3.3 | | |
| B80 | GND (Fixed) | Power Ground | PWR | - | - |
| B81 | LVDS_B_CK+ | LVDS Channel B Clock+ | DP-O | | |
| B82 | LVDS_B_CK- | LVDS Channel B Clock- | DP-O | | |
| B83 | LVDS_BKLT_CTRL | Backlight Brightness Control | O-3.3 | | |
| B84 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B85 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B86 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B87 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B88 | BIOS_DIS1# | BIOS Disable 1 (offboard SPI select) | I-3.3 | | |
| B89 | VGA_RED | Analog Video Red | O | | |
| B90 | GND (Fixed) | Power Ground | PWR | - | - |
| B91 | VGA_GRN | Analog Video Green | O | | |
| B92 | VGA_BLU | Analog Video Blue | O | | |
| B93 | VGA_HSYNC | Analog Video Horizontal Sync | O-3.3 | | |
| B94 | VGA_VSYNC | Analog Video Vertical | O-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Sync | | | |
| B95 | VGA_I2C_CK | Analog Video $I^2C$ Clock | IO/OD-3.3 | | |
| B96 | VGA_I2C_DAT | Analog Video $I^2C$ Data | IO/OD-3.3 | | |
| B97 | SPI_CS# | SPI Chip Select | O-3.3 | | |
| B98 | RSVD | Reserved | Not connected | nc | nc |
| B99 | RSVD | Reserved | Not connected | nc | nc |
| B100 | GND (Fixed) | Power Ground | PWR | - | - |
| B101 | RSVD | Reserved | Not connected | nc | nc |
| B102 | RSVD | Reserved | Not connected | nc | nc |
| B103 | RSVD | Reserved | Not connected | Nc | Nc |
| B104 | VCC_12V_16 | 12V VCC | PWR | - | - |
| B105 | VCC_12V_17 | 12V VCC | PWR | - | - |
| B106 | VCC_12V_18 | 12V VCC | PWR | - | - |
| B107 | VCC_12V_19 | 12V VCC | PWR | - | - |
| B108 | VCC_12V_20 | 12V VCC | PWR | - | - |
| B109 | VCC_12V_21 | 12V VCC | PWR | - | - |
| B110 | GND (Fixed) | Power Ground | PWR | | |

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express™ Design Guide for information about additional termination resistors.

## Table 5: Connector X1B - Row C

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| C1 | GND (Fixed) | Power Ground | PWR | - | - |
| C2 | IDE_D7 | IDE Data Bus | I/O-5T | | |
| C3 | IDE_D6 | IDE Data Bus | I/O-5T | | |
| C4 | IDE_D3 | IDE Data Bus | I/O-5T | | |
| C5 | IDE_D15 | IDE Data Bus | I/O-5T | | |
| C6 | IDE_D8 | IDE Data Bus | I/O-5T | | |
| C7 | IDE_D9 | IDE Data Bus | I/O-5T | | |
| C8 | IDE_D2 | IDE Data Bus | I/O-5T | | |
| C9 | IDE_D13 | IDE Data Bus | I/O-5T | | |
| C10 | IDE_D1 | IDE Data Bus | I/O-5T | | |
| C11 | GND (Fixed) | Power Ground | PWR | - | - |
| C12 | IDE_D14 | IDE Data Bus | I/O-5T | | |
| C13 | IDE_IORDY | IDE I/O Ready | I-5T | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| C14 | IDE_IOR# | IDE I/O Read | O-3.3 | | |
| C15 | PCI_PME# | PCI Power Management | I-3.3 | | |
| C16 | PCI_GNT2# | PCI Bus Grant 2 | O-3.3 | | |
| C17 | PCI_REQ2# | PCI Bus Request 2 | I-5T | | |
| C18 | PCI_GNT1# | PCI Bus Grant 1 | O-3.3 | | |
| C19 | PCI_REQ1# | PCI Bus Request 1 | I-5T | | |
| C20 | PCI_GNT0# | PCI Bus Grant 0 | O-3.3 | | |
| C21 | GND (Fixed) | Power Ground | PWR | - | - |
| C22 | PCI_REQ0# | PCI Bus Request 0 | I-5T | | |
| C23 | PCI_RST# | PCI Bus Reset | O-3.3 | | |
| C24 | PCI_AD0 | PCI Address & Data Bus line | I/O-5T | | |
| C25 | PCI_AD2 | PCI Address & Data Bus line | I/O-5T | | |
| C26 | PCI_AD4 | PCI Address & Data Bus line | I/O-5T | | |
| C27 | PCI_AD6 | PCI Address & Data Bus line | I/O-5T | | |
| C28 | PCI_AD8 | PCI Address & Data Bus line | I/O-5T | | |
| C29 | PCI_AD10 | PCI Address & Data Bus line | I/O-5T | | |
| C30 | PCI_AD12 | PCI Address & Data Bus line | I/O-5T | | |
| C31 | GND (Fixed) | Power Ground | PWR | - | - |
| C32 | PCI_AD14 | PCI Address & Data Bus line | I/O-5T | | |
| C33 | PCI_C/BE1# | PCI Bus Command & Byte Enable 1 | I/O-5T | | |
| C34 | PCI_PERR# | PCI Bus Grant Error | I/O-5T | | |
| C35 | PCI_LOCK# | PCI Bus Lock | I/O-5T | | |
| C36 | PCI_DEVSEL# | PCI Bus Device Select | I/O-5T | | |
| C37 | PCI_IRDY# | PCI Bus Initiator Ready | I/O-5T | | |
| C38 | PCI_C/BE2# | PCI Bus Command & Byte Enable 2 | I/O-5T | | |
| C39 | PCI_AD17 | PCI Address & Data Bus line | I/O-5T | | |
| C40 | PCI_AD19 | PCI Address & Data Bus line | I/O-5T | | |
| C41 | GND (Fixed) | Power Ground | PWR | - | - |
| C42 | PCI_AD21 | PCI Address & Data Bus line | I/O-5T | | |
| C43 | PCI_AD23 | PCI Address & Data Bus line | I/O-5T | | |
| C44 | PCI_C/BE3# | PCI Bus Command & Byte Enable 3 | I/O-5T | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| C45 | PCI_AD25 | PCI Address & Data Bus line | I/O-5T | | |
| C46 | PCI_AD27 | PCI Address & Data Bus line | I/O-5T | | |
| C47 | PCI_AD29 | PCI Address & Data Bus line | I/O-5T | | |
| C48 | PCI_AD31 | PCI Address & Data Bus line | I/O-5T | | |
| C49 | PCI_IRQA# | PCI Bus Interrupt Request A | I-5T | | |
| C50 | PCI_IRQB# | PCI Bus Interrupt Request B | I-5T | | |
| C51 | GND (Fixed) | Power Ground | PWR | - | - |
| C52 | PEG_RX0+ | PCI Express Graphics Receive Lane 0 Positive | DP-I | | |
| C53 | PEG_RX0- | PCI Express Graphics Receive Lane 0 Negative | DP-I | | |
| C54 | TYPE0# | Not connected for Type 2 module | Not connected | nc | nc |
| C55 | PEG_RX1+ | PCI Express Graphics Receive Lane 1 Positive | DP-I | | |
| C56 | PEG_RX1- | PCI Express Graphics Receive Lane 1 Negative | DP-I | | |
| C57 | TYPE1# | Not connected for Type 2 module | Not connected | nc | nc |
| C58 | PEG_RX2+ | PCI Express Graphics Receive Lane 2 Positive | DP-I | | |
| C59 | PEG_RX2- | PCI Express Graphics Receive Lane 2 Negative | DP-I | | |
| C60 | GND (Fixed) | Power Ground | PWR | - | - |
| C61 | PEG_RX3+ | PCI Express Graphics Receive Lane 3 Positive | DP-I | | |
| C62 | PEG_RX3- | PCI Express Graphics Receive Lane 3 Negative | DP-I | | |
| C63 | RSVD | Reserved | Not connected | nc | nc |
| C64 | RSVD | Reserved | Not connected | nc | nc- |
| C65 | PEG_RX4+ | PCI Express Graphics | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Receive Lane 4 Positive | | | |
| C66 | PEG_RX4- | PCI Express Graphics Receive Lane 4 Negative | DP-I | | |
| C67 | RSVD | Reserved | Not connected | nc | nc |
| C68 | PEG_RX5+ | PCI Express Graphics Receive Lane 5 Positive | DP-I | | |
| C69 | PEG_RX5- | PCI Express Graphics Receive Lane 5 Negative | DP-I | | |
| C70 | GND (Fixed) | Power Ground | PWR | - | - |
| C71 | PEG_RX6+ | PCI Express Graphics Receive Lane 6 Positive | DP-I | | |
| C72 | PEG_RX6- | PCI Express Graphics Receive Lane 6 Negative | DP-I | | |
| C73 | SDVO_DATA | SDVOController Data | Not connected | nc | nc |
| C74 | PEG_RX7+ | PCI Express Graphics Receive Lane 7 Positive | DP-I | | |
| C75 | PEG_RX7- | PCI Express Graphics Receive Lane 7 Negative | DP-I | | |
| C76 | GND (Fixed) | Power Ground | PWR | - | - |
| C77 | RSVD | Reserved | Not connected | nc | nc |
| C78 | PEG_RX8+ | PCI Express Graphics Receive Lane 8 Positive | DP-I | | |
| C79 | PEG_RX8- | PCI Express Graphics Receive Lane 8 Negative | DP-I | | |
| C80 | GND (Fixed) | Power Ground | PWR | - | - |
| C81 | PEG_RX9+ | PCI Express Graphics Receive Lane 9 Positive | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| C82 | PEG_RX9- | PCI Express Graphics Receive Lane 9 Negative | DP-I | | |
| C83 | RSVD | Reserved | Not connected | nc | nc |
| C84 | GND | Power Ground | PWR | - | - |
| C85 | PEG_RX10+ | PCI Express Graphics Receive Lane 10 Positive | DP-I | | |
| C86 | PEG_RX10- | PCI Express Graphics Receive Lane 10 Negative | DP-I | | |
| C87 | GND | Power Ground | PWR | - | - |
| C88 | PEG_RX11+ | PCI Express Graphics Receive Lane 11 Positive | DP-I | | |
| C89 | PEG_RX11- | PCI Express Graphics Receive Lane 11 Negative | DP-I | | |
| C90 | GND (Fixed) | Power Ground | PWR | - | - |
| C91 | PEG_RX12+ | PCI Express Graphics Receive Lane 12 Positive | DP-I | | |
| C92 | PEG_RX12- | PCI Express Graphics Receive Lane 12 Negative | DP-I | | |
| C93 | GND | Power Ground | PWR | - | - |
| C94 | PEG_RX13+ | PCI Express Graphics Receive Lane 13 Positive | DP-I | | |
| C95 | PEG_RX13- | PCI Express Graphics Receive Lane 13 Negative | DP-I | | |
| C96 | GND | Power Ground | PWR | - | - |
| C97 | RSVD | Reserved | Not connected | nc | nc |
| C98 | PEG_RX14+ | PCI Express Graphics Receive Lane 14 Positive | DP-I | | |
| C99 | PEG_RX14- | PCI Express Graphics | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Receive Lane 14 Negative | | | |
| C100 | GND (Fixed) | Power Ground | PWR | - | - |
| C101 | PEG_RX15+ | PCI Express Graphics Receive Lane 15 Positive | DP-I | | |
| C102 | PEG_RX15- | PCI Express Graphics Receive Lane 15 Negative | DP-I | | |
| C103 | GND | Power Ground | PWR | - | - |
| C104 | VCC_12V | 12V VCC | PWR | - | - |
| C105 | VCC_12V | 12V VCC | PWR | - | - |
| C106 | VCC_12V | 12V VCC | PWR | - | - |
| C107 | VCC_12V | 12V VCC | PWR | - | - |
| C108 | VCC_12V | 12V VCC | PWR 8 | - | - |
| C109 | VCC_12V | 12V VCC | PWR | - | - |
| C110 | GND (Fixed) | Power Ground | PWR | - | - |

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express™ Design Guide for information about additional termination resistors.

## Table 6: Type 2 Connector X1B - Row D

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D1 | GND (Fixed) | Power Ground | PWR | - | - |
| D2 | IDE_D5 | IDE Data Bus | I/O-5T | | |
| D3 | IDE_D10 | IDE Data Bus | I/O-5T | | |
| D4 | IDE_D11 | IDE Data Bus | I/O-5T | | |
| D5 | IDE_D12 | IDE Data Bus | I/O-5T | | |
| D6 | IDE_D4 | IDE Data Bus | I/O-5T | | |
| D7 | IDE_D0 | IDE Data Bus | I/O-5T | | |
| D8 | IDE_REQ | IDE Data Bus | I/O-5T | | |
| D9 | IDE_IOW# | IDE IO Write | O-3.3 | | |
| D10 | IDE_ACK# | IDE DMA Acknowledge | O-3.3 | | |
| D11 | GND (Fixed) | Power Ground | PWR | - | - |
| D12 | IDE_IRQ | IDE Interrupt Request | I-5T | | |
| D13 | IDE_A0 | IDE Address Bus | O-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D14 | IDE_A1 | IDE Address Bus | O-3.3 | | |
| D15 | IDE_A2 | IDE Address Bus | O-3.3 | | |
| D16 | IDE_CS1# | IDE Chip Select Channel 0 | O-3.3 | | |
| D17 | IDE_CS3# | IDE Chip Select Channel 1 | O-3.3 | | |
| D18 | IDE_RESET# | IDE Hard Drive Reset | O-3.3 | | |
| D19 | PCI_GNT3# | PCI Bus Grant 3 | O-3.3 | | |
| D20 | PCI_REQ3# | PCI Bus Request 3 | I-5T | | |
| D21 | GND (Fixed) | Power Ground | PWR | - | - |
| D22 | PCI_AD1 | PCI Address & Data Bus line | I/O-5T | | |
| D23 | PCI_AD3 | PCI Address & Data Bus line | I/O-5T | | |
| D24 | PCI_AD5 | PCI Address & Data Bus line | I/O-5T | | |
| D25 | PCI_AD7 | PCI Address & Data Bus line | I/O-5T | | |
| D26 | PCI_C/BE0# | PCI Bus Command & Byte Enable 0 | I/O-5T | | |
| D27 | PCI_AD9 | PCI Address & Data Bus line | I/O-5T | | |
| D28 | PCI_AD11 | PCI Address & Data Bus line | I/O-5T | | |
| D29 | PCI_AD13 | PCI Address & Data Bus line | I/O-5T | | |
| D30 | PCI_AD15 | PCI Address & Data Bus line | I/O-5T | | |
| D31 | GND (Fixed) | Power Ground | PWR | - | - |
| D32 | PCI_PAR | PCI Bus Parity | I/O-5T | | |
| D33 | PCI_SERR# | PCI Bus System Error | I/O-5T | | |
| D34 | PCI_STOP# | PCI Bus Stop | I/O-5T | | |
| D35 | PCI_TRDY# | PCI Bus Target Ready | I/O-5T | | |
| D36 | PCI_FRAME# | PCI Bus Cycle Frame | I/O-5T | | |
| D37 | PCI_AD16 | PCI Address & Data Bus line | I/O-5T | | |
| D38 | PCI_AD18 | PCI Address & Data Bus line | I/O-5T | | |
| D39 | PCI_AD20 | PCI Address & Data Bus line | I/O-5T | | |
| D40 | PCI_AD22 | PCI Address & Data Bus line | I/O-5T | | |
| D41 | GND (Fixed) | Power Ground | PWR | - | - |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D42 | PCI_AD24 | PCI Address & Data Bus line | I/O-5T | | |
| D43 | PCI_AD26 | PCI Address & Data Bus line | I/O-5T | | |
| D44 | PCI_AD28 | PCI Address & Data Bus line | I/O-5T | | |
| D45 | PCI_AD30 | PCI Address & Data Bus line | I/O-5T | | |
| D46 | PCI_IRQC# | PCI Bus Interrupt Request C | I-5T | | |
| D47 | PCI_IRQD# | PCI Bus Interrupt Request D | I-5T | | |
| D48 | PCI_CLKRUN# | PCI Clock Run | O-3.3 | | |
| D49 | PCI_M66EN | PCI_M66EN | I-5T | | |
| D50 | PCI_CLK | PCI Clock 33MHz | O-3.3 | | |
| D51 | GND (Fixed) | Power Ground | PWR | - | - |
| D52 | PEG_TX0+ | PCI Express Graphics Transmit Data Lane 0 Positive | DP-O | | |
| D53 | PEG_TX0- | PCI Express Graphics Transmit Data Lane 0 Negative | DP-O | | |
| D54 | PEG_LANE_RV# | PCI Express Graphics Lane Reversal Input strap | I-3.3 | | |
| D55 | PEG_TX1+ | PCI Express Graphics Transmit Data Lane 1 Positive | DP-O | | |
| D56 | PEG_TX1- | PCI Express Graphics Transmit Data Lane 1 Negative | DP-O | | |
| D57 | TYPE2# | Pulled low for Type 2 modules | PDS | | |
| D58 | PEG_TX2+ | PCI Express Graphics Transmit Data Lane 2 Positive | DP-O | | |
| D59 | PEG_TX2- | PCI Express Graphics Transmit Data Lane 2 Negative | DP-O | | |
| D60 | GND (Fixed) | Power Ground | PWR | - | - |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D61 | PEG_TX3+ | PCI Express Graphics Transmit Data Lane 3 Positive | DP-O | | |
| D62 | PEG_TX3- | PCI Express Graphics Transmit Data Lane 3 Negative | DP-O | | |
| D63 | RSVD | Reserved | Not connected | nc | nc |
| D64 | RSVD | Reserved | Not connected | nc | nc |
| D65 | PEG_TX4+ | PCI Express Graphics Transmit Data Lane 4 Positive | DP-O | | |
| D66 | PEG_TX4- | PCI Express Graphics Transmit Data Lane 4 Negative | DP-O | | |
| D67 | GND | Power Ground | PWR | - | - |
| D68 | PEG_TX5+ | PCI Express Graphics Transmit Data Lane 5 Positive | DP-O | | |
| D69 | PEG_TX5- | PCI Express Graphics Transmit Data Lane 5 Negative | DP-O | | |
| D70 | GND (Fixed) | Power Ground | PWR | - | - |
| D71 | PEG_TX6+ | PCI Express Graphics Transmit Data Lane 6 Positive | DP-O | | |
| D72 | PEG_TX6- | PCI Express Graphics Transmit Data Lane 6 Negative | DP-O | | |
| D73 | SDVO_CLK | SDVO Clock | Not connected | nc | nc |
| D74 | PEG_TX7+ | PCI Express Graphics Transmit Data Lane 7 Positive | DP-O | | |
| D75 | PEG_TX7- | PCI Express Graphics Transmit Data Lane 7 Negative | DP-O | | |
| D76 | GND | Power Ground | PWR | - | - |
| D77 | IDE_CBLID | 40/80-pin IDE cable ID | I-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D78 | PEG_TX8+ | PCI Express Graphics Transmit Data Lane 8 Positive | DP-O | | |
| D79 | PEG_TX8- | PCI Express Graphics Transmit Data Lane 8 Negative | DP-O | | |
| D80 | GND (Fixed) | Power Ground | PWR | - | - |
| D81 | PEG_TX9+ | PCI Express Graphics Transmit Data Lane 9 Positive | DP-O | | |
| D82 | PEG_TX9- | PCI Express Graphics Transmit Data Lane 9 Negative | DP-O | | |
| D83 | RSVD | Reserved | Not connected | nc | nc |
| D84 | GND | Power Ground | PWR | - | - |
| D85 | PEG_TX10+ | PCI Express Graphics Transmit Data Lane 10 Positive | DP-O | | |
| D86 | PEG_TX10- | PCI Express Graphics Transmit Data Lane 10 Negative | DP-O | | |
| D87 | GND | Power Ground | PWR | - | - |
| D88 | PEG_TX11+ | PCI Express Graphics Transmit Data Lane 11 Positive | DP-O | | |
| D89 | PEG_TX11- | PCI Express Graphics Transmit Data Lane 11 Negative | DP-O | | |
| D90 | GND (Fixed) | Power Ground | PWR | - | - |
| D91 | PEG_TX12+ | PCI Express Graphics Transmit Data Lane 12 Positive | DP-O | | |
| D92 | PEG_TX12- | PCI Express Graphics Transmit Data Lane 12 Negative | DP-O | | |
| D93 | GND | Power Ground | PWR | - | - |
| D94 | PEG_TX13+ | PCI Express Graphics | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Transmit Data Lane 13 Positive | | | |
| D95 | PEG_TX13- | PCI Express Graphics Transmit Data Lane 13 Negative | DP-O | | |
| D96 | GND | Power Ground | PWR | - | - |
| D97 | PEG_ENABLE# | Enable PCI Express x16 external Graphics Interface | I-3.3 | | |
| D98 | PEG_TX14+ | PCI Express Graphics Transmit Data Lane 14 Positive | DP-O | | |
| D99 | PEG_TX14- | PCI Express Graphics Transmit Data Lane 14 Negative | DP-O | | |
| D100 | GND (Fixed) | Power Ground | PWR | - | - |
| D101 | PEG_TX15+ | PCI Express Graphics Transmit Data Lane 15 Positive | DP-O | | |
| D102 | PEG_TX15- | PCI Express Graphics Transmit Data Lane 15 Negative | DP-O | | |
| D103 | GND | Power Ground | PWR | - | - |
| D104 | VCC_12V | 12V VCC | PWR | - | - |
| D105 | VCC_12V | 12V VCC | PWR | - | - |
| D106 | VCC_12V | 12V VCC | PWR | - | - |
| D107 | VCC_12V | 12V VCC | PWR | - | - |
| D108 | VCC_12V | 12V VCC | PWR | - | - |
| D109 | VCC_12V | 12V VCC | PWR | - | - |
| D110 | GND (Fixed) | Power Ground | PWR | - | - |

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express™ Design Guide for information about additional termination resistors.

## 4.2 COM Express™ Type 6 Pin-Outs

### Table 7: Type 6 Connector X1A - Row A

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A1 | GND (Fixed) | Power Ground | PWR | - | - |
| A2 | GBE0_MDI3- | Ethernet Receive Data- | DP-I | Intel® 82577 | - |
| A3 | GBE0_MDI3+ | Ethernet Receive Data+ | DP-I | Intel® 82577 | - |
| A4 | GBE0_LINK100# | Ethernet Speed LED 100Mbps | O-3.3 | Intel® 82577 | - |
| A5 | GBE0_LINK1000# | Ethernet Speed LED 1000Mbps | O-3.3 | Intel® 82577 | - |
| A6 | GBE0_MDI2- | Ethernet Receive Data- | DP-I | Intel® 82577 | - |
| A7 | GBE0_MDI2+ | Ethernet Receive Data+ | DP-I | Intel® 82577 | - |
| A8 | GBE0_LINK# | LAN Link LED | OD | Intel® 82577 | - |
| A9 | GBE0_MDI1- | Ethernet Receive Data- | DP-I | Intel® 82577 | - |
| A10 | GBE0_MDI1+ | Ethernet Receive Data+ | DP-I | Intel® 82577 | - |
| A11 | GND (Fixed) | Power Ground | PWR | - | - |
| A12 | GBE0_MDI0- | Ethernet Transmit Data- | DP-O | Intel® 82577 | - |
| A13 | GBE0_MDI0+ | Ethernet Transmit Data+ | DP-O | Intel® 82577 | - |
| A14 | GBE0_CTREF | LAN Reference Voltage | O-3.3 | is on a power rail controlled | - |
| A15 | SUS_S3# | Indicates Suspend to RAM state | O-3.3 | CPLD I/O | CPLD I/O |
| A16 | SATA0_TX+ | SATA 0 Transmit Data+ | DP-O | | - |
| A17 | SATA0_TX- | SATA 0 Transmit Data- | DP-O | | - |
| A18 | SUS_S4# | Indicates Suspend to Disk state | O-3.3 | CPLD I/O | CPLD I/O |
| A19 | SATA0_RX+ | SATA 0 Receive Data+ | DP-I | | |
| A20 | SATA0_RX- | SATA 0 Receive Data- | DP-I | | - |
| A21 | GND (Fixed) | Power Ground | PWR | | - |
| A22 | SATA2_TX+ | SATA 2 Transmit Data- | DP-O | | |
| A23 | SATA2_TX- | SATA 2 Transmit Data+ | DP-O | | |
| A24 | SUS_S5# | Indicates Soft Off state | O-3.3 | CPLD I/O | CPLD I/O |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A25 | SATA2_RX+ | SATA 2 Receive Data+ | Not connected | nc | nc |
| A26 | SATA2_RX- | SATA 2 Receive Data- | Not connected | nc | nc |
| A27 | BATLOW# | Indicates low external battery | I-3.3 | | CPLD I/O |
| A28 | (S)ATA_ACT# | SATA, IDE, SD Activity Indicator | O-3.3 | Buffered output | |
| A29 | AC/HDA_SYNC | HD Audio Sync | O-3.3 | | |
| A30 | AC/HDA_RST# | HD Audio Reset | O-3.3 | | |
| A31 | GND Fixed) | Power Ground | PWR | - | - |
| A32 | AC/HDA_BITCLK | HD Audio Clock | O-3.3 | | |
| A33 | AC/HDA_SDOUT | HD Audio Data | O-3.3 | | |
| A34 | BIOS_DIS0# | Disable Module BIOS Enables boot from a BIOS on Baseboard | I-3.3 | | |
| A35 | THRMTRIP# | CPU thermal shutdown indicator | O-3.3 | | |
| A36 | USB6- | USB Data- Port #6 | DP-I/O | | - |
| A37 | USB6+ | USB Data+ Port #6 | DP-I/O | | - |
| A38 | USB_6_7_OC# | USB Overcurrent Pair 6/7 | I-3.3 | | |
| A39 | USB4- | USB Data- Port #4 | DP-I/O | | |
| A40 | USB4+ | USB Data+ Port #4 | DP-I/O | | - |
| A41 | GND (Fixed) | Power Ground | PWR | - | - |
| A42 | USB2- | USB Data- Port #2 | | | |
| A43 | USB2+ | USB Data+ Port #2 | DP-I/O | | |
| A44 | USB_2_3_OC# | USB Overcurrent Pair 2/3 | I-3.3 | | |
| A45 | USB0- | USB Data- Port #0 | DP-I/O | | |
| A46 | USB0+ | USB Data+ Port #0 | DP-I/O | | |
| A47 | VCC_RTC | RTC Power Supply +3V | PWR | - | - |
| A48 | EXCD0_PERST# | PCIe Express Card 0 Reset | O-3.3 | | |
| A49 | EXCD0_CPPE# | PCIe Express Card 0 Request | I-3.3 | | |
| A50 | LPC_SERIRQ | LPC Serial Interrupt Request | IO-3.3 | | |
| A51 | GND (Fixed) | Power Ground | PWR | - | - |
| A52 | PCIE_TX5+ | PCIe 5 Transmit Data+ | DP-O | | |
| A53 | PCIE_TX5- | PCIe 5 Transmit | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Data- | | | |
| A54 | GPI0 | General Purpose Input 0 | I-3.3 | | |
| A55 | PCIE_TX4+ | PCIe 4 Transmit Data+ | DP-O | | |
| A56 | PCIE_TX4- | PCIe 4 Transmit Data- | DP-O | | |
| A57 | GND (Fixed) | Power Ground | PWR | - | - |
| A58 | PCIE_TX3+ | PCIe 3 Transmit Data+ | DP-O | | |
| A59 | PCIE_TX3- | PCIe 3 Transmit Data- | DP-O | | |
| A60 | GND (Fixed) | Power Ground | PWR | - | - |
| A61 | PCIE_TX2+ | PCIe 2 Transmit Data+ | DP-O | | |
| A62 | PCIE_TX2- | PCIe 2 Transmit Data- | DP-O | | |
| A63 | GPI1 | General Purpose Input 1 | I-3.3 | | |
| A64 | PCIE_TX1+ | PCIe 1 Transmit Data+ | DP-O | | |
| A65 | PCIE_TX1- | PCIe 1 Transmit Data- | DP-O | | |
| A66 | GND (Fixed) | Power Ground | PWR | - | - |
| A67 | GPI2 | General Purpose Input 2 | I-3.3 | | |
| A68 | PCIE_TX0+ | PCIe lane #0 Transmit+ | DP-O | | |
| A69 | PCIE_TX0- | PCIe lane #0 Transmit- | DP-O | | |
| A70 | GND (Fixed) | Power Ground | PWR | - | - |
| A71 | LVDS_A0+ | LVDS Channel A (positive) | DP-O | | |
| A72 | LVDS_A0- | LVDS Channel A (negative) | DP-O | | - |
| A73 | LVDS_A1+ | LVDS Channel A (positive) | DP-O | | - |
| A74 | LVDS_A1- | LVDS Channel A (negative) | DP-O | | |
| A75 | LVDS_A2+ | LVDS Channel A (positive) | DP-O | | |
| A76 | LVDS_A2- | LVDS Channel A (negative) | DP-O | | |
| A77 | LVDS_VDD_EN | LVDS Panel Power Controller | O-3.3 | | |
| A78 | LVDS_A3+ | LVDS Channel A (positive) | DP-O | | |
| A79 | LVDS_A3- | LVDS Channel A (negative) | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A80 | GND (Fixed) | Power Ground | PWR | - | - |
| A81 | LVDS_A_CK+ | LVDS Channel A Clock+ | DP-O | | |
| A82 | LVDS_A_CK- | LVDS Channel A Clock- | DP-O | | |
| A83 | LVDS_I2C_CK | LVDS I2C Clock | IO-3.3 | | |
| A84 | LVDS_I2C_DAT | LVDS I2C Data | IO-3.3 | | |
| A85 | GPI3 | General Purpose Input 3 | I-3.3 | | |
| A86 | RSVD | Reserved | Not connected | nc | nc |
| A87 | RSVD | Reserved | Not connected | Nc | nc |
| A88 | PCIE0_CK_REF+ | PCIe Clock (positive) | DP-O | | |
| A89 | PCIE0_CK_REF- | PCIe Clock (negative) | DP-O | | |
| A90 | GND (Fixed) | Power Ground | PWR | - | - |
| A91 | SPI_Power | Power for off-board SPI flash | O-3.3 | | |
| A92 | SPI_MISO | SPI Master In Slave Out data line | I-3.3 | | |
| A93 | GPO0 | General Purpose Output 0 | O-3.3 | | |
| A94 | SPI_CLK | SPI clock line for off-board SPI | O-3.3 | | |
| A95 | SPI_MOSI | SPI Master Out Slave In data line | O-3.3 | | - |
| A96 | TPM_PP | Trusted Platform Module Physical Presence pin | I-3.3 | | |
| A97 | TYPE10# | Indicates to Type 10 Carrier Board that Module is installed | Not connected | nc | nc |
| A98 | SER0_TX | Gen. Purpose Serial Port 0 Transmit | Not connected | nc | nc |
| A99 | SER0_RX | Gen. Purpose Serial Port 0 Receive | Not connected | nc | nc |
| A100 | GND (Fixed) | Power Ground | PWR | - | - |
| A101 | SER1_TX | Gen. Purpose Serial Port 1 Transmit | Not connected | nc | nc |
| A102 | SER1_RX | Gen. Purpose Serial Port 1 Receive | Not connected | nc | nc |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| A103 | LID# | LID Button | I/OP-3.3 | | |
| A104 | VCC_12V | 12V VCC | PWR | - | - |
| A105 | VCC_12V | 12V VCC | PWR | - | - |
| A106 | VCC_12V | 12V VCC | PWR | - | - |
| A107 | VCC_12V | 12V VCC | PWR | - | - |
| A108 | VCC_12V | 12V VCC | PWR | - | - |
| A109 | VCC_12V | 12V VCC | PWR | - | - |
| A110 | GND | Power Ground | PWR | - | - |

## Table 8: Type 6 Connector X1A - Row B

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| B1 | GND (Fixed) | Power Ground | PWR | - | - |
| B2 | GBE0_ACT# | Ethernet Activity LED | Not connected | nc | nc |
| B3 | LPC_FRAME# | LPC Frame Indicator | O-3.3 | | |
| B4 | LPC_AD0 | LPC Address/Data Bus | IO-3.3 | | |
| B5 | LPC_AD1 | LPC Address/Data Bus | IO-3.3 | | |
| B6 | LPC_AD2 | LPC Address/Data Bus | IO-3.3 | | |
| B7 | LPC_AD3 | LPC Address/Data Bus | IO-3.3 | | |
| B8 | LPC_DRQ0# | LPC Serial DMA Request | I-3.3 | | |
| B9 | LPC_DRQ1# | LPC Serial DMA Request | I-3.3 | | |
| B10 | LPC_CLK | LPC Clock | O-3.3 | | |
| B11 | GND (Fixed) | Power Ground | PWR | - | - |
| B12 | PWRBTN# | Power Button Input | I-3.3 | | |
| B13 | SMB_CLK | SMBus Clock | O-3.3 | | |
| B14 | SMB_DAT | SMBus Data | IO-3.3 | | |
| B15 | SMB_ALERT# | SMBus Interrupt | IO-3.3 | | |
| B16 | SATA1_TX+ | SATA 1 Transmit Data+ | DP-O | | |
| B17 | SATA1_TX- | SATA 1 Transmit Data- | DP-O | | |
| B18 | SUS_STAT# | Imminent suspend operation; used to notify LPC devices. | O-3.3 | | |
| B19 | SATA1_RX+ | SATA 1 Receive Data+ | DP-I | | |
| B20 | SATA1_RX- | SATA 1 Receive Data- | DP-I | | |
| B21 | GND (Fixed) | Power Ground | PWR | - | - |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| B22 | SATA3_TX+ | SATA 3 Transmit Data+ | DP-O | | |
| B23 | SATA3_TX- | SATA 3 Transmit Data- | DP-O | | |
| B24 | PWR_OK | Power OK from power supply | I-3.3 | | |
| B25 | SATA3_RX+ | SATA 3 Receive Data+ | DP-I | | |
| B26 | SATA3_RX- | SATA 3 Receive Data- | DP-I | | |
| B27 | WDT | Watchdog Timeout | O-3.3 | | |
| B28 | AC/HDA_SDIN2 | Audio CODEC Serial Data In 2 | I-3.3 | | |
| B29 | AC/HDA_SDIN1 | Audio CODEC Serial Data In 1 | I-3.3 | | |
| B30 | AC/HDA_SDIN0 | Audio CODEC Serial Data In 0 | I-3.3 | | |
| B31 | GND (Fixed) | Power Ground | PWR | - | - |
| B32 | SPKR | Speaker Interface | O-3.3 | | |
| B33 | I2C_CK | $I^2C$ Clock | IO-3.3 | | |
| B34 | I2C_DAT | $I^2C$ Data | IO-3.3 | | |
| B35 | THRM# | Over Temperature Indicator | I-3.3 | | |
| B36 | USB7- | USB Data- Port #7 | DP-I/O | | |
| B37 | USB7+ | USB Data+ Port #7 | DP-I/O | | |
| B38 | USB_4_5_OC# | USB Overcurrent Pair 4/5 | I-3.3 | | |
| B39 | USB5- | USB Data- Port #5 | DP-I/O | | |
| B40 | USB5+ | USB Data+ Port #5 | DP-I/O | | |
| B41 | GND (Fixed) | Power Ground | PWR | - | - |
| B42 | USB3- | USB Data- Port #3 | DP-I/O | | |
| B43 | USB3+ | USB Data+ Port #3 | DP-I/O | | |
| B44 | USB_0_1_OC# | USB Overcurrent Pair 0/1 | I-3.3 | | |
| B45 | USB1- | USB Data- Port #1 | DP-I/O | | |
| B46 | USB1+ | USB Data+ Port #1 | DP-I/O | | |
| B47 | EXCD1_PERST# | PCIe Express Card 1 Reset | O-3.3 | | |
| B48 | EXCD1_CPPE# | PCIe Express Card 1 Request | I-3.3 | | |
| B49 | SYS_RESET# | Reset button input | I-3.3 | | |
| B50 | CB_RESET# | Carrier Board Reset | O-3.3 | | |
| B51 | GND (Fixed) | Power Ground | PWR | - | - |
| B52 | PCIE_RX5+ | PCIe 5 Receive | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Data+ | | | |
| B53 | PCIE_RX5- | PCIe 5 Receive Data- | DP-I | | |
| B54 | GPO1 | General Purpose Output 1 | O-3.3 | | |
| B55 | PCIE_RX4+ | PCIe 4 Receive Data+ | DP-I | | |
| B56 | PCIE_RX4- | PCIe 4 Receive Data- | DP-I | | |
| B57 | GPO2 | General Purpose Output 2 | O-3.3 | | |
| B58 | PCIE_RX3+ | PCIe 3 Receive Data+ | DP-I | | |
| B59 | PCIE_RX3- | PCIe 5 Receive Data- | DP-I | | |
| B60 | GND (Fixed) | Power Ground | PWR | - | - |
| B61 | PCIE_RX2+ | PCIe 2 Receive Data+ | DP-I | | |
| B62 | PCIE_RX2- | PCIe 2 Receive Data- | DP-I | | |
| B63 | GPO3 | General Purpose Output 3 | O-3.3 | | |
| B64 | PCIE_RX1+ | PCIe 1 Receive Data+ | DP-I | | |
| B65 | PCIE_RX1- | PCIe 1 Receive Data- | DP-I | | |
| B66 | WAKE0# | PCI Express Wake Event | I-3.3 | | |
| B67 | WAKE1# | General Purpose Wake Event | I-3.3 | | |
| B68 | PCIE_RX0+ | PCIe lane #0 Receive+ | DP-I | | |
| B69 | PCIE_RX0- | PCIe lane #0 Receive- | DP-I | | |
| B70 | GND (Fixed) | Power Ground | PWR | - | - |
| B71 | LVDS_B0+ | LVDS Channel B0 (Positive) | DP-O | | |
| B72 | LVDS_B0- | LVDS Channel B0 (Negative) | DP-O | | |
| B73 | LVDS_B1+ | LVDS Channel B1 (Positive) | DP-O | | |
| B74 | LVDS_B1- | LVDS Channel B1 (Negative) | DP-O | | |
| B75 | LVDS_B2+ | LVDS Channel B2 (Positive) | DP-O | | |
| B76 | LVDS_B2- | LVDS Channel B2 (Negative) | DP-O | | |
| B77 | LVDS_B3+ | LVDS Channel B3 (Positive) | DP-O | | |
| B78 | LVDS_B3- | LVDS Channel B3 | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | (Negative) | | | |
| B79 | LVDS_BKLT_EN | Backlight Enable | O-3.3 | | |
| B80 | GND (Fixed) | Power Ground | PWR | - | - |
| B81 | LVDS_B_CK+ | LVDS Channel B Clock+ | DP-O | | |
| B82 | LVDS_B_CK- | LVDS Channel B Clock- | DP-O | | |
| B83 | LVDS_BKLT_CTRL | Backlight Brightness Control | O-3.3 | | |
| B84 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B85 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B86 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B87 | VCC_5V_SBY | +5V Standby | PWR | - | - |
| B88 | BIOS_DIS1# | BIOS Disable 1 (offboard SPI select) | I-3.3 | | |
| B89 | VGA_RED | Analog Video Red | O | | |
| B90 | GND (Fixed) | Power Ground | PWR | - | - |
| B91 | VGA_GRN | Analog Video Green | O | | |
| B92 | VGA_BLU | Analog Video Blue | O | | |
| B93 | VGA_HSYNC | Analog Video Horizontal Sync | O-3.3 | | |
| B94 | VGA_VSYNC | Analog Video Vertical Sync | O-3.3 | | |
| B95 | VGA_I2C_CK | Analog Video I2C Clock | IO/OD-3.3 | | |
| B96 | VGA_I2C_DAT | Analog Video I2C Data | IO/OD-3.3 | | |
| B97 | SPI_CS# | SPI Chip Select | O-3.3 | | |
| B98 | RSVD | Reserved | Not connected | nc | nc |
| B99 | RSVD | Reserved | Not connected | nc | nc |
| B100 | GND (Fixed) | Power Ground | PWR | - | - |
| B101 | FAN_PWMOUT | Fan Speed Control | O/OP-3.3 | | |
| B102 | FAN_TACHIN | Fan Tachometer Input | I/OP-3.3 | | |
| B103 | SLEEP# | Sleep Button | I/OP-3.3 | | |
| B104 | VCC_12V_16 | 12V VCC | PWR | - | - |
| B105 | VCC_12V_17 | 12V VCC | PWR | - | - |
| B106 | VCC_12V_18 | 12V VCC | PWR | - | - |
| B107 | VCC_12V_19 | 12V VCC | PWR | - | - |
| B108 | VCC_12V_20 | 12V VCC | PWR | - | - |
| B109 | VCC_12V_21 | 12V VCC | PWR | - | - |
| B110 | GND (Fixed) | Power Ground | PWR | | |

NOTE: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express™ Design Guide for information about additional termination resistors.

## Table 9: Type 6 Connector X1B - Row C

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| C1 | GND (Fixed) | Power Ground | PWR | - | - |
| C2 | GND | Power Ground | PWR | - | - |
| C3 | USB_SSRXO- | SuperSpeed USB Data Receive Path 0- | Not connected | nc | nc |
| C4 | USB_SSRXO+ | SuperSpeed USB Data Receive Path 0+ | Not connected | nc | nc |
| C5 | GND | Power Ground | PWR | - | - |
| C6 | USB_SSRX1- | SuperSpeed USB Data Receive Path 1- | Not connected | nc | nc |
| C7 | USB_SSRX1+ | SuperSpeed USB Data Receive Path 1+ | Not connected | nc | nc |
| C8 | GND | Power Ground | PWR | - | - |
| C9 | USB_SSRX2- | SuperSpeed USB Data Receive Path 2- | Not connected | nc | nc |
| C10 | SUB_SSRX2+ | SuperSpeed USB Data Receive Path 2+ | Not connected | nc | nc |
| C11 | GND (Fixed) | Power Ground | PWR | | |
| C12 | USB_SSRX3- | SuperSpeed USB Data Receive Path 3- | Not connected | nc | nc |
| C13 | USB_SSRX3+ | SuperSpeed USB Data Receive Path 3+ | Not connected | nc | nc |
| C14 | GND | Power Ground | PWR | - | - |
| C15 | DDI1_PAIR6+ | Digital Display Interface | Not connected | nc | nc |
| C16 | DDI1_PAIR6- | Digital Display Interface | Not connected | nc | nc |
| C17 | RSVD | Reserved | Not connected | nc | nc |
| C18 | RSVD | Reserved | Not connected | nc | nc |
| C19 | PCIE_RX6+ | PCI Express Differential Receive Pair 6+ | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| C20 | PCIE_RX6- | PCI Express Differential Receive Pair 6- | DP-I | | |
| C21 | GND (Fixed) | Power Ground | PWR | | |
| C22 | PCIE_RX7+ | PCI Express Differential Receive Pair 7+ | Not connected | nc | nc |
| C23 | PCIE_RX7- | PCI Express Differential Receive Pair 7- | Not connected | nc | nc |
| C24 | DDI1_HPD | Digital Display Interface Hot-plug detect | I-3.3 | | |
| C25 | DDI1_PAIR4+ | Digital Display Interface | Not connected | nc | nc |
| C26 | DDI1_PAIR4- | Digital Display Interface | Not connected | nc | nc |
| C27 | RSVD | Reserved | Not connected | nc | nc |
| C28 | RSVD | Reserved | Not connected | nc | nc |
| C29 | DDI1_PAIR5+ | Digital Display Interface | Not connected | nc | nc |
| C30 | DDI1_PAIR5- | Digital Display Interface | Not connected | nc | nc |
| C31 | GND (Fixed) | Power Ground | PWR | - | - |
| C32 | DDI2_CRTLCLK_AUX+ | HDMI/DVI $I^2C$ CRTLCLK | I/O-3.3 | | |
| C33 | DDI2_CRTLDATA_AUX- | HDMI/DVI $I^2C$ CRTLDATA | I/O-3.3 | | |
| C34 | DDI2_DDC_AUX_SEL | Selects function of DDI CRTL & DATA Aux | I-3.3 | | |
| C35 | RSVD | Reserved | Not connected | nc | nc |
| C36 | DDI3_CRTLCLK_AUX+ | HDMI/DVI I2C CRTLCLK | I/O-3.3 | | |
| C37 | DDI3_CRTLDATA_AUX- | HDMI/DVI I2C CRTLDATA | I/O-3.3 | | |
| C38 | DDI3_DDC_AUX_SEL | Selects function of DDI CRTL & | I-3.3 | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | DATA Aux | | | |
| C39 | DDI3_PAIR0+ | Digital Display Interface | DP-O | | |
| C40 | DDI3_PAIR0- | Digital Display Interface | DP-O | | |
| C41 | GND (Fixed) | Power Ground | PWR | - | - |
| C42 | DDI3_PAIR1+ | Digital Display Interface | DP-O | | |
| C43 | DDI3_PAIR1- | Digital Display Interface | DP-O | | |
| C44 | DDI3_HPD | Digital Display Interface Hot-plug detect | I-3.3 | | |
| C45 | RSVD | Reserved | Not connected | nc | nc |
| C46 | DDI3_PAIR2+ | Digital Display Interface | DP-O | | |
| C47 | DDI3_PAIR2- | Digital Display Interface | DP-O | | |
| C48 | RSVD | Reserved | Not connected | nc | nc |
| C49 | DDI3_PAIR3+ | Digital Display Interface | DP-O | | |
| C50 | DDI3_PAIR3- | Digital Display Interface | DP-O | | |
| C51 | GND (Fixed) | Power Ground | PWR | - | - |
| C52 | PEG_RX0+ | PCI Express Graphics Receive Lane 0 Positive | DP-I | | |
| C53 | PEG_RX0- | PCI Express Graphics Receive Lane 0 Negative | DP-I | | |
| C54 | TYPE0# | Not connected for Type 6 module | Not connected | nc | nc |
| C55 | PEG_RX1+ | PCI Express Graphics Receive Lane 1 Positive | DP-I | | |
| C56 | PEG_RX1- | PCI Express | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Graphics Receive Lane 1 Negative | | | |
| C57 | TYPE1# | Not connected for Type 6 module | Not connected | nc | nc |
| C58 | PEG_RX2+ | PCI Express Graphics Receive Lane 2 Positive | DP-I | | |
| C59 | PEG_RX2- | PCI Express Graphics Receive Lane 2 Negative | DP-I | | |
| C60 | GND (Fixed) | Power Ground | PWR | - | - |
| C61 | PEG_RX3+ | PCI Express Graphics Receive Lane 3 Positive | DP-I | | |
| C62 | PEG_RX3- | PCI Express Graphics Receive Lane 3 Negative | DP-I | | |
| C63 | RSVD | Reserved | Not connected | nc | nc |
| C64 | RSVD | Reserved | Not connected | nc | nc- |
| C65 | PEG_RX4+ | PCI Express Graphics Receive Lane 4 Positive | DP-I | | |
| C66 | PEG_RX4- | PCI Express Graphics Receive Lane 4 Negative | DP-I | | |
| C67 | RSVD | Reserved | Not connected | nc | nc |
| C68 | PEG_RX5+ | PCI Express Graphics Receive Lane 5 Positive | DP-I | | |
| C69 | PEG_RX5- | PCI Express Graphics Receive Lane 5 Negative | DP-I | | |
| C70 | GND (Fixed) | Power Ground | PWR | - | - |
| C71 | PEG_RX6+ | PCI Express Graphics Receive Lane 6 Positive | DP-I | | |
| C72 | PEG_RX6- | PCI Express Graphics Receive Lane 6 Negative | DP-I | | |
| C73 | GND | Power Ground | PWR | - | - |
| C74 | PEG_RX7+ | PCI Express Graphics | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Receive Lane 7 Positive | | | |
| C75 | PEG_RX7- | PCI Express Graphics Receive Lane 7 Negative | DP-I | | |
| C76 | GND (Fixed) | Power Ground | PWR | - | - |
| C77 | RSVD | Reserved | Not connected | nc | nc |
| C78 | PEG_RX8+ | PCI Express Graphics Receive Lane 8 Positive | DP-I | | |
| C79 | PEG_RX8- | PCI Express Graphics Receive Lane 8 Negative | DP-I | | |
| C80 | GND (Fixed) | Power Ground | PWR | - | - |
| C81 | PEG_RX9+ | PCI Express Graphics Receive Lane 9 Positive | DP-I | | |
| C82 | PEG_RX9- | PCI Express Graphics Receive Lane 9 Negative | DP-I | | |
| C83 | RSVD | Reserved | Not connected | nc | nc |
| C84 | GND | Power Ground | PWR | - | - |
| C85 | PEG_RX10+ | PCI Express Graphics Receive Lane 10 Positive | DP-I | | |
| C86 | PEG_RX10- | PCI Express Graphics Receive Lane 10 Negative | DP-I | | |
| C87 | GND | Power Ground | PWR | - | - |
| C88 | PEG_RX11+ | PCI Express Graphics Receive Lane 11 Positive | DP-I | | |
| C89 | PEG_RX11- | PCI Express Graphics Receive Lane 11 Negative | DP-I | | |
| C90 | GND (Fixed) | Power Ground | PWR | - | - |
| C91 | PEG_RX12+ | PCI Express Graphics Receive Lane 12 Positive | DP-I | | |
| C92 | PEG_RX12- | PCI Express Graphics Receive Lane 12 Negative | DP-I | | |
| C93 | GND | Power Ground | PWR | - | - |
| C94 | PEG_RX13+ | PCI Express Graphics | DP-I | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Receive Lane 13 Positive | | | |
| C95 | PEG_RX13- | PCI Express Graphics Receive Lane 13 Negative | DP-I | | |
| C96 | GND | Power Ground | PWR | - | - |
| C97 | RSVD | Reserved | Not connected | nc | nc |
| C98 | PEG_RX14+ | PCI Express Graphics Receive Lane 14 Positive | DP-I | | |
| C99 | PEG_RX14- | PCI Express Graphics Receive Lane 14 Negative | DP-I | | |
| C100 | GND (Fixed) | Power Ground | PWR | - | - |
| C101 | PEG_RX15+ | PCI Express Graphics Receive Lane 15 Positive | DP-I | | |
| C102 | PEG_RX15- | PCI Express Graphics Receive Lane 15 Negative | DP-I | | |
| C103 | GND | Power Ground | PWR | - | - |
| C104 | VCC_12V | 12V VCC | PWR | - | - |
| C105 | VCC_12V | 12V VCC | PWR | - | - |
| C106 | VCC_12V | 12V VCC | PWR | - | - |
| C107 | VCC_12V | 12V VCC | PWR | - | - |
| C108 | VCC_12V | 12V VCC | PWR 8 | - | - |
| C109 | VCC_12V | 12V VCC | PWR | - | - |
| C110 | GND (Fixed) | Power Ground | PWR | - | - |

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express™ Design Guide for information about additional termination resistors.

## Table 10: Type 6 Connector X1B - Row D

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D1 | GND (Fixed) | Power Ground | PWR | - | - |
| D2 | GND | Power Ground | PWR | - | - |
| D3 | USB_SSTX0- | SuperSpeed USB Data Transmit Path 0- | Not connected | nc | nc |
| D4 | USB_SSTX0+ | SuperSpeed USB Data Transmit Path 0+ | Not connected | nc | nc |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D5 | GND | Power Ground | PWR | - | - |
| D6 | USB_SSTX1- | SuperSpeed USB Data Transmit Path 1- | Not connected | nc | nc |
| D7 | USB_SSTX1+ | SuperSpeed USB Data Transmit Path 1+ | Not connected | nc | nc |
| D8 | GND | Power Ground | PWR | - | - |
| D9 | USB_SSTX2- | SuperSpeed USB Data Transmit Path 2- | Not connected | nc | nc |
| D10 | USB_SSTX2+ | SuperSpeed USB Data Transmit Path 2+ | Not connected | nc | nc |
| D11 | GND (Fixed) | Power Ground | PWR | - | - |
| D12 | USB_SSTX3- | SuperSpeed USB Data Transmit Path 3- | Not connected | nc | nc |
| D13 | USB_SSTX3+ | SuperSpeed USB Data Transmit Path 3+ | Not connected | nc | nc |
| D14 | GND | Power Ground | PWR | - | - |
| D15 | DDI1_CTRLCLK_AUX+ | HDMI/DVI $I^2C$ CRTLCLK | I/O-3.3 | - | - |
| D16 | DDI1_CTRLDATA_AUX- | HDMI/DVI $I^2C$ CRTLDATA | I/O-3.3 | - | - |
| D17 | RSVD | Reserved | Not connected | nc | nc |
| D18 | RSVD | Reserved | Not connected | nc | nc |
| D19 | PCIE_TX6+ | PCI Express Differential Transmit Pair 6+ | DP-O | | |
| D20 | PCIE_TX6- | PCI Express Differential Transmit Pair 6- | DP-O | | |
| D21 | GND (Fixed) | Power Ground | PWR | - | - |
| D22 | PCIE_TX7+ | PCI Express Differential Transmit Pair 7+ | Not connected | nc | nc |
| D23 | PCIE_TX7- | PCI Express Differential Transmit Pair 7- | Not connected | nc | nc |
| D24 | RSVD | Reserved | Not connected | nc | nc |
| D25 | RSVD | Reserved | Not connected | nc | nc |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D26 | DDI1_PAIR0+ | Digital Display Interface | DP-O | | |
| D27 | DDI1_PAIR0- | Digital Display Interface | DP-O | | |
| D28 | RSVD | Reserved | Not connected | nc | nc |
| D29 | DDI1_PAIR1+ | Digital Display Interface1+ | DP-O | | |
| D30 | DDI1_PAIR1- | Digital Display Interface1- | DP-O | | |
| D31 | GND (FIXED) | Power Ground | PWR | - | - |
| D32 | DDI1_PAIR2+ | Digital Display Interface2+ | DP-O | | |
| D33 | DDI1_PAIR2- | Digital Display Interface2- | DP-O | | |
| D34 | DDI1_DDC_AUX_SEL | Selects function of DDI CRTL & DATA Aux | I-3.3 | | |
| D35 | RSVD | Reserved | | | |
| D36 | DDI1_PAIR3+ | Digital Display Interface3+ | DP-O | | |
| D37 | DDI1_PAIR3- | Digital Display Interface3- | DP-O | | |
| D38 | RSVD | Reserved | - | - | - |
| D39 | DDI2_PAIR0+ | Digital Display Interface0+ | DP-O | | |
| D40 | DDI2_PAIR0- | Digital Display Interface0- | DP-O | | |
| D41 | GND (FIXED) | Power Ground | PWR | - | - |
| D42 | DDI2_PAIR1+ | Digital Display Interface1+ | DP-O | | |
| D43 | DDI2_PAIR1- | Digital Display Interface1- | DP-O | | |
| D44 | DDI2_HPD | Digital Display Interface Hot-Plug Detect | I-3.3 | | |
| D45 | RSVD | Reserved | Not connected | nc | nc |
| D46 | DDI2_PAIR2+ | Digital Display Interface2+ | DP-O | | |
| D47 | DDI2_PAIR2- | Digital Display Interface2- | DP-O | | |
| D48 | RSVD | Reserved | Not connected | nc | nc |
| D49 | DDI2_PAIR3+ | Digital Display Interface3+ | DP-O | | |
| D50 | DDI2_PAIR3- | Digital Display Interface3- | DP-O | | |
| D51 | GND (Fixed) | Power Ground | PWR | - | - |
| D52 | PEG_TX0+ | PCI Express Graphics | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Transmit Data Lane 0 Positive | | | |
| D53 | PEG_TX0- | PCI Express Graphics Transmit Data Lane 0 Negative | DP-O | | |
| D54 | PEG_LANE_RV# | PCI Express Graphics Lane Reversal Input strap | I-3.3 | | |
| D55 | PEG_TX1+ | PCI Express Graphics Transmit Data Lane 1 Positive | DP-O | | |
| D56 | PEG_TX1- | PCI Express Graphics Transmit Data Lane 1 Negative | DP-O | | |
| D57 | TYPE2# | Not connected - for Type 2 modules | Not Connected | nc | nc |
| D58 | PEG_TX2+ | PCI Express Graphics Transmit Data Lane 2 Positive | DP-O | | |
| D59 | PEG_TX2- | PCI Express Graphics Transmit Data Lane 2 Negative | DP-O | | |
| D60 | GND (Fixed) | Power Ground | PWR | - | - |
| D61 | PEG_TX3+ | PCI Express Graphics Transmit Data Lane 3 Positive | DP-O | | |
| D62 | PEG_TX3- | PCI Express Graphics Transmit Data Lane 3 Negative | DP-O | | |
| D63 | RSVD | Reserved | Not connected | nc | nc |
| D64 | RSVD | Reserved | Not connected | nc | nc |
| D65 | PEG_TX4+ | PCI Express Graphics Transmit Data Lane 4 Positive | DP-O | | |
| D66 | PEG_TX4- | PCI Express Graphics Transmit Data Lane 4 Negative | DP-O | | |
| D67 | GND | Power Ground | PWR | - | - |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D68 | PEG_TX5+ | PCI Express Graphics Transmit Data Lane 5 Positive | DP-O | | |
| D69 | PEG_TX5- | PCI Express Graphics Transmit Data Lane 5 Negative | DP-O | | |
| D70 | GND (Fixed) | Power Ground | PWR | - | - |
| D71 | PEG_TX6+ | PCI Express Graphics Transmit Data Lane 6 Positive | DP-O | | |
| D72 | PEG_TX6- | PCI Express Graphics Transmit Data Lane 6 Negative | DP-O | | |
| D73 | GND | Power Ground | PWR | | |
| D74 | PEG_TX7+ | PCI Express Graphics Transmit Data Lane 7 Positive | DP-O | - | - |
| D75 | PEG_TX7- | PCI Express Graphics Transmit Data Lane 7 Negative | DP-O | - | - |
| D76 | GND | Power Ground | PWR | - | - |
| D77 | RSVD | Reserved | Not connected | nc | nc |
| D78 | PEG_TX8+ | PCI Express Graphics Transmit Data Lane 8 Positive | DP-O | | |
| D79 | PEG_TX8- | PCI Express Graphics Transmit Data Lane 8 Negative | DP-O | | |
| D80 | GND (Fixed) | Power Ground | PWR | - | - |
| D81 | PEG_TX9+ | PCI Express Graphics Transmit Data Lane 9 Positive | DP-O | | |
| D82 | PEG_TX9- | PCI Express Graphics Transmit Data Lane 9 Negative | DP-O | | |
| D83 | RSVD | Reserved | Not connected | nc | nc |
| D84 | GND | Power Ground | PWR | - | - |
| D85 | PEG_TX10+ | PCI Express | DP-O | | |

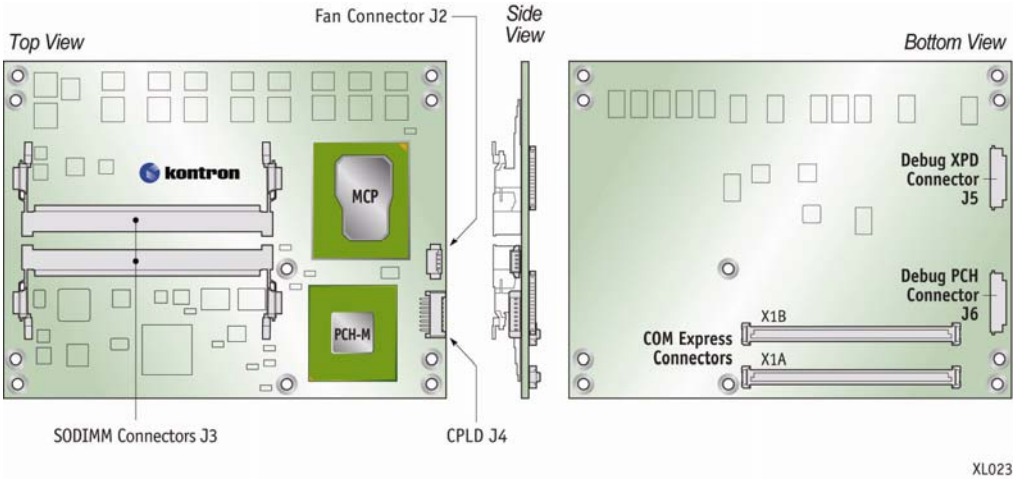
| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| | | Graphics Transmit Data Lane 10 Positive | | | |
| D86 | PEG_TX10- | PCI Express Graphics Transmit Data Lane 10 Negative | DP-O | | |
| D87 | GND | Power Ground | PWR | - | - |
| D88 | PEG_TX11+ | PCI Express Graphics Transmit Data Lane 11 Positive | DP-O | | |
| D89 | PEG_TX11- | PCI Express Graphics Transmit Data Lane 11 Negative | DP-O | | |
| D90 | GND (Fixed) | Power Ground | PWR | - | - |
| D91 | PEG_TX12+ | PCI Express Graphics Transmit Data Lane 12 Positive | DP-O | | |
| D92 | PEG_TX12- | PCI Express Graphics Transmit Data Lane 12 Negative | DP-O | | |
| D93 | GND | Power Ground | PWR | - | - |
| D94 | PEG_TX13+ | PCI Express Graphics Transmit Data Lane 13 Positive | DP-O | | |
| D95 | PEG_TX13- | PCI Express Graphics Transmit Data Lane 13 Negative | DP-O | | |
| D96 | GND | Power Ground | PWR | - | - |
| D97 | RSVD | Reserved | -- | -- | -- |
| D98 | PEG_TX14+ | PCI Express Graphics Transmit Data Lane 14 Positive | DP-O | | |

| Pin | Signal | Description | Type | Termination | Comment |
|---|---|---|---|---|---|
| D99 | PEG_TX14- | PCI Express Graphics Transmit Data Lane 14 Negative | DP-O | | |
| D100 | GND (Fixed) | Power Ground | PWR | - | - |
| D101 | PEG_TX15+ | PCI Express Graphics Transmit Data Lane 15 Positive | DP-O | | |
| D102 | PEG_TX15- | PCI Express Graphics Transmit Data Lane 15 Negative | DP-O | | |
| D103 | GND | Power Ground | PWR | - | - |
| D104 | VCC_12V | 12V VCC | PWR | - | - |
| D105 | VCC_12V | 12V VCC | PWR | - | - |
| D106 | VCC_12V | 12V VCC | PWR | - | - |
| D107 | VCC_12V | 12V VCC | PWR | - | - |
| D108 | VCC_12V | 12V VCC | PWR | - | - |
| D109 | VCC_12V | 12V VCC | PWR | - | - |
| D110 | GND (Fixed) | Power Ground | PWR | - | - |

NOTE: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express™ Design Guide for information about additional termination resistors.

## 4.3 Onboard Connectors

### Figure 4: J2, J3, J4, J5 and J6 Connector Locations




### 4.3.1Connector J4 – CPLD Debug

The onboard 12-pin connector J4 is for accessing the CPLD.

**WARNING**: The debug port is for internal use only. Do not connect any devices.

### 4.3.2Connector J3 – SODIMM DDR3

Up to 8 GBytes of DDR3 SODIMM memory can be installed on the ETXexpress-AI module (4GBytes in each of the two sockets). ECC is supported. Modules with non-ECC memory are also available on request.

### 4.3.3Connectors J5 and J6- BIOS Debugging Connectors

The ETXexpress-AI does not have any JTAG debug connector(s). Instead, there are two multi-purpose flat ribbon connectors that can be connected to the processor (the XDP connector, J5) and the platform controller hub (the PCH XDP connector, J6) for bring up and debug of the BIOS.

**WARNING**: The debug ports are for internal use only. Do not connect any devices to them.

### 4.3.4Connector J2 - Fan

This is a 4-pin connector for a 5V fan. J2 can be configured in the BIOS setup. See Section 6.2, "Onboard Fan Connector" for more detailed information.

## 4.4 Signal Descriptions

### 4.4.1PCI Express Interface

The PCI Express* x1 lane is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the COM Express™ specification. Refer to the PICMG COM Express™ Design Guide for additional implementation information.

The ETXexpress®-AI COM supports up to 7 PCI Express x1 lanes. See Table 11 and Table 12 for detailed configuration information.

**Table 11: PCI Express Configuration (Type 2)**

| Source | Target |
|---|---|
| Intel PCIe lane 1 | COMe PCIe lane 0 |
| Intel PCIe lane 2 | COMe PCIe lane 1 |
| Intel PCIe lane 3 | COMe PCIe lane 2 |
| Intel PCIe lane 4 | COMe PCIe lane 3 |
| Intel PCIe lane 5 | COMe PCIe lane 4 |
| Intel PCIe lane 6 | COMe PCIe lane 5 |
| Intel PCIe lane 7 | COMe PCIe lane 6 |

**Table 12: PCI Express Configuration (Type 6)**

| Source | Target |
|---|---|
| Intel PCIe lane 1 | COMe PCIe lane 0 |
| Intel PCIe lane 2 | COMe PCIe lane 1 |
| Intel PCIe lane 3 | COMe PCIe lane 2 |
| Intel PCIe lane 4 | COMe PCIe lane 3 |
| Intel PCIe lane 5 | COMe PCIe lane 4 |
| Intel PCIe lane 6 | COMe PCIe lane 5 |
| Intel PCIe lane 7 | COMe PCIe lane 6 |

### 4.4.2USB Interface

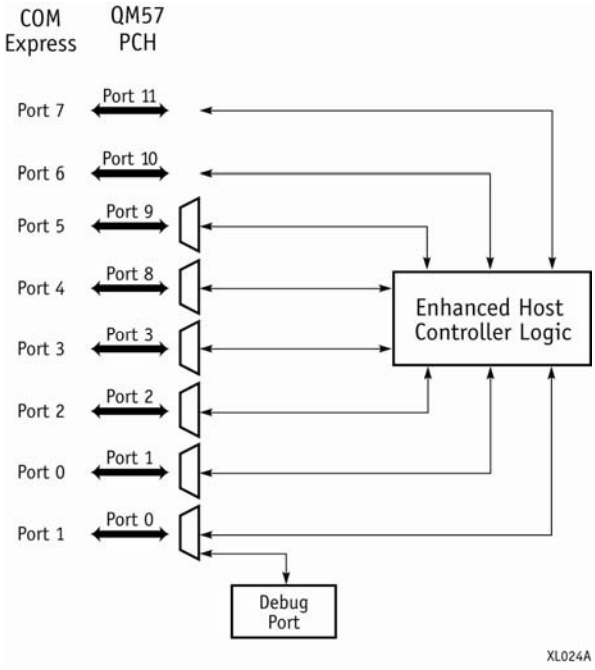
The USB interface supports up to eight USB 2.0 ports. Table 13 shows the USB configuration for the ETXexpress®-AI module.

### Table 13 USB Configuration

| COMexpress™ Port | QM57 PCH Port | Description |
|---|---|---|
| USB0 | USB0 | USB 2.0 compliant ports |
| USB1 | USB1 | |
| USB2 | USB4 | |
| USB3 | USB5 | |
| USB4 | USB6 | |
| USB5 | USB7 | |
| USB6 | USB3 | |
| USB7 | USB2 | |

Figure 5 shows the internal USB mapping from theMobile Intel® QM57 Platform Controller Hub (PCH).

### Figure 5: USB Mapping




NOTE: Additional USB connections can be added using external USB hubs.

## Configuration

There are two 480 mb/s USB EHCI controllers. The USB controllers are PCI bus devices. The BIOS allocates the required system resources during configuration of the PCI bus.

### 4.4.3SATA Interface

#### Configuration

The SATA controller is a PCIe bus device. The BIOS allocates the required system resources during the PCIe device configuration.

### 4.4.4Audio Interface

The Intel® QM57 PCH supports Intel® High Definition Audio (HDA). This HD audio configuration supports up to four audio streams (with up to 16 channels each), 32-bit sample depth, and sample rates up to 192 KHz.

With this configuration you can implement hardware CODECs on your baseboard for 7.1/5.1 audio systems and SDIF output. The pins for the HD audio are defined in Section 4.3.2.

#### Configuration

The audio controller is a PCI bus device. The BIOS allocates the required system resources during configuration of the PCI device.

### 4.4.5Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

#### Configuration

The serial IRQ machine is in "Continuous Mode".

### 4.4.6Graphics Interface

The ETXexpress-AI uses the GMA4500 graphics controller.

The key features of the GMA 4500 are :

» Intel® Dynamic Video Memory Technology support

» Intel® Smart 2D Display Technology (Intel® S2DDT)

» Intel® Clear Video Technology

- MPEG2 Hardware Acceleration
- WMV9/VC1 Hardware Acceleration
- AVC Hardware Acceleration
- ProcAmp

- Advanced Pixel Adaptive De-interlacing
- Sharpness Enhancement
- De-noise Filter
- High Quality Scaling
- Film Mode Detection (3:2 pull-down) and Correction
- Intel® TV Wizard

» 12 EUs

» Dedicated analog and digital display ports are supported through the PCH

### VGA

The analog VGA graphics core, with a maximum resolution of 1400x1050, is integrated in the processor.

## LVDS Flat Panel Interface (JILI)

The ETXexpress®-AI supports dual-channel LVDS via the COM Express™ connector. The implementation of this subsystem complies with the COM Express™ specification. For additional implementation information, refer to the ***PICMG COM Express™ Design Guide*** on the PIGMG website.

### 4.4.7Ethernet Interface

The Ethernet interface on the ETXexpress®-AI COM is the Intel® 82577LM PHY, which contains an integrated 10/100/1000 Gigabit Ethernet MAC. This interface is connected to Intel PCH PCIe Port 8. The controller supports a 10/100/1000 Base-T interface and it auto-negotiates the use of 10 Mbit/sec, 100 Mbit/sec or 1Gbit/sec connections.

The network interface operates at its lowest power (<1W) when GbE is fully active. The interface supports functions such as WOL (WakeOnLAN) and PXE (Preboot eXecution Environment) boot.

For cable lengths and terminations on your baseboard, refer to the PICMG ***COM Express™ Design G***uide on the PICMG website.

## Configuration

The Ethernet controller is a PCI Express bus device. The BIOS allocates the required system resources during the configuration of the PCIe device.

### 4.4.8SPI Bus Interface

The Serial Peripheral Interface (SPI) signals are connected to the QM57 platform controller hub using pins that were previously reserved on the COM Express™ connector. The SPI interface can be used to connect two carrier board devices, including external BIOS flash memory. The implementation of this subsystem complies with the COM Express™ specification. For additional implementation information, refer to the ***PICMG COM Express™ Design Guide*** on the PICMG website

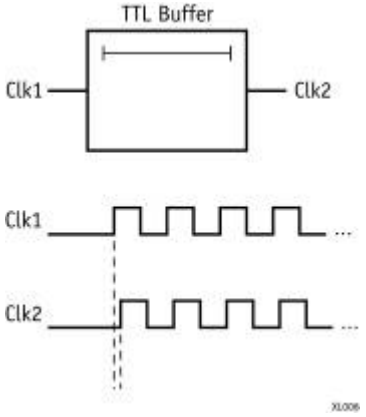
### 4.4.9LPC Bus Interface

The Low Pin Count (LPC) interface signals go to the COM Express™ X1A connector from the QM57 PCH. The LPC low-speed interface can be used for peripheral circuits. For example, it can be used as an external super I/O controller to combine legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express™ specification. For additional implementation information, refer to the ***PICMG COM Express™ Design Guide*** on the PICMG website.

The LPC bus does not support DMA (Direct Memory Access) and therefore imposes limitations for ISA bus and standard I/Os (SIOs) like floppy or LPT interface implementations.

**WARNING:** When more than one device is connected to the LPC bus, a clock buffer is required. Because of the power management of the LPC bus, you must use great care with clock buffers that require synchronization as they could prevent the board from booting up.

**Figure 6: Standard Clock Buffer**

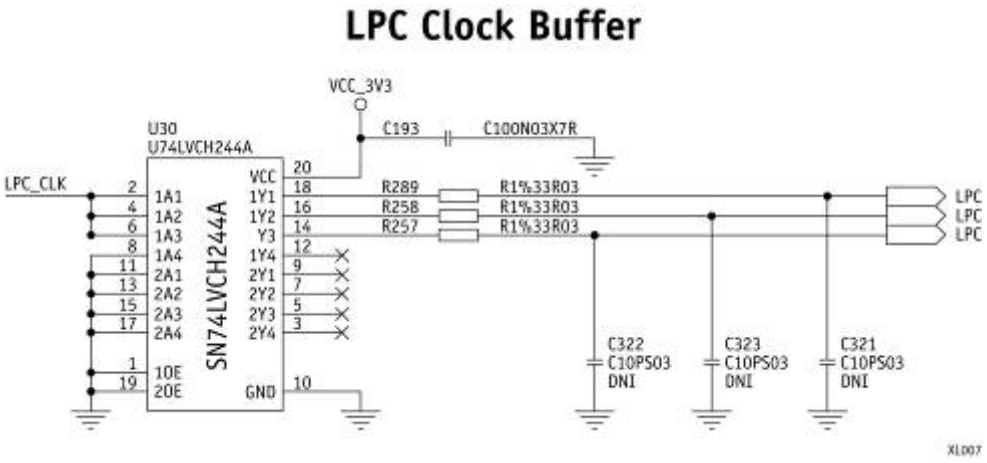


NOTE: When using a standard clock buffer on the baseboard, be aware that the generated delay must be considered for the length matching of the layout.

## Clock Buffer Reference Schematic

The schematic in Figure 7 shows an implementation example for the clock buffer.

### Figure 7: LPC Clock Buffer




### Table 14: LPC Addresses

| Address (HEX) | Device |
|---|---|
| 0000 - 00FF | IBM PC-compatible devices (IRQ-controller, keyboard, RTC etc.) |
| 002E-002F | Optional: Super I/O W83627 |
| 004e - 004f | TPM |
| 01F0 - 01F7 | Fixed disk |
| 03C0 - 03CF | VGA/EGA compatible registers |
| 03F6 | Fixed disk |
| 0400 - 043F | SMBus |
| 0480 - 04BF | GPIO SCH |
| 04D0 - 04D1 | IRQ configuration |
| 08F0 - 08FF | Optional |
| 0900 - 091F | Power Management |
| 0A80 - 0A83 | Reserved |
| 0CF8 - 0CFF | PCI configuration |
| D880 - D887 | PCI LAN Controller * |
| E080 - E09F | PCI USB Controller * |
| E480 - E49F | PCI USB Controller * |

| Address (HEX) | Device |
|---|---|
| E880 - E887 | PCI VGA Controller * |
| EF00 - EF1F | PCI USB Controller* |
| FFA0 - FFAF | PCI IDE Controller * |

* = Not fixed, configured by the BIOS automatically and may be different in other system configurations.

## Table 15: Device Addresses

| Address (HEX) | Device |
|---|---|
| 00000000 - 0009FFFF | DOS- (Real mode-) memory |
| 000A0000 - 000BFFFF | Display memory |
| 000C0000 - 000CBFFF | VGA BIOS |
| 000CC000 - 000DFFFF | Other Option ROM |
| 000E0000 - 000EFFFF | System BIOS extended space |
| 000F0000 - 000FFFFF | System BIOS base segment |
| 00100000 - 7FFFFFFF | System Memory |
| 80000000 - FFF00000 | PCI Memory, other extensions |
| CFDDC000 - CFFFFFFF | PCI LAN Controller |
| D0000000 - DFFFFFFF | PCI VGA Controller / Audio Controller / USB Controller |
| FEC00000 - FEC00040 | APIC Configuration |
| FED00000 - FED003FF | Event Timer |
| FED10000 - dynamic | Audio Controller |
| FED40000 - FED4BFFF | LPC Configuration |
| F0000000 - F0003FFF | RCRB (Root Complex) |
| FFC00000 - FFF00000 | Reserved |
| FFF00000 - FFFFFFFF | Firmware Hub |
| FFF80000 - FFFFFFFF | Mapping space for BIOS ROM |

For further details, please refer to the Intel® QM57 Platform Controller Hub External Design Specification (EDS) on the Intel website at http://www.intel.com.

### 4.4.10 Power Control Interface

#### Power Good (PWR_OK)

The ETXexpress®-AI COM provides an external input for a power-good signal (pin B24). The implementation of this subsystem complies with the COM Express™ Specification. PWR_OK is internally pulled up to 3.3V and must be high-level to power on the module.

#### Power Button (PWRBTN#)

The power button (pin B12) is available through the module connector as defined in the pin-out list. To start the module using the power button, the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4sec) at low-level power.

You can put the module into power-off mode by pressing the power button for at least four seconds.

#### Reset Button (SYS_RESET#)

The reset button (pin B49) is available through the module connector as defined in the pin-out list. The module stays in reset as long as SYS_RESET# is grounded.

#### Power Supply

The ETXexpress®-AI COM has a wide range of power inputs, from 8V to 18V DC. The supply voltage is applied through 42 pins (VCC) on the module connector. In ATX mode with 5V standby voltage, the VCC input must be higher than the standby voltage.

In general, single supply mode means the module starts as soon as power is applied to the module and ATX mode is for power button-controlled operation.

##### ATX Mode / Single Supply Mode

**ATX Mode:**

When an ATX power supply is connected, PWR_OK is set to low-level and VCC is off. Pressing the power button enables the ATX PSU setting PWR_OK to high-level and powers on VCC. The ATX PSU is controlled by the PS_ON# signal, which is generated by SUS_S3# via inversion.

**Table 16: ATX Mode**

| State | PWRBTN# | PWR_OK | V5_StdBy | PS_ON# | VCC |
|---|---|---|---|---|---|
| G3 | x | x | 0V | x | 0V |
| S5 | high | low | 5V | high | 0V |
| S5 -> S0 | PWRBTN Event | low -> high | 5V | high -> low | 0 V-> VCC |
| S0 | high | high | 5V | low | VCC |

**Single Supply Mode:**

In single supply mode the module starts automatically when VCC power is connected and Power Good input is open or at high-level (internal PU to 3.3V). PS_ON# is not used in single supply mode.

To power on the module from the S5 state, press the power button or reconnect VCC.

**Table 17: Single Supply Mode**

| State | PWRBTN | PWR_OK | V5_StdBy | VCC |
|---|---|---|---|---|
| G3 | x | x | x | 0 |
| G3 -> S0 | high | open / high | x | connecting VCC |
| S5 | high | open / high | x | VCC |
| S5 -> S0 | PWRBTN Event | open / high | x | reconnecting VCC |

NOTES: 1) Columns marked "x" are not relevant for the specified power state.
2) All ground pins have to be tied to the ground plane of the carrier board.

### 4.4.11 Miscellaneous Circuits

#### Speaker

The implementation of this subsystem complies with the COM Express™ Specification. For additional implementation information, refer to the PICMG COM Express™ Design Guide.

#### Battery

The implementation of this subsystem complies with the COM Express™ specification. For additional implementation information, refer to the ***PICMG COM Express™ Design Guide*** on the PICMG website.

In compliance with the EN60950 standard, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

## I²C Bus

The CPLD implementation connects LPC to the I²C controller to allow higher speed I²C transactions than in previous I/O implementations.

For additional information, refer to the ***PICMG COM Express™ Design Guide*** on the PICMG website and I²C application notes and JIDA specifications, which are available on the Kontron website at http://emdcustomersection.kontron.com/.

See the Chapter 8, "BIOS Operation" for supported I²C features.

## SMBus

System Management Bus (SMBbus) signals are connected to the SMBus controller, which is located on the QM57 platform controller hub. The SMBus is a two-wire bi-directional bus (clock and serial data) used for system management tasks such as reading parameters from a memory card or reading temperatures and voltages of system components.

The SMBus uses the same signaling scheme as the I²C bus.

## PCI Bus

The Intel® QM57 PCH provides a standard PCI 2.3 32-bit/33 MHz interface on the COM Express™ connector Type 2 implementation. The COM Express Type 6 connector does not support a PCI interface.

## IDE Port

PATA (IDE) is supported on the Type 2 COM Express™ connector via a SATA-to-PATA bridge. The Type 6 connector does not support IDE (PATA).

# 5 Special Features

## 5.1 Hyper-Threading

Hyper-Threading (officially termed Hyper-Threading Technology or HTT) is an Intel-proprietary technology used to improve parallelization of computations performed on PCs. Hyper-threading works by duplicating certain sections of the processor—those that store the architectural state -- but not duplicating the main execution resources. A hyper-threading equipped processor can appear to be two "logical" processors to the host operating system, thus allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always depends on the operating system.

## 5.2 Enhanced Speedstep Technology

The Intel® Core™ i7 and Core™ i5 processors support the Intel® Enhanced SpeedStep™ technology, which automatically switches the processor between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. Speedstep technology lets you optimize the system performance to match application requirements. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage to conserving battery life while maintaining a high level of performance. The frequency is set back to high automatically, allowing you to customize performance.

NOTE: To use Enhanced SpeedStep™ technology, you need an operating system that supports it.

Disabling Speedstep in the BIOS enables manual control of CPU performance. You can set the CPU performance state in the BIOS setup or use third-party software to control CPU performance states.

## 5.3 Watchdog

This feature is implemented within an $I^2C$ Watchdog and offers a single-stage watchdog. You can configure the Watchdog Timer (WDTimer) using the Kontron EAPI, or through the BIOS setup, or directly through register settings. The application software should strobe the WDTrigger to prevent a timeout. The WDTrigger resets and restarts the system after a timeout to provide a way to recover from program crashes or lockups.

The Watchdog can be enabled through:

» BIOS Setup

» K-Station

» Direct programming over register settings

The Watchdog can be triggered through

» K-Station

» Direct programming (i.e., writing data into one register of the CPLD)

For information about programming this feature, see the K-Station driver packet in the Kontron Customer section or contact your local sales support representative to get an application note about low level programming.

## 5.4 General Purpose Input and Output (GPIO)

The ETXexpress®-AI COM provides eight GPIOs that can be accessed through the module COM Express™ connector described in the pin-out lists, in Chapter 4, "COM Connectors".

NOTE: GPIO cannot drive applications faster than 2 msec. Data transfer rates up to 1 kHz maximum are recommended.

**Table 18: GPIO COM Express Pin-Outs**

| Bit of GPIO Port0 | Function | COM Express Pin |
|---|---|---|
| 0 | GPI0 | A54 |
| 1 | GPI1 | A63 |
| 2 | GPI2 | A67 |
| 3 | GPI3 | A85 |
| 4 | GPO0 | A93 |
| 5 | GPO1 | B54 |
| 6 | GPO2 | B57 |
| 7 | GPO3 | B63 |

## 5.5 Fast $I^2C$

The ETXexpress®-AI COM integrates two configurable $I^2C$ buses. The external $I^2C$ clock and data signals are provided via the CPLD on COM Express™ connector pins B33/B34 and the (LVDS) $I^2C$ clock and data signals from the Intel QM57 PCH are assigned to COM Express™ connector pins A83/A84. The $I^2C$ interface offers full multimaster and clock stretching support.

## 5.6 ACPI Suspend Modes and Resume Events

The ETXexpress®-AI COM only supports the S3 state (=Save to RAM). S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but S4_OS is supported by the following operating systems:

» Windows XP

» Windows Vista

» Windows 7

## Events that Resume the System from S3

» USB keyboard (1)

» USB mouse (1)

» Power button

» WakeOnLan (2)

## Events that Resume the System from S4/S5

» Power button

» WakeOnLan

NOTES: 1) The OS must support wake-up via USB devices and the baseboard must power the USB port with StandBy-Voltage
2) WakeOnLan must be enabled in the driver options

# 6 Design Consideration

## 6.1 Thermal Management

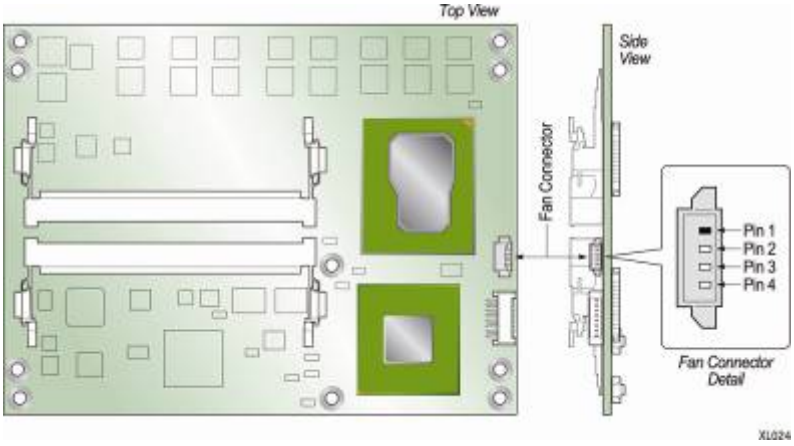
A heatsink assembly (38010-0000-99-0C02) is available from Kontron Embedded Modules for the ETXexpress®-AI COM. The heatsink fits on top of this assembly and serves as an active cooling solution.

The optimum cooling solution varies, depending on the COM Express™ application and environmental conditions and the module is fully functional at the full 0°C to +60°C temperature. Drawings for the active heatsink are available on request. Also, see the *PICMG COM Express™ Design Guide* on the PICMG website for further information about thermal management.

## 6.2 Onboard Fan Connector

This section describes how to connect an optional fan to the connector located directly on the ETXexpress®-AI COM.

**Figure 8: Fan Connector Location and Pin-Out**

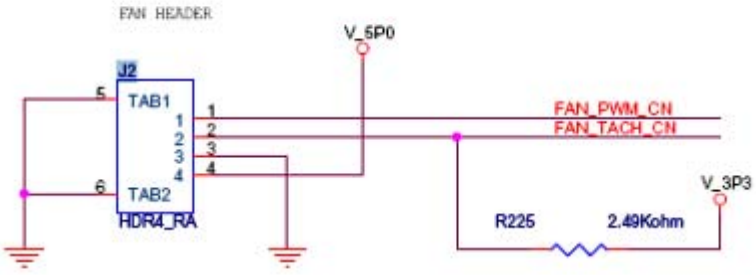



The onboard fan connector (J2) is on the right top side of the PCB. The connection details are covered in the Figure 9 schematic.

**Table 19. Fan Connector (J2) Pin-Out**

| Pin | Description |
|---|---|
| 1 | FAN PWM CN |
| 2 | FAN TACH CN |
| 3 | GND |
| 4 | V 5P0 |

## Figure 9: Fan Connector Schematic




Connector J2 specifications and Kontron part numbers for the components are:

» Part number: (Molex) J2: 53261-0471 (Kontron PN: 301-149)

» Mates with: Molex 51021-0400

» Crimp terminals: Molex 50058-8100 28-32AWG (bag) or Molex 50058-8000 28-32AWG (reel)

# 7 System Resources

## 7.1 Interrupt Request (IRQ) Lines

### Table 20: 8259 PIC Mode

| IRQ # | Used For | Available | Comment |
|---|---|---|---|
| 0 | Timer0 | No | |
| 1 | Keyboard | No | |
| 2 | Cascade | No | |
| 3 | External SIO - COM2 | Yes (No) | Note (1) |
| 4 | External SIO - COM1 | Yes (No) | Note (1) |
| 5 | PCI | For PCI | Dynamic (BIOS default) |
| 6 | External SIO | Yes (No) | Note (1) |
| 7 | External SIO - LPT1 | Yes (No) | Note (1) |
| 8 | RTC | No | |
| 9 | ACPI | No | Note (2) |
| 10 | PCI | For PCI | Dynamic (BIOS default) |
| 11 | PCI | For PCI | Dynamic (BIOS default) |
| 12 | PS/2 Mouse | Yes (No) | Note (1) |
| 13 | FPU | No | |
| 14 | Primary IDE | No | Note (1) |
| 15 | PCI | For PCI | Dynamic (BIOS default) |

NOTES: 1) If the "Used For" device is disabled in setup, the interrupt is available for other devices.
2) Not available if ACPI is used

### Table 21: APIC Mode

| IRQ # | Used For | Available | Comment |
|---|---|---|---|
| 0 | Timer0 | No | |
| 1 | Keyboard | No | |
| 2 | Cascade | No | |
| 3 | External SIO - COM2 | Yes (No) | Note (1) |
| 4 | External SIO - COM1 | Yes (No) | Note (1) |
| 5 | PCI | for PCI | Dynamic (BIOS default) |
| 6 | External SIO | Yes (No) | Note (1) |
| 7 | External SIO - LPT1 | Yes (No) | Note (1) |
| 8 | RTC | No | Option for HPET#1 (Legacy Mode) |
| 9 | ACPI | No | Option for SCI, TCO; Note (2) |
| 10 | PCI | for PCI | Dynamic assignment; Option for SCI, TCO or PIRQ# |
| 11 | PCI | for PCI | Dynamic assignment; Option for SCI, TCO or |

| IRQ # | Used For | Available | Comment |
|---|---|---|---|
| | | | PIRQ# or HPET#2 |
| 12 | PS/2 Mouse | Yes (No) | Option for SCI, TCO, or PIRQ#, or HPET#3; Note (1) |
| 13 | FPU | No | FERR# Logic |
| 14 | SATA | Yes (No) | SATA Primary (Legacy Mode); Note(1) |
| 15 | SATA | Yes (No) | SATA Secondary (Legacy Mode); Note(1) |
| 16 | PIRQ [A] | No | Dynamic assignment; PCI IRQ line 1; Note (3) |
| 17 | PIRQ [B] | No | Dynamic assignment; PCI IRQ line 2; Note (3) |
| 18 | PIRQ [C] | No | Dynamic assignment; PCI IRQ line 3; Note (3) |
| 19 | PIRQ [D] | No | Dynamic assignment; PCI IRQ line 4; Note (3) |
| 20 | PIRQ [E] | No | Dynamic assignment; Note (3) |
| 21 | PIRQ [F] | No | Dynamic assignment; Note (3) |
| 22 | PIRQ [G] | No | Dynamic assignment; Note (3) |
| 23 | PIRQ [H] | No | Dynamic assignment; Note (3) |

NOTES: 1) If the "Used For" device is disabled in setup, the interrupt is available for other devices.
2) Not available if ACPI is used
3) ACPI OS decides on the particular IRQ usage

## 7.2 Memory Area

The first 640 KBytes of DRAM are used as main memory. With DOS, you can address 1 MB of memory directly. Memory area above 1 MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

| Upper Memory | Used for | Available | Comment |
|---|---|---|---|
| A0000h – BFFFFh | VGA Memory | No | Mainly used by graphics controller |
| C0000h – CFFFFh | VGA BIOS | No | Used by onboard VGA ROM |
| D0000h – DFFFFh | | Yes | Free for shadow RAM in standard configurations |
| E0000h – FFFFFh | System BIOS | No | Fixed |

## 7.3 I/O Address Map

The I/O-port addresses of the ETXexpress®-AI COM are functionally identical to those of a standard PC/AT system, so any addresses not mentioned in Table 22 should also be available. All addresses are fixed I/O ranges that are decoded by the PCH used in this module.

**Table 22: I/O Address Assignments**

| I/O Address | Read Target | Write Target | Internal Unit |
|---|---|---|---|
| 00h-08h | DMA Controller | DMA Controller | DMA |
| 09h-oEh | Reserved | DMA Controller | DMA |
| 0Fh | DMA Controller | DMA Controller | DMA |
| 10h-18h | DMA Controller | DMA Controller | DMA |
| 19h-1Eh | Reserved | DMA Controller | DMA |
| 1Fh | DMA Controller | DMA Controller | DMA |
| 20h-21h | Interrupt Controller | Interrupt Controller | Interrupt |
| 24h-25h | Interrupt Controller | Interrupt Controller | Interrupt |
| 28h-29h | Interrupt Controller | Interrupt Controller | Interrupt |
| 2Ch-2Dh | Interrupt Controller | Interrupt Controller | Interrupt |
| 2E-2F | LPC SIO | LPC SIO | Forwarded to LPC |
| 30h-31h | Interrupt Controller | Interrupt Controller | Interrupt |
| 34h-35h | Interrupt Controller | Interrupt Controller | Interrupt |
| 38h-39h | Interrupt Controller | Interrupt Controller | Interrupt |
| 3Ch-3Dh | Interrupt Controller | Interrupt Controller | Interrupt |
| 40h-42h | Timer/Counter | Timer/Counter | PIT (8254) |
| 43h | Reserved | Timer/Counter | PIT |
| 4E-4F | LPC SIO | LPC SIO | Forwarded to LPC |
| 50h-52h | Timer/Counter | Timer/Counter | PIT |
| 53h | Reserved | Timer/Counter | PIT |
| 60h | Microcontroller | Microcontroller | Forwarded to LPC |
| 61h | NMI Controller | NMI Controller | Processor I/F |
| 62h | Microcontroller | Microcontroller | Forwarded to LPC |
| 64h | Microcontroller | Microcontroller | Forwarded to LPC |
| -66h | Microcontroller | Microcontroller | Forwarded to LPC |

| I/O Address | Read Target | Write Target | Internal Unit |
|---|---|---|---|
| 70h | Reserved | NMI and RTC Controller | RTC |
| -71h | RTC Controller | RTC Controller | RTC |
| 72h | RTC Controller | NMI and RTC Controller | RTC |
| 73h | RTC Controller | RTC Controller | RTC |
| 74h | RTC Controller | NMI and RTC Controller | RTC |
| 75h | RTC Controller | RTC Controller | RTC |
| 76h | RTC Controller | NMI and RTC Controller | RTC |
| -77h | RTC Controller | RTC Controller | RTC |
| 80h | DMA Controller, or LPC, or PCI | DMA Controller and LPC or PCI | DMA |
| 81h-83h | DMA Controller | DMA Controller | DMA |
| 84h-86h | DMA Controller | DMA Controller and LPC or PCI | DMA |
| 87h | DMA Controller | DMA Controller | DMA |
| 88h | DMA Controller | DMA Controller and LPC or PCI | CMA |
| 89h-8Bh | DMA Controller | DMA Controller | DMA |
| 8Ch-8Eh | DMA Controller | DMA controller and LPC or PCI | DMA |
| 08Fh | DMA Controller | DMA Controller | DMA |
| 90h-91h | DMA Controller | DMA Controller | DMA |
| 92h | Reset Generator | Reset Generator | Processor I/F |
| 93h-9Fh | DMA Controller | DMA Controller | DMA |
| A0h-A1h | Interrupt Controller | Interrupt Controller | Interrupt |
| A4h-A5h | Interrupt Controller | Interrupt Controller | Interrupt |
| A8h-A9h | Interrupt Controller | Interrupt Controller | Interrupt |
| Ach-ADh | Interrupt Controller | Interrupt Controller | Interrupt |
| B0h-B1h | Interrupt Controller | Interrupt Controller | Interrupt |
| B2h-B3h | Power Management | Power Management | Power Management |
| B4h-B5h | Interrupt Controller | Interrupt Controller | Interrupt |
| B8h-B9h | Interrupt Controller | Interrupt Controller | Interrupt |
| BCh-BDh | Interrupt Controller | Interrupt Controller | Interrupt |
| C0h-D1h | DMA Controller | DMA Controller | DMA |
| D2h-DDh | Reserved | DMA Controller | DMA |
| DEh-Dfh | DMA Controller | DMA Controller | DMA |

| I/O Address | Read Target | Write Target | Internal Unit |
|---|---|---|---|
| F0h | PCI and Master Abort[1] | FERR#/IGNNE#/Interrupt Controller | Processor I/F |
| 170h-177h | SATA Controller or PCI | SATA Controller or PCI | Forwarded to SATA |
| 1F0h-1F7h | SATA Controller or PCI | SATA Controller or PCI | Forwarded to SATA |
| 376h | SATA Controller or PCI | SATA Controller or PCI | Forwarded to SATA |
| 3F6h | SATA Controller or PCI | SATA Controller or PCI | Forwarded to SATA |
| 4D0h-4D1h | Interrupt Controller | Interrupt Controller | Interrupt |
| CF9h | Reset Generator | Reset Generator | Processor I/F |

[1]A Read to this address will subtractively go to PCI, where it will master abort.

## 7.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) and the PCI Express Base 1.0a specifications. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

### Table 23: PCI Device IRQs

| PCI Device | PCI IRQ | Interface | Comment |
|---|---|---|---|
| Host Bridge / Memory Controller | None | | Integrated in processor |
| Graphics / Video Controller | INTA | | Integrated in processor |
| USB Client Controller | INTA | | Integrated in chipset |
| HD Audio Controller | INTA | | Integrated in chipset |
| PCI Express Port | INTA | | Integrated in chipset |
| PCI Express Port | INTB | | Integrated in chipset |
| UHCI USB Controller 1 | INTE | | Integrated in chipset |
| UHCI USB Controller 2 | INTF | | Integrated in chipset |
| UHCI USB Controller 3 | INTG | | Integrated in chipset |
| EHCI USB Controller | INTH | | Integrated in chipset |
| ISA/PATA Bridge / LPC | None | | Integrated in |

| PCI Device | PCI IRQ | Interface | Comment |
|---|---|---|---|
| Controller | | | chipset (with Type 2 connector only) |
| IDE Controller | None | | Integrated in chipset (with Type 2 connector only) |
| Network Controller | INTC | PCI Express | External i82577 |
| SATA | INTA | PCI Express | External SIL3132 |

## Table 24: External I²C Bus #1

| I²C Address | Used For | Available | Comment | JIDA Bus Nr. |
|---|---|---|---|---|
| A0h | JIDA-EEPROM | No | EEPROM for CMOS Data | 0 |
| A2h | JIDA-EEPROM | No | EEPROM for CMOS Data | 0 |

## Table 25: LVDS I²C Bus

| I²C Address | Used For | Available | Comment | JIDA Bus Nr. |
|---|---|---|---|---|
| A0h | JILI-EEPROM | No | EEPROM for JILI Data | 4 |

# 8 BIOS Operation

## 8.1 Determining the BIOS Version

The ETXexpress®-AI COM has the next-generation AMI® Aptio BIOS installed on the onboard 8-Mbit firmware hub. The same BIOS is used for both Type 2 and Type 6 modules. To determine the BIOS version, press the Pause key on your keyboard immediately, as soon as you see text such as this example displayed in the upper left corner of your screen:

» Aptio BIOS © 2009 American Megatrends, Inc.

» BIOS Date: 06/14/2010 16:41:09 Ver: 2.00.1201

» Kontron® BIOS Version <CCA1RXXX>
© Copyright 2002-2010 Kontron

NOTE: The BIOS version can also be determined by checking the Main screen of the Aptio BIOS setup utility.

## 8.2 Setup Guide

The Aptio Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

NOTE: Selecting incorrect values may cause a system boot failure. Load setup default values to recover by pressing the <F3> key.

### 8.2.1 Invoking the AMI® Aptio BIOS Setup Utility

To invoke the Aptio BIOS setup utility, press <DEL> when the following string appears during boot-up:

**Press <DEL> to enter Setup**

The BIOS Setup Main screen then appears.

The setup screen has several sections:

| Setup Screen | Location | Function |
|---|---|---|
| Menu Bar | Top | Lists and selects all top level menus. |
| Legend Bar | Right side Bottom | Lists setup navigation keys. |
| Item Specific Help Window | Right side Top | Help for selected item. |
| Menu Window | Left Center | Selection fields for current menu. |

## Menu Bar

The menu bar at the top of the window lists different screens. Use the ← or → key to make a selection.

## Legend Bar

Use the keys listed on the bottom of the legend bar to make your selections or exit the current screen.

## Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Changes and Exit command in the Exit menu saves the values displayed in all the menus and exits BIOS Setup.

## Displaying Sub-Screens

Use the ↑ or ↓ key to move the cursor to the sub-screen you want and then press <Enter>. A pointer (▶) marks all sub-screens.

## Item-Specific Help Window

The Help window on the right side of each screen displays the Help text for the selected item. It updates as you move the cursor through each field.

## General Help Window

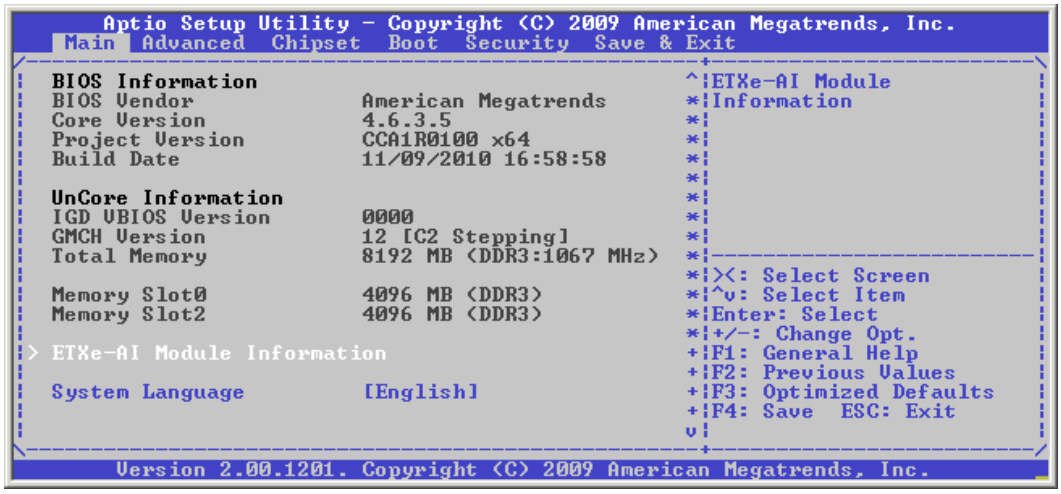
Pressing the <F1> key brings up the General Help window that describes the legend keys and their alternates. Press <Esc> or <Enter> to exit the General Help window.

## 8.3 BIOS Setup

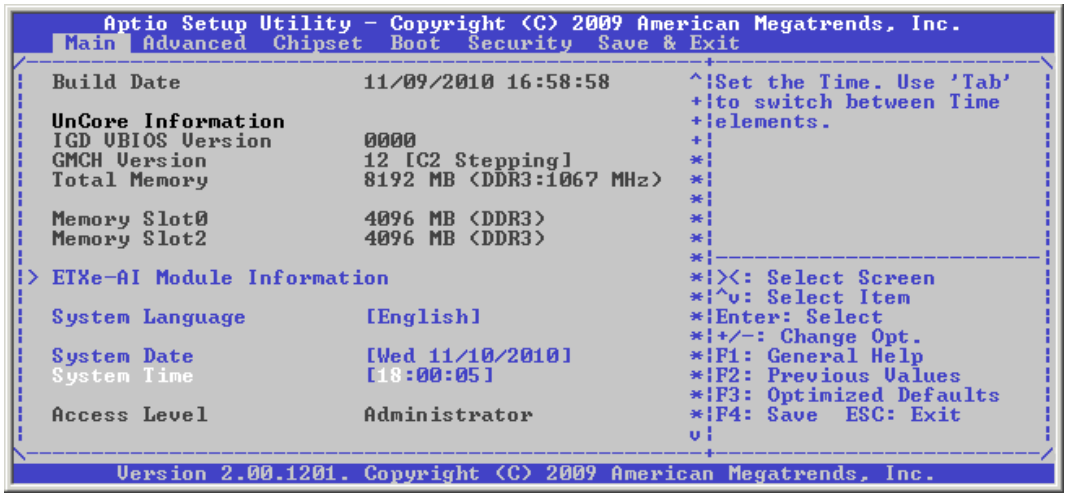
| NOTE: | Default Settings are in bold |
|---|---|

### 8.3.1Main Menu

#### Platform Information



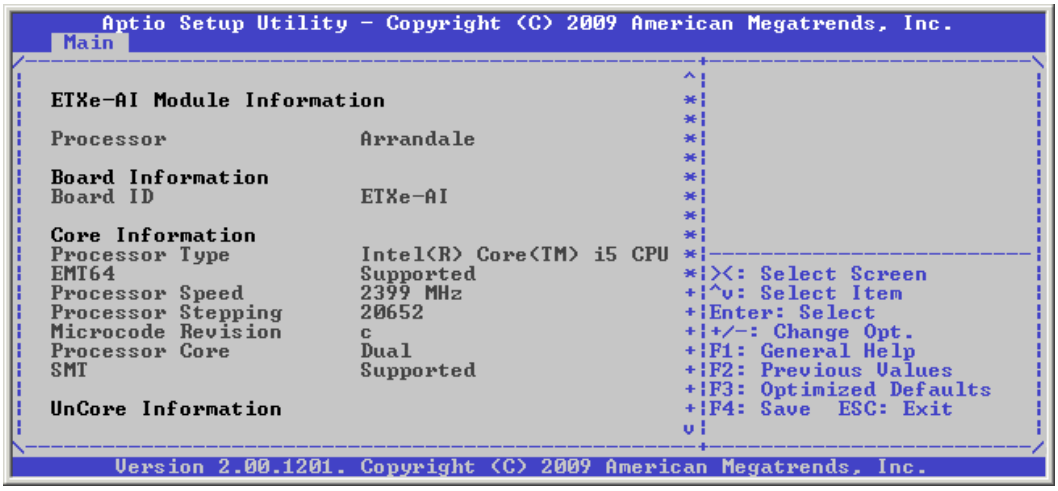

#### System Time Setting




| Features | Options | Description |
|---|---|---|
| System Language | **English** | Choose the system default language. |
| System Date | [mm/dd/yyyy] | <Tab>, <Shift-Tab>, or <Enter> selects field |

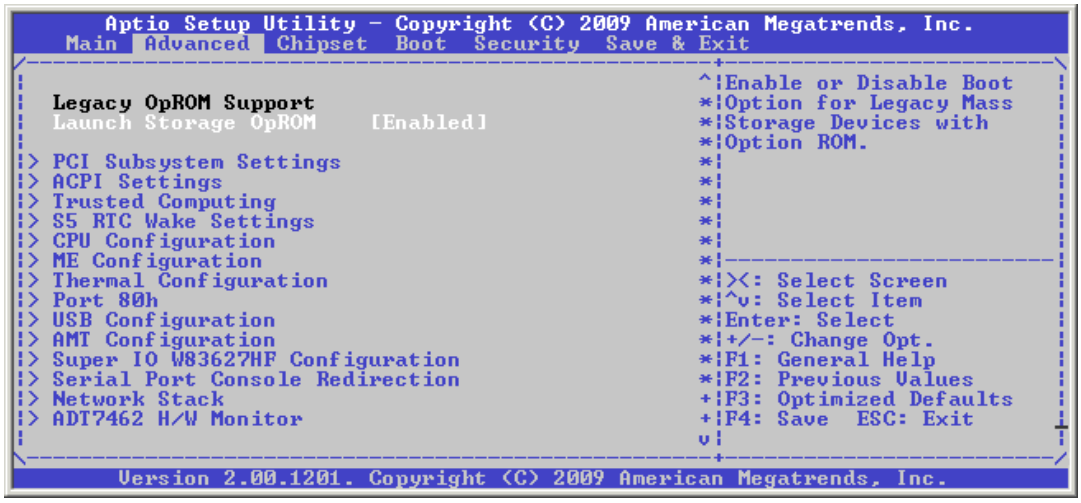
| | | |
|---|---|---|
| System Time | [hh:mm:ss] | <Tab>, <Shift-Tab>, or <Enter> selects field |

## System Information




### 8.3.2Advanced Menu

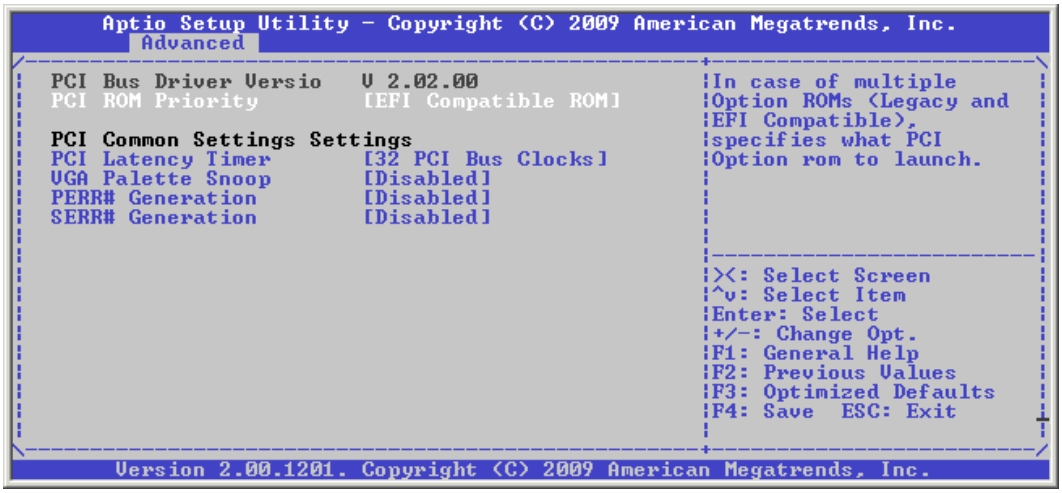
## Launch Storage opROM Option




| Features | Options | Description |
|---|---|---|
| Launch Storage | Disabled<br>**Enabled** | Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM |

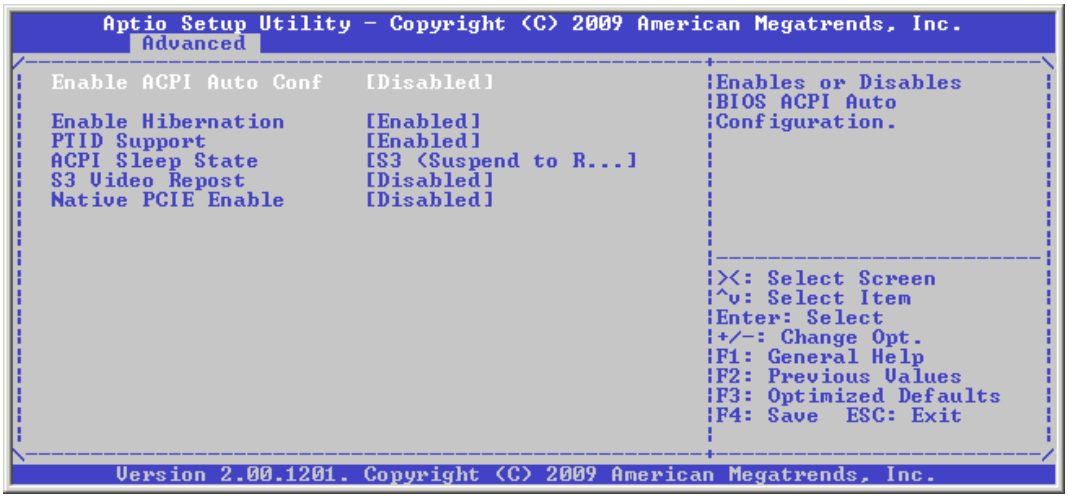
| | | |
|---|---|---|
| OpROM | | |

## PCI Subsystem Settings



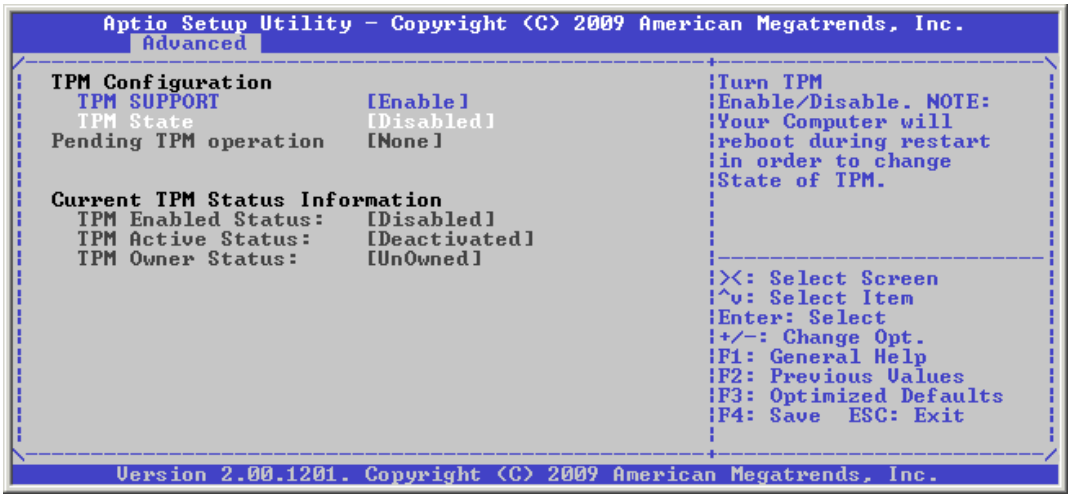

| Features | Options | Description |
|---|---|---|
| PCI ROM Priority | Legacy ROM<br>**EFI Compatible ROM** | In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch. |
| PCI Latency Timer | **32 PCI Bus Clocks**<br>64 PCI Bus Clocks<br>96 PCI Bus Clocks<br>128 PCI Bus Clocks<br>160 PCI Bus Clocks<br>192 PCI Bus Clocks<br>224 PCI Bus Clocks<br>248 PCI Bus Clocks | Value to be programmed into PCI Latency Timer Register. |
| VGA Palette Snoop | **Disabled**<br>Enabled | Enables or Disables VGA Palette Registers Snooping. |
| PERR# Generation | **Disabled**<br>Enabled | Enables or Disables PCI Device to Generate PERR# |
| SERR# Generation | **Disabled**<br>Enabled | Enables or Disables PCI Device to Generate SERR# |

## ACPI Settings



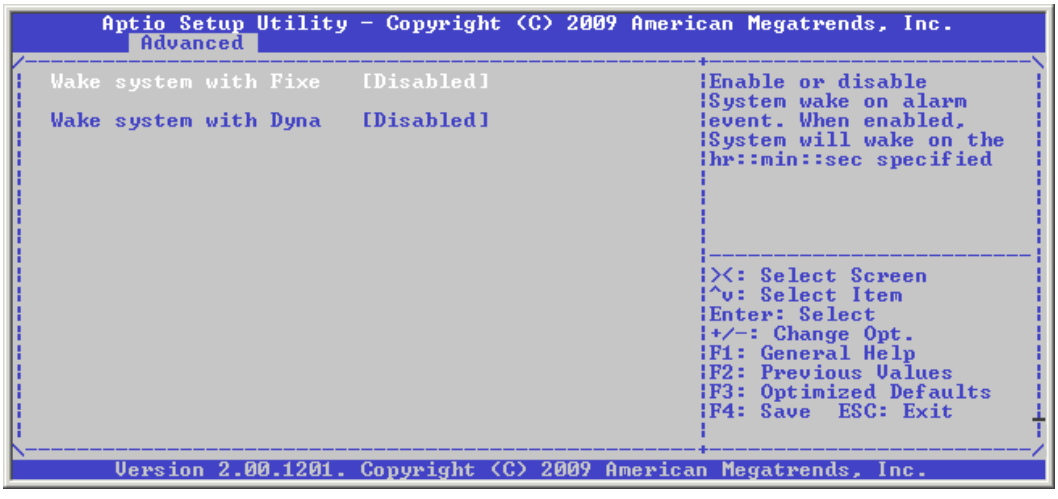

| Features | Options | Description |
|---|---|---|
| Enable ACPI Auto Conf | **Disabled**<br>Enabled | Enables or Disables BIOS ACPI Auto Configuration. |
| Enable Hibernation | Disabled<br>**Enabled** | Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some OSs. |
| PTID Support | Disabled<br>**Enabled** | PTID Support will be loaded if enabled. |
| ACPI Sleep State | Suspend Disable<br>**S3 (Suspend to RAM)** | Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed. |
| S3 Video Repost | **Disabled**<br>Enabled | On enabling, Video Option ROM will be dispatched during S3 resume. |
| Native PCIE Enable | **Disabled**<br>Enabled | PCI Express Native Support Enable/Disable. This feature is only available in Vista. |

## Trusted Computing




| Features | Options | Description |
|---|---|---|
| TPM Support | **Disabled**<br>Enabled | Enable/disable TPM support<br>OS will not show TPM, reset of platform is required. |
| TPM State | **Disabled**<br>Enabled | Enable/disable TPM.<br>NOTE: Your computer will reboot during restart in order to change the TPM state |

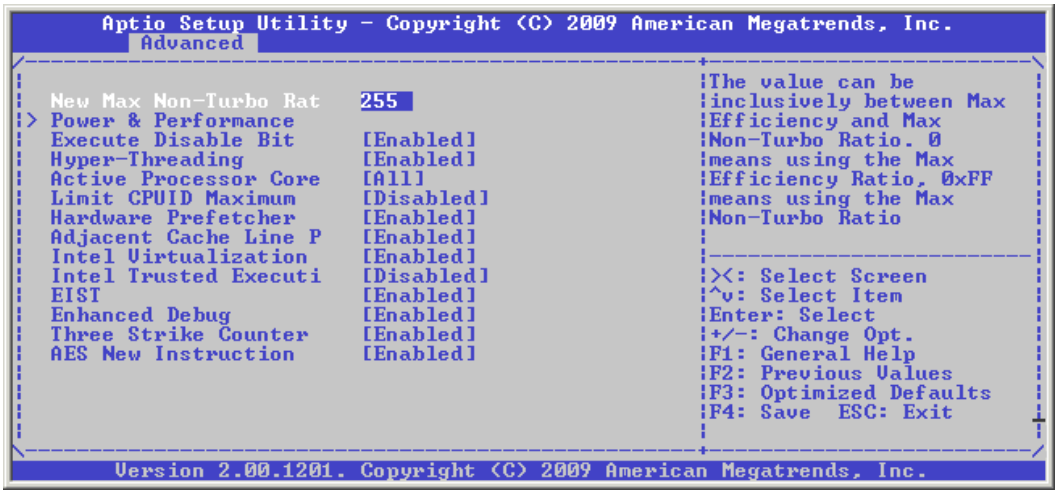
## S5 RTC Alarm Wake Settings




| Features | Options | Description |
|---|---|---|
| Wake system with Fixed Time | **Disabled**<br>Enabled | Enable /disable system wake-on-alarm event. When enabled, system will wake on the hr:min:sec specified. |

| Features | Options | Description |
|---|---|---|
| Wake system with Dynamic Time | **Disabled**<br>Enabled | Enable/disable system wake on alarm event. When enabled, system will wake on the current time + increase minute(s) |

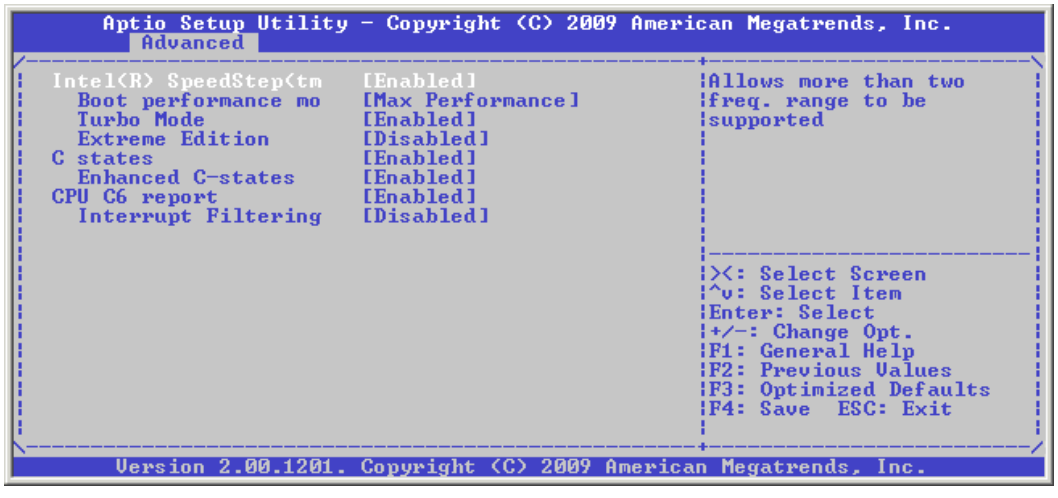
## CPU Configuration




| Features | Options | Description |
|---|---|---|
| New Max Non-Turbo Ratio | 0<br>1<br>2<br>…<br>…<br>…<br>**255** | The value can be inclusively between Max Efficiency and Max Non-Turbo Ration.<br>O = using the Max Efficiency Ratio<br>0xFF = using the Max Non-TurboRatio |
| Power & Performance | **Submenu** | |
| Execute Disable Bit | Disabled<br>**Enabled** | XD can prevent certain classes of malicious buffer overflow attacks when combined with supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Red Hat Enterprise 3 Update 3.) |
| Hyper-threading | Disabled<br>**Enabled** | Enable for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disable for other OS (OS not optimized for Hyper-Threading Technology |
| Active Processor Core | **All**<br>1<br>2 | Number of cores to enable in each processor package. |
| Limit CPUID Maximum | **Disabled**<br>Enabled | Disable for Windows XP |
| Hardware | Disabled | To turn on/off the MLC streamer prefetcher. |

| Features | Options | Description |
|---|---|---|
| Prefetcher | **Enabled** | |
| Adjacent Cache Line Prefetcher | Disabled<br>**Enabled** | To turn on/off prefetching of adjacent cache lines. |
| Intel® Virtualization Technology | Disabled<br>**Enabled** | When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. |
| Intel® Trusted Execution Technology | **Disabled**<br>Enabled | Enable utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology.<br>Changes require a full power cycle to take effect |
| EIST | Disabled<br>**Enabled** | Enable/disable Intel SpeedStep |
| Enhanced Debug | Disabled<br>**Enabled** | Disable for normal system operation<br>Enable for test environments |
| Three Strike Counter | Disabled<br>**Enabled** | Enable/disable Three Strike counter. |
| AES New Instruction | Disabled<br>**Enabled** | Enable/disable AES New Instruction |

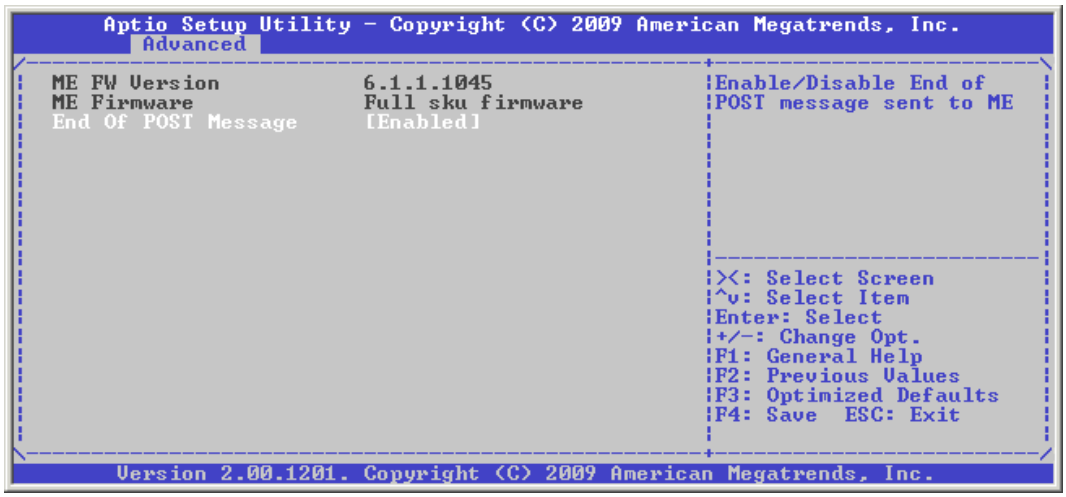
## Power and Performance Settings




| Features | Options | Description |
|---|---|---|
| Intel® SpeedStep™ | Disabled<br>**Enabled** | Enable = allows more than two frequency ranges to be supported |
| Boot performance mode | **Max Performance**<br>Max Battery | Select the performance state that the BIOS will set before OS hand-off |
| Turbo Mode | Disabled<br>**Enabled** | Enable/disable processor Turbo Mode (requires EMTTM enable, too). |

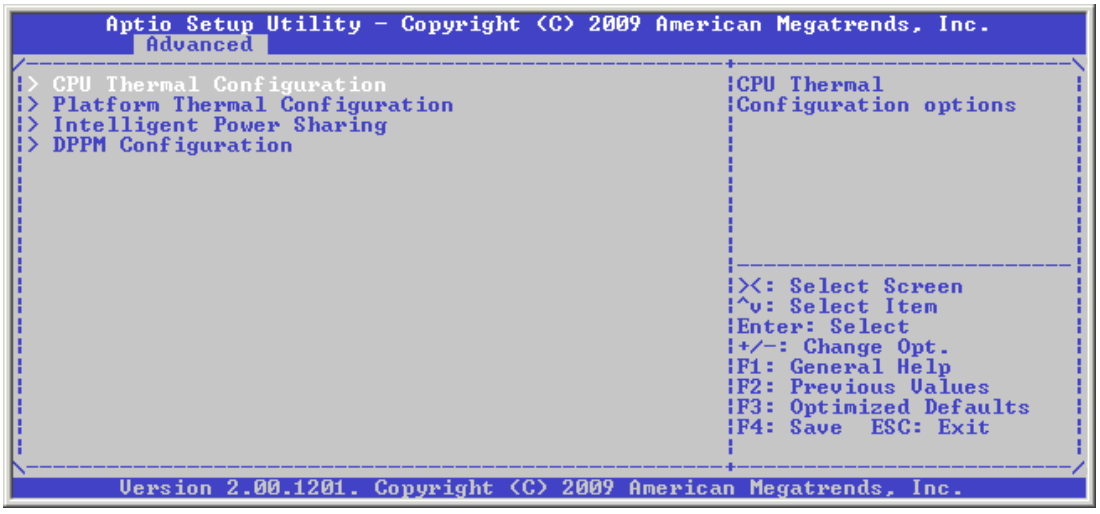
| Features | Options | Description |
|---|---|---|
| Extreme Edition | **Disabled**<br>Enabled | Enable/disable Extreme Edition support |
| C States | Disabled<br>**Enabled** | Enable/disable CPU Power management<br>Enable = allows CPU to go to C state when it not 100% utilized |
| Enhanced C-States | Disabled<br>**Enabled** | Enable/disable C1E<br>Enable = CPU will switch to the minimum speed when all cores enter C-State |
| CPU C6 report | Disabled<br>**Enabled** | Enable/disable CPU C6(APCI C3) report to OS |
| Interrupt Filtering | **Disabled**<br>Enabled | Enable = only the core that is the destination of the interrupt while in the C3/C6 will not be notified of the transition to the C0.<br>Disable = all cores that are in C3/C6 will be notified of the transition |

## Management Engine (ME) Technology Settings

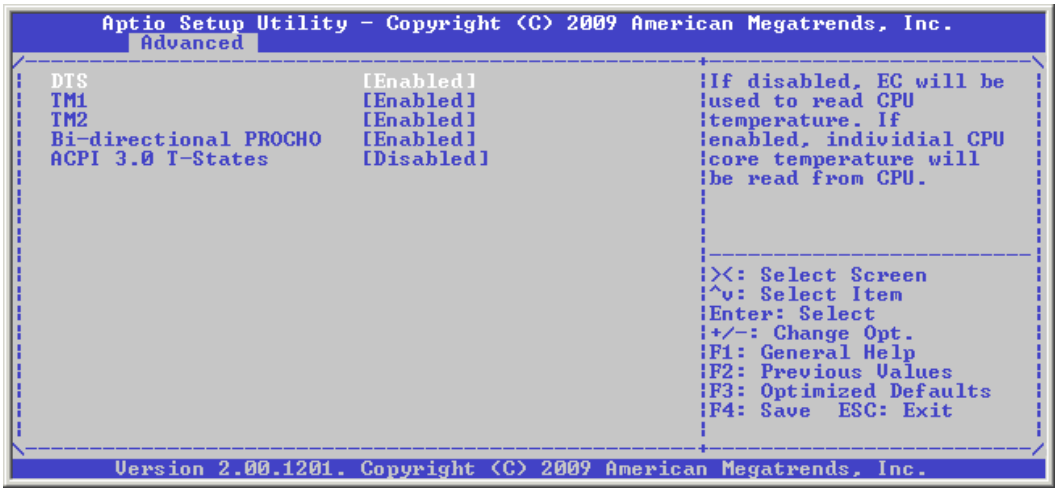



| Features | Options | Description |
|---|---|---|
| End of POST Message | Disabled<br>**Enabled** | Enable/disable End of POST message sent to ME. |

## Thermal Configuration Settings



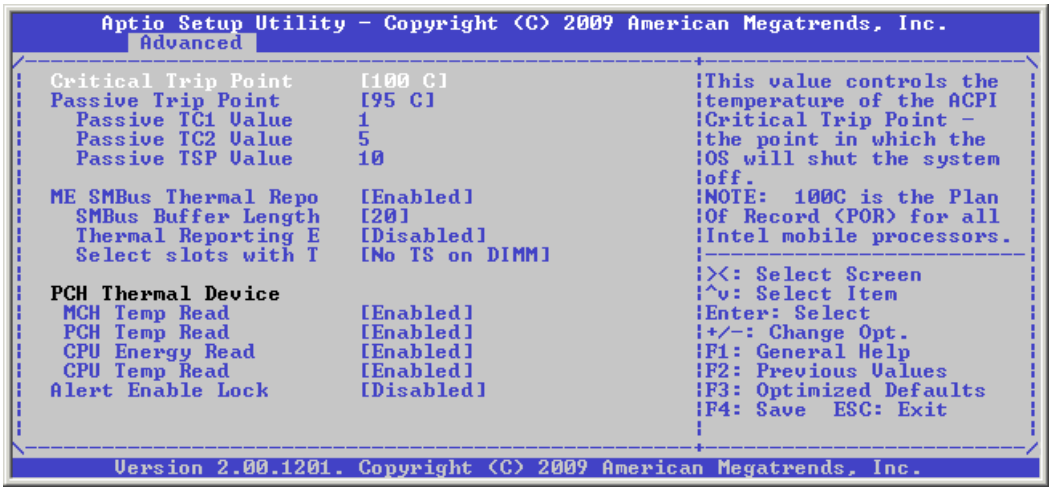

## Thermal Configuration Settings: CPU Thermal Configuration




| Features | Options | Description |
|---|---|---|
| DTS | Disabled<br>**Enabled**<br>Critical Temp Reporting (Out of spec) | Disable = EC will be used to read CPU temperature<br>Enable = individual CPU core temperature will be read from CPU. |
| TM1 | Disabled<br>**Enabled** | Enable/disable thermal monitor1 |
| TM2 | Disabled<br>**Enabled** | Enable/disable thermal monitor2 |

| | | |
|---|---|---|
| Bi-directional PROCHOT# | Disabled<br>**Enabled** | When the processor thermal sensor trips (either core), the PROCHOT# will be driven If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor. |
| APCI 3.0 T-States | **Disabled**<br>Enabled | Enable/disable ACPI 3.0 T-states |

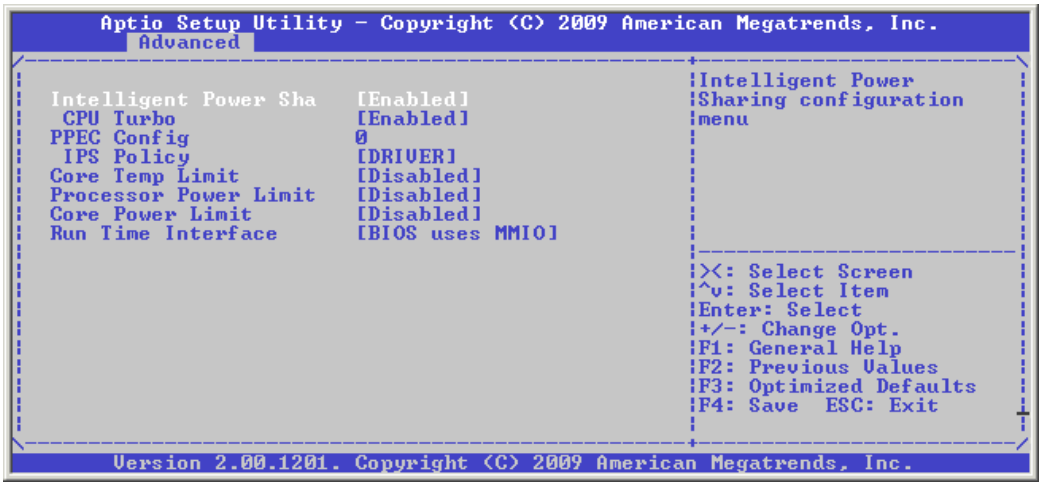
## Thermal Configuration Settings: Platform Thermal Configuration




| Features | Options | Description |
|---|---|---|
| Critical Trip Point | **100 C**<br>55 C<br>60 C<br>…<br>…<br>…<br>119C | This value controls the temperature of the ACPI Critial Trip Point – the point at which the OS will shut the system off. **NOTE** 100C is the Plan Of Record (POR) for all Intel mobile processors. |
| Passive Trip Point | 55 C<br>60 C<br>65 C<br>…<br>**95 C**<br>…<br>119 C | This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the processor. |
| Passive TC1 Value | 1 | This value sets the TC1 value for the ACPI Passive Cooling Formula. Range 1 - 16 |
| Passive TC2 Value | 5 | This value sets the TC2 value for the ACPI Passive Cooling Formula. Range 1 - 16 |

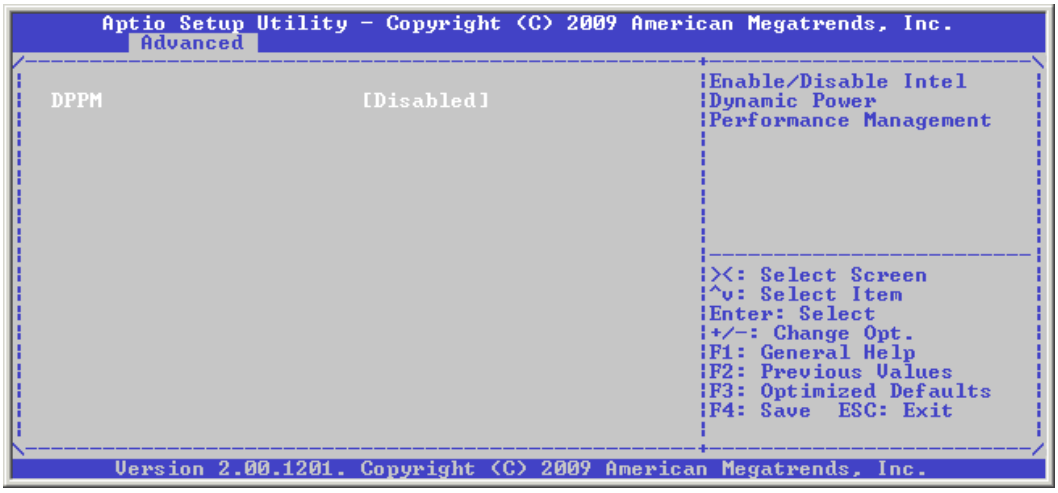
| | | |
|---|---|---|
| Passive TSP Value | 10 | This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when passive cooling is enabled. Range 2 – 32 |
| ME SMBus Thermal Repo | Disabled<br>**Enabled** | Enable/disable ME SMBus Thermal Reporting Configuration |
| SMBus Buffer Length | 1<br>2<br>5<br>…<br>…<br>**20** | SMBus Block Read message length for EC |
| Thermal Reporting EC PEC | **Disabled**<br>Enabled | Enable Packet Error Checking (PEC) for SMBus Block Read |
| Select slots with TS on DIMMs | **No TS on DIMM**<br>TS on DIMM in Slot SODIMM0<br>TS on DIMM in Slot SODIMM1<br>TS on DIMM in Slot SODIMM0 and SODIMM1 | Enable temperature reporting for slots with TS on DIMM. Note: SODIMM0 is the one closer to CPU. |
| MCH Temp Read | Disabled<br>**Enabled** | MCH Temperature Read Enable |
| PCH Temp Read | Disabled<br>**Enabled** | PCH Temperature Read Enable |
| CPU Energy Read | Disabled<br>**Enabled** | CPU Energy Read Enable |
| CPU Temp Read | Disabled<br>**Enabled** | CPU Temperature Read Enable |
| Alert Enable Lock | **Disabled**<br>Enabled | Lock all Alert Enable settings |

## Thermal Configuration Settings: Intelligent Power Sharing

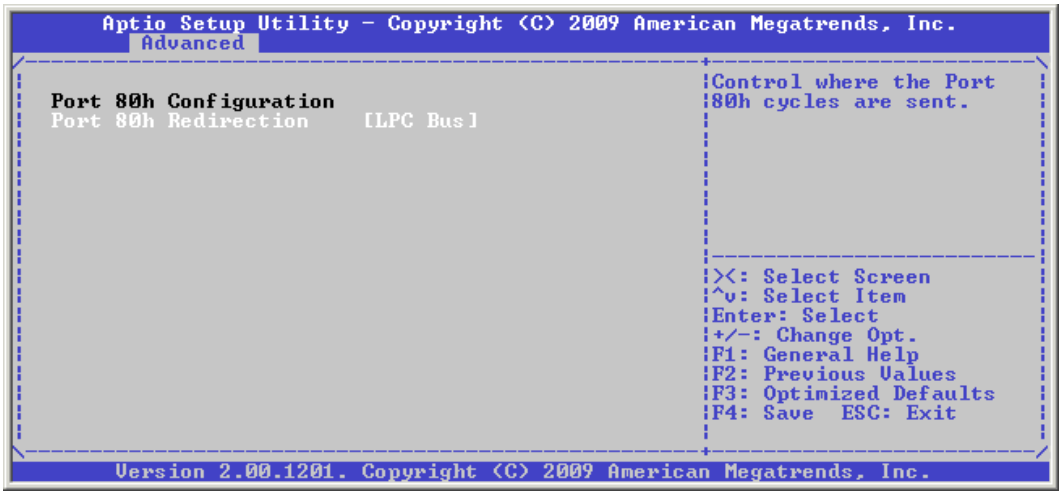



| Features | Options | Description |
|---|---|---|
| Intelligent Power Sharing | Disabled<br>**Enabled** | Intelligent Power Sharing configuration menu |
| CPU Turbo | Disabled<br>**Enabled** | CPU turbo enable or disable |
| PPEC Config | **0** | Processor Power Error Correction |
| IPS Policy | **DRIVER**<br>PROCESSOR<br>BALANCED<br>GRAPHICS | Platform BIOS policy preference |
| Core Temp Limit | **Disabled**<br>Enabled | Core temperature limit |
| Processor Power Limit | **Disabled**<br>Enabled | Max processor power clamp |
| Core Power Limit | **Disabled**<br>Enabled | Max core power clamp |
| Run Time Interface | EC uses SMBus<br>**BIOS uses MMIO** | Choose runtime interface for PCH communication |

## Thermal Configuration Settings: DPPM Configuration

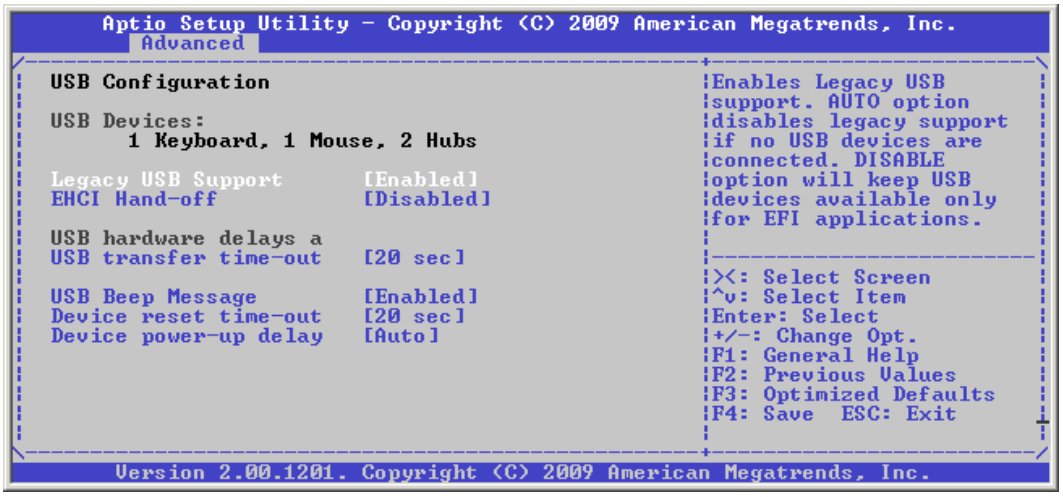



## Port 80h Settings: Port 80h Redirection



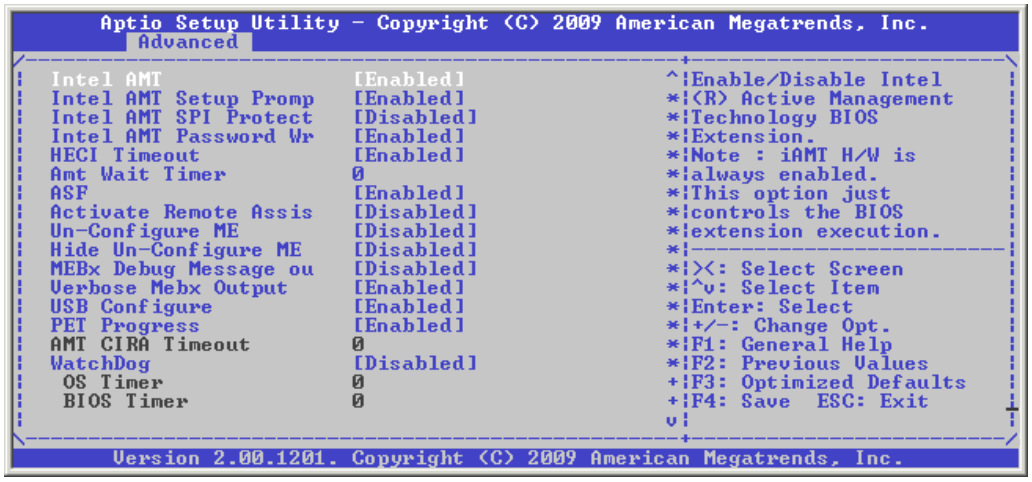

| Features | Options | Description |
|---|---|---|
| Port 80h Redirection | **LPC Bus**<br>PCI Bus | Control where the Port 80h cycles are sent |

## USB Configuration




| Features | Options | Description |
|---|---|---|
| Legacy USB Support | **Enabled**<br>Disabled<br>Auto | Enable = legacy USB support. Auto = disables legacy support if no USB devices are connected Disable = keep USB devices available only for EFI applications. |
| EHCI Hands-off | **Disabled**<br>Enabled | This is a workaround for OSs without EHCI hand-off support The EHCI ownership change should be claimed by the EHCI driver |
| USB transfer time-out | 1 sec<br>5 sec<br>10 sec<br>**20 sec** | The time-out value for Control, Bulk and Interrupt transfers |
| USB Beep Message | Disabled<br>**Enabled** | Enable/disable the beep during USB device enumeration. |
| Device reset time-out | 10 sec<br>**20 sec**<br>30 sec<br>40 sec | Selects USB mass storage device Start Unit command time-out. |
| Device power-up delay | **Auto**<br>Manual | Maximum time the device will take before it properly reports itself to the host controller. Auto = use default value: for a Root port the delay is 100ms, for a Hub port the delay is taken from the Hub descriptor. |

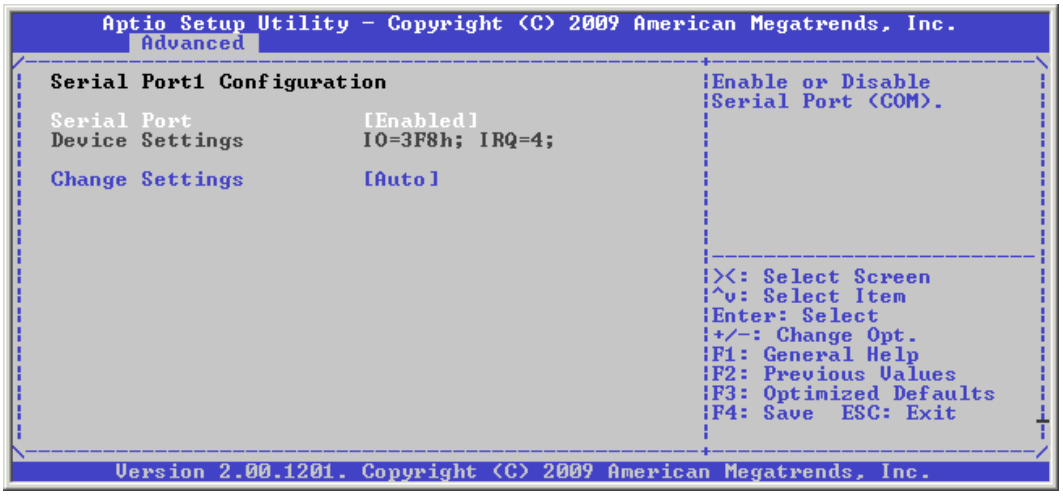
## AMT Configuration




| Features | Options | Description |
|---|---|---|
| Intel AMT | **Disabled**<br>Enabled | Enable/disable Intel® Active Management Technology BIOS Extension.<br>**NOTE**: iAMT H/W is always enabled. This option just controls the BIOS extension execution. |
| Intel AMT Setup Prompt | Disabled<br>**Enabled** | Enable/disable Intel AMT Setup Prompt to wait for hot-key to enter setup. |
| Intel AMT SPI Protect | **Disabled**<br>Enabled | Enable/disable Intel AMT SPI write protect. |
| Intel AMT Password Write Enable | Disabled<br>**Enabled** | Enable/disable Intel AMT Password Write. Enable = Password is writeable |
| HECI Timeout | Disabled<br>**Enabled** | Enable/disable HECI Timeout for Send/Read Message and Wait for Initialization. |
| AMT Wait Timer | **0** | Set timer to wait before sending ASF_GET_BOOT_OPTIONS. |
| ASF | Disabled<br>**Enabled** | Enable/disable Alert Specification Format. |
| Activate Remote Assistance Process | **Disabled**<br>Enabled | Trigger CIRA boot |
| Un-Configure ME | **Disabled**<br>Enabled | Un-Configure ME without password. |
| Hide Un-Configure ME Confirmation Prompt | **Disabled**<br>Enabled | Hide Un-Configure ME without password Confirmation Prompt |

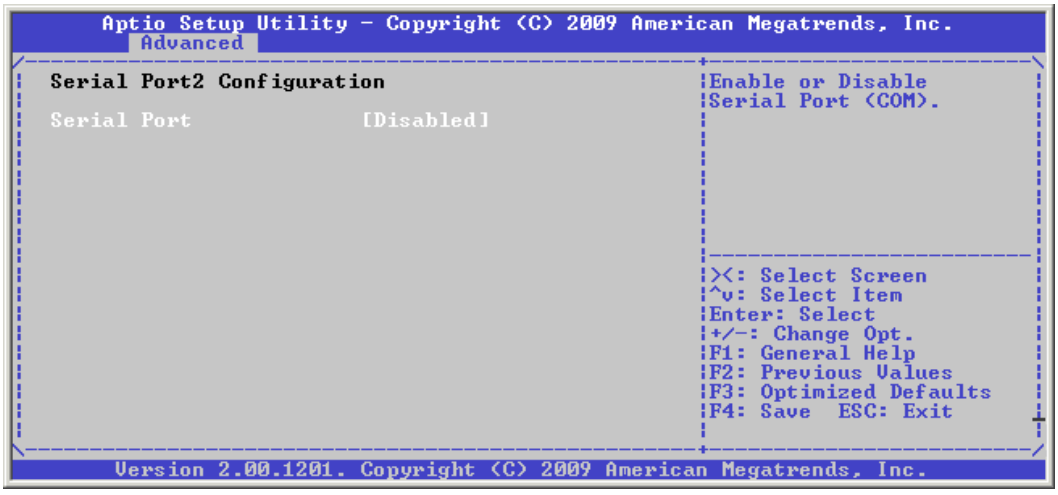
| | | |
|---|---|---|
| MEBx Debug Message Output | **Disabled**<br>Enabled | Enable MEBx debug message output. |
| Verbose MEBx Output | Disabled<br>**Enabled** | Enable/disable Verbose Mebx Output. |
| USB Configure | Disabled<br>**Enabled** | Enable/disable USB Configure function. |
| PET Progress | Disabled<br>**Enabled** | Enable/disable PET event progress to receive PET events or not. |
| WatchDog | **Disabled**<br>Enabled | Enable/disable WatchDog timer. |
| KVM Feature | **Disabled**<br>Enabled | Enable/disable KVM feature. |
| Me FW Downgrade | **Disabled**<br>Enabled | Enable/disable Me FW Downgrade function. |

## Super I/O W83627HF Configuration: Serial Port 1 Configuration



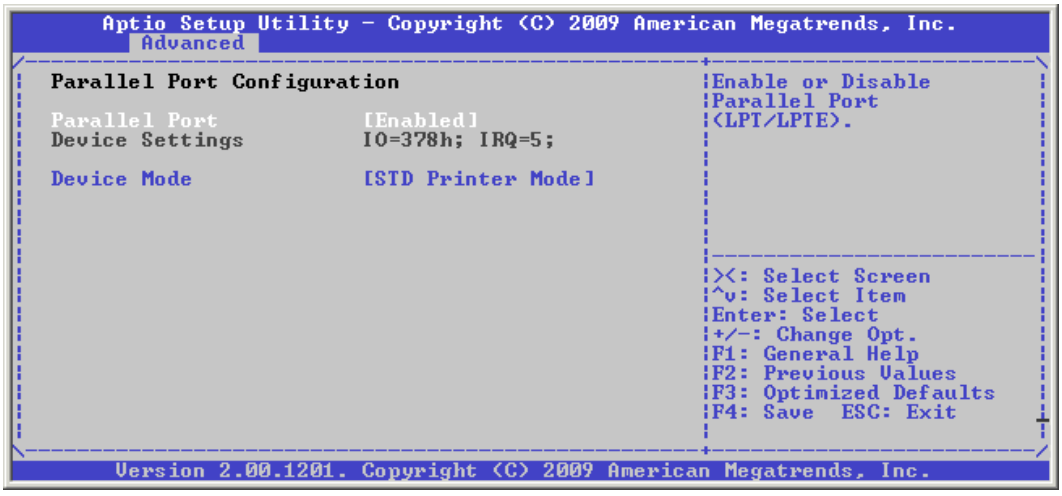

| Features | Options | Description |
|---|---|---|
| Serial Port | Disabled<br>**Enabled** | Enable /disable Serial Port (COM). |
| Change Settings | **Auto**<br>IO=3F8h; IRQ=4;<br>IO=3F8h;<br>IRQ=3,4,5,6,7,10,11,12;<br>IO=2F8h;<br>IRQ=3,4,5,6,7,10,11,12;<br>IO=3E8h;<br>IRQ=3,4,5,6,7,10,11,12;<br>IO=2E8h;<br>IRQ=3,4,5,6,7,10,11,12; | Select an optimal setting for Super IO Devices |

## Super I/O W83627HF Configuration: Serial Port 2 Configuration



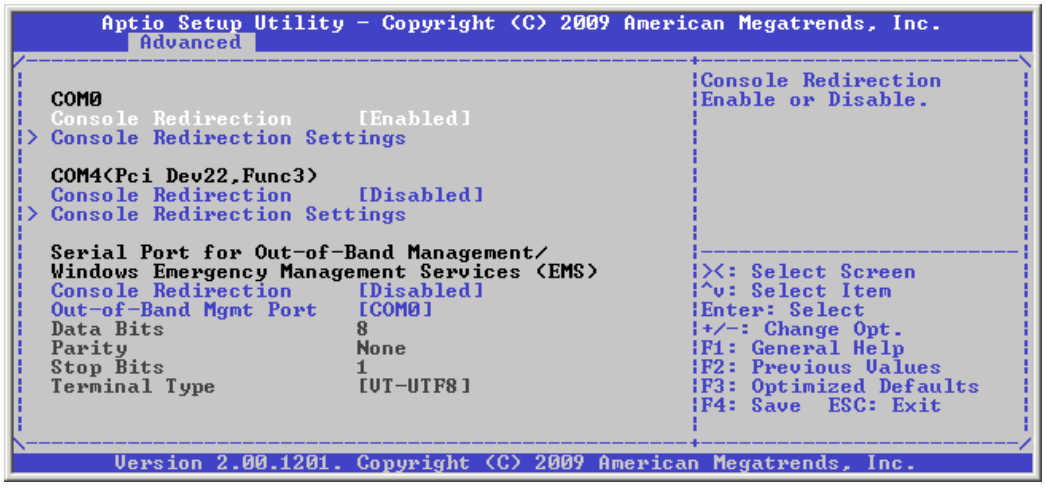

| Features | Options | Description |
|---|---|---|
| Serial Port | **Disabled**<br>Enabled | Enable /disable Serial Port (COM). |
| Change Settings | **Auto**<br>IO=3F8h; IRQ=4;<br>IO=3F8h;<br>IRQ=3,4,5,6,7,10,11,12;<br>IO=2F8h;<br>IRQ=3,4,5,6,7,10,11,12;<br>IO=3E8h;<br>IRQ=3,4,5,6,7,10,11,12;<br>IO=2E8h;<br>IRQ=3,4,5,6,7,10,11,12 | Select an optimal setting for Super IO Devices |

## Super I/O W83627HF Configuration: Parallel Port Configuration



| Features | Options | Description |
|---|---|---|
| Parallel Port | Disabled<br>**Enabled** | Enable /disable Parallel Port(LPT/LPTE). |
| Device Mode | **STD Printer Mode**<br>SPP Mode<br>EPP-1.9<br>EPP-1.7<br>ECP Mode<br>ECP and EPP 1.9 Mode<br>ECP and EPP 1.7 Mode | Change the printer port mode |

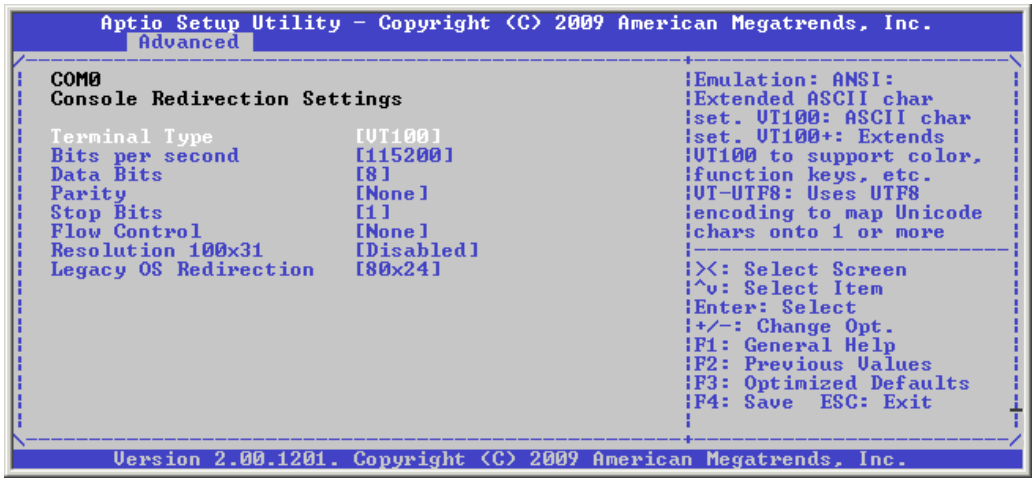
## Serial Port Console Redirection




| Features | Options | Description |
|---|---|---|
| COM0 Console Redirection | Disabled<br>**Enabled** | Enable /disable Console Redirection |
| COM0 Console Redirection Settings | Submenu | The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. |
| COM4 Console Redirection | **Disabled**<br>Enabled | Enable /disable Console Redirection |
| COM4 Console Redirection Settings | Submenu | The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. |

| | | |
|---|---|---|
| Windows EMS Console Redirection | **Disabled**<br>Enabled | Enable /disable Console Redirection |
| Out-of-Band Mgmt Port | **COM0**<br>COM4(PCI Dev22, Func3) | Microsoft Windows Emergency Management Services (EMS) for remote management of a Windows Server OS through a serial port. |

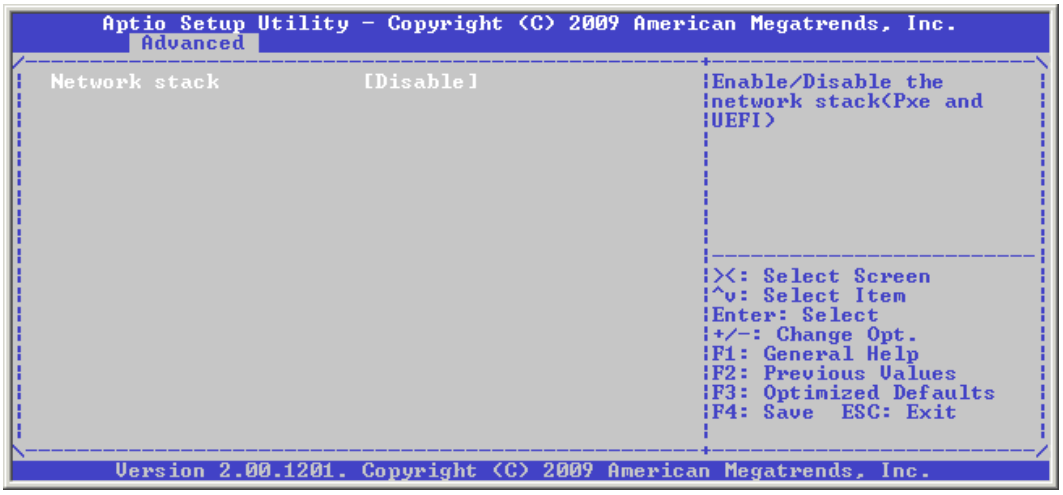
## Console Redirection Settings



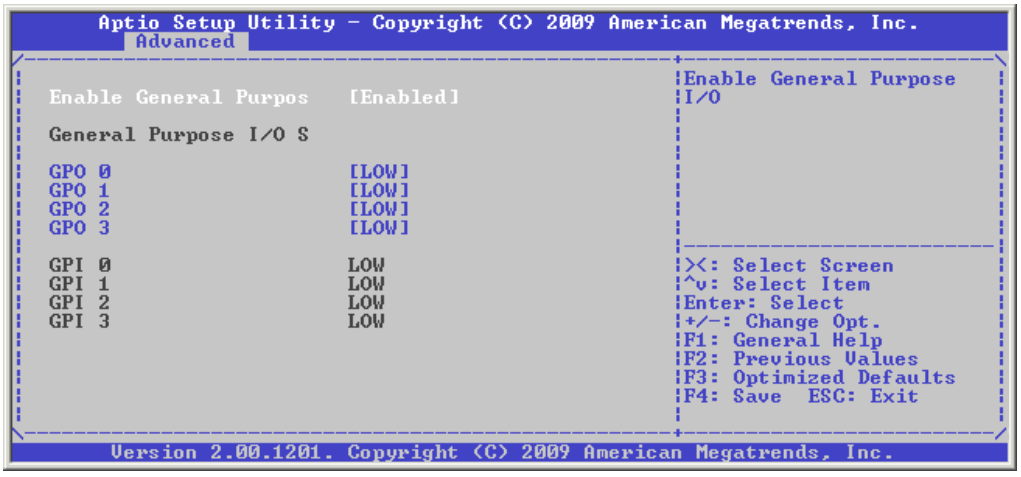

| Features | Options | Description |
|---|---|---|
| Terminal Type | VT100<br>VT100+<br>VT-UTF8<br>**ANSI** | Emulation: ANSI Extended ASCII char set.<br>VT100: ASCII char set.<br>VT100+: Extents VT100 to support color, function keys, etc.<br>VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more |
| Bits per second | 9600<br>19200<br>57600<br>**115200** | Select serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. |
| Data Bits | 7<br>**8** | Data Bits |

| | | |
|---|---|---|
| Parity | **None**<br>Even<br>Odd<br>Mark<br>Space | A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the number of the 1s in the data bits is even. Odd: parity bit is 0 if number of 1s in the data bits is odd. |
| Stop Bits | **1**<br>2 | Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1. |
| Flow Control | **None**<br>Hardware RTS/CTS<br>Software Xon/Xoff | Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, , then a 'start' signal can be sent to re-start the flow of data. Hardware flow control uses two wires for sending the 'stop' and 'start' signals. Software flow control uses ASCII characters sending the 'stop' and 'start' signals. The use of ASCII characters slows down the data flow and can be problematic if binary data is being transferred. |
| Resolution<br>100x31 | **Disabled**<br>Enabled | Enable/disable extended terminal resolution |
| Legacy OS Redirection Resolution | **80x24**<br>80x25 | On legacy OSs, the number of rows and columns supported with redirection |

## Network Stack

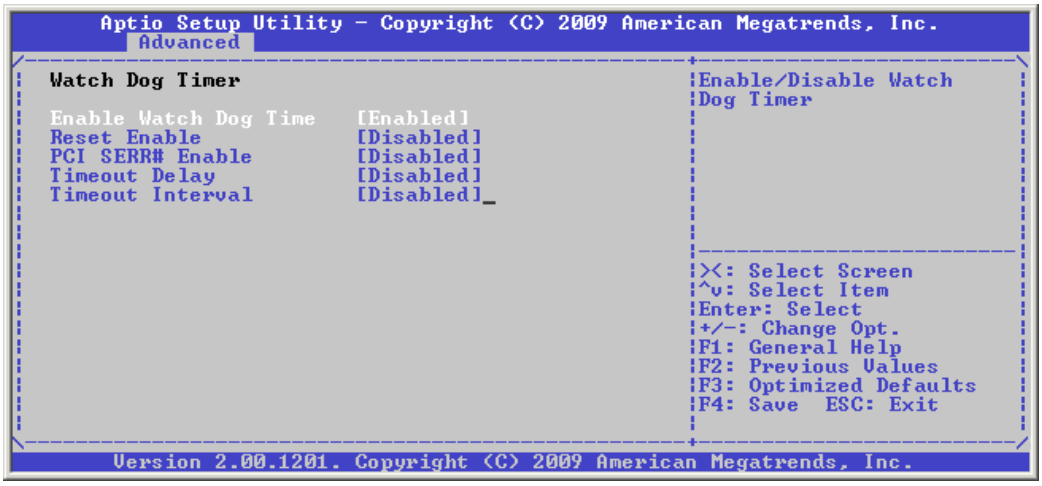



## ADT7462 H/W Monitor: General Purpose Register




| Features | Options | Description |
|---|---|---|
| Enable General Purpose I/O | Disabled<br>Enabled | Enable General Purpose I/O |
| GPO 0 | HIGH<br>LOW | |
| GPO 1 | HIGH<br>LOW | |
| GPO 2 | HIGH<br>LOW | |
| GPO 3 | HIGH<br>LOW | |

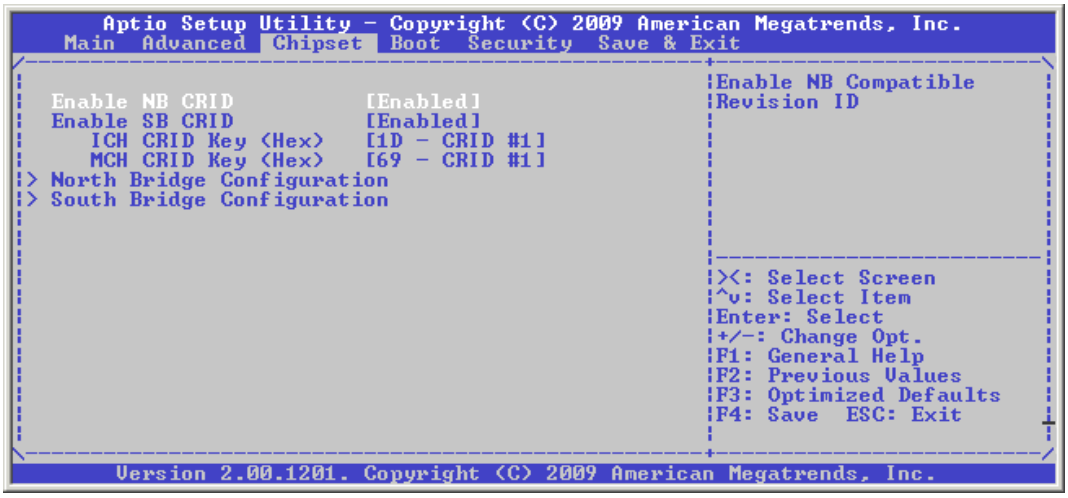
## WatchDog Timer




| Features | Options | Description |
|---|---|---|
| Enable Watch Dog Timer | **Disabled**<br>Enabled | Enable Watch Dog Timer |
| Reset Enable | **Disabled**<br>Enabled | Timeout Reset System |
| PCI SERR# Enable | **Disabled**<br>Enabled | Timeout Asserts PCI SERR# |
| Timeout Delay | **Disabled**<br>5 Seconds<br>10 Seconds<br>…<br>1 Minute<br>…<br>15 Minute | Initial Timeout Delay |
| Timeout Interval | **Disabled**<br>5 Seconds<br>10 Seconds<br>…<br>1 Minute<br>…<br>15 Minute | Timeout interval |

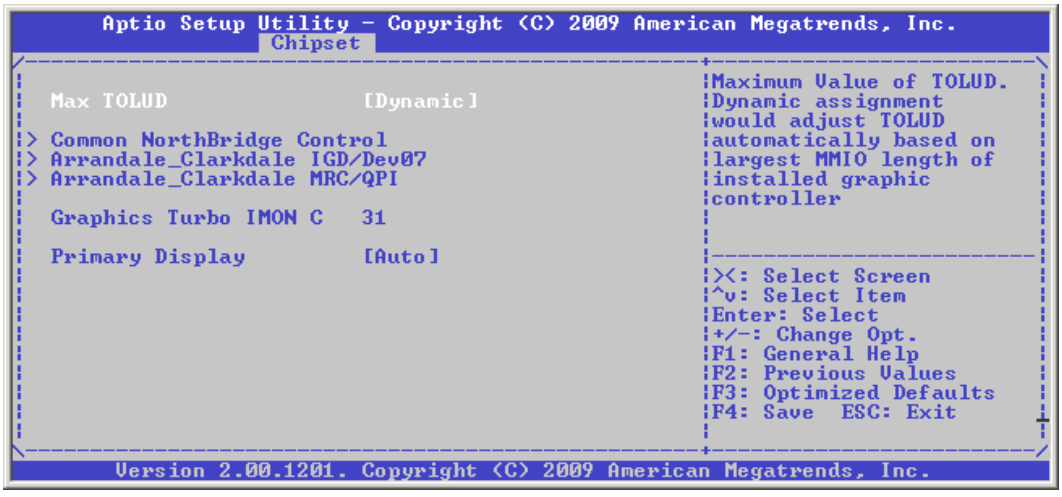
## 8.3.3Chipset

### Chipset Menu



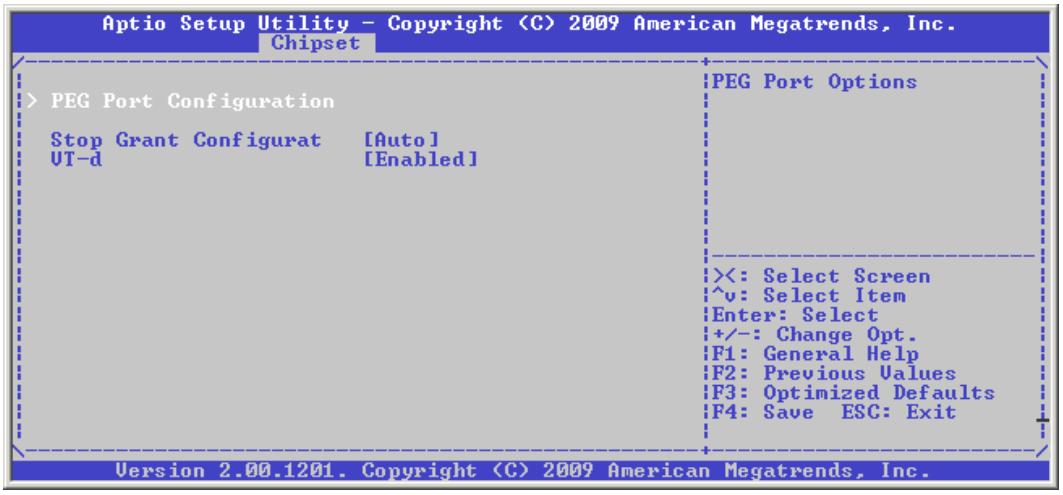

| Features | Options | Description |
|---|---|---|
| Enable NB CRID | Disable<br>**Enable** | Enable NB Compatible Revision ID |
| Enable SB CRID | Disable<br>**Enable** | Enable SB Compatible Revision ID |
| ICH CRID Key (Hex) | **1D** – CRID #1<br>2D – CRID #2 | ICH Compatible Revision ID key value |
| MCH CRID Key (Hex) | 69 – CRID #1 | MCH Compatible Revision ID key value |

### North Bridge Configuration



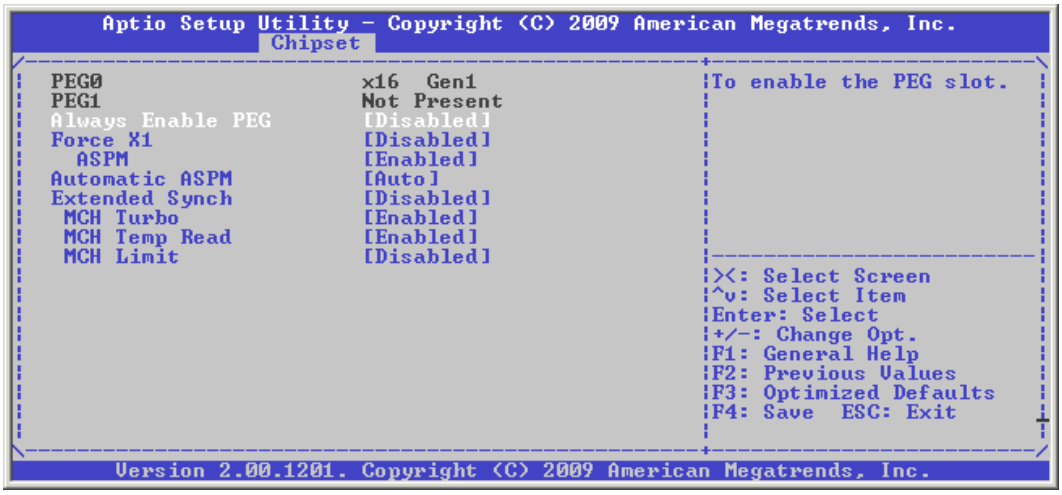
| Features | Options | Description |
|---|---|---|
| Max TOLUD | **Dynamic**<br>2GBytes<br>2.25GBytes<br>2.5GBytes<br>…<br>…<br>3.25GBytes | Maximum Value of TOLUD. Dynamic assignment adjusts TOLUD automatically based on largest MMIO length of installed graphic controller |
| Graphics Turbo IMON C | **31** | Graphics turbo IMON current values supported (14-31) |
| Primary Display | **Auto**<br>IGD<br>PEG<br>PCI<br>SG | Selects either IGD/PEG/PCI Graphics device to be Primary Display or selects SG for switchable graphics. |

## North Bridge Configuration Settings: Common North Bridge Control



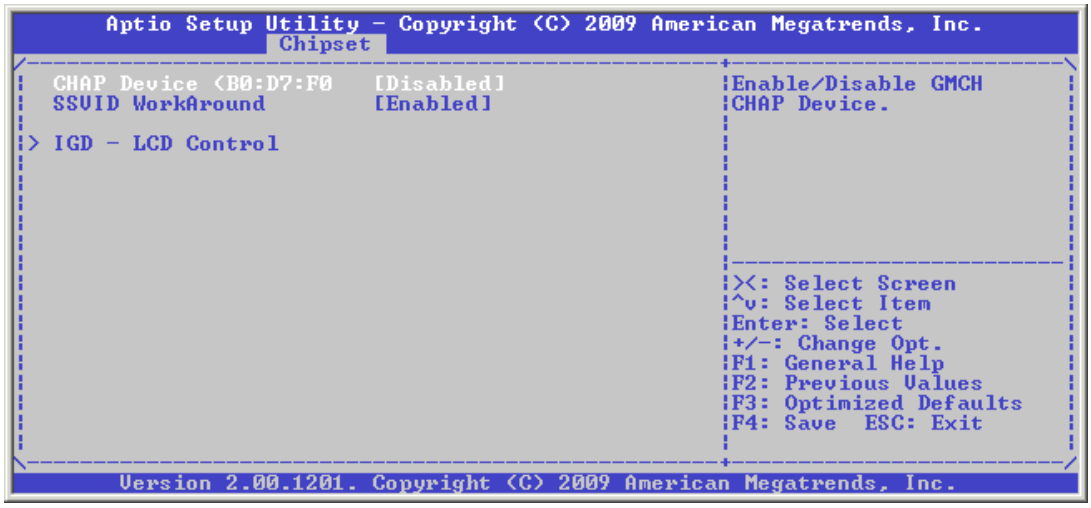

| Features | Options | Description |
|---|---|---|
| Stop Grant Configuration | **Auto**<br>Manual | Automatic/manual stop grant configuration |
| VT-d | Disabled<br>**Enabled** | Check to enable VT-d function on MCH. |

## Common North Bridge Control Settings: PEG Port Configuration




| Features | Options | Description |
|---|---|---|
| Always Enable PEG | Enabled<br>**Disabled** | Enable/disable PEG slot. |
| Force X1 | Enabled<br>**Disabled** | Force PEG link to retrain to X1 mode. |
| ASPM | **Enabled**<br>Disabled | Control ASPM support for the PEG device. This has no effect if PEG is not the currently active device. |
| Automatic ASPM | Manual<br>**Auto** | Automatically enable ASPM based on reported capabilities and known issues. |
| Extended Synch | **Disabled**<br>Enabled | Enable PCIe Extended Synchronization for logic analyzer use. |
| MCH Turbo | Disabled<br>**Enabled** | Enable/disable MCH Turbo |
| MCH Temp Read | Disabled<br>**Enabled** | Enable/disable MCH temperature read |
| MCH Limit | **Disabled**<br>Enabled | Enable/disable MAC MCH Power Clamp |

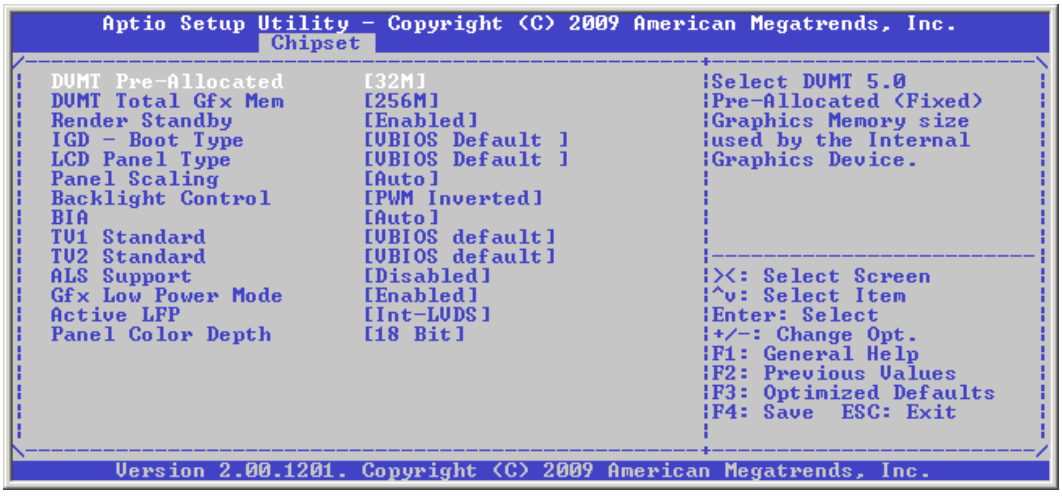
## North Bridge Settings: IGD/Dev07




| Features | Options | Description |
|---|---|---|
| CHAP Device(B0:D7:F0) | **Disabled**<br>Enabled | Enable/Disable GMCH CHAP Device. |
| SSVID WorkAround | Disabled<br>**Enabled** | Enable/Disable SSVID WorkAround |

NOTE: System features traditionally controlled by either the north bridge or south bridge chipset components now have been distributed between the Intel® Core™ i7/i5 processor and the QM57 PCH have distributed. Control via the processor or the PCH is indicated in the headings for the BIOS screen shorts provided below.

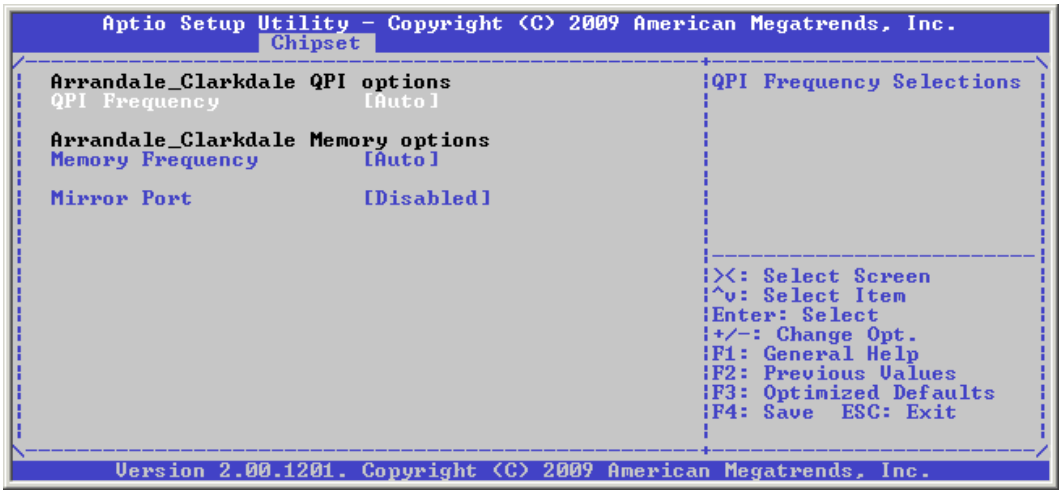
## North Bridge Settings: IGD – LCD Control



| Features | Options | Description |
|---|---|---|
| DVMT Pre-Allocated | **32M**<br>64M<br>128M | Select DVMT 5.0 Pre-Allocated (fixed) Graphics Memory size used by the Internal Graphics Device (IGD) |
| DVMT Total Gfx Memory | 128M<br>**256M**<br>MAX | Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device (IGD) |
| Render Standby | Disabled<br>**Enabled** | Enable/disable render standby support. |
| IGD – Boot Type | **VBIOS Default**<br>CRT<br>LFP<br>CRT + LFP<br>LFP-SDVO<br>EFP2<br>EFP3<br>EFP<br>CRT + LFP-SDVO<br>CRT + EFP | Select the video device to be activated during POST. This has no effect if external graphics present. |
| LCD Panel Type | **VBIOS Default**<br>800x600 LVDS<br>1024x768 LVDS<br>1280x1024 LVDS<br>…<br>…<br>…<br>2040x1536 LVDS | Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item |
| Panel Scaling | **Auto**<br>Force Scaling<br>Off<br>Maintain Aspect Ratio | Select the LCD panel scaling option used by the Internal Graphics Device (IGD) |
| Backlight Control | **PWM Inverted**<br>PWM Normal<br>GMBus Inverted<br>GMBus Normal | Backlight control setting |
| BIA | **Auto**<br>Disabled<br>Level 1<br>Level 2<br>Level 3<br>Level 4<br>Level 5 | Auto: GMCH Use VBT default; Level n" Enable with Selected Aggressiveness Level. |
| TV1 Standard | **VBIOS Default** | |
| TV2 Standard | **VBIOS Default** | |
| ALS Support | Enabled<br>**Disabled** | Valid only for ACPI<br>Legacy = ALS Support through the IGD INIT10 function<br>ACPI = ALS support through an ACPI ALS driver |

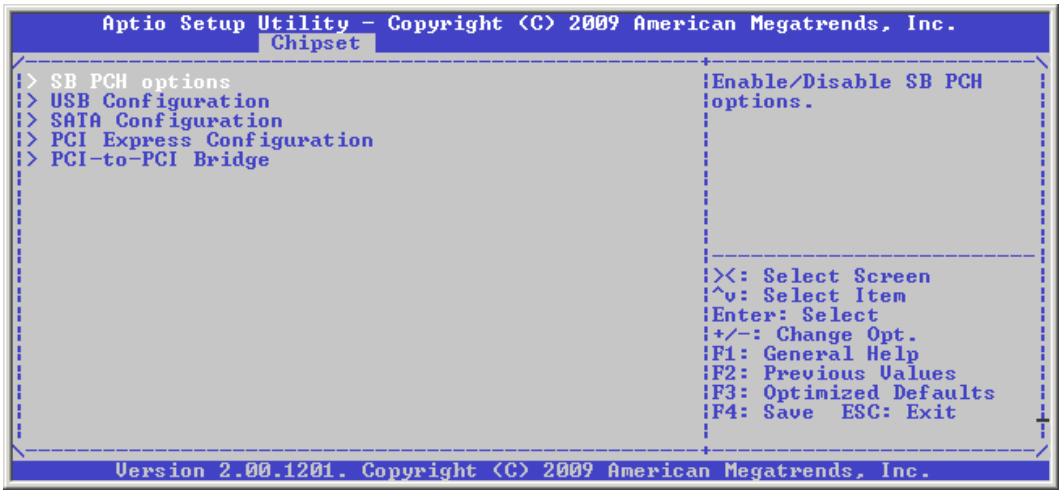
| | | |
|---|---|---|
| Gfx Low Power Mode | **Enabled**<br>Disabled | Valid only for SFF |
| Active LFP | No LVDS<br>**Int-LVDS**<br>SDVO LVDS<br>eDP Port-A<br>eDP Port-D | Select the Active LFP configuration<br>No LVDS: VBIOS does not enable LVDS.<br>Int-LDVS: VBIOS enables LDVS driver by Integrated encoder.<br>SDVO LVDS: VBIOS enables LDVS driver by SDVO. |
| Panel Color Depth | **18 Bits**<br>24 Bits | Select the LFP Panel Color Depth |

## North Bridge Settings: MRC/QPI Options

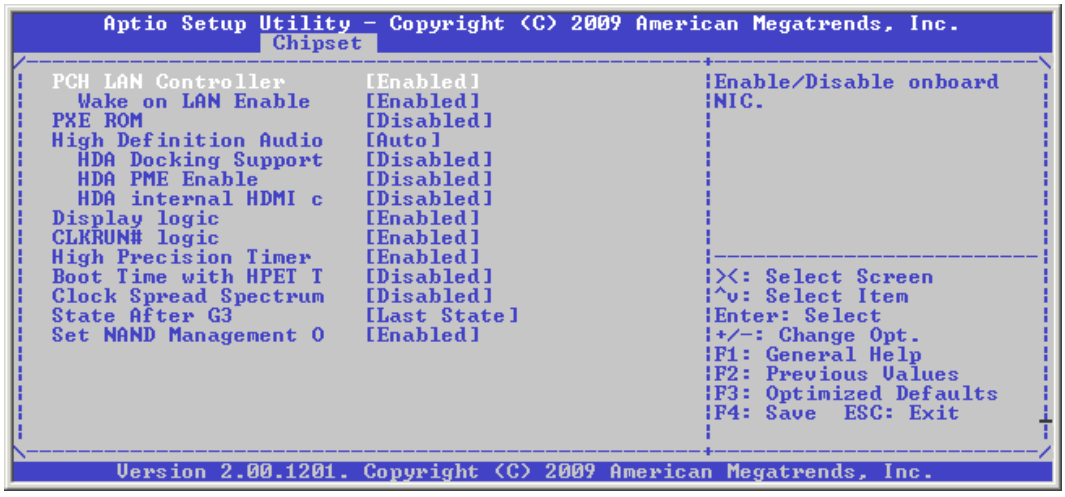



| Features | Options | Description |
|---|---|---|
| QPI Frequency | **Auto**<br>3.200 GT<br>4.800 GT<br>…<br>...<br>Disabled | QPI Frequency selections |
| Memory Frequency | **Auto**<br>800<br>1066<br>1333 | Maximum Memory Frequency selections in MHz |
| Mirror Port | **Disabled**<br>Enabled | Disable/Enable Mirror Port |

## South Bridge Configuration Settings



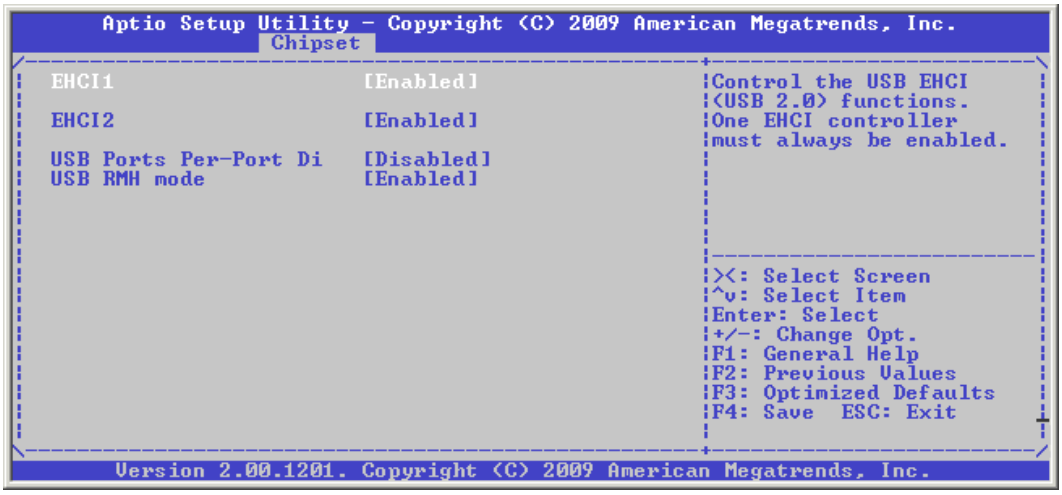

## South Bridge Settings: PCH Options




| Features | Options | Description |
|---|---|---|
| PCH LAN Controller | **Enabled**<br>Disabled | Enable/disable onboard NIC |
| Wake on LAN Enable | **Enabled**<br>Disabled | Enable/disable integrated LAN to wake the system |
| PXE ROM | Enabled<br>**Disabled** | Enable/disable PXE Option ROM execution for onboard LAN |

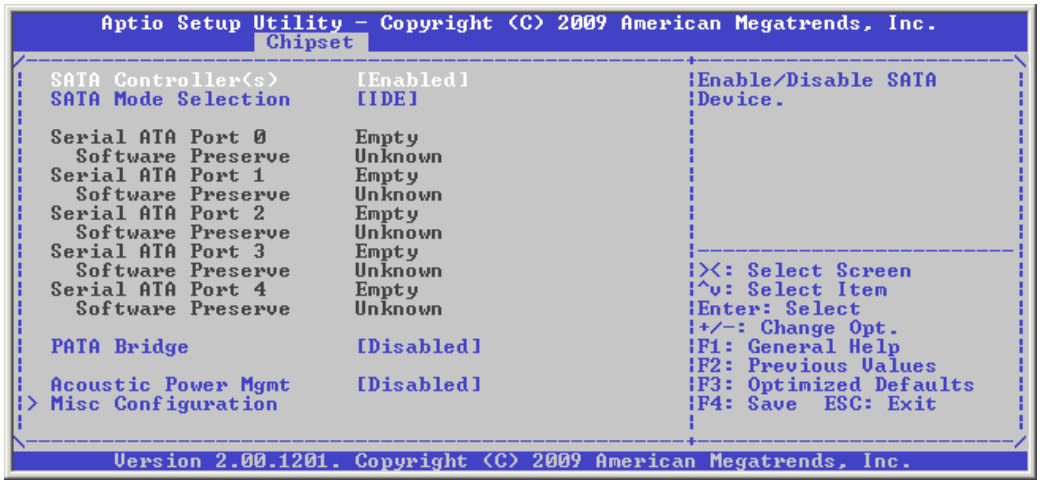
| | | |
|---|---|---|
| High Definition Audio | Disabled<br>Enabled<br>**Auto** | Enable/disable HAD docking support for the audio controller<br>Disabled = HAD is unconditionally disabled<br>Enabled = HAD is unconditionally enabled<br>Auto = HAD is enabled if present, and disabled if not |
| HDA Docking Support | **Disabled**<br>Enabled | Enable/disable HAD Docking Support of Audio Controller |
| HAD PME Enable | **Disabled**<br>Enabled | Enable/disable Power Management capability of Audio Controller. |
| HDA Internal HDMI codec | **Disabled**<br>Enabled | Enable/disable internal HDMI codec for HDA |
| Display logic | **Disabled**<br>Enabled | Enable/disable the PCH Display logic |
| CLKRUN# logic | Disabled<br>**Enabled** | Enable/disable the CLKRUN# logic to stop the PCI clocks |
| High Precision Timer | Disabled<br>**Enabled** | Enable /disable the High Precision Event Timer |
| Boot Time with HPET Timer | **Disabled**<br>Enabled | Enable/disable Boot time calculation with High Precision Event Timer |
| Clock Spread Spectrum | **Disabled**<br>Enabled | Enable/disable Clock chi Spread Spectrum feature |
| State After G3 | Power On State<br>Power Off State<br>**Last State** | Specify what state to go to when power is re-applied after a power failure (G3 state) |
| Set NAND Management Overrride | Disabled<br>**Enabled** | Option to override NAND management to allow driver or 3rd party software to configure the NAND module after POST |

## South Bridge Settings: USB Configuration



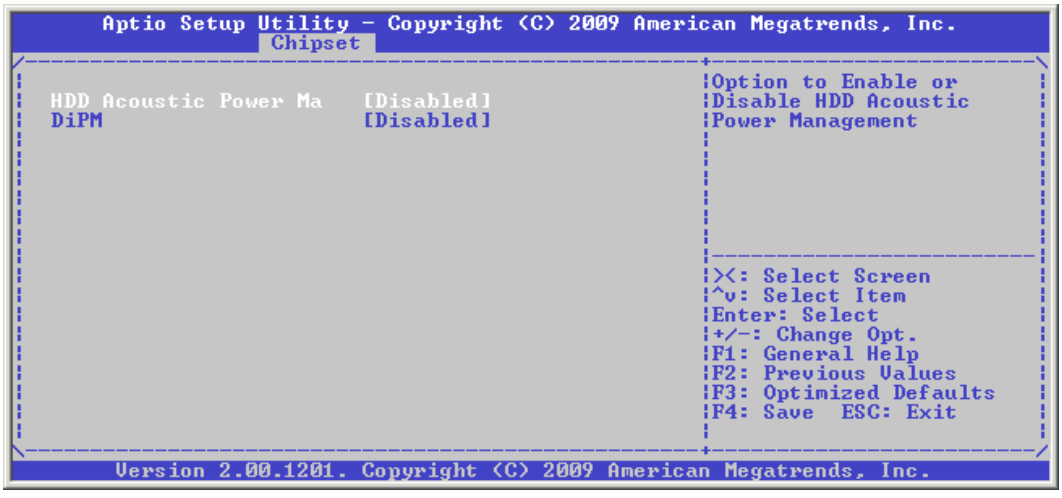

| Features | Options | Description |
|---|---|---|
| EHCI 1 | Disabled<br>**Enabled** | Enable/disable the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled. |
| EHCI 2 | Disabled<br>**Enabled** | Enable/disable the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled. |
| USB Ports Per-Port Disable Control | **Disabled**<br>Enabled | Enable/disable control of each of the USB ports (0~9) |
| USB Port #N Disable | **Disabled**<br>Enabled | Enable/disable USB port |
| USB RMH mode | Disabled<br>**Enabled** | Enable/disable PCH USB Rate Matching Hubs mode |

## South Bridge Settings: SATA Device Configuration



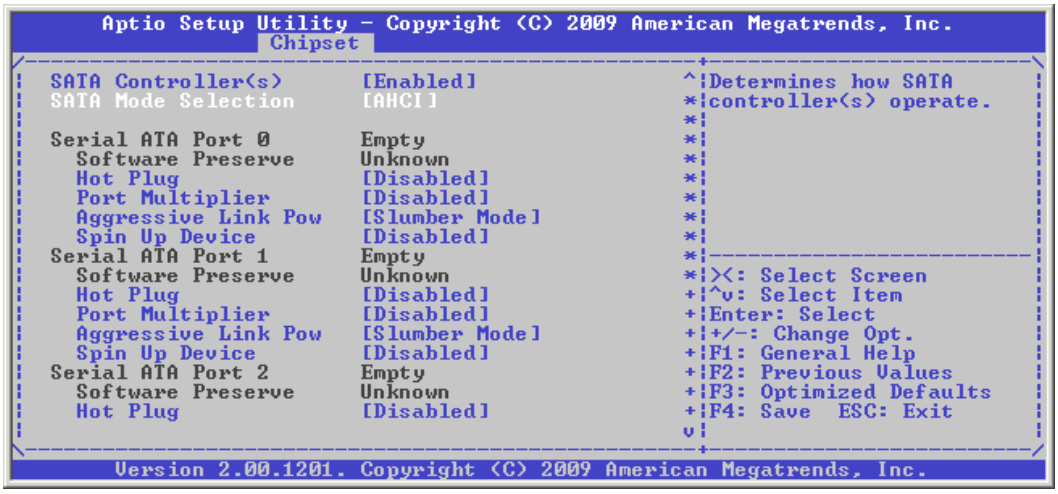

| Features | Options | Description |
|---|---|---|
| SATA Controller(s) | Disabled<br>**Enabled** | Enable/Disable SATA device |
| SATA Mode Selection | **IDE**<br>AHCI<br>RAID | Determines how SATA controller(s) operate |
| PATA Bridge | Disabled<br>**Enabled** | Enable/disable SATA-to-PATA Bridge |
| Acoustic Power Mgmt | Disabled<br>**Enabled** | Enable/disable HDD acoustic power management |

## Miscellaneous Configuration Options



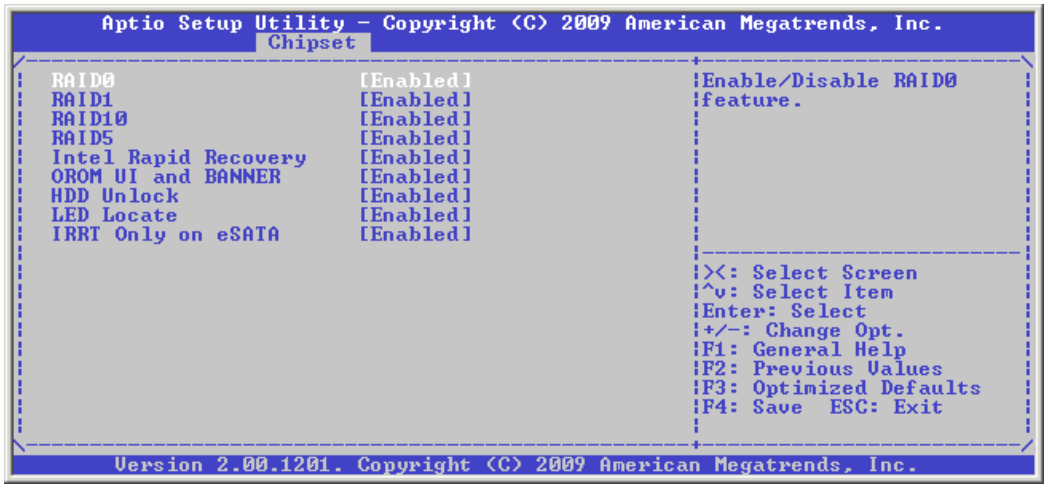
| Features | Options | Description |
|---|---|---|
| HDD Acoustic Power Management | Enabled<br>**Disabled** | Enable/disable HDD Acoustic Power Management |
| DiPM | Enabled<br>**Disabled** | Enable/disable DiPM |

## ACHI Mode



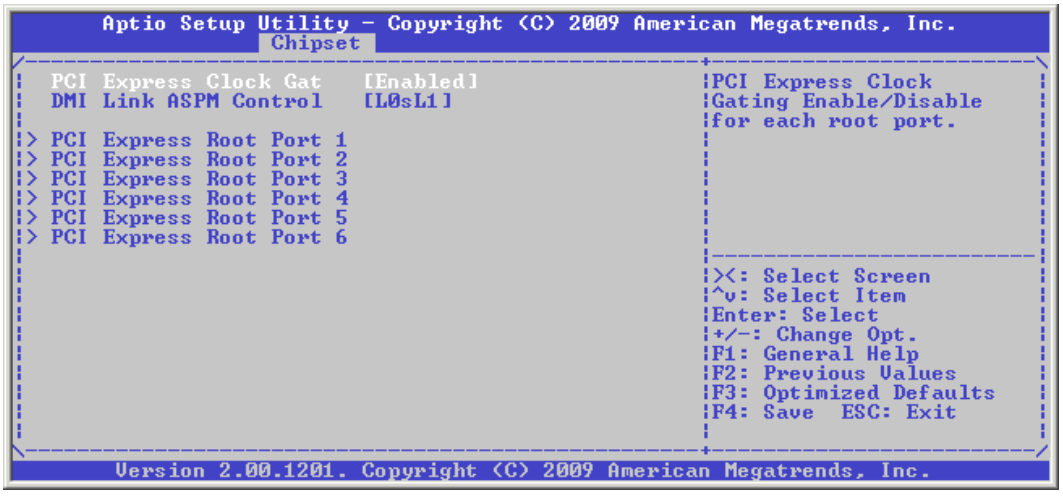

| Features | Options | Description |
|---|---|---|
| Hot Plug | **Disabled**<br>Enabled | Enable/disable this port as Hot Pluggable. |
| Port Multiplier | **Disabled**<br>Enabled | Enable/disable this port to support port multiplier. |
| Aggressive Link Power Mode Select | Disabled<br>Partial Mode<br>**Slumber Mode** | Select the lower link power state the PCH will aggressively enter. |
| Spin Up Device | Disabled<br>**Enabled** | On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device. |

## RAID Mode



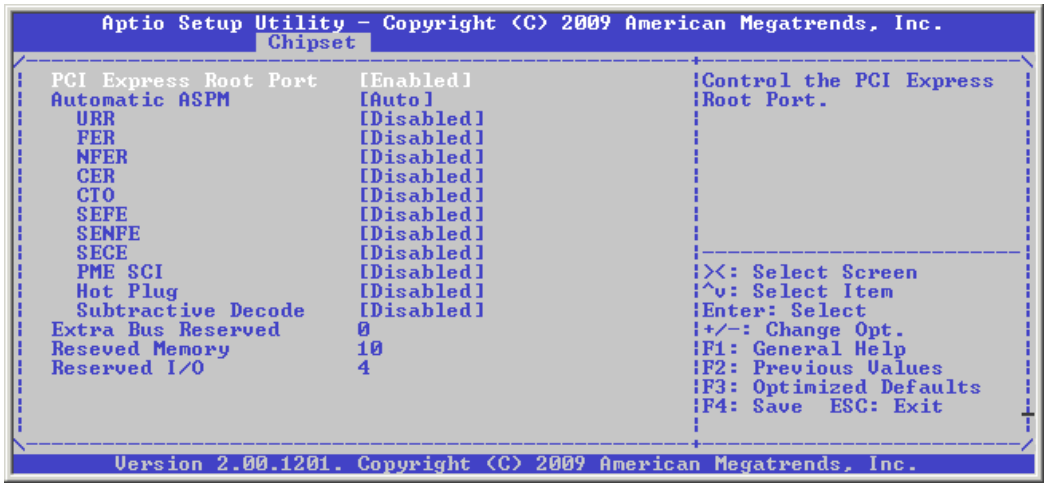

| Features | Options | Description |
|---|---|---|
| RAID0 | Disabled<br>**Enabled** | Enable/disable RAID0 feature |
| RAID1 | Disabled<br>**Enabled** | Enable/disable RAID1 feature |
| RAID10 | Disabled<br>**Enabled** | Enable/disable RAID10 feature |
| RAID5 | Disabled<br>**Enabled** | Enable/disable RAID5 feature |
| Intel Rapid Recovery Technology | Disabled<br>**Enabled** | Enable/disable Intel Rapid Recovery |
| OPOM UI and BANNER | Disabled<br>**Enabled** | Enable = the OROM UI is shown<br>Disable = no OROM banner or information will be displayed |
| HDD Unlock | Disabled<br>**Enabled** | If enabled, indicates that the HDD password unlock in the OS is enabled. |
| LED Locate | Disabled<br>**Enabled** | If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS. |
| IRRT Only on eSATA | Disabled<br>**Enabled** | If enabled, only the IRRT volume can span internal and eSATA drives<br>If disabled, any RAID volume can span internal and eSATA drives. |

## PCI Express Configuration



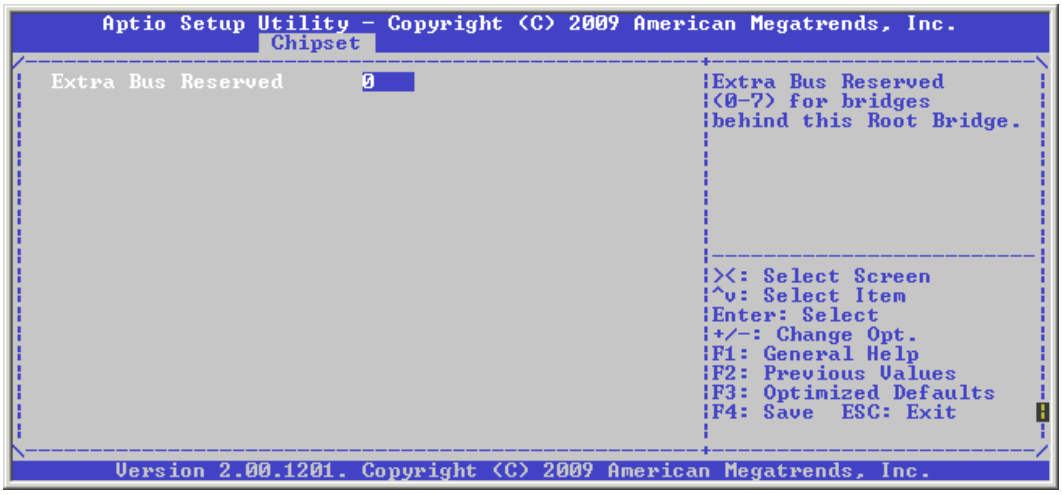

| Features | Options | Description |
|---|---|---|
| PCI Express Clock Gating | Disabled<br>**Enabled** | Enable/disable PCI Express clock gating for each root port. |
| DMI Link ASPM Control | Disabled<br>L0s<br>**L0sL1** | Active State Power Management control on both NB side and SB side of the DMI Link. |

## PCI Express Configuration Settings: PCI Express Root Port



| Features | Options | Description |
|---|---|---|
| PCI Express Root Port | Disabled<br>**Enabled** | Enable/disable control of the PCI Express Root Port |
| Automatic ASPM | Disabled<br>L0s<br>L1<br>L0sL1<br>**Auto** | Automatically enable ASPM based on reported capabilities and known issues |
| URR | **Disabled**<br>Enabled | Enable/disable PCI Express Unsupported Request Reporting. |
| FER | **Disabled**<br>Enabled | Enable/disable PCI Express Device Fatal Error Reporting |
| NFER | **Disabled**<br>Enabled | Enable/disable PCI Express Device Non-Fatal Error Reporting |
| CER | **Disabled**<br>Enabled | Enable/disable PCI Express Device Correctable Error Reporting |
| CTO | **Disabled**<br>Enabled | Enable/disable PCI Express Completion Timer TO |
| SEFE | **Disabled**<br>Enabled | Enable/disable Root PCI Express System Error on Fatal Error |
| SENFE | **Disabled**<br>Enabled | Enable/disable Root PCI Express System Error on Non-Fatal Error |
| SECE | **Disabled**<br>Enabled | Enable/disable Root PCI Express System Error on Correctable Error |
| PME SCI | **Disabled**<br>Enabled | Enable/disable PCI Express PME SCI |
| Hot Plug | **Disabled**<br>Enabled | Enable/disable PCI Express Hot Plug |
| Subtractive Decode | **Disabled**<br>Enabled | Enable/disable PCI Express Subtractive Decode |
| Extra Bus Reserved | **0** | Extra bus reserved (0-7) for bridge behind this root bridge |
| Reserved Memory | **10** | Reserved memory and prefetchable memory (1-20MB) range for this root bridge |
| Reserved I/O | **4** | Reserved I/O (4K/8K/12K/16K/20K) range for this root bridge |

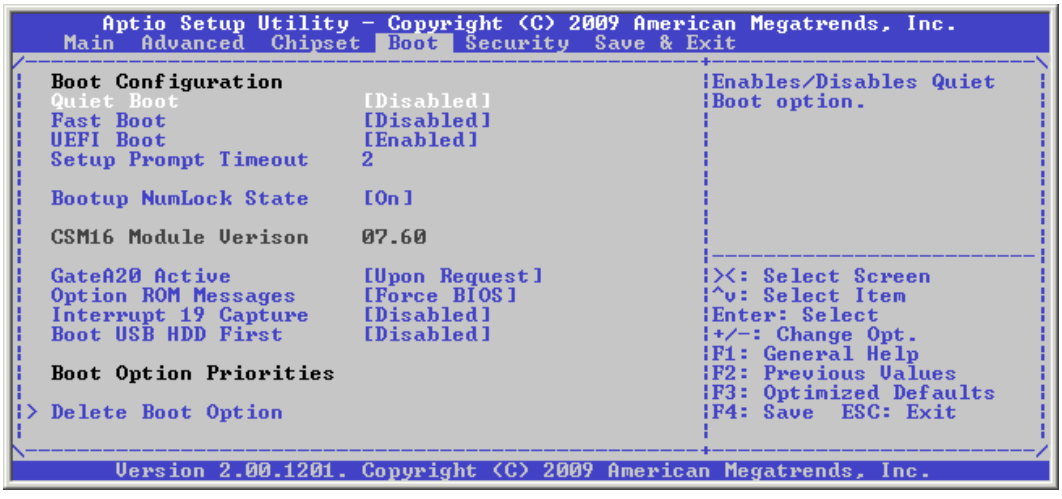
### PCI Express Root Port: PCI-to-PCI Bridge




| Features | Options | Description |
|---|---|---|
| Extra Bus Reserved | **0** | Extra Bus Reserved (0-7) for bridges behind this root bridge |

## 8.3.4Boot

## Boot Configuration



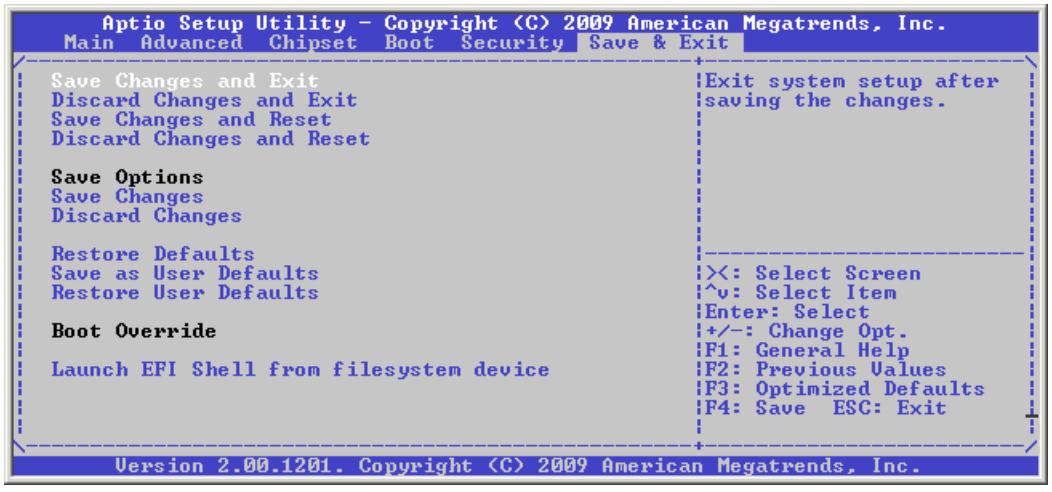
| Features | Options | Description |
|---|---|---|
| Quiet Boot | **Disabled**<br>Enabled | Enable/disable Quiet Boot option |
| Fast Boot | **Disabled**<br>Enabled | Enable/disable boot with initialization of a minimal set of devices required to launch active boot option<br>Has no effect for BBS boot options |
| UEFI Boot | Disabled<br>**Enabled** | Enable/disable UEFI boot for disks |
| Setup Prompt Timeout | **2** | Number of seconds to wait for setup activation key<br>65535(0xFFFF) means indefinite waiting<br>0 means no wait (not recommended) |
| Bootup NumLock State | **On**<br>Off | Select the keyboard NumLock state |
| GateA20 Active | **Upon Request**<br>Always | Upon Request = GA20 can be disabled using BIOS services<br>Always = do not allow disabling GA20<br>(this option is useful when any RT code is executed above 1MB) |
| Option ROM Messages | **Force BIOS**<br>Keep Current | Set display mode for Option ROM |
| Interrupt 19 Capture | **Disabled**<br>Enabled | Enabled = allows option ROMs to trap Int 19 |
| Boot USB HDD First | **Disabled**<br>Enabled | Enabled = allows USB HDD to boot first |
| Hard Drive BBS Priorities | | Set the order of the legacy devices in this group |
| Add New Boot Option | | Add a new EFI boot option to the boot order |
| Delete Boot Option | | Remove an EFI boot option from the boot order |

## 8.3.5Security

### Security Password Options


## 8.3.6Save and Exit Setup

### Save and Exit




| Features | Options | Description |
|---|---|---|
| Save Changes and Exit | | Exit system setup after saving the changes. |
| Discard Changes and Exit | | Exit system setup without saving any changes |
| Save Changes and Reset | | Reset the system after saving the changes |

| | |
|---|---|
| Discard Changes and Reset | Reset system setup without saving any changes |
| Save Changes | Save changes made so far to any of the setup options |
| Discard Changes | Discard changes made so far to any of the setup options |
| Restore Defaults | Restore/Load Defaults values for all the setup options |
| Save as User Defaults | Save the changes made so far as User Defaults |
| Restore User Defaults | Restore the User Defaults to all the setup options |
| Launch EFI Shell for filesystem device | Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available file system devices |
| Save Changes and Exit | Exit system setup after saving the changes |

## 8.4 vPro Functionality

The components of vPro supported by the ETXexpress-AI BIOS are as follows:

» AMT (Active Management Technology) v6.0

» TXT (Trusted Execution Technology)

» VT (Virtualization Technology)

» GbE (Gigabit Ethernet)

» Dual Core (or better) CPU

NOTE: All of these features have been tested and Kontron is awaiting the results of Intel's vPro compliance testing and subsequest marking as "vPro Capable".

# 9 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

» AH=Eah

» AL=function number

» DX=4648h (security word)

» CL=board number (starting with 1)

The interrupt returns a CL□0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

## 9.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

» Call Get BIOS ID with CL=1. The name of the first device installed will be returned. If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.

» Repeat until you see Board not present (CL□0). You now know the names of all boards within your system that follow the JIDA standard.

» You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

NOTE: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Web site, for further information on implementing and using JIDA calls with C sample code.

# 10 Appendix B: Architecture Information

The following sources of information can help you better understand PC architecture.

## 10.1 Buses

### 10.1.1 ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol. 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

### 10.1.2 PCI/104

- Embedded PC/104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI-SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

## 10.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3

» The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

» The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

## 10.3 Ports

### 10.3.1 RS-232 Serial

» EIA-232-E standard
The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

» RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

» National Semiconductor: The Interface Data Book includes application notes. Type "232" as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor's Web site.

### 10.3.2 Serial ATA

» Serial AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

### 10.3.3 USB

» USB Specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

## 10.4 Programming

» C Programmer's Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0

» Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

» The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X

» Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

# 11 Appendix C: Document Revision History

| Revision | Date | Changes |
|---|---|---|
| 0.5 | 10-May-10 | Initial review draft |
| 0.8 | 6-July-10 | Second draft with review comments and new source material added |
| 0.85 | 22-July-10 | Updates to pin-out tables, addition of current rev limitations, and various other updates through out the document. |
| 1.0 | 15-Dec-10 | First production version |
| 1.1 | 20-Jan-11 | Updated production version. Updates to USB, Graphics and BIOS sections. |
| 1.2 | 8-Apr-11 | Update to Table 10 – Pin D57 |

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