Charge Pump Circuit for High Speed PLL Application

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***Abstract*—This work presents a high-precision fully differential charge pump designed for modern high-speed phase-locked loop (PLL) applications. The proposed architecture integrates a reference-tracking voltage circuit to mitigate common problems encountered in traditional charge pump designs, including current mismatch, leakage-induced phase shift, and ripple at the control node. By adopting a differential topology, the design minimizes the influence of parasitic charge errors and enhances output stability. Simulation results demonstrate excellent current matching, a wide output swing, and reduced noise sensitivity—making the architecture particularly suitable for high-performance frequency-synthesis systems.**

***Keywords*—Charge pump; phase locked loop; differential circuit; current matching**

I. INTRODUCTION

In high-frequency communication systems, the performance of the PLL plays a critical role in determining timing accuracy and spectral purity. A crucial component of the PLL is the charge pump (CP), which converts the UP/DOWN logic pulses from the phase/frequency detector (PFD) into incremental voltage adjustments at the control input of the voltage-controlled oscillator (VCO). Even minor fluctuations in this control voltage can significantly alter the oscillation frequency, especially in high-gain VCOs. Therefore, achieving a stable and low-ripple CP output is essential for maintaining lock and minimizing jitter.

Furthermore, modern low-voltage CMOS technologies impose additional challenges: output swing must remain sufficiently wide to cover the VCO tuning range, while maintaining accurate current matching over the entire range of operating conditions. Non-idealities such as leakage, finite device output resistance, and switching delays introduce phase errors and degrade loop stability. Thus, enhancing the robustness and precision of the charge pump is critical for next-generation PLL design.[2,3].

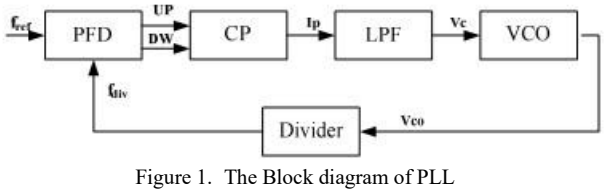


Figure 1. The Block diagram of PLL

There are two output periodic pulse signal with equal pulse width, Up and Dw, which output from PFD to control the two circuit sources. The currents I_{up} and I_{dw} flew through two switchers. These two currents make the capacitance charge or discharge to obtain the direct current to feed to the VOC. Therefore, the currents I_{up} and I_{dw} should be equal.

However, I_{up} and I_{dw} were sent to the charge pump from the PFD even at the locked state. Therefore, the pull-up current and the pull-down current should be matched with high accurate, otherwise the loop circuits will be hardly arrive to the stable state. Moreover, the voltage V_{co} will be increased similarly as staircase during the lock period, the current of the charge pump should be keep stable, it could not be varied following as the output voltage of the current source varies.

In order to reduce the power consumption, the power supplies are lower in the communication area. Therefore, the wider swing range of charge pump is required to satisfy the wide oscillation frequency range of the VCO.

The phase errors of the output frequency caused by the charge leakage, charge/discharge current mismatch and delay of the charge pump switch. The phase error can be expressed as:

$$\phi_\epsilon = \pi \frac{I_{\text{leak}}}{I_{\text{cp}}} \frac{\Delta t_{\text{on}}}{T_{\text{ref}}} + \pi \frac{\Delta I}{I_{\text{cp}}} \frac{\Delta t_d}{T_{\text{ref}}}$$

Where I_{leak} is the leakage current of charge pump, I_{cp} is the pump current, $\triangle t_{on}$ is the on time of the PFD, T_{ref} is the period of the reference timing, $\triangle I$ is the error of charge /discharge current, $\triangle t_d$ is the pump switch time delay[4]. To the third-order charge pump phase locked loop, the rejection ability to the jump of input reference frequency is described as follows:

$$P_r = 20\log\left(\frac{I_{cp}\,\phi_e\,K_{VCO}}{2\,f_{\text{ref}}}\right) - 20\log\left(\frac{f_{\text{ref}}}{f_{p1}}\right)$$

Where, K_{VCO} is the gain of VCO, f_{ref} is the reference clock frequency, f_{p1} is the polo frequency of the filter, and I_{cp} is the charge pump current[5-8].

According to the equations above, the performance of the high speed PLL is depend on the quality and structure of the charge pump, especially to the current match accuracy and the stability of the voltage output.

II. CONFIGURATION OF THE CHARGE PUMP OVERVIEW

The charge pump functions as an interface translating logic-level PFD outputs into controlled charge and discharge currents. Ideally, the UP signal should inject a fixed current into the loop filter, while the DOWN signal should remove the same amount, ensuring linear behavior. In practice, implementing this ideal functionality requires careful current-source design, switching arrangements, and compensation for transistor non-idealities.

A.The Model of Charge Pump

The charge pump of PLL consists of two current sources Iup and Idw, which controlled by switch signal UP and DW. The ideal charge pump model is shown as Fig.2. Three states of charge pump were listed in Table 1.

TABLE I.

STATES OF CHARGE PUMP

State	S_{M1}	S_{M2}	V_c
Up	on	off	Rise, charge
Hold	off	off	Hold, lock
Down	off	on	Fall, discharge

The switcher S_{M1} and S_{M2} could not be on simultaneously.

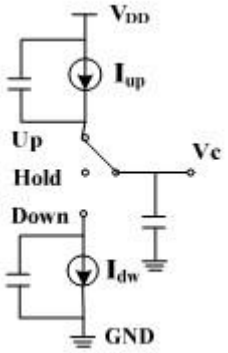


Figure 2. The model of charge pump

B. The Basic Charge Pump

Traditional charge pump circuit implemented by MOS technology is shown as Fig. 3. Although the two biased constant-current sources I_{cp} are identical, current I_{up} would be decreased, and I_{dw} would be increased following as the output voltage varied V_{out} towards the positive power VDD.

On the contrary, current I_{up} would be increased, while I_{dw} decreased when the output voltage V_{out} moving to the negative power VSS due to the dynamic resistance is exist in the MOS transistor [9]. The dynamic resistance results in the mismatch of charge and discharge currents of the charge pump, and the errors of the phase φ_ε would be introduced as well. In the differential scheme, the UP and DOWN actions create opposing current flows at two output nodes. An UP pulse charges one node while discharging the other, increasing the differential voltage. A DOWN pulse performs the reverse operation. Leakage currents or parasitic charge injections typically affect both nodes similarly; therefore, these common-mode components cancel out when computing the differential control voltage. This greatly reduces leakage-induced phase shifts and enhances stability. Furthermore, ensuring that key switching devices remain in saturation minimizes charge sharing and improves linearity.

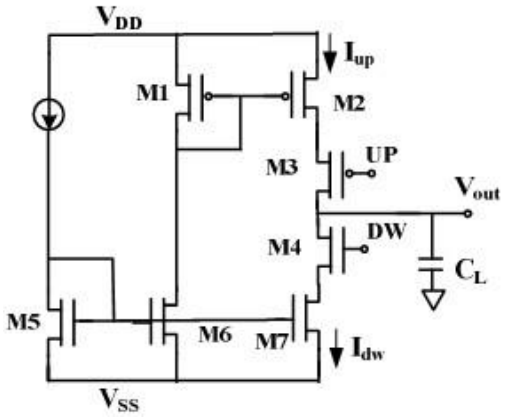


Figure 3. Schematic of basic charge pump

C Reference Voltage Circuit

Even in locked operation, the PFD generates narrow UP/DOWN pulses that impose small disturbances on the CP output. To suppress these perturbations, a reference-tracking circuit is incorporated. An operational amplifier generates a stable reference level and couples it to the differential outputs through a controlled matching network. Additional MOS devices isolate the reference node from back-injection, preventing unwanted current flow whenever the CP output rises above the reference level. A small capacitor at the reference point further enhances stability by filtering high-frequency fluctuations. As a result, the differential output remains substantially smoother and more resilient to switching noise.

The operation amplifier works as voltage follower to make the voltage V_{ref} approaching to V_{out}. The four transistors M17 to M20 and the capacitor consist of the reference voltage circuit as shown in the middle area.

Since the response characteristics of the operational amplifier and the effect of the point V_{ref} to the output voltage V_{out} interrupted the stability of output voltage of the charge pump. These four transistors avoided the point V_{out} sucking the current from V_{ref} via the operation amplifier if the voltage of V_{out} is higher than V_{ref}. Otherwise, the reverse circuits would be broken, and resulted in the output voltage changed by force. The capacitor is used to improve the stability of the reference voltage.

The control signals of M17 to M20 are identical to the signals applied to the main circuit. Moreover, the distribution of the four signals to the transistors should meet the requirement of which the current I_{up} or I_{dw} can flow in the circuit formed by M17 and M20, or M19 and M19. The voltage output of the charge pump should keep stable when reference voltage circuit applied due to the two input signals f_{ref} and f_{div} are equal.

D. Power Consumption and Speed Consideration

Several transistor-level optimizations are applied to support high-speed operation without increasing power consumption. Placing the switching elements at the source side of the current sources reduces charge injection effects and accelerates transition times. Additional pre-charge transistors improve the current waveform's shape and maintain linearity across a wide output range. Collectively, these techniques yield faster settling behavior and reduced

power dissipation. As to the circuit consists of M7 and M10, would precharge to the M11 and M6, so the waveform of current of I2 and I6 were improved, and the linearity of the output Vo1 and Vo2 was optimized. Therefore the high speed charge pump with wider swing range and stable output voltage were obtained.

IV. RESULT ANALYSIS AND CONCLUSION

The proposed architecture was evaluated using a 0.35-µm CMOS process with a 3.3-V supply. Simulations confirm that the charge pump maintains an almost constant current across an output range of approximately 1 V to 3 V. Current mismatch remains below 0.3%, even under worst-case conditions—significantly outperforming conventional designs. Time-domain simulations show a clean output waveform with greatly suppressed ripple and no visible spurious jumps, indicating strong immunity to switching disturbances. The design achieves an output swing from near ground to approximately 3.1 V, making it well suited for wide-tuning-range VCOs in high-frequency PLLs.

Overall, the differential architecture combined with reference-based stabilization delivers excellent current matching, reduced noise sensitivity, improved linearity, and superior stability. These features make it an attractive solution for high-speed, low-power PLL applications.

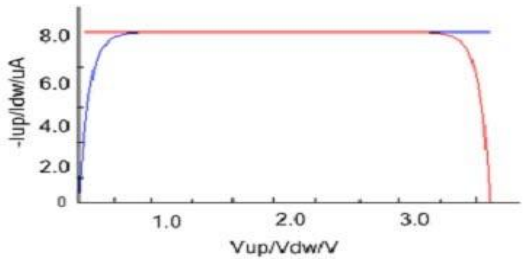
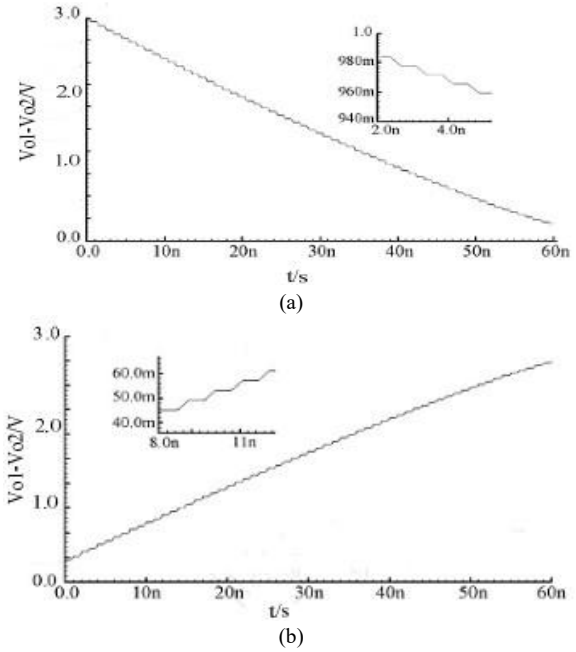


Figure 6. The relationship of the output voltage and the current of charge and discharge of the charge pump.



(a) Output voltage of charge, (b) Output of discharge

Figure 7. The variation of the output voltage with the timing

The range of output of this charge pump is about zero to 3.1V, and the wider swing of output voltage is available under 3.3V power supply. These characteristics could meet the requirement of the high speed PLL application.

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