Title: Mismatch-Resilient, Glitch-Suppressed CMOS Charge Pump for GHz PLLs in 45 nm

Abstract:
This project proposes a high-speed, low-power CMOS charge pump (CP) for phase-locked loops (PLLs) operating in the multi-GHz regime. The design explicitly targets three longstanding bottlenecks—current mismatch, switching-induced glitches, and propagation delay—by combining a low-glitch switch-based primary CP with a fast current-steering assist path that accelerates charging/discharging only when needed. The assist is realized with compact current-mode logic style devices to preserve speed without significant static overhead, while careful device sizing and biasing maintain current matching across PVT. Building on feasibility demonstrated at 10 GHz in 45 nm with 1.0 V supply—including near-rail output swing (~0–0.98 V), sub-20 ps delay, and ~13 µW power—the project sets similar or tighter targets and validates them in Cadence Virtuoso/SpectreRF using a behavioral PLL bench. Evaluation includes transient lock-in, ripple/spur proxies, SpectreRF PSS/Pnoise for CP-induced noise, full corner (TT/FF/SS/SF/FS) sweeps, and 200-run Monte-Carlo for mismatch, followed by post-layout RC-extracted verification. Expected outcomes are (i) reduced up/down current mismatch to limit spurs, (ii) minimized output glitches during UP/DN transitions, (iii) fast, stable control-voltage dynamics enabling reliable GHz-range locking, and (iv) demonstrated robustness over supply and temperature. The resulting CP is intended as a drop-in for integer-N or fractional-N PLLs targeting clocking and RF frequency-synthesis in deeply-scaled CMOS.

Keywords (6): Charge Pump; Phase-Locked Loop; Current Matching; Glitch Suppression; PVT/Monte-Carlo; SpectreRF