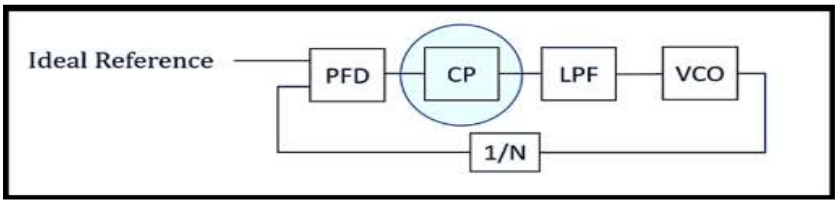
PLL

PLL is closed loop negative feedback system which maintains same phase as the reference signal.

It is used in signal synchronization, communication systems.



Use of Charge Pump

It is a type of DC-DC converter which uses capacitors to store charge through which it either raises or lowers the voltage levels

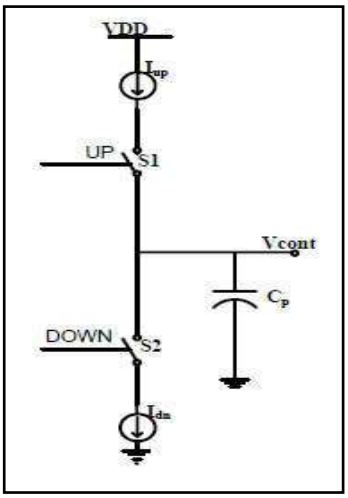
Charge Pumps are very important components in the PLL (Phase Lock Loop).

It is used in PLL to convert the error signal generated by the PFD (Phase Frequency Detector) to it's equivalent Control voltage which controls the frequency of the VCO.

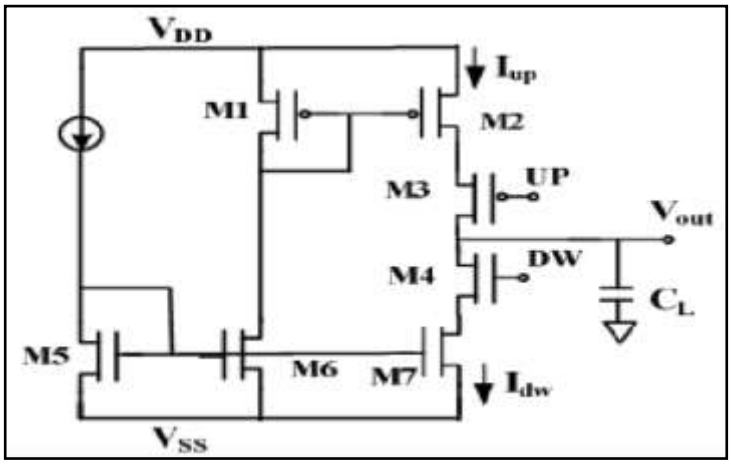
Working of CP

A Charge Pump converts the digital UP and DOWN control signals (generated by the Phase-Frequency Detector) into analog currents. These currents are then integrated by the Loop Filter to generate the control voltage for the VCO.

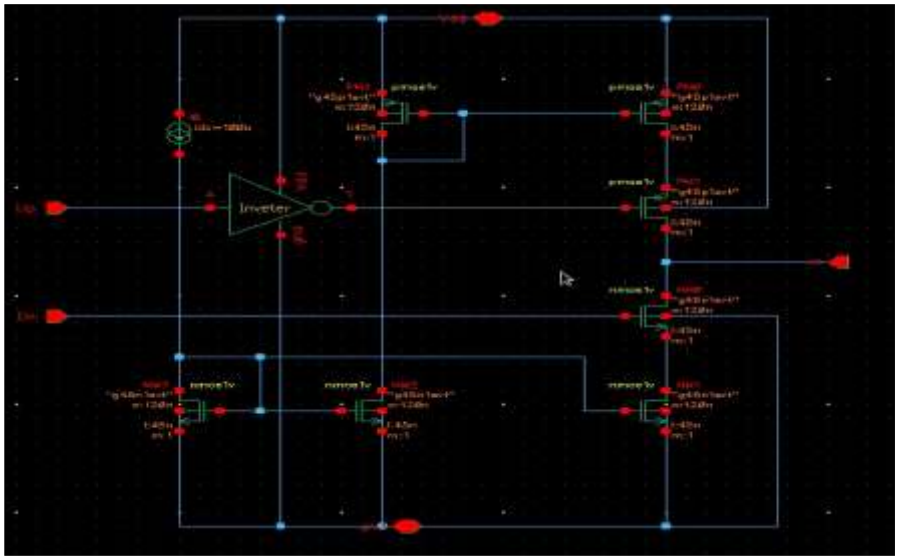
Basic CP architecture



CMOS Current Mirror CP



Schematic



Charge-Pump Design Steps

Stage-1: Build Build

1. Set Icp: I_{CP}(100 µA), target V_{OV}≈0.12 V for mirrors.
2. Match Transistors: size DN NMOS to sink I_{CP}; size UP PMOS ≈1.8–2× NMOS width so $I_{UP} = I_{DN}$.
3. Cascodes (fixed-bias): add simple cascodes above/below mirrors to raise r_o.

Stage-2: Values refinement

4. Lengthen mirrors: L=0.10–0.12 µm for increased current driving ability. scale W to keep I_{CP}.
5. Re-trim Icp: if current shifted, scale all mirror widths by a single factor.

Stage-3: Tiny optimization (optional)

6. Series-R @ V_{CTRL}: ~150 Ω (sweep 100–300 Ω) to cut kick/ripple;
7. Bleed (1–2 µA) PMOS diode to reduce dead-zone;
8. Dummies (0.5×) pass FETs with complementary gate to cancel charge injection.

Targets to be achieved:

ΔI/I ≤ ~1–1.5% over V_{CTRL}.

Ripple ≲ ~5 $mV_{pp.}$

similar UP/DN delays (UP branch delay ≈ DOWN branch delay).

References

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3. Su, D.; Pamarti, S. “Mismatch-Shaping Techniques to Linearize Charge-Pump Errors in Fractional-N PLLs,” *IEEE TCAS-I*, 2010 — key treatment of CP mismatch & spur mitigation (background/theory).
4. Noh, J.; Jeong, D. “Charge Pump with a Regulated-Cascode Circuit for Reducing Current Mismatch in PLLs,” *ISCAS* — canonical RGC CP idea (motivates why longer-L/ro helps).
5. Wang, Y. et al. “A Wideband Low-Reference-Spur PLL with Clock-Feedthrough-Suppressed Charge Pump,” *Electronics*, 2023 — practical low-glitch CP switching tricks (timing/feedthrough).