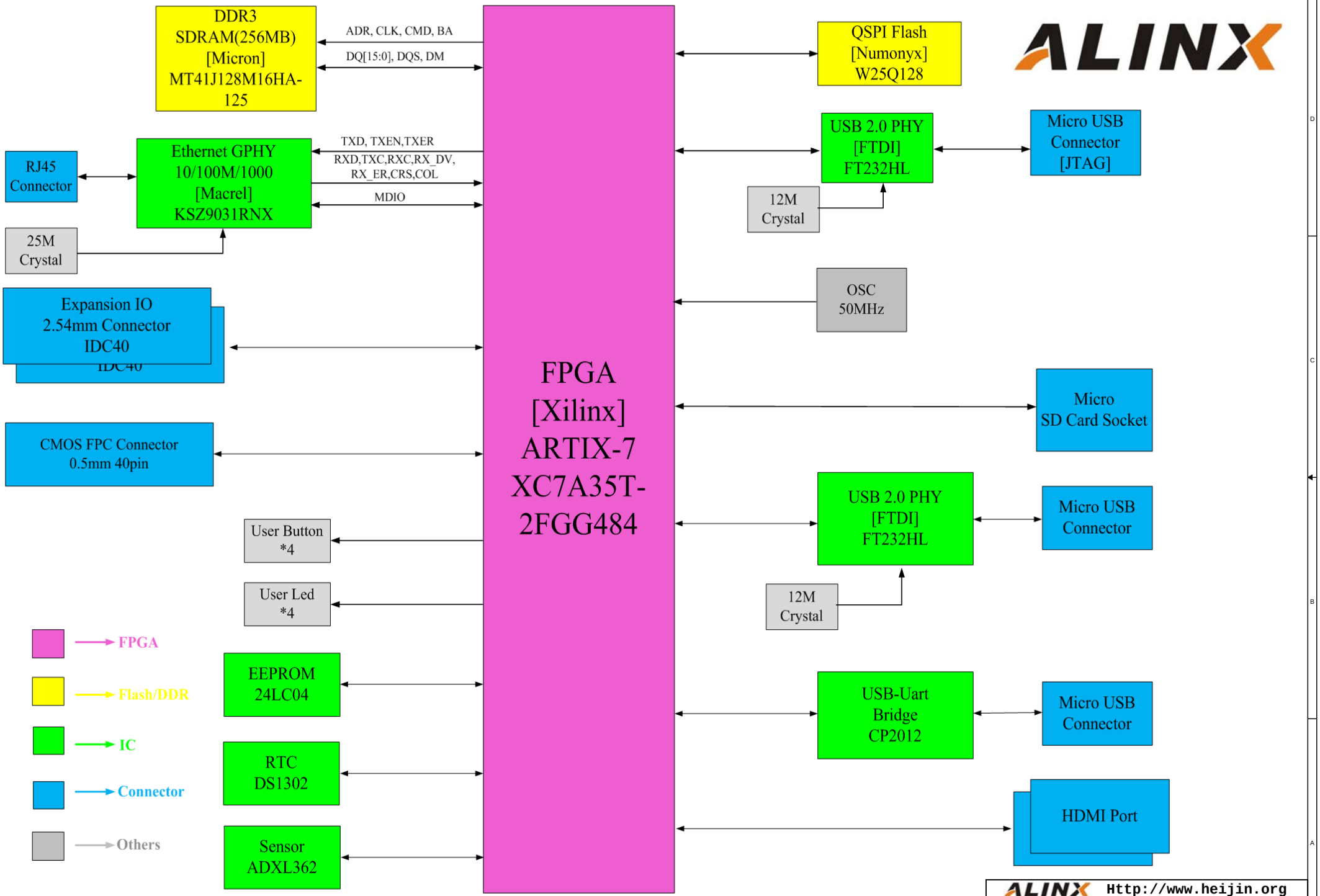

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Title	PAGE01 Block diagram	
Size	Document Number: AX7035 开发板原理图	Rev: 1.0
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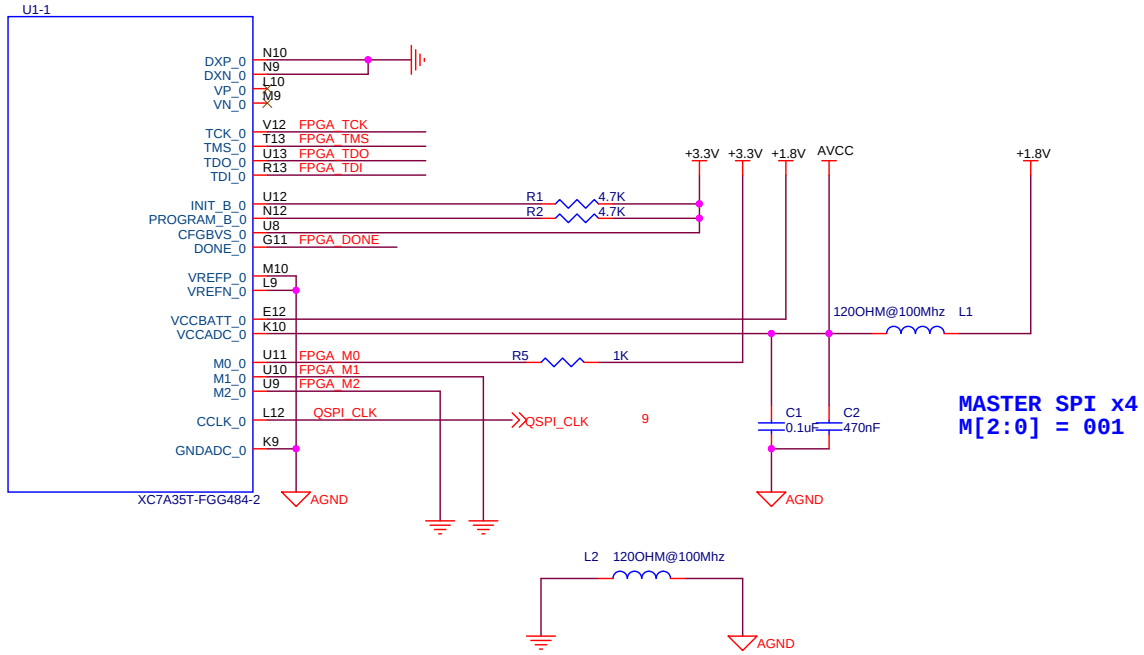
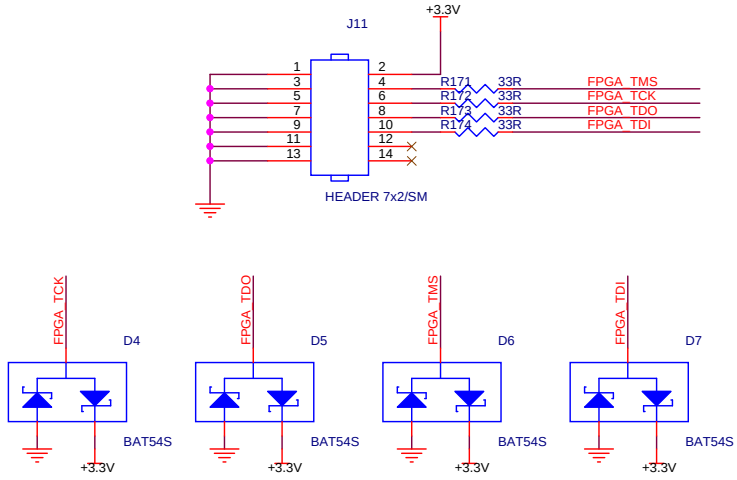
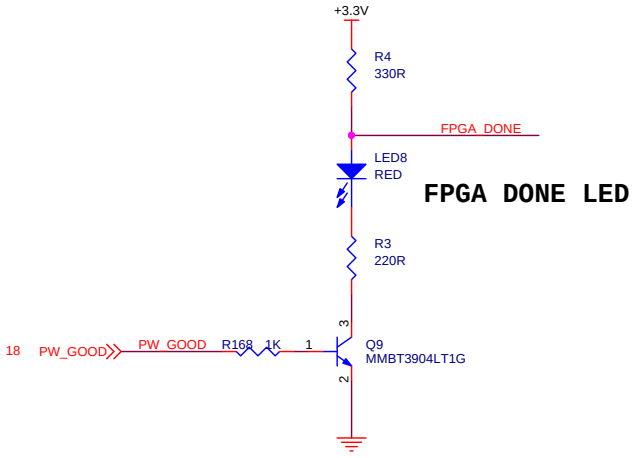


JTAG Connector



Power LED



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Title: PAGE02 ARTIX7 Bank0 & JTAG		
Size	Document Number: AX7035 开发板原理图	Rev: 1.0
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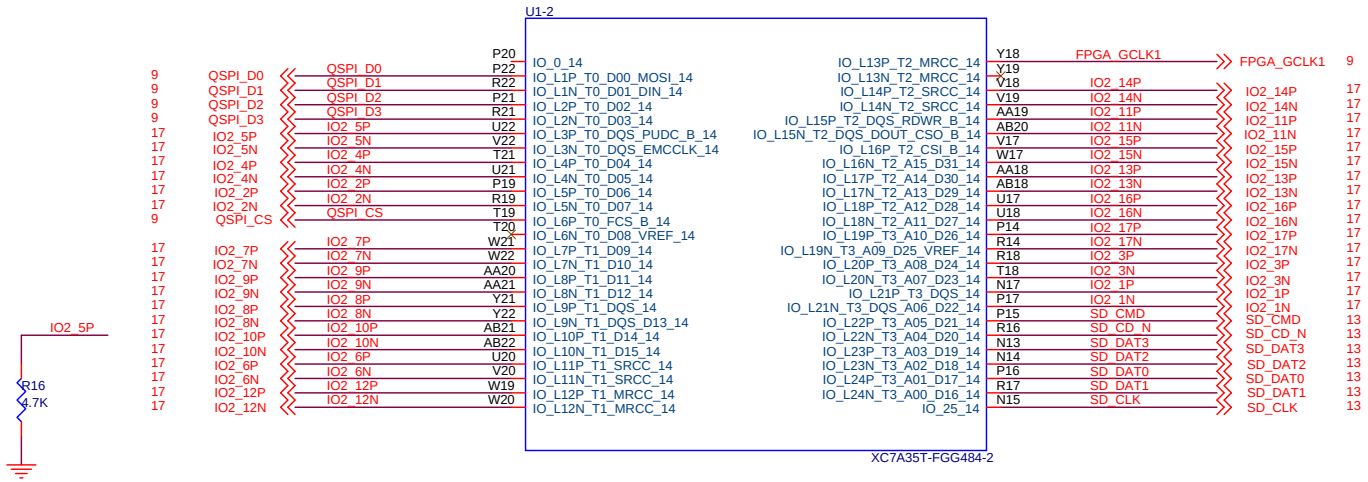

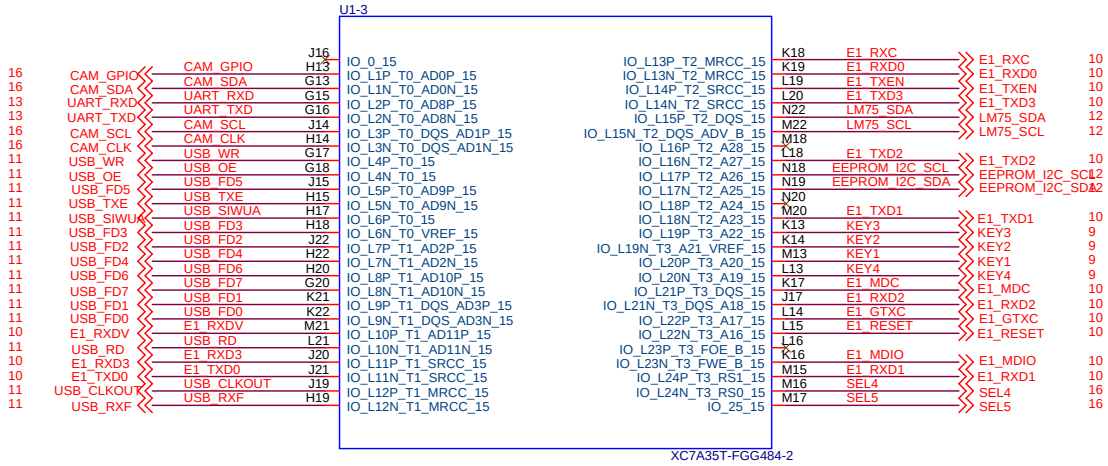

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ALINX	Http://www.heijin.org	
Title: PAGE03 ARTIX7 Bank14 & Bank15		
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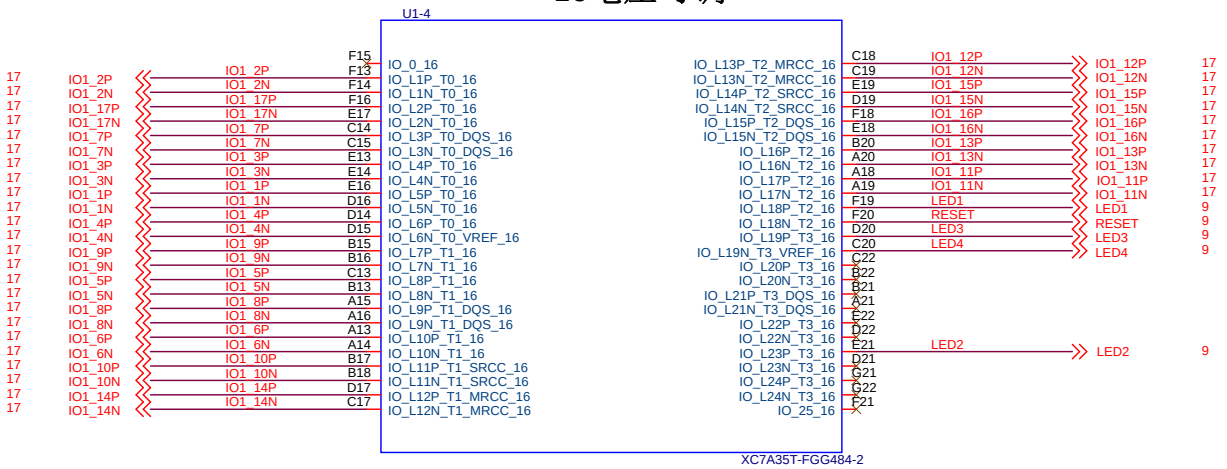
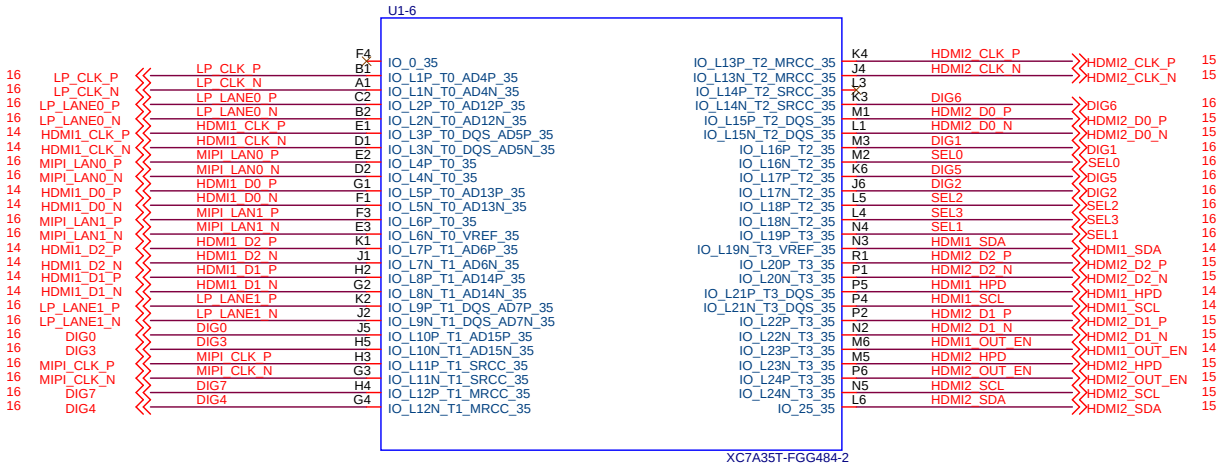
IO电压可调





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Title: PAGE04 ARTIX7 Bank16 & Bank35

Size	Document Number	Rev
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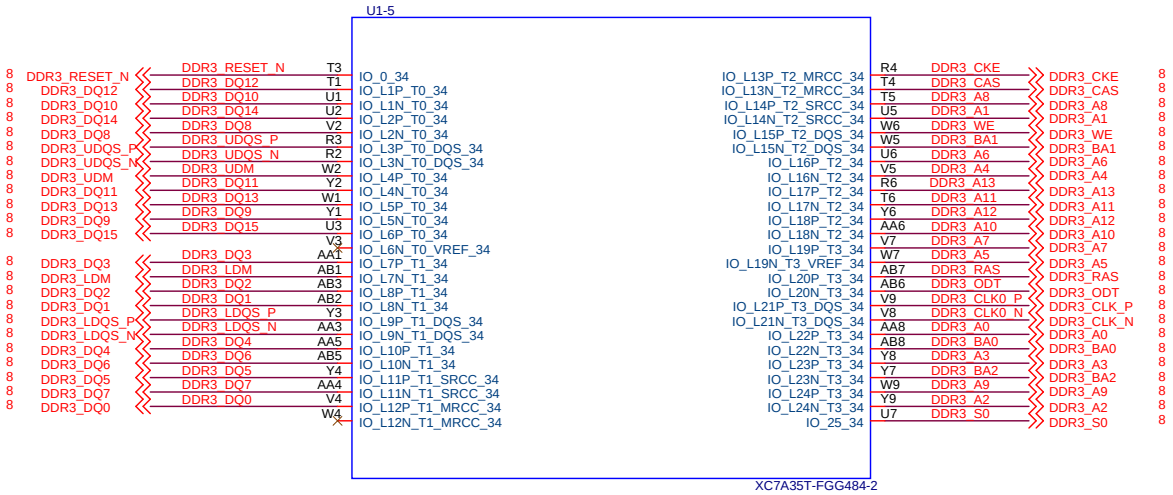
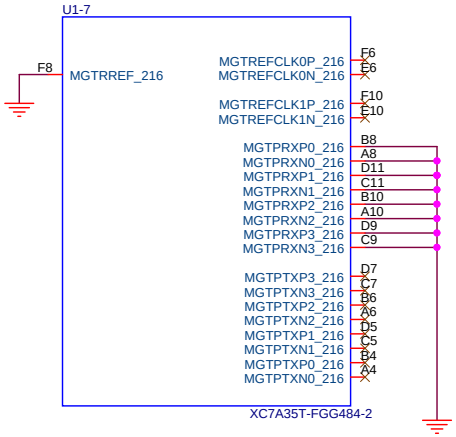
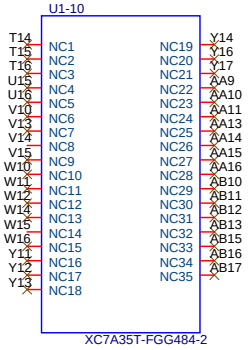
Internal VREF is used in this example



ALINX Http://www.heijin.org

Title	PAGE05 ARTIX7 Bank 34	
Size	Document Number: AX7035 开发板原理图	Rev: 1.0
Date: Friday, April 13, 2018	Sheet 5 of 18	





ALINX Http://www.heijin.org

Title: PAGE06 ARTIX7 Bank216

Size | Document Number: AX7035 开发板原理图 | Rev: 1.0

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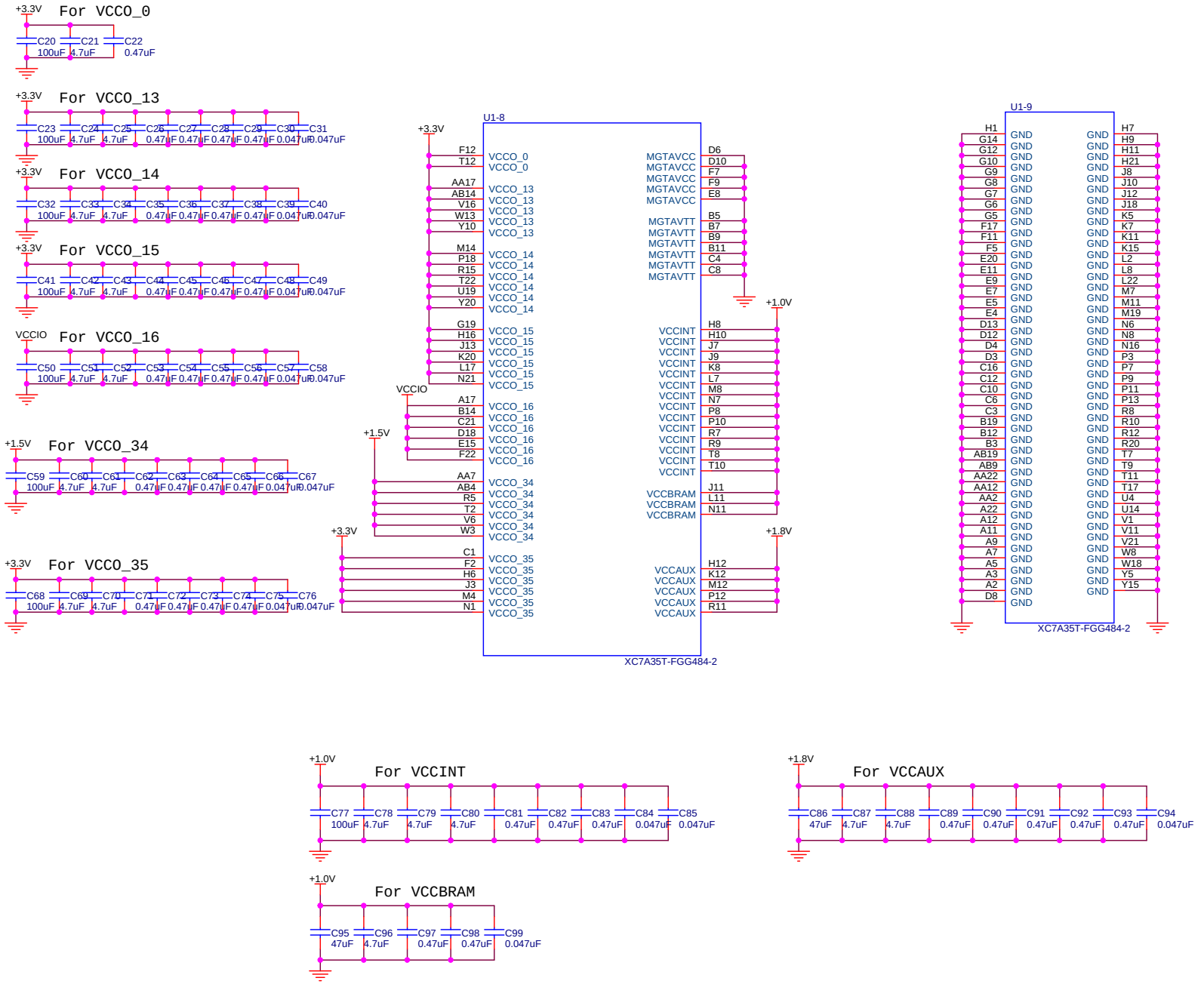

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Title: PAGE07 ARTIX7 Power

Size	Document Number	Rev
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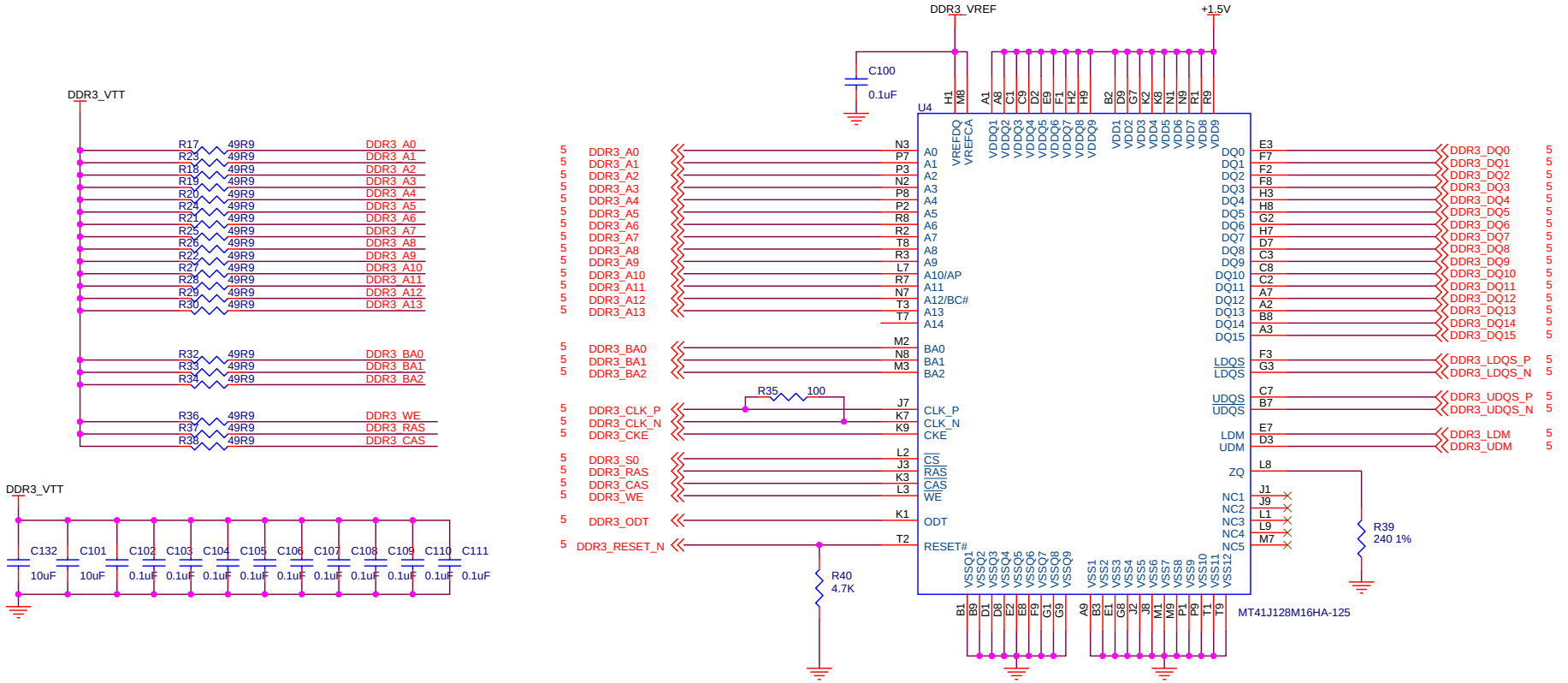

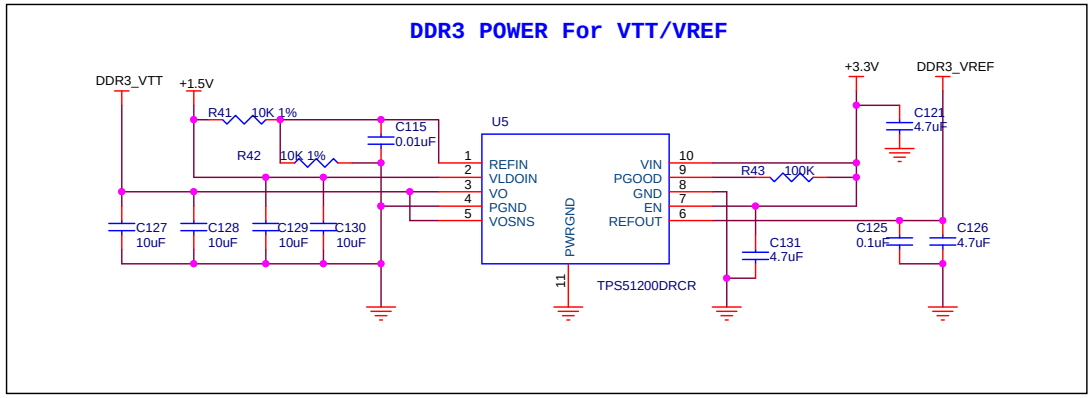

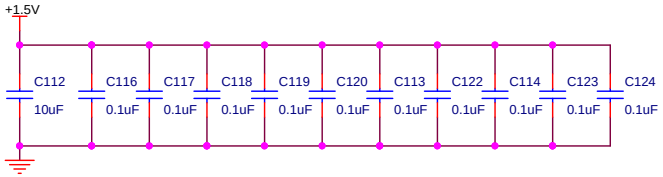

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ALINX	Http://www.heijin.org	
Title: PAGE08 DDR3		
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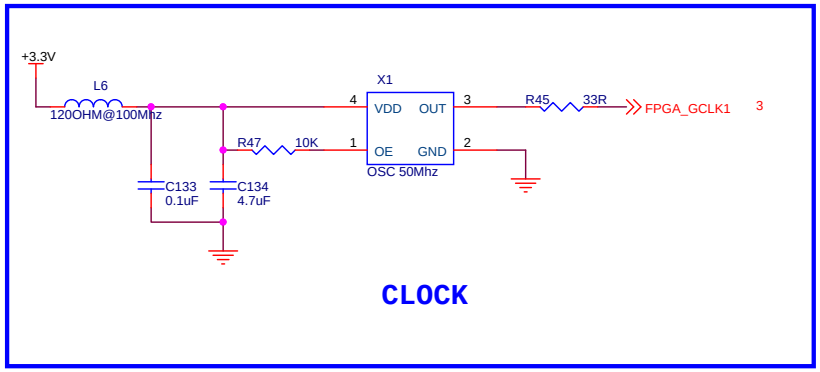

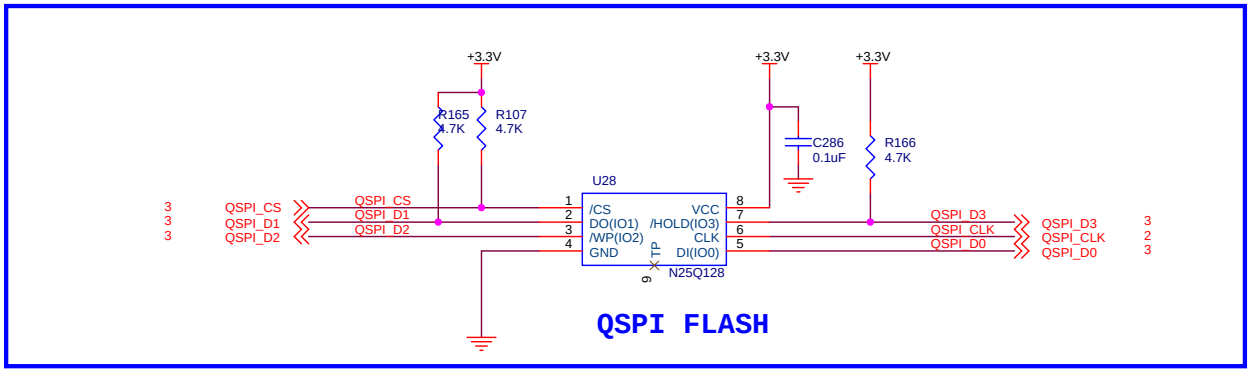

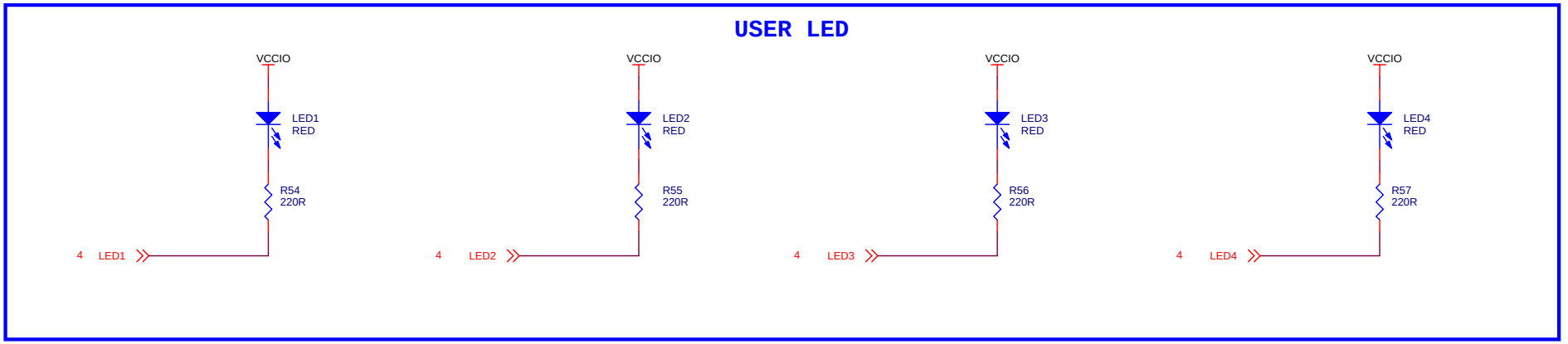

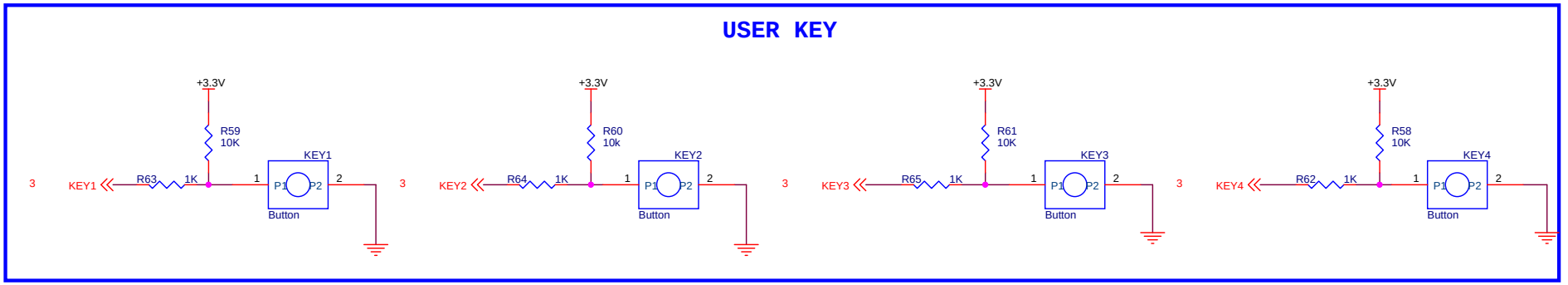

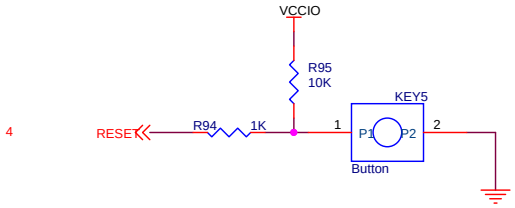

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ALINX	Http://www.heijin.org	
Title: PAGE09 Flash, Clock, JTAG		
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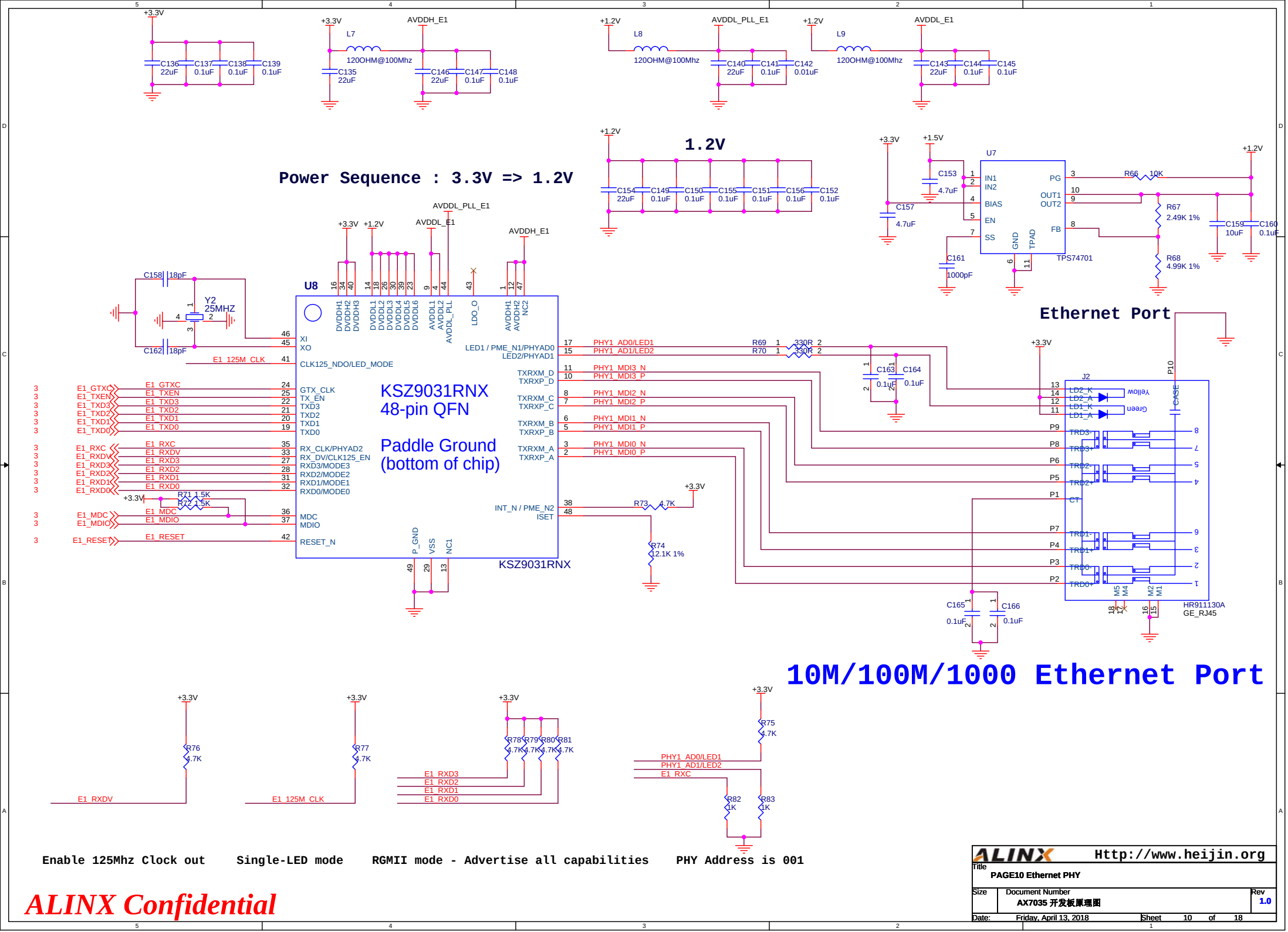
Power Sequence : 3.3V => 1.2V
1.2V
Ethernet Port
KSZ9031RNX
48-pin QFN
Paddle Ground
(bottom of chip)
KSZ9031RNX
10M/100M/1000 Ethernet Port
TPS74701
HR911130A
GE_RJ45
Enable 125Mhz Clock out
Single-LED mode
RGMII mode - Advertise all capabilities
PHY Address is 001
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ALINX
Http://www.heijin.org
PAGE10 Ethernet PHY
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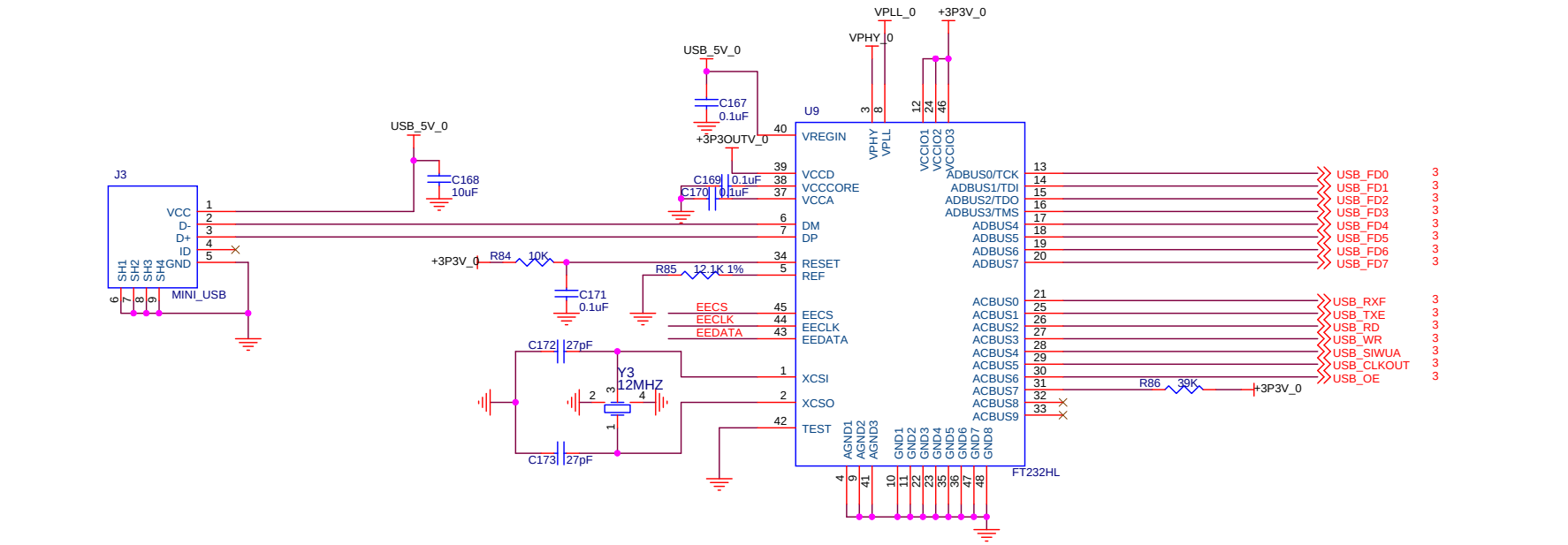

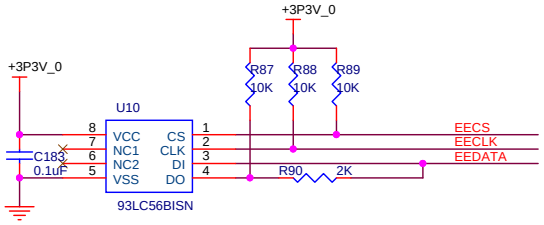

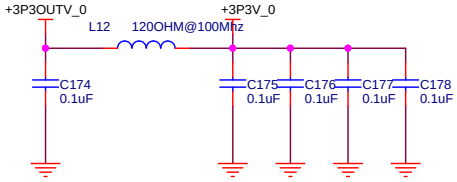

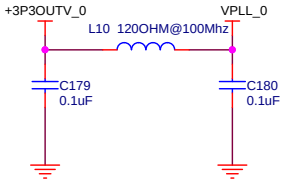

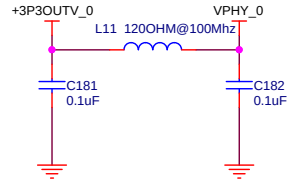

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Title: PAGE11 USB 2.0		
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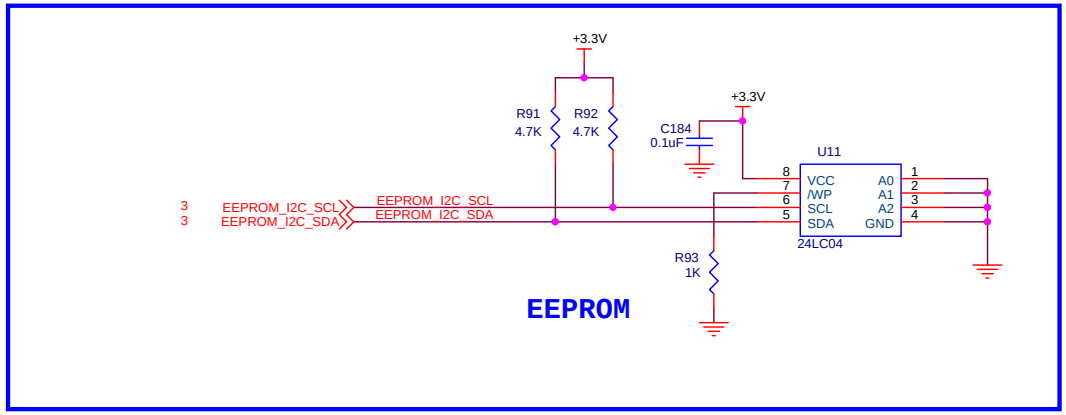

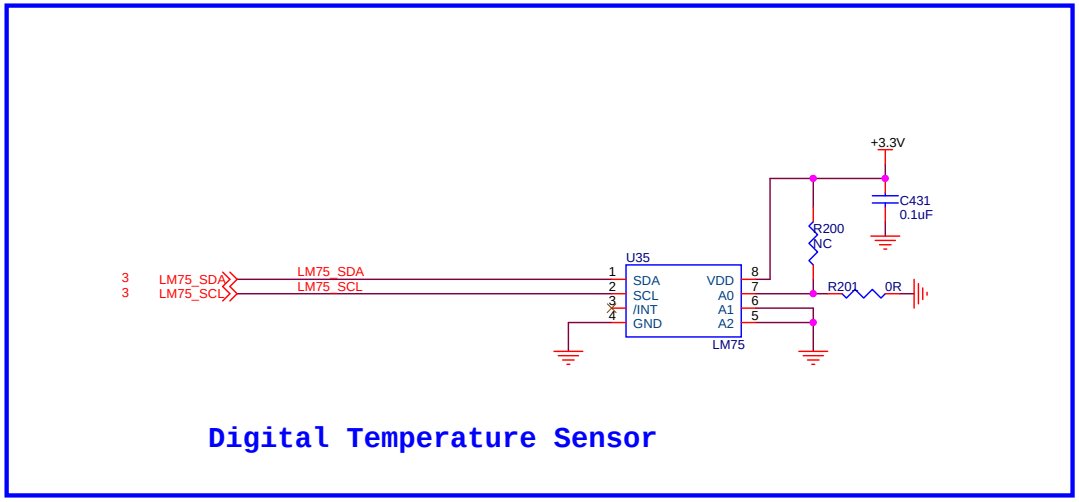

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Title	PAGE12 Temperature Sensor, EEPROM	
Size	Document Number: AX7035 开发板原理图	Rev: 1.0
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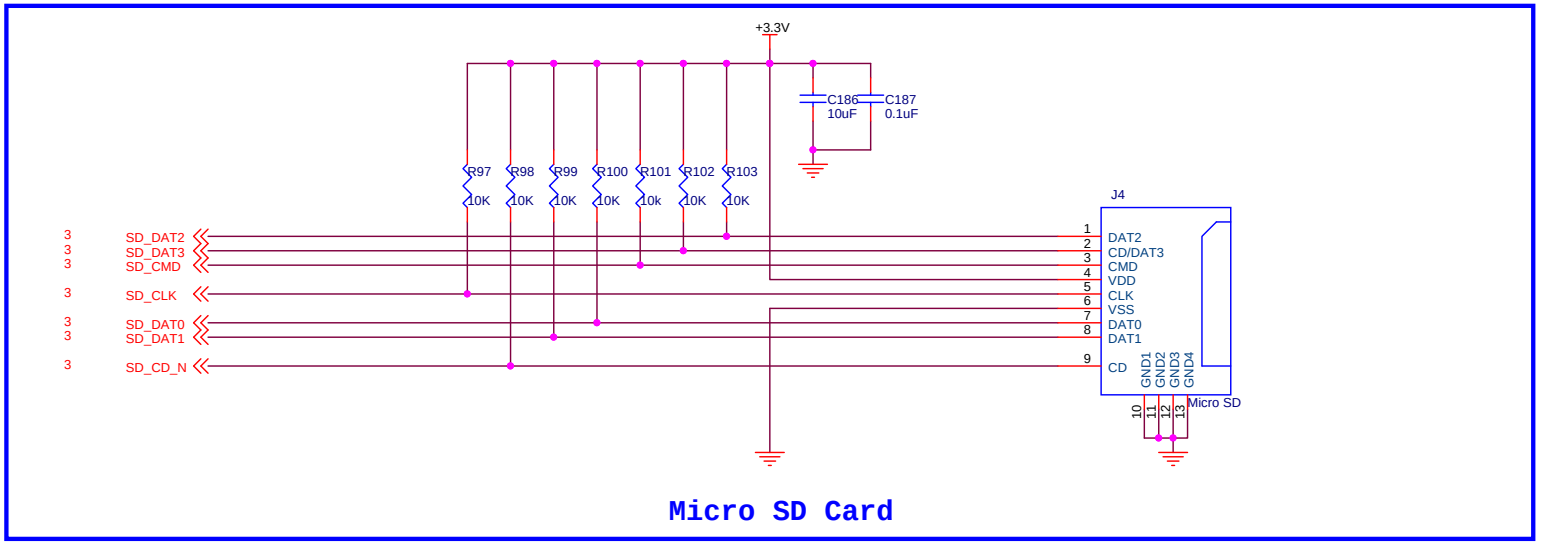
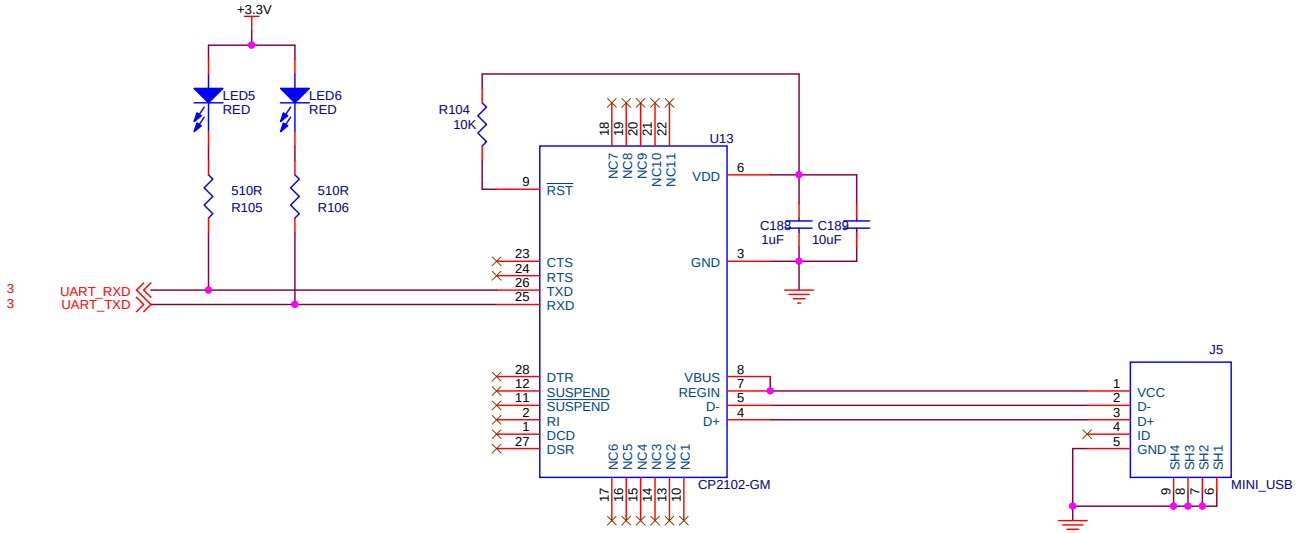


Micro SD Card



USB Uart

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Title	PAGE13 USB_UART, SD	
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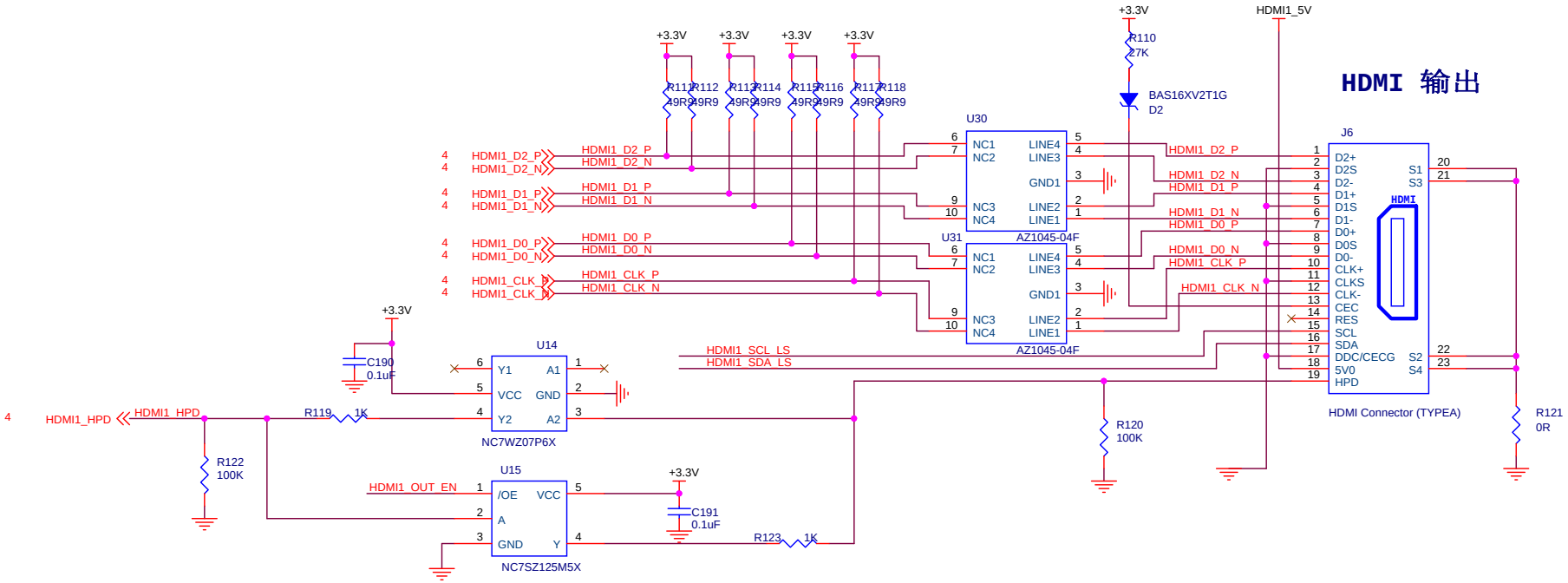

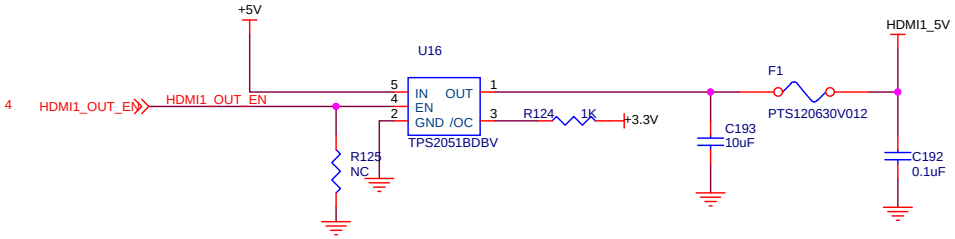

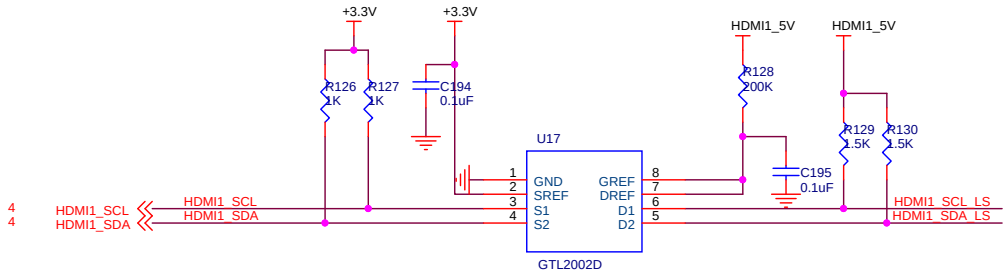

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ALINX	Http://www.heijin.org	
Title: PAGE14 HDMI1		
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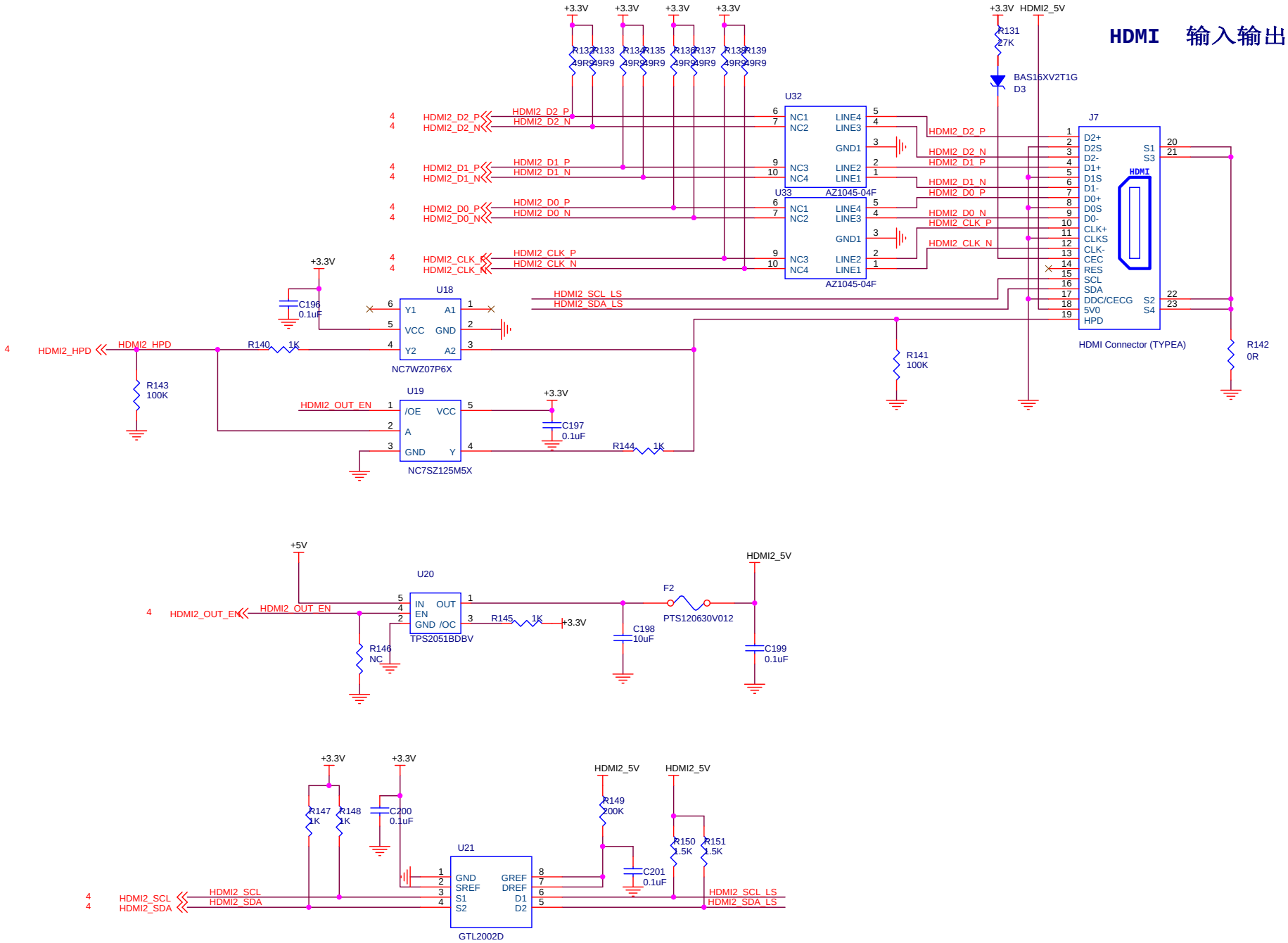

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ALINX	Http://www.heijin.org
Title	PAGE15 HDMI2
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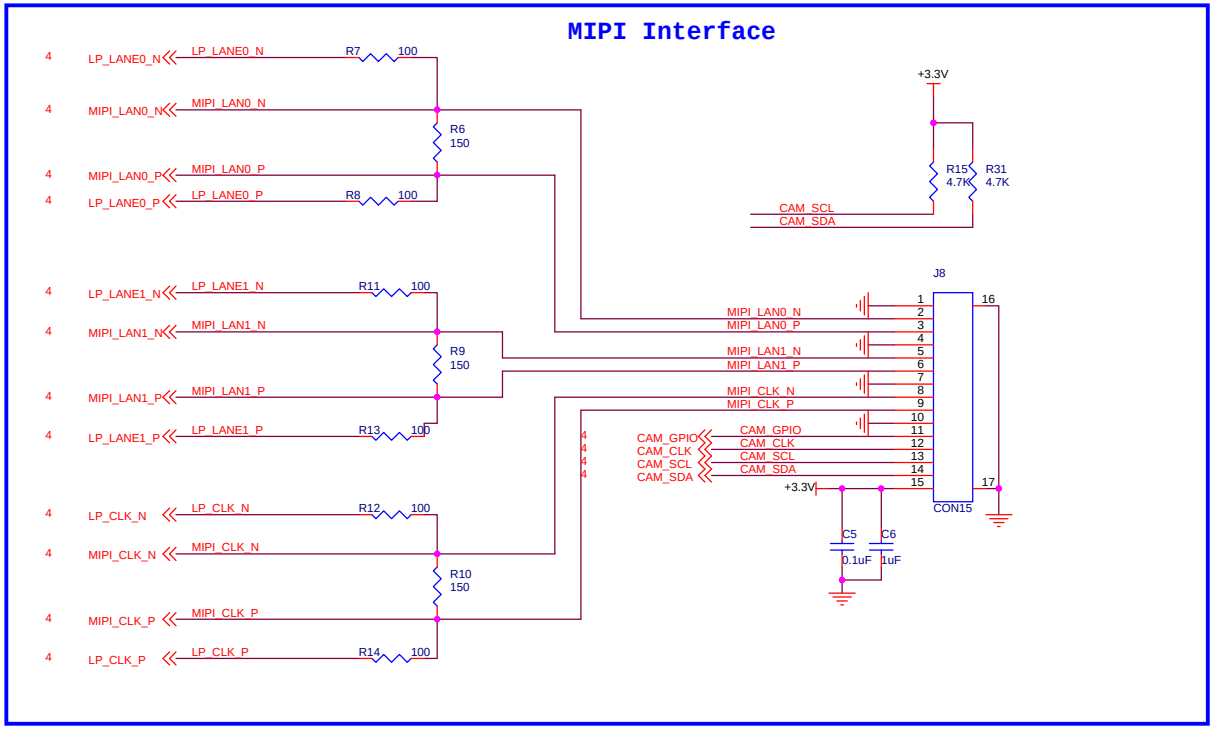
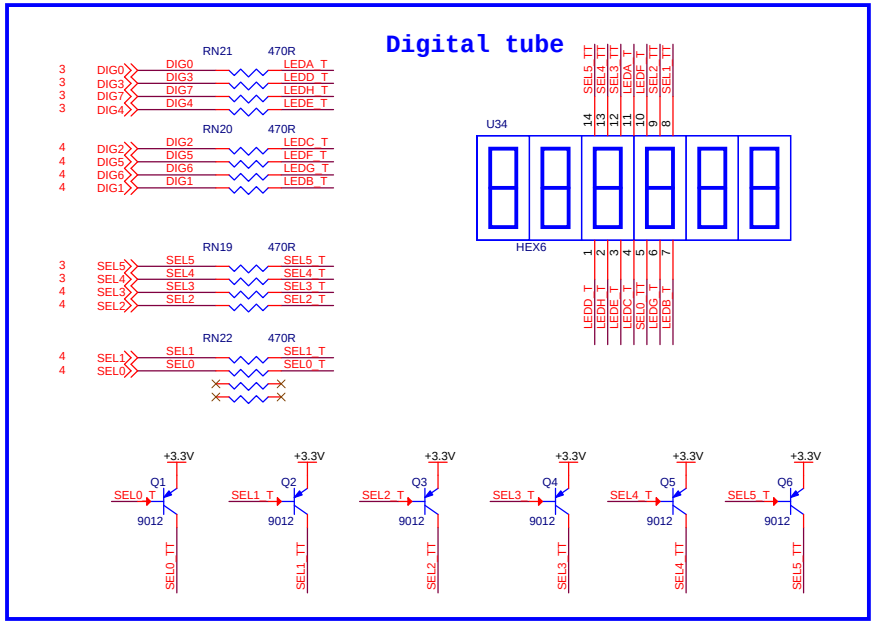
MIPI Interface



Digital tube



ALINX Http://www.heijin.org

Title	PAGE16 CMOS & DIG	
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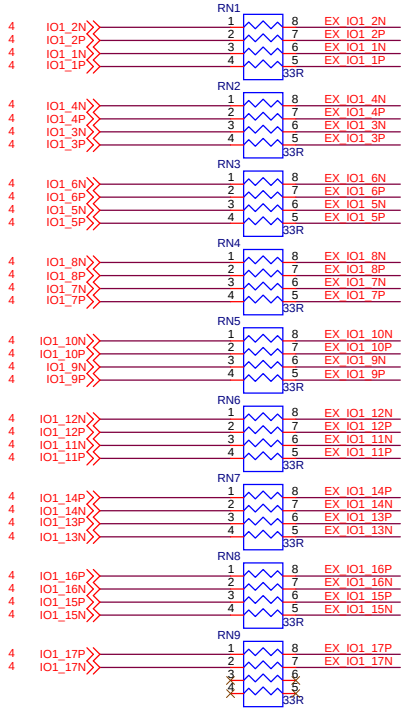
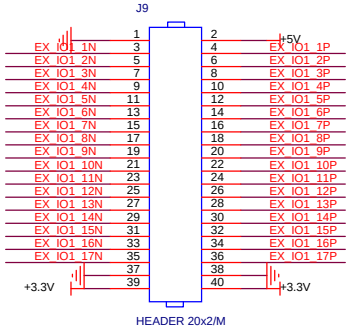
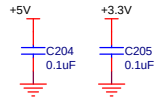
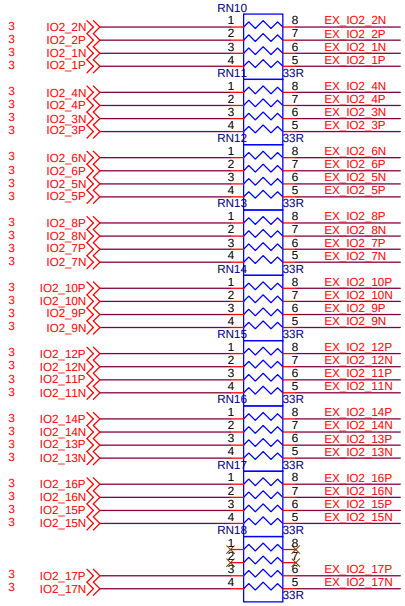


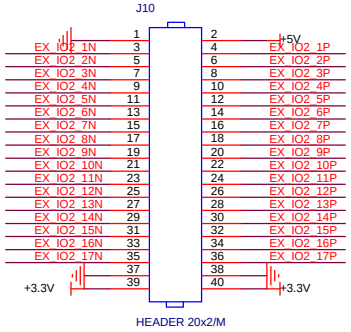
FPGA 40 PIN External IO

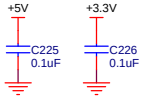






FPGA 40 PIN External IO





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Title	PAGE17 Connectors GPIO	
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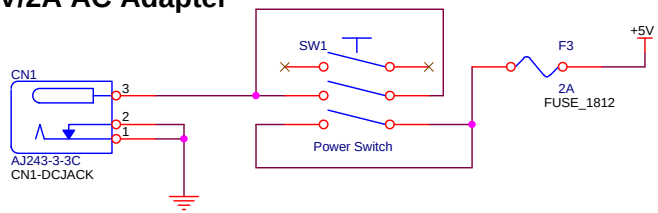
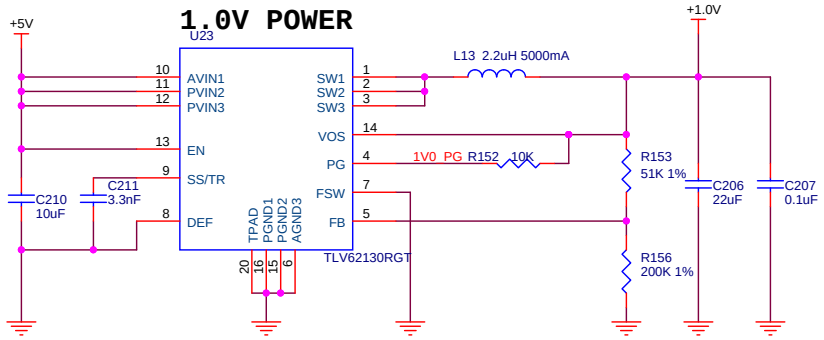
5V/2A AC Adapter

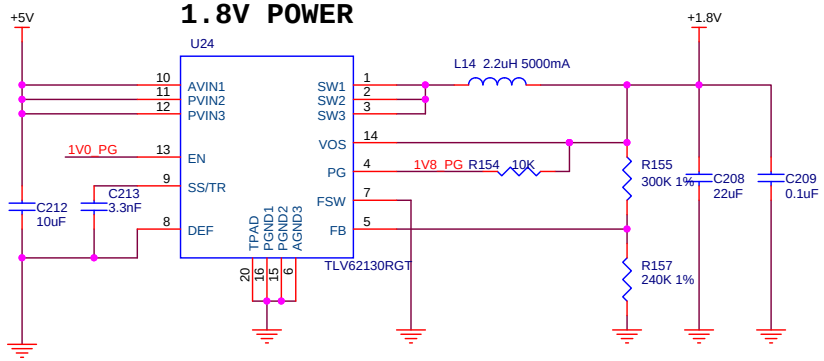


POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)

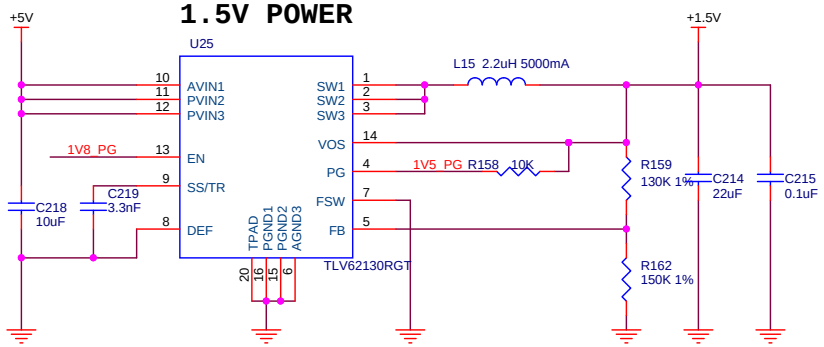
1.0V POWER



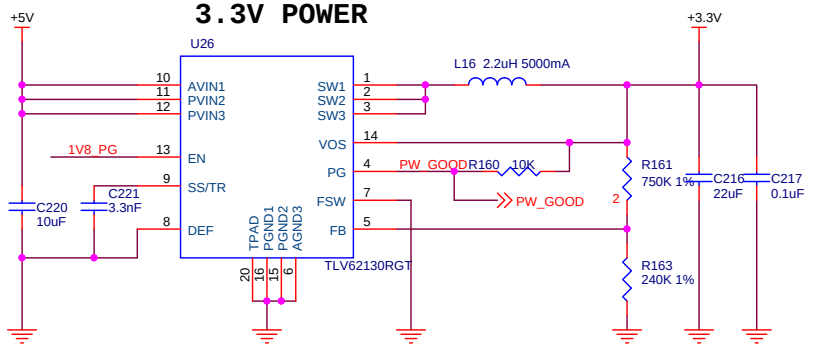
1.8V POWER

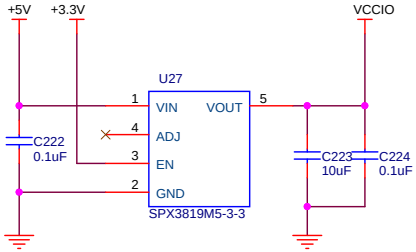


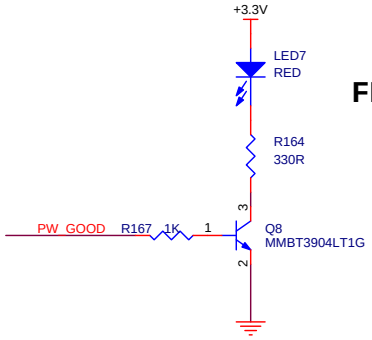
1.5V POWER



3.3V POWER







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