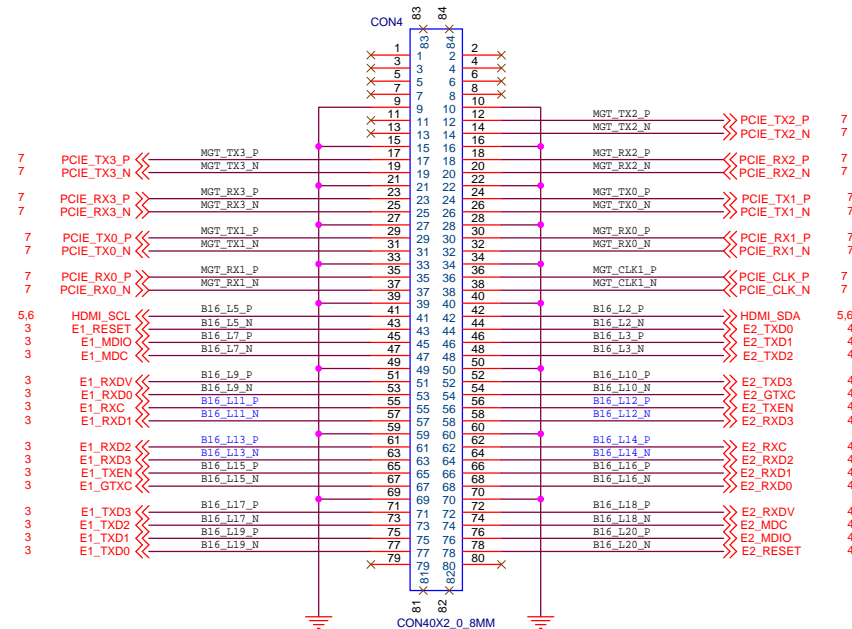
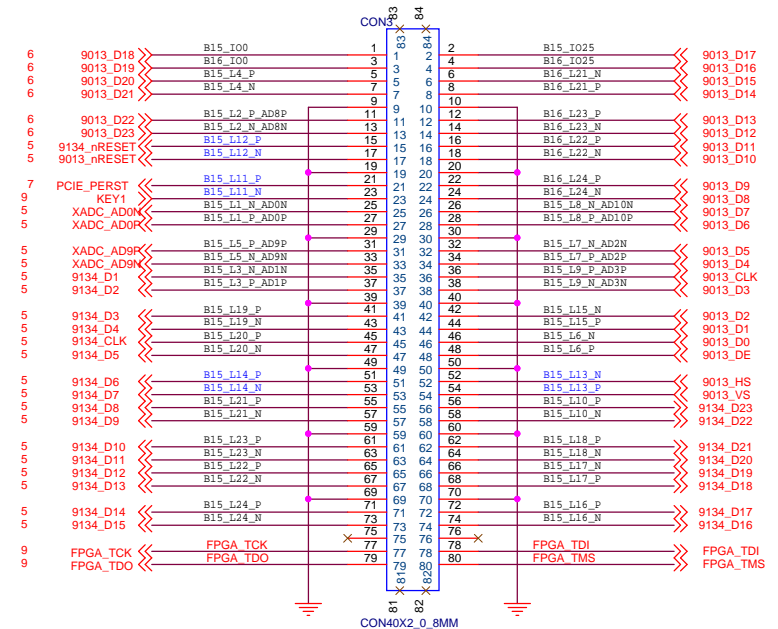
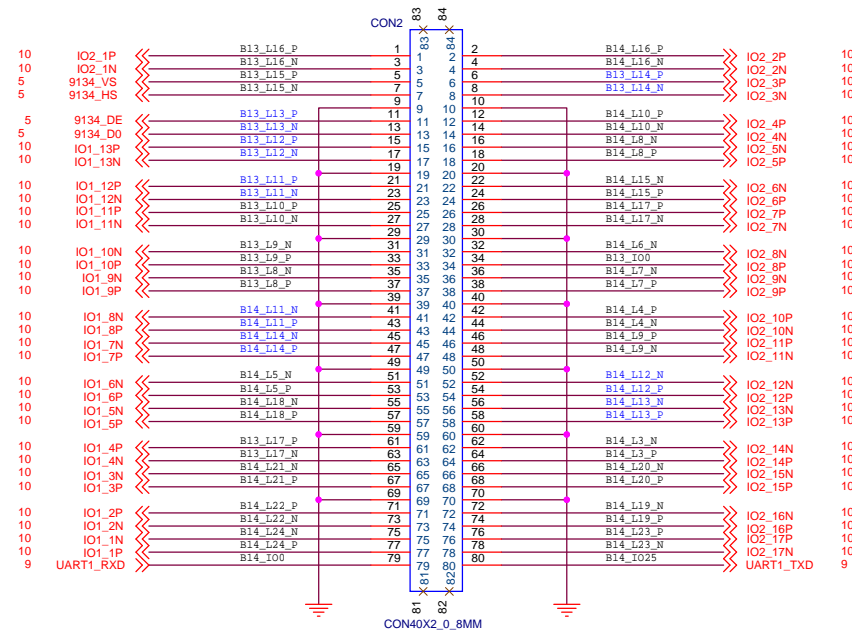
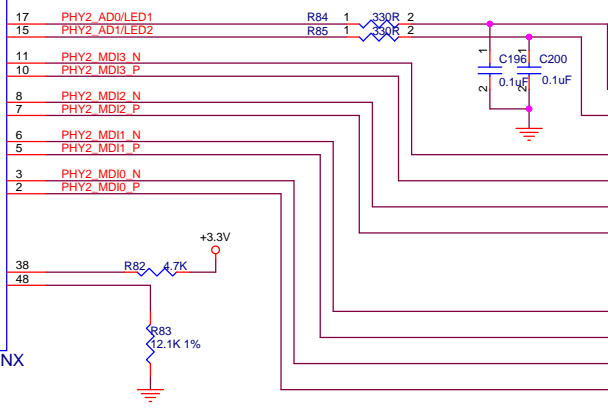
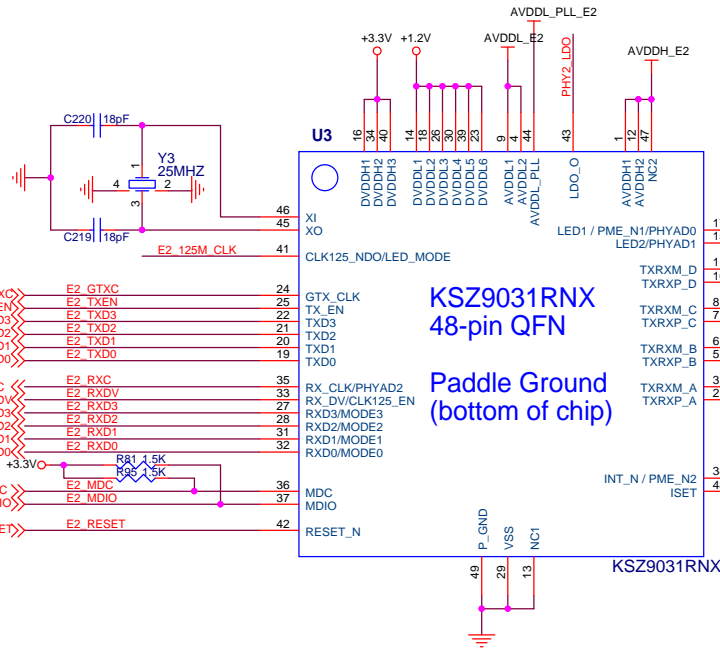
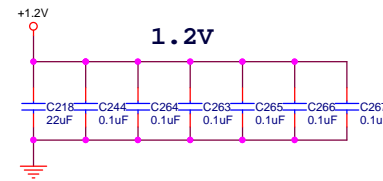
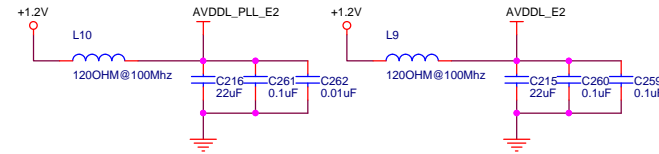
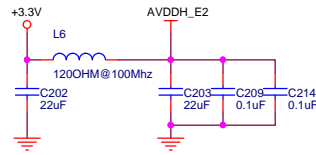
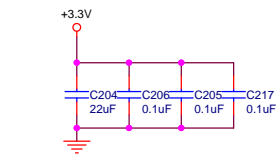


Diagram illustrating the pinout of the CON40X2_0_8MM connector. The connector has 40 pins, numbered 1 through 40. The pins are organized into two rows of 20 pins each. The top row (pins 1-20) is connected to +5.0V, and the bottom row (pins 21-40) is connected to ground. The diagram shows the internal connections of the connector, including the B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32, B33, B34, B35, B36, B37, B38, B39, B40 pins. The diagram is labeled CON40X2_0_8MM.





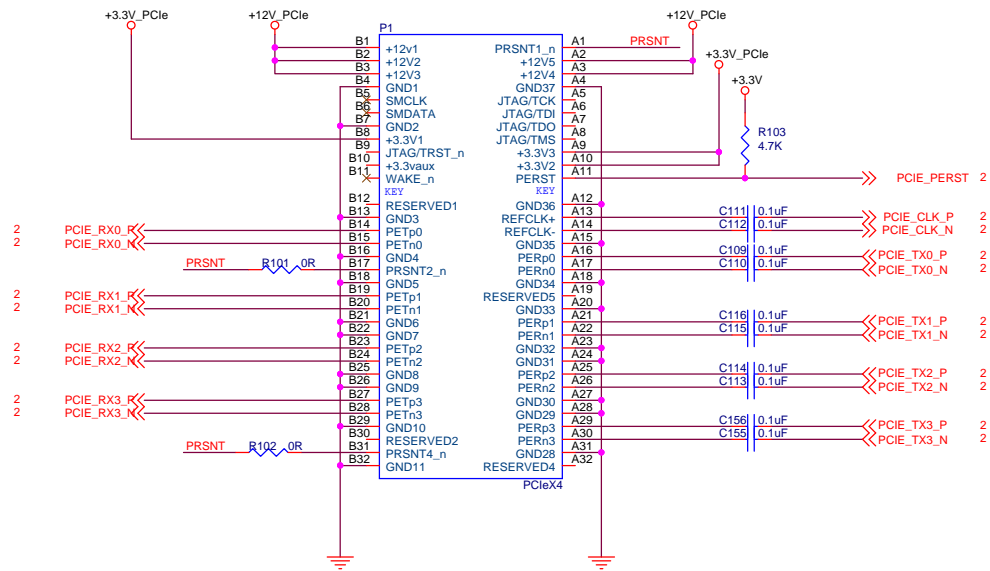
Ethernet Port

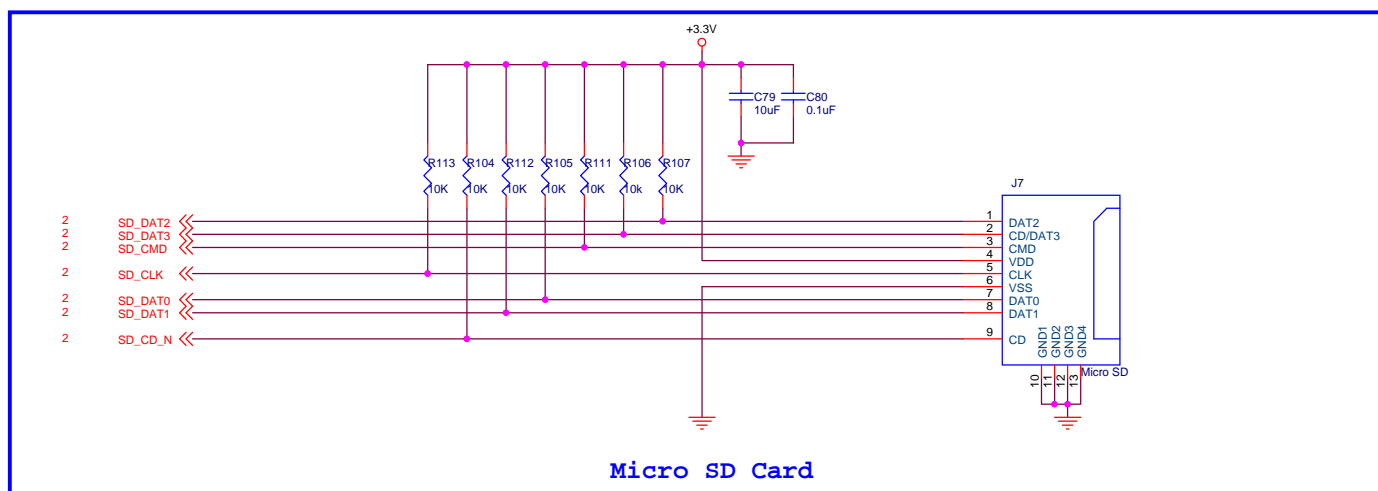
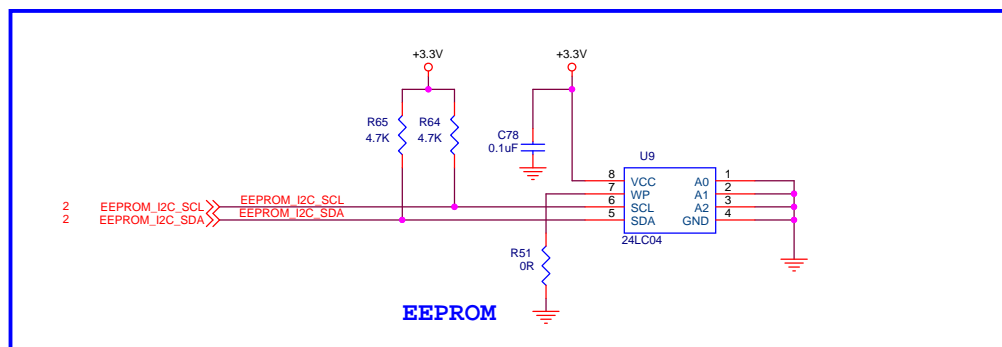
10M/100M/1000 Ethernet Port

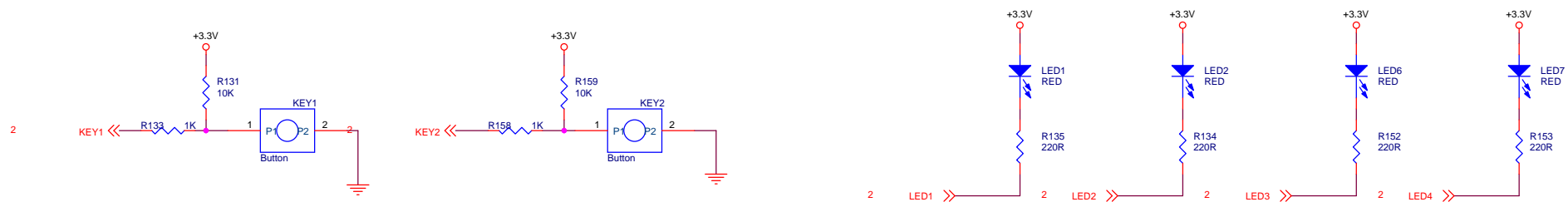
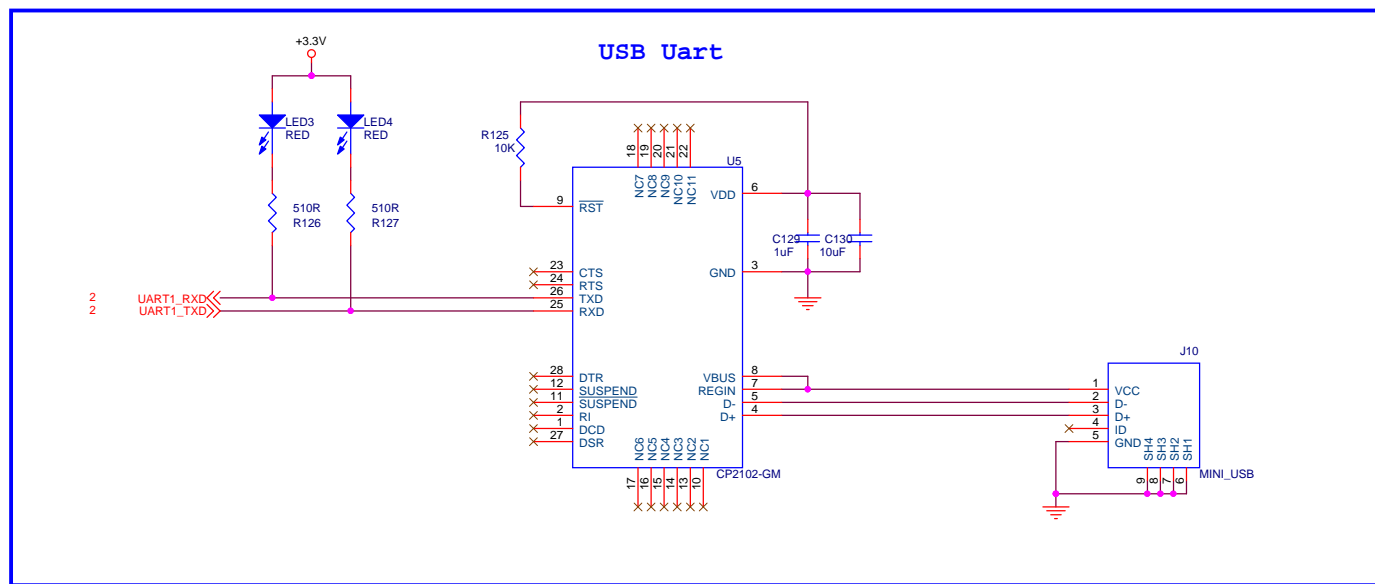
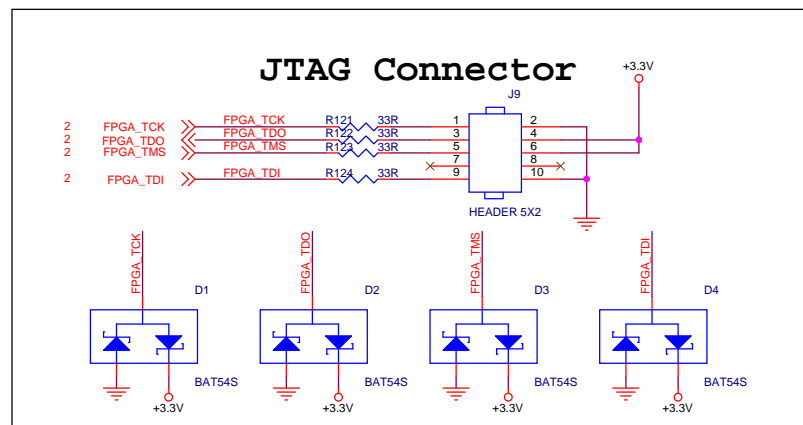
Enable 125Mhz Clock out Single-LED mode GMII mode - Advertise all capabilities PHY Address is 001

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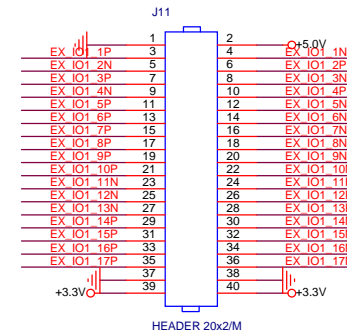
PCIE X4 SLOT



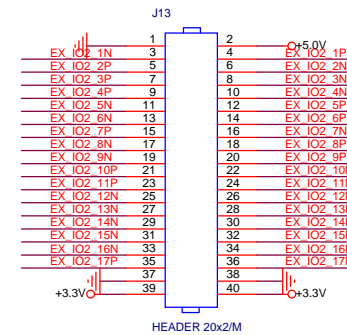




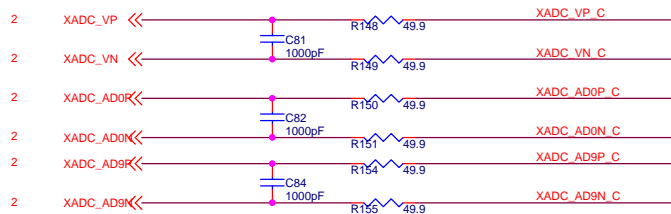
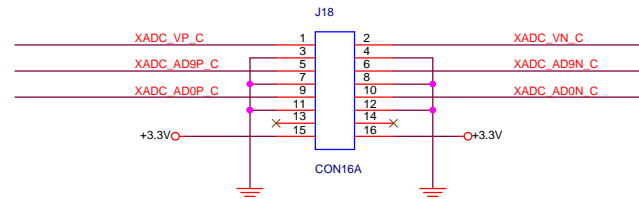
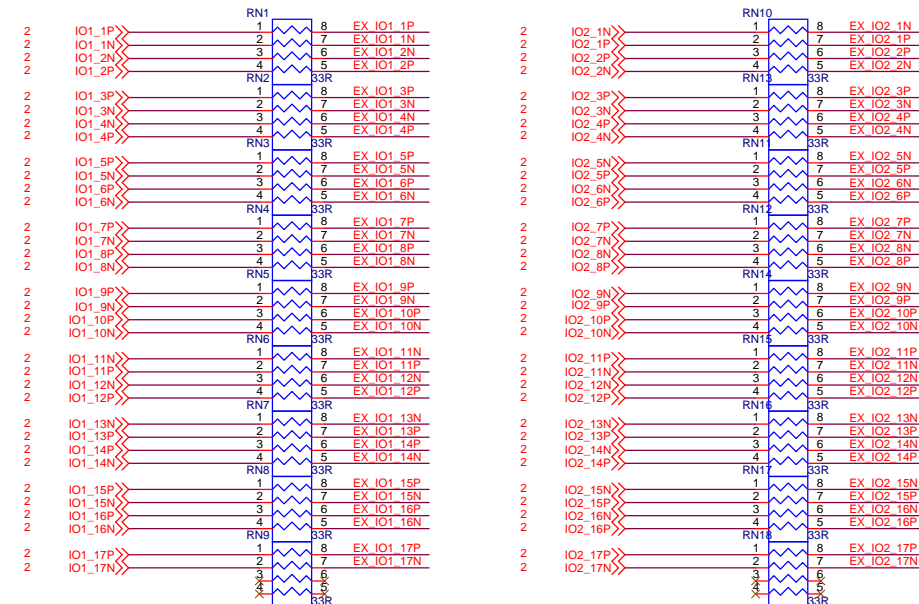
FPGA 40 PIN External IO



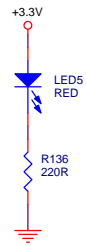
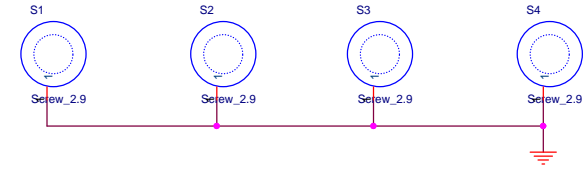
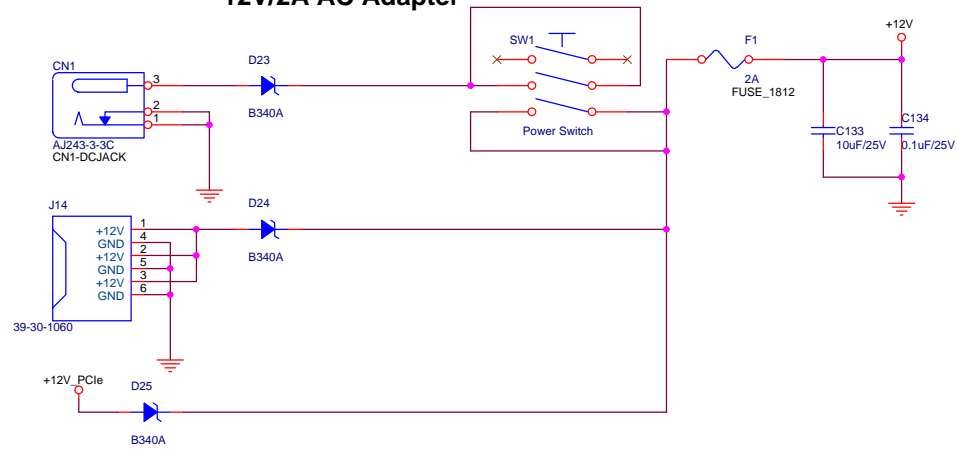
FPGA 40 PIN External IO



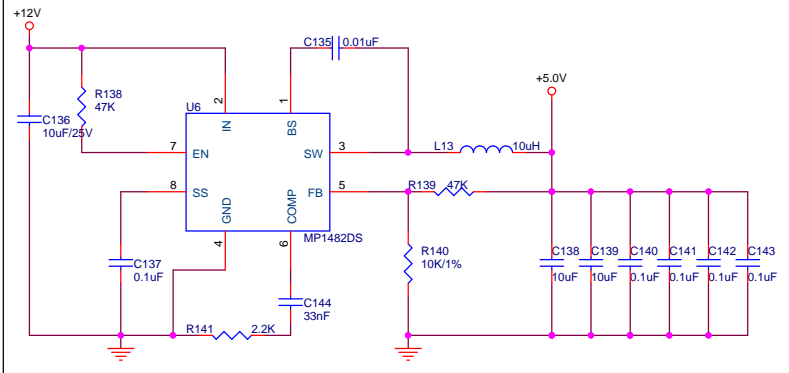
XADC Connector



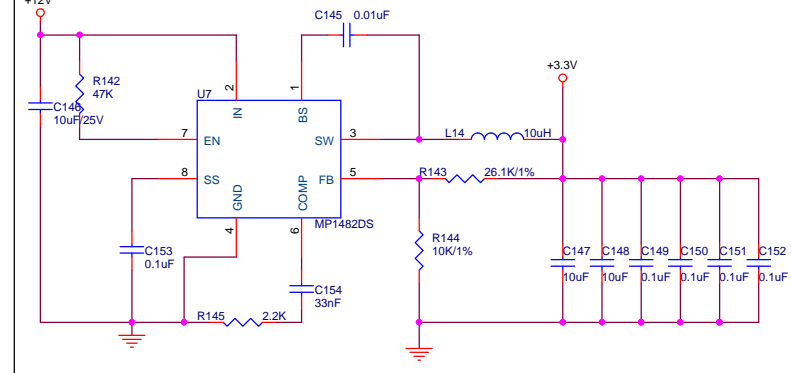
12V/2A AC Adapter



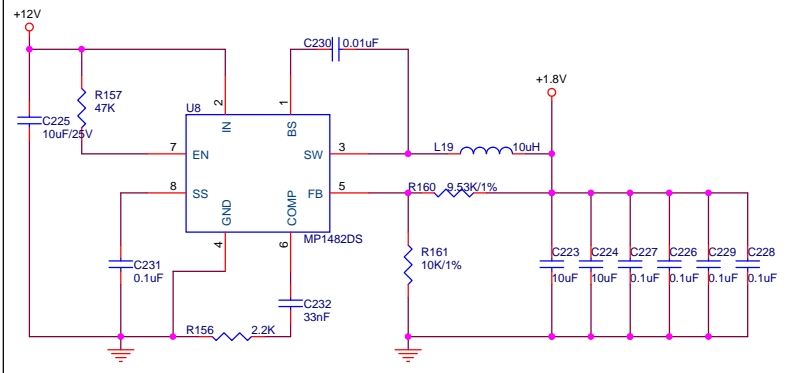
+5.0V POWER



+3.3V POWER



+1.8V POWER



+1.2V POWER

