

Experiment 3: Binary Arithmetic

Due date: 31.03.2021 23:00

Res. Asst. Ayşe Sayın

sayinays@itu.edu.tr

1 Introduction

In the following experiment, you are going to implement a 16-bit Full adder using the Verilog. In this experiment, you are allowed to use '&' (Bitwise AND), '|' (Bitwise OR), '~' (Bitwise NOT) operations. Other operations such as '^', '+', '-', '*', '/', '<<', '>>', '{' (Concatenate), and '>' are forbidden. More complex experiments will be later experiments, so you cannot use `always`, `parametric modules`, `switch case`, and `if else` etc. in this experiment.

2 Preliminary

- Recall signed and unsigned addition for binary numbers in 2's complement notation.
- Recall signed and unsigned subtraction for binary numbers in 2's complement notation.
- Recall what carry, borrow and overflow mean, when they occur and how are they interpreted.

3 Part 1

In this part, you are requested to implement AND, OR, NOT, XOR modules which you will use in the following parts of the experiment. You are not allowed to use these operators in the following parts, you can only use these modules when you need them.

4 Part 2

In this part, you should implement 1-Bit Half Adder module by using AND, OR, NOT, XOR modules which you designed in the first part. Then, you should simulate it for each different combination of input.

5 Part 3

In this part, you should implement 1-Bit Full Adder by using half adder and OR modules which you designed in the previous parts. Then, you should simulate it for each different combination of input.

6 Part 4

In this part, you should implement a 4-Bit Full Adder by using 1-Bit Full Adder modules which you designed in the previous part. Then, you should simulate it for '7+1', '2+8', '2+3', '14+10', '10+5', '15+4', '6+5', and '8+5' operations.

7 Part 5

In this part, you should implement a 16-Bit Full Adder by using 4-Bit Full Adder module which you designed in the previous part. Then, you should simulate it for '29+3', '21+83', '16800+16900', '65534+65100', '202+97', '44+19', '644+255', and '86+572' operations.

8 Part 6

In this part, you should implement a 16-Bit Full Adder-Subtractor by using 16-Bit Full Adder, NOT, XOR, AND, and OR modules which you designed in the previous parts. You should receive an additional input 'S' to indicate the numbers are signed or unsigned numbers. If S equals to 0 then the number is unsigned, if S equals to 1 then the number is signed. After that, you should simulate it for '29-3, S=0', '21+83, S=0', '16800+16900, S=1', '103-145, S=0', '202+97, S=0', '32400+32200, S=1', '6478-2585, S=0', and '8-52, S=0' operations.

If there is an overflow or borrow occurs on operation above, then show the these results with flags. Then, show that the operation above is whether valid or not.

Hint: You can find slides in the references that can help with overflow, borrow and carry operations.

9 Part 7

In this part, you should implement a module which calculates the $3A - 2B$ by using 16-Bit Adder-Subtractor, Adder, NOT, XOR, AND, and OR modules. Then, you should simulate it for 'A=3105, B=11275', 'A=21, B= 83', 'A=24, B=32', 'A=16386, B=353', 'A=202,B=97', 'A=44, B=9', 'A=64, B=65535', and 'A=8, B=52' inputs.

10 Report

You should show your work of Preliminary study on the report in detail. You can use any tool for creating tables and circuit designs. You may attach them to the report as figures by properly referencing them in the text.

Your report should also contain the results of your simulations for each module. If your implementations are not fully correct, discuss what the source of the errors might be in your report.

11 Submission

- Please do not send any document via e-mail to one of the assistants.
- Your reports must be written with Latex format. Latex report template is available on Ninova. You can use any Latex editor whichever you want. If you upload your report without Latex file, you directly get 0 as your report grade. You should upload both .pdf and .tex files of your report.
- You should submit 2 separate “.v” files for your Verilog codes. One of them should contain the modules and other one should contain the simulation codes.
- It will be sufficient for one person from each group to upload the homework.
- Be aware of the deadline. Late submissions are not accepted.
- Please do not hesitate to contact me (*sayinays@itu.edu.tr*) for any question.

12 References

<https://ninova.itu.edu.tr/tr/dersler/bilgisayar-bilisim-fakultesi/1591/blg-231e/>