

Experiment 2: Combinational Logic Circuits

Due: 24.03.2021 - 23.00

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*There are only 10 types of people in the world:
those who understand binary, and those who don't.*

1 Introduction

The aim in this experiment is to find the expression with the lowest cost for combinational logic circuits and implement them. In this experiment, you are allowed to use '&' (Bitwise AND), '|' (Bitwise OR), '~' (Bitwise NOT), and '{}' (Concatenate) operations. Other operations such as '+', '-', '*', '/', '<<', '>>', '^', **always**, **switch case**, and **if else** are forbidden.

2 Preliminary

1. For the function F_1 given in Equation 1, apply the following operations:
 - a) Find its prime implicants using Karnaugh diagram.
 - b) Find its prime implicants using Quine-McCluskey method.
 - c) Create prime implicant chart and find the expression with the minimum cost with 2 units of cost for each variable and 1 unit of cost for complement of a variable.
 - d) Design and draw the lowest cost expression using NOT, AND, and OR gates.
 - e) Design and draw the lowest cost expression using only NAND gates.
 - f) Design and draw the lowest cost expression using a single 8:1 Multiplexer and NOT gates.

$$F_1(a, b, c, d) = \cup_1(0, 1, 3, 5, 8, 10, 13, 14) + \cup_\phi(2, 7, 11, 12) \quad (1)$$

2. Design and draw the functions F_2 and F_3 given in Equations 2 and 3 using ONE single 3:8 decoder, 2-input OR gates (x' represents the complement of x).

$$F_2(a, b, c) = abc' + a'c \quad (2)$$

$$F_3(a, b, c) = ab'c' + bc \quad (3)$$

3 Experiment

Part 1

Please implement the circuit that you have designed in Preliminary 1.d. section using NOT, AND, and OR modules in Verilog. You should write these “gates” as modules and use them later in your implementations. In other words, for example, when you need to apply an AND operation to two input wires, you should use the modules you have written before, rather than using operators like “&” or “|” directly. Following the implementation, please run simulations for various input combinations to validate your design.

Part 2

Please implement the circuit that you have designed in Preliminary 1.e. section using only NAND modules in Verilog. You should implement the gate as a module and use it later in your implementations. Following the implementation, please run simulations for various input combinations to validate your design.

Part 3

Please implement the circuit that you have designed in Preliminary 1.f. section using a 8:1 multiplexer and NOT gates in Verilog. You should write the multiplexer and NOT gate as modules and use them later in your implementations. Following the implementation, please run simulations for various input combinations to validate your design.

Part 4

Please implement the circuit that you have designed in Preliminary 2 section using a 3:8 decoder and OR gates in Verilog. You should write the decoder and OR gate as modules and use them later in your implementations. Following the implementation, please run simulations for various input combinations to validate your design.

4 Report

You should show your work of Preliminary study on the report in detail. You can use any tool for creating tables (for Preliminary 1.a., 1.b. and 1.c.) and circuit designs (for Preliminary 1.d., 1.e. and 1.f.). You may attach them to the report as figures by properly referencing them in the text.

Your report should also contain information about the results of your simulations. If your implementations are not fully correct, discuss what the source of the errors might

be in your report.

5 Submission

- Please add comments to the code to clarify your intends.
- Please don't send any document via e-mail to one of the assistants.
- Your reports must be written in Latex format. Latex report template is available on Ninova. You can use any Latex editor whichever you want. If you upload your report without Latex file, you directly get 0 as your report grade. You should upload both .pdf and .tex files of your report.
- You should submit 2 separate “.v” files for your Verilog codes: one containing the modules, one containing the simulation codes.
- Please make sure that you have written your full name and student ID number to every document you are submitting.
- Note that late submissions are not accepted, be aware of the deadline.
- Please do not hesitate to contact me (erturkr15@itu.edu.tr) for any question. Don't forget to have fun and stay healthy.