Experiment 1 Boolen Algebra

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1 Introduction

The aim of this experiment is to recall the axioms and theorems of Boolean algebra and validate these axioms and theorems using the Verilog.

- Please complete the preliminary work and explain their in detail in your report.
- You are allowed to use '&' (Bitwise AND), '|' (Bitwise OR), and '∼' (Bitwise NOT) operations. Other operations such as '^ ', '+', '-', '*', '/', '<<', and '>>' are forbidden.
- More complex experiments will be later experiments, so you can not use `always`, `parametric modules`, `switch case`, and `if else` etc. in this experiment.

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2 Preliminary

- Revise the axioms and theorems of Boolean algebra.
- Prove the given equalities below by using the axioms of Boolean algebra. Please specify which axioms you use.
  - $a + a \cdot b = a$
  - $(a + b) \cdot (a + b') = a$
- Determine and prove the duals of the equalities defined above.
- Calculate the complementary expression (F') for the function F which is defined as follows ($F = a \cdot b + a' \cdot c$) by using De Morgan theorem and draw the logic circuit for both expressions (F and F').
- Simplify given logical function and draw the logic circuit.
  - $F(a, b, c, d) = \cup_1(1, 2, 5, 6, 9, 10, 13, 14)$

3 Experiment

Part 1

In this part, you are requested to implement AND, OR, NOT modules which you will use in the following experiments. You are not allowed to use these operators in the following parts, you can only use these modules when you need them.

Part 2

In this part, you should design and implement the logic circuits for the given expressions below by using AND, OR, NOT modules which you designed in the first part. Then, you should simulate it for each different combination of input and validate the correctness of your implementation.

- $F_1(a, b) = a + a \cdot b = a$
- $F_2(a, b) = (a + b) \cdot (a + b') = a$

Part 3

A theorem is given as: $(a + a \cdot b = a)$.
First, determine the dual of the given theorem and then, implement the functions for both sides of the dual theorem using AND, OR, NOT modules which you designed in the first part. Please validate the truth of the theorem by comparing the changes in the outputs using simulation.

Part 4

$F_3(a, b, c) = a \cdot b + a' \cdot c$ is given.
Firstly, determine the complement of the given function (F_3). Then, implement the circuit which realizes the complementary function (F_3'). Please validate your implementation by using the truth table and simulate it for each different combination of input.

Part 5

A basic logical function ($F4$) is defined as follows.

$$F_4(a, b, c, d) = \cup_1(1, 2, 5, 6, 9, 10, 13, 14)$$

First, simplify given logical function and implement the simplified expression using AND, OR, NOT modules which you designed in the first part. Please validate your implementation by observing the outputs for each possible input.

4 Report

Prepare your report using the guidelines and the report template which are posted on Ninova e-Learning System. Please report the preliminary work in detail. Your report should also include the following materials:

- Circuits diagrams of the expressions which were implemented during this experiment.
- Function tables (or truth tables) of the implemented expressions.
- Simulation outputs of each part.

Additionally, if there were any complications which affect your performance during the experiment, please also indicate these difficulties in your report.

5 Submission Policy

- You should upload your experiment codes and report on Ninova, and please, do not send your experiment files via e-mail.
- Please submit 2 Verilog Design files for the experiment codes. One of them contain modules' codes, the other one consists of simulation codes.
- Your reports must be written with Latex format. Latex report template is available on Ninova. You can use any Latex editor whichever you want. If you upload your report without Latex file, you directly get 0 as your report grade. You should upload both .pdf and .tex files of your report.
- Please do not forget that late submissions are not accepted.