Silicon Interconnect Fabric

At CHIPS we are focusing on packaging and system level integration schemes to improve the overall system performance rather than improving the individual packaged components. We have introduced our “CHIPS Fine Pitch Integration (FPI) Approach” that allows us to integrate heterogeneous (size, technology, semiconductor base etc.) dielets on a silicon based platform, which we call as “Silicon Interconnect Fabric (Si-IF)”. The interconnect pitches (2-10 μm) on Si-IF are similar to the fat wire level pitches of a microelectronic chip. For fine-pitch interconnections, we employ a direct metal-metal (Cu or Au) thermal-compression bonding (TCB) process, which is carried out in a flip chip fashion. In comparison with the soldered contacts, metal-metal interconnects exhibit excellent thermal and electrical properties. Furthermore, we can place dielets with an inter-dielet distance of ≤ 50 μm allowing us to achieve short links (100-500 μm) on Si-IF. By implementing both fine-pitch interconnects and short links on Si-IF, we can achieve low latency, low energy per bit, low I/O power and high band-width per unit edge length in comparison with the printed circuit board based assemblies.