WASP: A WAFER-SCALE MASSIVELY PARALLEL PROCESSOR

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INTRODUCTION

The new decade heralds the age of very powerful compute-, graphics- and information-servers, based on Massively Parallel Processors (MPPs), capable of TOPS (Tera Operations-Per-Second) performance in networked scientific, engineering, knowledge-base and artificial intelligence applications. In addition, MPP applications will include real-time signal and data processing in real-world locations; for example, computer vision systems (for aerospace, biomedical, automotive and general robotics environments) suggest typical examples.

However, although pioneer and first-generation MPPs have achieved MOPS (and, in some cases, GOPS) performance levels, they have not yet demonstrated a sufficiently significant breakthrough in application flexibility and cost-effectiveness to be commercially successful. Moreover, such MPPs have been highly machine-oriented; each being dominated (in cost and performance) by the particular inter-processor communication network (e.g. pipeline, mesh, hypercube, tree, pyramid, Omega, Banyan etc.) which, probably, have borne little relation to application requirements.

Thus, to be commercially successful, MPPs will not only require a step-function advance in performance, nor just represent an upgrade in parallel computer implementation technology. Indeed, second-generation MPPs must target the following user/application-oriented requirements.

architectural requirements : programmability, scalability and reconfigurability of the processor ensemble and the inter-processor network (i.e. opportunity to match the applied parallelism of the MPP architecture with the natural parallelism of the application) plus computation and communication efficiency.

engineering requirements : reliability and ease of maintenance within environmental restrictions (i.e. size, weight and power) and cost limitations.

Current trends in microelectronics and packaging technologies towards highly-compact plug-in WSI MPP modules augur the desired breakthrough. Moreover, in addition to the defect-tolerance necessary for monolithic

WSI manufacture, such MPPs could offer in-service maintenance, by adding redundancy to the processor ensemble and achieving fault-tolerance with self-testing and electronic reconfiguration to isolate faulty processors.

The purpose of this paper is to describe a fault-tolerant WSI MPP architecture which satisfies both the architectural and engineering requirements outlined above and, thereby, offers a step-function improvement in cost-effectiveness compared with first-generation MPPs.

MPP MODULES

MPP modules comprise highly-versatile parallel processing building-blocks for the simple construction of MPPs. Indeed, according to application requirements, an appropriate combination of MPP modules would be plugged into the control bus and Data Communications Network of some modular racking system, as indicated in Figure 1.

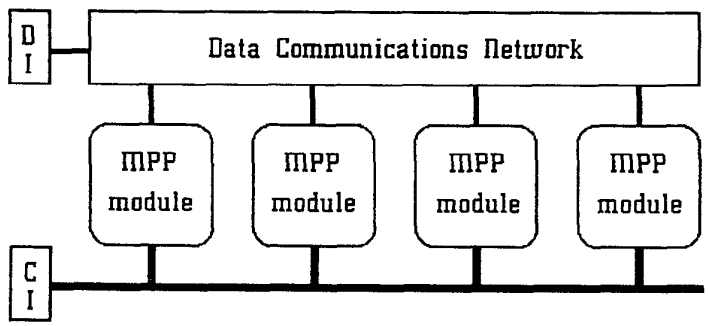


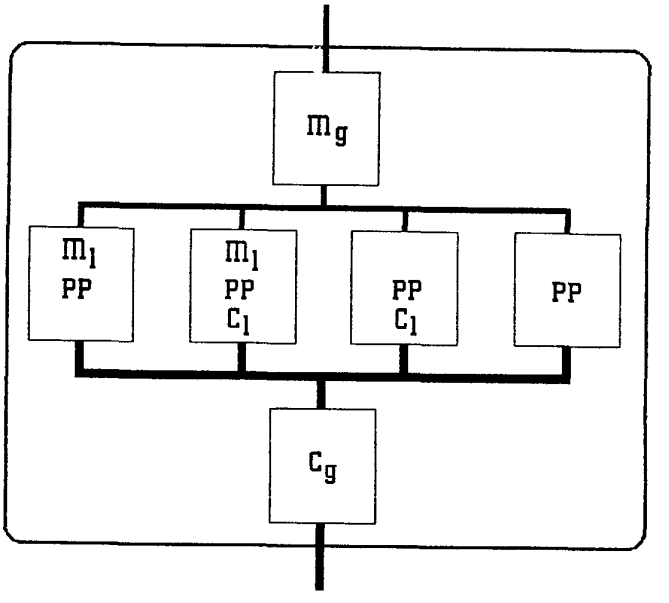
Figure 1. Modular MPP system

MPP modules constitute a family of packaged configurations of 6 types of component, as indicated in Figure 2. Since each component may or may not be included, there are 19 different MPP module configurations.

The most significant of these components comprises a WSI fine-grain SIMD (Single-Instruction control of Multiple-Data streams) massively Parallel Processor (PP). Four PP variants are shown in Figure 2.

Since the MPP module configuration variants allow the provision of multiple local Control Units, and multiple global Control Units can be achieved with multiple modules, a limited coarse-grain MIMD (Multiple-Instruction control of Multiple-Data streams) parallel processing capability can also be supported.

Thus, custom low-MIMD high-SIMD MPP modular systems can be configured to cost-effectively match application requirements.



M_g = global Memory
C_g = global Control Unit
PP = SIMD Parallel Processor plus an optional local memory (M_l) and/or Control Unit (C_l)

Figure 2. MPP module schematic

WASP DEVICES

Based on the encouraging results emerging from research into parallel computing technology at Brunel University and being developed by Aspex Microsystems Ltd., a WASP device is a WSI implementation of an ASP (Associative String Processor) substring (see below) and, as such, constitutes a fundamental building-block for the assembly of the PP components shown in Figure 2.

An ASP substring is a programmable, homogeneous and fault-tolerant fine-grain SIMD MPP incorporating a string of identical processors, a reconfigurable inter-processor communication network and buffer storage for fully-overlapped data input-output [1-3].

ASP substrings offer considerable application flexibility, maintaining high efficiency (in computation and communication) over a particularly wide range of signal and data processing applications, due to

(1) simple configuration of ASP substrings to simplify the development of MIMD/SIMD MPP systems which are well matched to functional application requirements

(2) pipelining and overlapping input-output data transfers (via the Data Communications Network) with parallel processing (within ASP substrings), by separating input-output from processing with local and global ADBs and Vector Data Buffers

(3) overlapping of sequential (scalar) processing (in local or global ACUs) with parallel processing (in ASP substrings)

(4) mapping different application data structures to a common string representation within ASP substrings (supporting content-addressing, parallel processing and a reconfigurable inter-processor communication network)

(5) elimination of processor (location) addressing, for the purposes of

    (a) achieving unlimited architectural scalability

    (b) implementing cost-effective fault-tolerance with simple (hierarchical) bypassing of faulty processor substrings, which, until failure occurs, are available for parallel processing

    (c) further minimisation of sequential processing overheads

(6) minimisation of inter-processor data movement, with high-speed activity transfer between processor subsets and in-situ processing.

As an example of an MPP module component, Figure 3 illustrates a WASP substrate supporting 4 WASP devices, 2 (32-bit) Data Interfaces (DIs) and a single local Control Unit (CU).

As indicated in Figure 3, WASP devices are composed from 3 different "chip" reticle-masks; implementing Data Routers (DRs), ASP rows and Control Routers (CRs). The DR and CR reticles incorporate routing to connect ASP rows to a common Data Interface (DI) and a common Control Interface (CI) respectively. Thus, MPP modules can be assembled with WASP devices interfaced to local or global memories and control units or directly to the Data Communications Network and control bus via their DIs/CIs.

In practice, WASP form-factors will depend on the packaging standards adopted for MPP module construction for particular application environments. Of the possible packaging standards being considered for aerospace applications in the 1990s, a light-weight thin-profile SEM-E compatible module is assumed for the following projection.

A priori considerations suggest that such an MPP module could be assembled with 2 WASP substrates, mounted on the 2 surfaces of a single

thermal conduction plate, which also provides mechanical support for the module edge connector.

Extrapolation, from the results of current WASP experimental progress, suggests that, with standard 1.2um CMOS (double-layer metal) fabrication technology, (nominal) harvests of 8,192 APEs per WASP device can be forecast. Consequently, a 65,536-APE WSI MPP module with 8 (32-bit) data channels can be predicted.

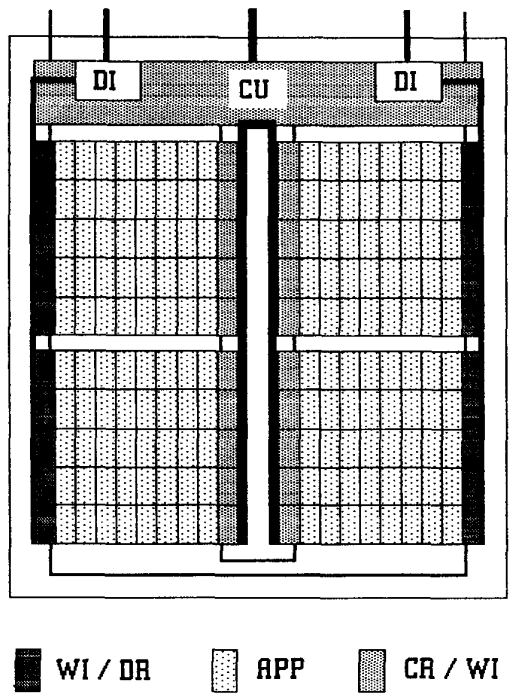


Figure 3. WASP substrate

Experimental progress

The WASP project was started at Brunel University in October 1983 and has been funded since 1985 under a UK Alvey (VLSI) contract, involving Plessey, GEC, ICL and Middlesex Polytechnic, which has included the fabrication (by Plessey, UK) and evaluation of defect/fault-tolerant test chips and the WASP 1, WASP 2a and WASP 2b WSI ASP technology demonstrators [3,4]. In a separate project, the WASP 3 application demonstrator for iconic-to-symbolic image processing, scheduled for fabrication in 1990, is being developed by Aspex Microsystems under a US SDI IS&T contract. Subsequent such WASP prototypes are also being planned. Thus, the research strategy is to approach the ideal WASP target, as described above, with a stepping-stone sequence of

experimental prototypes (i.e. WASP 1/2/3/4 ...); analysis of each prototype helping to redefine WASP potential and to specify the experimental objectives of the next step.

CONCLUSIONS

The progress of WASP hardware and software research heralds the development of highly-versatile and fault-tolerant building-blocks for the construction of Massively Parallel Processors (MPPs); with significant benefits, compared with contemporary MPP implementations. Indeed, the following forecasts summarise the potential of the thin-profile SEM-E compatible MPP module described above.

Configuration	1, 2, 4 or 8 MIMD processors
Performance	100 GOPS (12-bit adds at 40 MHz)
Maximum I/O bandwidth	640 Mbytes/sec (at 20 MHz)
Number of processors	65,536
Package size	6.4" x 5.88" x 0.3" (SEM-E)
Power dissipation	< 100 W
Market cost	< $100,000

Being based on extrapolation of experimental results, the first 4 forecasts are fairly conservative. Since, a performance of 1 TOPS (i.e. 1000 GOPS) could be achieved with only 10 MPP modules within an eighth of a cubic foot, allowance for a similarly miniaturised global controller and Data Communications Network (see Figure 1) would suggest that a target of 1 TOPS/ft^3 is achievable. Moreover, the quoted cost includes ample provision for marketing overheads, product support and profit, thereby indicating that a 1 MOPS/$ target could be exceeded with higher volume marketing. In fact, the most speculative forecast is that for power dissipation, aiming to exceed a 1 GOPS/W target with a compromise between the 50 Watts commonly quoted for SEM-E packaging technology and the desire to maximise performance. Hence, current research is addressing this issue not only in terms of minimising power dissipation in WSI circuit design, but also in improvement of the thermal characteristics of SEM-E module assembly and packaging materials.

Of course, such performance forecasts refer only to the low-level arithmetic operations of numeric-to-symbolic data conversion process of real-time signal and data processing. Indeed, a more realistic performance indication can be gained from real-time signal and data processing benchmarks, which include all processing from data input to

the output of the required response. To this end, the ASP architecture has been evaluated in terms of the 2 US DARPA Image Understanding benchmarks set in 1986 and 1988 and the European CERN LAA (particle Physics track analysis) benchmark in 1989. Although beyond the scope of this paper, the results [5-7], nevertheless, indicate significant performance advantages for MPP modules compared with contemporary parallel computers.

In summary, WASP-based MPP modules offer considerable promise for second-generation massively parallel computer applications. Indeed, the modules offer the application flexibility needed for the efficient configuration of custom massively parallel computing systems and, indeed, the prospect of breaking through the cost-barrier currently impeding the wider commercial exploitation of such systems.

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