

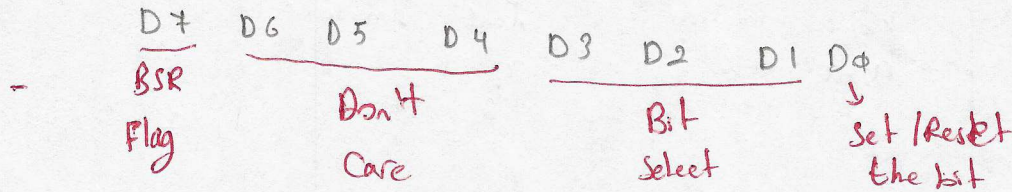
8086 Modes

- BSR (Bit Set reset) : PC'nin ilgili bitleri/port uclarını, I/O yapmak için.
 - mod0 (Basic IO) : Veri aktarımı ile ilgili degirukema joh.
 - mod1 (handshaking) : Tek jorlo handshaking (Strobe,ack)
 - mod2 (handshaking) : Gilt jorlo hand shaking (Strobe,ack)
- [PA/PB: data transfer PC: handshaking]
[PA: data transfer PC: handshaking]

MP
w6/11

Basic I/O PC
Mod1 ve Mod2 Config

Control word (BSR)



Ex. 80H adresinden itibaren gitt adreslerde 8255'de.

- PC2'de 1, PC6'da ise duty cycle'i %66 olan bir kare dalga oluşt şekilde programlayın.

PA: 80H
PB: 82H
PC: 84H
kontrol: 86H

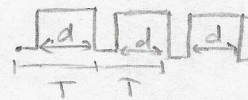
a) PC2=1

→ kontrol kelimesini belirle

→ CW'a aktar

mov AL, 0000101B ; AL ← 05H
out 86H, AL

b) PC6



duty cycle

$$dc = \frac{d}{T} = \frac{2}{3} = \%66$$

① - PC6'yi 0 yapan CW'a çık

- Call delay

- PC6'yi 1 yapan CW'a çık

- Call delay

- Call delay

- ①'i tekrarla

.. b) L1: mov AL, 00001101B

out 86H, AL

CALL DELAY

mov AL, 00001101B

CALL DELAY

CALL DELAY

JMP L1

△ Grup A ve Grup B ayrı ayrı mod1 ian kullanılabilir

group A mod Φ 'de group B mod Φ 'da ise PC mod Φ 'da kullanılamaz.
(Handshaking için kullanılabiliyorlar)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	1/2	x	x	x

Hand-drawn block diagram of a 4-bit parallel adder. It shows four 1-bit full adders (FA) connected in a chain. The carry-in (CIN) is 0. The carry-out (COUT) of the first FA is connected to the carry-in of the second FA, and so on. The outputs are labeled PA3, PA2, PA1, and PA0. The inputs are labeled PC0, PC1, PC2, and PC3. The output of the fourth FA is labeled PC4,5.

Hand-drawn schematic diagram of a 3-bit counter using three J-K flip-flops (PC₀, PC₁, PC₂) and an AND gate. The counter is initialized to 000. The output of the AND gate (labeled INTER) is connected to the clock input of PC₀. The clock input of PC₁ is connected to the output of PC₀ (labeled IBF_B). The clock input of PC₂ is connected to the output of PC₁ (labeled STB_A). The output of PC₂ is labeled PB-PR₀. The output of PC₀ is labeled INTR_B. A reset input RD is shown at the bottom left.

Hand-drawn block diagram of a 3-bit counter circuit. The circuit is enclosed in a box labeled PB_3-PB_0 with a double slash indicating a bus. Inside the box, there are three flip-flops labeled PC_2 , PC_1 , and PC_0 . The output of PC_2 is labeled Ack_B . The output of PC_1 is labeled \overline{OBF}_B . The output of PC_0 is labeled PC_0 . The inputs to the flip-flops are labeled $INTER$ and wR . The output of the AND gate is connected to the clock input of PC_0 .

Hand-drawn block diagram of the 8086-8255 system architecture:

- 8086 Microprocessor:** Labeled "8086", connected to "Input".
- 8255 PPI:** Labeled "8255", connected to the 8086 via a bidirectional data bus and a 16-bit address bus (A₁₅ to A₀).
- 8087 Coprocessor:** Labeled "8087", connected to the 8255 via a bidirectional data bus and control signals: I/O Master Function (IO/M), Status Buffer (STB), and Command/Status (C/S).
- 8087 Add-on Card:** Labeled "Add. Göz.", connected to the 8255's C/S and STB signals.

ediyor. İşlemci sürekli IBF'yi kontrol eder.
 → Yukarıdaki örnek için PE₄ üzerinde set edilir.

Interrupt: İşlemci ITEA (interrupt enable A) 'yi set etmişse IBF set olursa 8086'ya INTR (interrupt request) gelir.

2055

Genet. Binnl.

PA

DBF

FC₂ = Acl

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graph LR; 2055[2055] -- PA --> GenetBinnl[Genet. Binnl.]; 2055 -- DBF --> GenetBinnl; 2055 -- "FC2 = Acl" --> GenetBinnl;
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• 8255 A'ch geldikten sonra \overline{OBF} ucuna $\overline{1}$ set edilir. Bu ucu kontrol edilerek yeni verinin alınıp alınmayacağına karar verilir.

⑨ For interrupt: PC₂ is used to enable interrupt