

**Application**

- iNIC

The RT3662 SOC combines Ralink's 802.11n draft compliant 2T3R MAC/BBP/RF, a high performance 500MHz MIPS74Kc CPU core, a Gigabit Ethernet MAC, and a USB Host/Device. With the RT3662, there are very few external components required for 2.4/5GHz 11n wireless products. The RT3662 employs Ralink 2nd generation 11n technologies for longer range and better throughput. The embedded high performance CPU can process advanced applications effortlessly, such as WI-FI data processing without overloading the host processor. In addition, the RT3662 has rich hardware interfaces (SPI/ I2S/ I2C/ PCM/ UART/ USB/ PCI/ PCIe/ RGMII/ MII) to enable many possible applications.

**Features**

- ◆ Embedded 2T3R 2.4/5G CMOS RF
- ◆ Embedded 802.11n 2T3R MAC/BBP w/MLD enhancement
- ◆ 450Mbps PHY data rate
- ◆ 20Mhz/40Mhz channel width
- ◆ Legacy and high throughout modes
- ◆ Compressed Block ACK
- ◆ Bluetooth Co-existence
- ◆ Multiple BSSID (up to 16)
- ◆ WEP64/128, WPA, WPA2 engines
- ◆ QOS - WMM, WMM Power Save
- ◆ Hardware frame aggregation
- ◆ International Regulation - 802.11h TPC
- ◆ MIPS 74KEc 500Mhz with 64KB I cache/32KB D cache

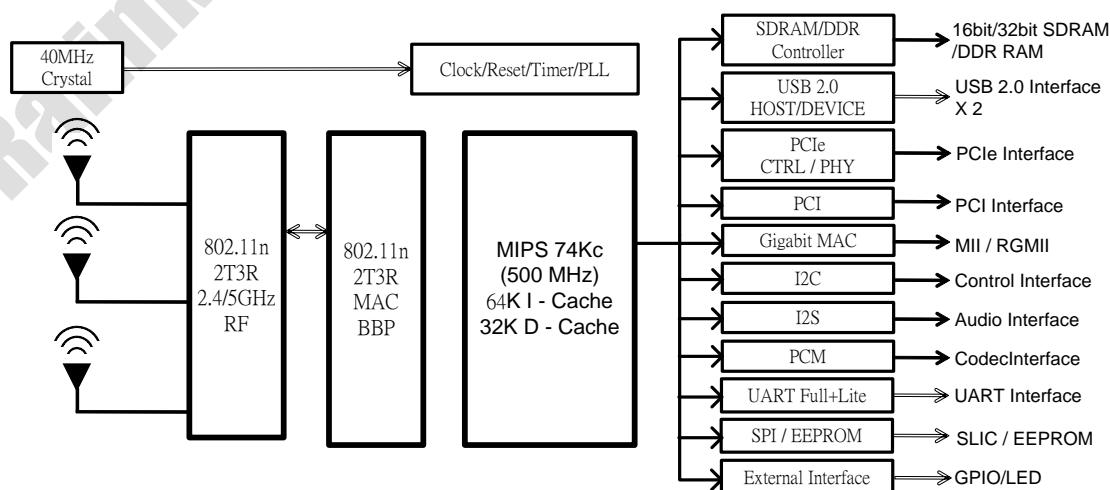
- ◆ Support 16/32-bit SDR/DDR2 SDRAM (up-to 256M bytes) and 8/16-bit NOR Flash (up-to 32M bytes)
- ◆ Support boot from ROM, FLASH
- ◆ Support HW WAPI
- ◆ USB2.0 HOSTx2, Device1, PCI, PCIe, RGMII, MII
- ◆ IPv6 support.
- ◆ Slow speed I/O: GPIO, SPI, I2C, I2S, PCM, UART, and JTAG
- ◆ Package and I/O voltage
  - 17mm x 17mm TFBGA-448 Package
  - I/O: 3.3v I/O

**Order Information**

Part Number	Temp Range	Package
RT3662F	-10~70°C	Green/ RoHS Compliant TFBGA 448ball (17mmx17mm)

Ralink Technology, Corp. (Taiwan)  
5th F. No. 36,Taiyuan St, Jhubei City, Hsin-Chu, Taiwan,  
R.O.C.  
Tel: 886-3-560-0868 Fax: 886-3-560-0818

Ralink Technology, Corp. (USA)  
20833 Stevens Creek Blvd., Suite 200 Cupertino, CA95014  
Tel: (408) 725-8070 Fax: (408)725-8069  
<http://www.ralinktech.com>

**Functional Block Diagram**


**Table of Content**

<b>1</b>	<b>Pin Description.....</b>	<b>7</b>
1.1	448-Pins BGA Package Diagram .....	7
1.2	Pin Description .....	8
1.3	Pins Sharing Scheme.....	16
1.4	Boot strapping description.....	23
<b>2</b>	<b>Maximum Ratings and Operating Conditions.....</b>	<b>24</b>
2.1	Absolute Maximum Ratings .....	24
2.2	Thermal Information .....	24
2.3	Operating Conditions.....	24
2.4	Storage Condition.....	24
2.5	External Xtal Specification .....	24
2.6	DC Electrical Characteristics.....	24
2.6.1	DC characteristics for GPIO pins with 4mA driving capability .....	25
2.6.2	DC characteristics for GPIO pins with 8mA driving capability .....	25
2.6.3	DC characteristics for RGMII related pins.....	25
2.7	AC Electrical Characteristics.....	26
2.7.1	SDRAM Interface.....	26
2.7.2	RGMII Interface.....	26
2.7.3	Flash/SRAM Interface.....	27
2.7.4	Power On Sequence .....	28
<b>3</b>	<b>Function Description.....</b>	<b>29</b>
3.1	Overview .....	29
3.2	Memory Map Summary .....	29
3.3	MIPS 74K Processor .....	31
3.3.1	Features .....	31
3.3.2	Block Diagram .....	33
3.3.3	Clock Plan.....	34
3.4	System Control.....	35
3.4.1	Features .....	35
3.4.2	Block Diagram .....	35
3.4.3	Register Description (base: 0x1000.0000) .....	35
3.5	Timer.....	46
3.5.1	Features .....	46
3.5.2	Block Diagram .....	47
3.5.3	Register Description (base: 0x1000.0100) .....	47
3.6	Interrupt Controller .....	50
3.6.1	Features .....	50
3.6.2	Block Diagram .....	50
3.6.3	Register Description (base: 0x1000.0200) .....	51
3.7	UART .....	55
3.7.1	Features .....	55
3.7.2	Block Diagram .....	55
3.7.3	Register Description (base: 0x1000.0500) .....	55
3.8	UART Lite.....	62
3.8.1	Features .....	62
3.8.2	Block Diagram .....	62
3.8.3	Register Description (base: 0x1000.0C00) .....	62
3.9	Programmable I/O.....	67
3.9.1	Features .....	67

3.9.2	Block Diagram .....	67
3.9.3	Register Description (base: 0x1000.0600).....	67
3.10	I2C Controller .....	76
3.10.1	Features.....	76
3.10.2	Block Diagram.....	76
3.10.3	Register Description (base: 0x1000.0900).....	76
3.11	PCM Controller.....	80
3.11.1	Features.....	80
3.11.2	Block Diagram .....	80
3.11.3	Register Description (base: 0x1000.2000).....	81
3.12	Generic DMA Controller .....	87
3.12.1	Features.....	87
3.12.2	Block Diagram .....	87
3.12.3	Peripheral Channel Connection .....	87
3.12.4	Register Description (Base: 0x1000.2800).....	88
3.13	SPI Controller .....	91
3.13.1	Features.....	91
3.13.2	Block Diagram .....	91
3.13.3	Register Description (base: 0x1000.0B00).....	91
3.14	I2S Controller.....	96
3.14.1	Features.....	96
3.14.2	Block Diagram .....	96
3.14.3	Register Description of I2S (base:1000.0A00) .....	97
3.15	Memory Controller.....	100
3.15.1	Features.....	100
3.15.2	Block Diagram .....	100
3.15.2.1	SDRAM Initialization Sequence.....	100
3.15.2.2	DDR2 Initialization Sequence.....	100
3.15.3	Register Description (base: 0x1000.0300).....	100
3.16	Flash/SRAM/Codec Controller .....	113
3.16.1	Features.....	113
3.16.2	Register Description (base: 0x1000.0700).....	113
3.16.3	Codec0 Memory Space (base: 0x1000.3000) .....	116
3.16.4	Codec1 Memory Space (base: 0x1000.3800) .....	116
3.17	NAND Flash Controller.....	117
3.17.1	Introduction .....	117
3.17.2	Specification .....	117
3.17.2.1	Features.....	117
3.17.2.2	Normal Mode Flow .....	117
3.17.2.3	ECC .....	118
3.17.2.4	Interfaces.....	119
3.17.2.5	Major interfaces.....	119
3.17.2.6	In/Out ports.....	119
3.17.3	Register Description (base: 1000.0800) .....	120
3.18	USB Host Controller & PHY .....	123
3.18.1	Features.....	123
3.18.2	Block Diagram .....	123
3.18.3	Register Description (base: 0x101C.0000).....	124
3.18.3.1	EHCI Operation register (BASE: 0x101C.0000) .....	124
3.18.3.2	OHCI Operation register (BASE: 0x101C.1000).....	125

3.19	USB Device Controller.....	126
3.19.1	Features.....	126
3.19.1.1	PDMA descriptor format .....	126
3.19.1.2	Bulk-out aggregation format .....	127
3.19.2	Register Description (base: 0x1012.0000).....	128
3.19.2.1	USB control registers.....	128
3.19.2.2	UDMA registers.....	128
3.19.2.3	PDMA registers .....	128
3.20	Frame Engine.....	133
3.20.1	Features.....	133
3.20.1.1	Network Interface.....	133
3.20.1.2	PSE (Packet Switch Engine) Features .....	133
3.20.1.3	PPE Features .....	133
3.20.1.4	QoS Related Features.....	134
3.20.1.5	Packet DMA (PDMA) Features.....	134
3.20.2	Block Diagram .....	135
3.20.2.1	PDMA FIFO-like Ring Concept.....	136
3.20.2.2	PDMA Descriptor Format.....	137
3.20.3	Register Description (base: 0x1010.0000).....	138
3.20.3.1	Register Description – GDMA1 .....	142
3.20.3.2	Register Description - PSE .....	144
3.20.3.3	Register Description – GDMA2 .....	145
3.20.3.4	Register Description - CPU Port .....	147
3.20.3.5	Register Description - PDMA .....	151
3.20.3.6	Register Description – Frame Engine Counters (base: 0x1010.0400).....	157
3.21	802.11n 2T3R MAC/BBP .....	159
3.21.1	Features.....	159
3.21.2	Block Diagram .....	159
3.21.3	Register Description - SCH/WPDMA (base: 1018.0000).....	160
3.21.3.1	Register Description - PBF (base: 1018.0000) .....	165
3.21.3.2	Register Description - MAC (base: 1018.0000).....	170
3.21.3.3	MAC search table (base: 1018.0000, offset: 0x1800) .....	202
3.22	Security table/CIS/Beacon/NULL frame (base: 1018.0000, offset: 0x4000).....	202
3.22.1	Security Key Format (8DW) .....	202
3.22.2	IV/EIV format (2 DW) .....	203
3.22.3	WCID attribute entry format (1DW) .....	203
3.22.4	Share key mode entry format (1DW).....	204
3.22.5	Security Table .....	204
3.22.5.1	Pair-wise key table (offset:0x4000) .....	204
3.22.5.2	IV/EIV table (offset:0x6000) .....	205
3.22.5.3	WCID attribute table (offset:0x6800) .....	205
3.22.5.4	Shared Key Table (offset:0x6C00).....	205
3.22.5.5	Shared Key Mode (offset:0x7000) .....	206
3.22.5.6	Spared Memory Space Mode (offset:0x7010~0x73EC) .....	206
3.22.5.7	Shared Key Mode Extension (for BSS_IDX=8~15) (offset:0x73F0).....	206
3.22.5.8	Shared Key Table Extension (for BSS_IDX=8~15) (offset:0x7400) .....	206
3.22.5.9	WAPI PN table (extension of IV/EIV table) (offset:0x7800) .....	207
3.23	Descriptor and Wireless information .....	207
3.23.1	TX frame information .....	207
3.23.1.1	TX descriptor format .....	208

3.23.1.2	TXWI format .....	210
3.23.2	RX descriptor ring.....	211
3.23.2.1	RX descriptor format.....	212
3.23.2.2	RXWI format .....	213
3.23.3	Brief PHY rate format and definition.....	213
3.23.4	Driver implementation note.....	216
3.23.4.1	Instruction of down load 8051 firmware .....	216
3.23.4.2	Instruction of initialize DMA.....	216
3.23.4.3	Instruction of clock control.....	216
3.23.4.4	Instruction of TX/RX control .....	217
3.23.4.5	Instruction of RF power on/off sequence .....	217
3.23.4.6	Power saving procedure.....	218
3.23.4.7	Power recovery procedure.....	218
3.23.4.8	Parameters .....	218
3.24	PCI/PCI Express Controller .....	219
3.24.1	Features.....	219
3.24.2	Block Diagram .....	219
3.24.2.1	Host bridge with both PCI and PCIe Slot .....	219
3.24.2.2	PCI/PCIe controller behaves as a PCI/PCIe Device.....	220
3.24.2.3	Block Diagram.....	222
3.24.3	PCI/PCIe master access in Host mode.....	222
3.24.3.1	PCI/PCIe Controller Host mode initialization example.....	224
3.24.3.2	PCI Device mode initialization example .....	224
3.24.4	Host-PCI Bridge Register Description (base: 0x1014.0000).....	224
3.24.5	PCI Host/Dev Control Register Description (base: 0x1014.1000).....	227
3.24.6	PCIe RC/EP Control Register Description (base: 0x1014.2000) .....	228
4	Package Physical Dimension.....	230
4.1	TFBGA 17x17.....	230
5	Revision History .....	232

**Table of Figures**

Fig. 1-3-1 PCI pin share scheme .....	18
Fig. 1-3-2 RT3662 MII → MII PHY.....	20
Fig. 1-3-3 RT3662 RvMII → MII MAC.....	21
Fig. 1-3-4 RT3662 RGMII → RGMII PHY.....	21
Fig. 1-3-5 RT3662 RGMII → RGMII MAC .....	22
Fig. 2-6-1 SDRAM Interface.....	26
Fig. 2-6-2 Flash/SRAM Interface.....	27
Fig. 2-6-3 Power ON Sequence .....	28
Fig. 3-1-1 RT3662 Block Diagram .....	29
Fig. 3-3-1 MIPS 74KEc Processor Diagram.....	33
Fig. 3-5-1 Timer Block Diagram.....	47
Fig. 3-6-1 Interrupt Controller Block Diagram .....	50
Fig. 3-7-1 UART block diagram.....	55
Fig. 3-8-1 UART Lite Block Diagram.....	62
Fig. 3-9-1 Program I/O Block Diagram.....	67
Fig. 3-12-1 Generic DMA controller block diagram.....	87
Fig. 3-13-1 SPI controller Block Diagram .....	91
Fig. 3-14-1 The block diagram of I <sup>2</sup> S Transmitter.....	96
Fig. 3-14-2 I <sup>2</sup> S Transmitter .....	96
Fig. 3-15-1 Flash/SRAM/SDRAM controller Block Diagram .....	100
Fig. 3-16-1 Flash/SRAM/SDRAM Controller R/W waveform .....	114
Fig. 3-17-1 Normal Mode Flow .....	117
Fig. 3-17-2 24-bit ECC was generated from 512-byte data .....	118
Fig. 3-17-3 hardware ECC detection flowchart.....	119
Fig. 3-17-4 Interfaces of NAND flash controller.....	119
Fig. 3-18-1 USB HOST Controller & PHY Block Diagram .....	123
Fig. 3-19-1 PDMA TX descriptor format .....	126
Fig. 3-19-2 PDMA RX descriptor format .....	127
Fig. 3-20-1 Frame Engine block diagram .....	135
Fig. 3-20-2 PDMA FIFO-like ring concept.....	136
Fig. 3-20-3 PDMA TX descriptor format .....	137
Fig. 3-20-4 PDMA RX descriptor format .....	137
Fig. 3-21-1 802.11n 2T3R MAC/BBP block diagram .....	159
Fig. 3-21-2 802.11n 2T3R MAC/BBP register map .....	160
Fig. 3-23-1 TX frame information.....	208
Fig. 3-23-2 TX descriptor format.....	209
Fig. 3-23-3 TXWI format .....	210
Fig. 3-23-4 RX descriptor ring .....	211
Fig. 3-23-5 RX descriptor format.....	212
Fig. 3-23-6 RXWI format .....	213
Fig. 3-24-1 PCI/PCIe Host Topology.....	219
Fig. 3-24-2 PCI/PCIe AP mode.....	220
Fig. 3-24-3 PCI controller behaves as a PCI device.....	220
Fig. 3-24-4 PCIe controller behaves as a PCIe endpoint.....	221
Fig. 3-24-5 PCI/PCIe host/device controller block diagram.....	222
Fig. 3-24-6 PCIe memory space programmable mapping .....	223
Fig. 3-24-7 PCI memory space fixed mapping.....	223
Fig. 3-24-8 PCI I/O space programmable mapping .....	223

## 1 Pin Description

### 1.1 448-Pins BGA Package Diagram

Top view (left portion)

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	PLL_VC_CAP	PLL_X1	PLL_X2	BG_RES_12K	BG_V33A	ADC_VREF	ADC_V12A	RFO_TSSI_IN	ADC_V12D	ANT_TRN	PCIE_VCCA33CG
B	GND	VCO_LO_V12A	PLL_V12A	LDO_OUT2_V12A	LDO_OUT1_V12A	RF_IO_V33A	RF2_TSSI5_IN	RF1_PA_PE	RFO_PAPE	LNA_PE_G2	ANT_TRNB	LNA_PE_A1
C	GND	GND	LDO_IN12_VX	BASE_TRX_IN	BASE_TRX_QN	NC	RF1_TSSI_IN	RF1_PA5_PE	RFO_PA5PE	CPLL_AVDD_V12A	LNA_PE_G0	LNA_PE_A0
D	RFO_RF2G_INP	RFO_RF2G_INN	GND	BASE_TRX_IP	BASE_TRX_QP	RF2_TSSI_IN	NC	RF1_TSSI5_IN	RFO_TSSI5_IN	BPLL_AVDD_V12A	LNA_PE_G1	LNA_PE_A2
E	RFO_RF5G_INP	RFO_RF5G_INN	RF_BB1_V12A	GND								
F	RFO_RF5G_OUTTP	RFO_RF2G_OUTTP	RFO_IF_V12A	RF_BB2_V12A								
G	RF1_RF2G_INP	RF1_RF2G_INN	RF0_RF_V12A	GND		GND	GND					
H	RF1_RF5G_INP	RF1_RF5G_INN	RF1_IF_V12A	GND		GND	GND					
J	RF1_RF5G_OUTTP	RF1_RF2G_OUTTP	RF1_RF_V12A	GND		GND	GND					
K	RF2_RF2G_INP	RF2_RF2G_INN	RF2_IF_V12A	GND		GND						
L	RF2_RF5G_INP	RF2_RF5G_INN	RF2_RF_V12A	GND		GND						
M	NC	NC	GND	MDO								
N	GND	GND	MD1	MD5								
P	MD3	MD4	MD2	MDQMO								
R	MD6	MD7	MDQSO	MD9								
T	MDQS1	MDQM1	MD8	MD11								
U	MD12	MD13	MD10	MCAS_N								
V	MD14	MD15	MDOT	MRAS_N								
W	GND	GND	MCKE	MWE_N								
Y	MCK_P	MCK_N	MBA0	DDR_IOR_V09D								
AA	GND	GND	DDR_IOL_V33D		MA1	MA4	MD16	MD20	MDQM2	MD24	MD28	SOC_CO_V12D
AB	DDR_IO_V33D	DDR_IO_V33D	DDR_IO_V33D	MA0	MA5	MA10	MD18	MD22	MDQS2	MD26	MD30	DDR_IOC_V12D
AC	MBA1	MBA2	MA2	MA6	MA8	MA11	MD17	MD21	MDQS3	MD25	MD29	DDR_IOC_V12D
AD	MCS_N	MA3	MA7	MA9	MA13	MA12	MD19	MD23	MDQM3	MD27	MD31	DDR_IOR_V09D_1

JTAG_TDI	JTAG_TCLK	JTAG_TDO	SOC_CO_V12D	NC
GND	GND	CPLL_DVDD_V12D	JTAG_TMS	GPIO6
TXD2	GND	GND	BPLL_DVDD_V12D	GND
GPIO1	GPIO0	GND	GND	GND
GPIO3	GPIO2	GND	GND	GND
RXD2	DSR_N	GND	GND	GND
RIN	CTS_N	GND	GND	GND
RXD	TXD	GND	GND	GND
DDC_N	GND	GND	GND	GND
GND	GND	GND	GND	GND
DDR_IOC_V12D	SOC_CO_V12D	GND	RTS_N	DTR_N
DDR_IOC_V12D	WLAN_LED_N	I2C_SD	PORST_N	I2C_SCLK

Top view (right portion)

13	14	15	16	17	18	19	20	21	22	23	24		
PCIE_CGREXT	GND	PCIE_PEXCLKN1	GND	PCIE_PEXCLKN0	GND	REFCLK_P	GND	RXO_P	PCIE_25	TX0_M	TX0_P	A	
GND	GND	PCIE_PEXCLKP1	GND	PCIE_PEXCLKP0	GND	REFCLK_M	GND	RXO_M	GND	GND	GND	B	
PCIE_VCCA33DR	GND	GND	GND	GND	GND	GND	GND	PCIE_RECT	GND	PCIE_VP	GE2_TXD2	GE2_TXCLK	C
PCIE_VCCA12CG	GND	PCIE_CGTTEST	GND	PCIE_VCCA33DR	GND	GND	GND	GND	GND	GE2_RXD3	GE2_RXD0	GE2_RXEN	D
								GE2_RXD1	GE2_RXD2	GE2_RXD0	GE2_RXCLK	GE2_RXCLK	E
								GE2_RXDV	GE2_RXD3	UPHY1_ID	UPHY1_VBUS	UPHY1_VBUS	F
								GE2_RXD1	UPHY1_VDDL_V12D	UPHY1_PADP	UPHY1_PADM	UPHY1_PADM	G
								UPHY0_VDDL_V12D	UPHY1_VRES	UPHY1_VDDA_V33A	UPHY0_VDDA_V33A	UPHY0_VDDA_V33A	H
								GND	UPHY0_ID	UPHY0_PADP	UPHY0_PADM	UPHY0_PADM	J
								UPHY0_VBUS	GND	GND	GND	GND	K
								UPHY0_VRES	GE1_RXD3	GE1_RXD2	GE1_RXD2	GE1_RXD2	L
								GE1_RXD1	GE1_RXD0	GE1_RXD3	GE1_RXEN	GE1_RXEN	M
								GE1_RXD1	GE1_RXD2	GE1_RXD0	GE1_RXCLK	GE1_RXCLK	N
								REQ2_N	GE1_RXDV	GNT2_N	INTB_N	INTB_N	P
								SERR_N	REQ1_N	GNT1_N	PCICLK	PCICLK	R
								STOP_N	PAR	PERR_N	INTA_N	INTA_N	T
								FRAME_N	IRDY_N	TRDY_N	DEVSEL_N	DEVSEL_N	U
								CBE0_N	CBE1_N	CBE2_N	CBE3_N	CBE3_N	V
								IDSEL	AD29	AD30	AD31	AD31	W
								AD28	AD25	AD26	AD27	AD27	Y
DDR_IOL_V33D	DCDC_VSSD	EXTMOS_LDO	DCDC_V33A	GND	AD0	AD4	AD8	AD12	AD16	AD20	AD24	AD24	AA
DDR_IO_V33D	DCDC_V33D	LDO_V26A	VFB_1P2	OUT_1P8	GND	AD3	AD7	AD11	AD15	AD19	AD23	AD23	AB
SOC_IO_V33D	LGATE	DCDC_VSSA	COMP	VOUT_1P2	LDO_V15A	AD2	AD6	AD10	AD14	AD18	AD22	AD22	AC
SOC_IO_V33D	UGATE	DIS_SW	FB	VOUT_1P2	LDO_V15A	AD1	AD5	AD9	AD13	AD17	AD21	AD21	AD

## 1.2 Pin Description

Pin	Name	I/O/IPU/IPD	Driving	Description
<b>JTAG interfaces: 5 pins</b>				
G13	JTAG_TRST_N	I, IPU	4mA	JTAG TRST (active low)
G9	JTAG_TCLK	I, IPD	4mA	JTAG TCLK
H11	JTAG_TMS	I, IPD	4mA	JTAG TMS
G8	JTAG_TDI	I, IPD	4mA	JTAG TDI
G10	JTAG_TDO	O, IPD	4mA	JTAG TDO
<b>UART Lite interface: 2 pins</b>				
M8	RXD2	I, IPU	4mA	UART Lite RXD
J8	TXD2	O, IPD	4mA	UART Lite TXD
<b>UART Full interface: 8 pins</b>				
P8	RXD	I, IPD	4mA	UART RXD.
N8	RIN	I, IPD	4mA	UART RIN.
N9	CTS_N	I, IPD	4mA	UART CTS_N.
M9	DSR_N	I, IPD	4mA	UART DSR_N.
R8	DCD_N	I, IPD	4mA	UART DCD_N.
P9	TXD	O, IPD	4mA	UART TXD.
U12	DTR_N	O, IPD	4mA	UART DTR.
U11	RTS_N	O, IPD	4mA	UART RTS.
<b>SPI/EEPROM interface: 5 pins</b>				
L16	SPI_MISO	I, IPD	4mA	SPI master in slave out
L17	SPI莫斯	O, IPD	4mA	SPI master out slave in
K17	SPI_CLK	O, IPD	4mA	SPI clock
J17	SPI_CS0	O, IPD	4mA	SPI chip select0
K16	SPI_CS1	O, IPD	4mA	SPI chip select1
<b>I2C interface: 2 pins</b>				
V12	I2C_SCLK	I/O, IPU	4mA	I2C Clock
V10	I2C_SD	O, IPU	4mA	I2C Data
<b>RGMII/MII interface: 24 pins (2.5v or 3.3v)</b>				
N24	GE1_RXCLK	I/O, IPD	8mA	RGMII1 /GMII RX Clock
P22	GE1_RXDV	I, IPD	8mA	RGMII1 /GMII RX Data Valid
N23	GE1_RXD0	I, IPD	8mA	RGMII1 RX Data bit #0/GMII RX Data bit #0
N21	GE1_RXD1	I, IPD	8mA	RGMII1 RX Data bit #1/GMII RX Data bit #1
N22	GE1_RXD2	I, IPD	8mA	RGMII1 RX Data bit #2/GMII RX Data bit #2
M23	GE1_RXD3	I, IPD	8mA	RGMII1 RX Data bit #3/GMII RX Data bit #3
L24	GE1_TXCLK	I/O, IPD	8mA	RGMII1 /GMII TX Clock
M24	GE1_TXEN	O, IPD	8mA	RGMII1 /GMII TX Data Valid
M22	GE1_RXD0	O, IPD	8mA	RGMII1 TX Data bit #0/GMII TX Data bit #0
M21	GE1_RXD1	O, IPD	8mA	RGMII1 TX Data bit #1/GMII TX Data bit #1
L23	GE1_RXD2	O, IPD	8mA	RGMII1 TX Data bit #2/GMII TX Data bit #2
L22	GE1_RXD3	O, IPD	8mA	RGMII1 TX Data bit #3/GMII TX Data bit #3
E24	GE2_RXCLK	I/O, IPD	8mA	RGMII2 RX Clock
F21	GE2_RXDV	I, IPD	8mA	RGMII2 RX Data Valid
E23	GE2_RXD0	I, IPD	8mA	RGMII2 RX Data bit #0/GMII RX Data bit #4
G21	GE2_RXD1	I, IPD	8mA	RGMII2 RX Data bit #1/GMII RX Data bit #5
E22	GE2_RXD2	I, IPD	8mA	RGMII2 RX Data bit #2/GMII RX Data bit #6
F22	GE2_RXD3	I, IPD	8mA	RGMII2 RX Data bit #3/GMII RX Data bit #7
C24	GE2_TXCLK	I/O, IPD	8mA	RGMII2 TX Clock
D24	GE2_TXEN	O, IPD	8mA	RGMII2 TX Data Valid
D23	GE2_RXD0	O, IPD	8mA	RGMII2 TX Data bit #0/GMII TX Data bit #4

Pin	Name	I/O/IPU/IPD	Driving	Description
E21	GE2_TXD1	O, IPD	8mA	RGMII2 TX Data bit #1/GMII TX Data bit #5
C23	GE2_TXD2	O, IPD	8mA	RGMII2 TX Data bit #2/GMII TX Data bit #6
D22	GE2_TXD3	O, IPD	8mA	RGMII2 TX Data bit #3/GMII TX Data bit #7
PHY Management interface: 2 pins (2.5v or 3.3v)				
R17	MDC	O, IPD	8mA	PHY Management Clock. Shared with GPIO23
P17	MDIO	I/O, IPD	8mA	PHY Management Data. Shared with GPIO22
GPIO interface: 8 pins				
K9	GPIO0	I/O, IPD	8mA	GPIO0
K8	GPIO1	I/O, IPD	8mA	GPIO1/ REF_CLK0
L9	GPIO2	I/O, IPU	8mA	GPIO2/ WATCH DOG RESET
L8	GPIO3	I/O, IPD	8mA	GPIO3/BT_ACT (Blue tooth active; can be treated as a request)
G14	GPIO4	I/O, IPD	8mA	GPIO4/BT_STATE (TX or RX) <i>(Default is OUTPUT)</i>
H14	GPIO5	I/O, IPD	8mA	GPIO5/BT_FREQ (Blue tooth overlap WLAN band or not) <i>(Default is OUTPUT)</i>
H12	GPIO6	I/O, IPD	8mA	GPIO6/BT_WLAN_ACT (WLAN is active; can be treated as a grant) <i>(Default is OUTPUT)</i>
H13	GPIO7	I/O, IPD	8mA	GPIO7/BT_ANT_SEL (Antenna select) <i>(Default is OUTPUT)</i>
Misc signals: 10 pins				
V11	PORST_N	I, IPU	4mA	Power on reset
V9	WLAN_LED_N	O, IPD	4mA	WLAN Activity LED
C12	LNA_PE_A0	O, IPD	16mA	LNA power enable for 5G BAND#0
B12	LNA_PE_A1	O, IPD	16mA	LNA power enable for 5G BAND#1
D12	LNA_PE_A2	O, IPD	16mA	LNA power enable for 5G BAND#2
C11	LNA_PE_G0	O, IPD	16mA	LNA power enable for 2.4G BAND#0
D11	LNA_PE_G1	O, IPD	16mA	LNA power enable for 2.4G BAND#1
B10	LNA_PE_G2	O, IPD	16mA	LNA power enable for 2.4G BAND#2
A11	ANT_TRN	O, IPD	8mA	Positive signal for antenna T/R switch
B11	ANT_TRNB	O, IPD	8mA	Negative signal for antenna T/R switch
USB PHY interface: 14 pins				
H24	UPHY0_VDDA_V33A	P		3.3v USB PHY analog power supply
H21	UPHY0_VDDL_V12D	P		1.2v USB PHY digital power supply
L21	UPHY0_VRES	I/O		Connect to an external 8.2K Ohm resistor for band-gap reference circuit
K21	UPHY0_VBUS	I/O		USB VBUS pin; Connect to the VBUS pin of the USB connector
J24	UPHY0_PADM	I/O		USB data pin Data-
J23	UPHY0_PADP	I/O		USB data pin Data+
J22	UPHY0_ID	I/O		USB ID pin. Connect to ID pin on the Mini-type connect
H23	UPHY1_VDDA_V33A	P		3.3v USB PHY analog power supply
G22	UPHY1_VDDL_V12D	P		1.2v USB PHY digital power supply
H22	UPHY1_VRES	I/O		Connect to an external 8.2K Ohm resistor for band-gap reference circuit
F24	UPHY1_VBUS	I/O		USB VBUS pin; Connect to the VBUS pin of the USB connector

Pin	Name	I/O/IPU/IPD	Driving	Description
G24	UPHY1_PADM	I/O		USB data pin Data-
G23	UPHY1_PADP	I/O		USB data pin Data+
F23	UPHY1_ID	I/O		USB ID pin. Connect to ID pin on the Mini-type connect
PCI Host/Device & Flash Interface: 53 pins				
R24	PCICLK	I/O	24mA	PCI clock
V17	RST_N	I/O	24mA	PCI reset
T24	INTA_N	I/O	24mA	PCI interrupt for slot #1
P24	INTB_N	I/O	24mA	PCI interrupt for slot #2
R22	REQ1_N	I/O	24mA	PCI bus request for slot #1
P21	REQ2_N	I/O	24mA	PCI bus request for slot #2
R23	GNT1_N	I/O	24mA	PCI bus grant for slot #1
P23	GNT2_N	I/O	24mA	PCI bus grant for slot #2
V24	CBE3_N	I/O	24mA	PCI bus command and byte enable
V23	CBE2_N	I/O	24mA	PCI bus command and byte enable
V22	CBE1_N	I/O	24mA	PCI bus command and byte enable
V21	CBE0_N	I/O	24mA	PCI bus command and byte enable
W21	IDSEL	I	24mA	PCI initialization device select
T22	PAR	I/O	24mA	PCI parity
U22	IRDY_N	I/O	24mA	PCI initiator ready
U21	FRAME_N	I/O	24mA	PCI cycle frame
U23	TRDY_N	I/O	24mA	PCI target ready
R21	SERR_N	I/O	24mA	PCI system error
T21	STOP_N	I/O	24mA	PCI target stop
T23	PERR_N	I/O	24mA	PCI parity error
U24	DEVSEL_N	I/O	24mA	PCI device select
W24	AD31	I/O	24mA	PCI address and data
W23	AD30	I/O	24mA	PCI address and data
W22	AD29	I/O	24mA	PCI address and data
Y21	AD28	I/O	24mA	PCI address and data
Y24	AD27	I/O	24mA	PCI address and data
Y23	AD26	I/O	24mA	PCI address and data
Y22	AD25	I/O	24mA	PCI address and data
AA24	AD24	I/O	24mA	PCI address and data
AB24	AD23	I/O	24mA	PCI address and data
AC24	AD22	I/O	24mA	PCI address and data
AD24	AD21	I/O	24mA	PCI address and data
AA23	AD20	I/O	24mA	PCI address and data
AB23	AD19	I/O	24mA	PCI address and data
AC23	AD18	I/O	24mA	PCI address and data
AD23	AD17	I/O	24mA	PCI address and data
AA22	AD16	I/O	24mA	PCI address and data
AB22	AD15	I/O	24mA	PCI address and data
AC22	AD14	I/O	24mA	PCI address and data
AD22	AD13	I/O	24mA	PCI address and data
AA21	AD12	I/O	24mA	PCI address and data
AB21	AD11	I/O	24mA	PCI address and data
AC21	AD10	I/O	24mA	PCI address and data
AD21	AD9	I/O	24mA	PCI address and data
AA20	AD8	I/O	24mA	PCI address and data
AB20	AD7	I/O	24mA	PCI address and data

Pin	Name	I/O/IPU/IPD	Driving	Description
AC20	AD6	I/O	24mA	PCI address and data
AD20	AD5	I/O	24mA	PCI address and data
AA19	AD4	I/O	24mA	PCI address and data
AB19	AD3	I/O	24mA	PCI address and data
AC19	AD2	I/O	24mA	PCI address and data
AD19	AD1	I/O	24mA	PCI address and data
AA18	AD0	I/O	24mA	PCI address and data
PCIe interface: 12 pins				
C22	PCIE_VP	P		1.2V power
A22	PCIE_25	P		3.3V power
A23	TX0_M	O		PCIE's TX-
A24	TX0_P	O		PCIE's TX+
A21	RX0_P	I		PCIE's Rx+
B21	RX0_M	I		PCIE's Rx-
C20	PCIE_REXT	I		Connect to external 190ohm resistor
A19	REFCLK_P	I		PCIe's REFCLK+
B19	REFCLK_M	I		PCIe's REFCLK-
A22	PCIE_25	P		3.3V power
C22	PCIE_VP	P		1.2V power
G17	PERST_N	I, IPU		PCIE reset
SDRAM/DDR2 Interface: 64 pins				
AD11	MD31	I/O	8mA	SDRAM/DDR2 Data bit #31
AB11	MD30	I/O	8mA	SDRAM/DDR2 Data bit #30
AC11	MD29	I/O	8mA	SDRAM/DDR2 Data bit #29
AA11	MD28	I/O	8mA	SDRAM/DDR2 Data bit #28
AD10	MD27	I/O	8mA	SDRAM/DDR2 Data bit #27
AB10	MD26	I/O	8mA	SDRAM/DDR2 Data bit #26
AC10	MD25	I/O	8mA	SDRAM/DDR2 Data bit #25
AA10	MD24	I/O	8mA	SDRAM/DDR2 Data bit #24
AD8	MD23	I/O	8mA	SDRAM/DDR2 Data bit #23
AB8	MD22	I/O	8mA	SDRAM/DDR2 Data bit #22
AC8	MD21	I/O	8mA	SDRAM/DDR2 Data bit #21
AA8	MD20	I/O	8mA	SDRAM/DDR2 Data bit #20
AD7	MD19	I/O	8mA	SDRAM/DDR2 Data bit #19
AB7	MD18	I/O	8mA	SDRAM/DDR2 Data bit #18
AC7	MD17	I/O	8mA	SDRAM/DDR2 Data bit #17
AA7	MD16	I/O	8mA	SDRAM/DDR2 Data bit #16
V2	MD15	I/O	8mA	SDRAM/DDR2 Data bit #15
V1	MD14	I/O	8mA	SDRAM/DDR2 Data bit #14
U2	MD13	I/O	8mA	SDRAM/DDR2 Data bit #13
U1	MD12	I/O	8mA	SDRAM/DDR2 Data bit #12
T4	MD11	I/O	8mA	SDRAM/DDR2 Data bit #11
U3	MD10	I/O	8mA	SDRAM/DDR2 Data bit #10
R4	MD9	I/O	8mA	SDRAM/DDR2 Data bit #9
T3	MD8	I/O	8mA	SDRAM/DDR2 Data bit #8
R2	MD7	I/O	8mA	SDRAM/DDR2 Data bit #7
R1	MD6	I/O	8mA	SDRAM/DDR2 Data bit #6
N4	MD5	I/O	8mA	SDRAM/DDR2 Data bit #5
P2	MD4	I/O	8mA	SDRAM/DDR2 Data bit #4
P1	MD3	I/O	8mA	SDRAM/DDR2 Data bit #3
P3	MD2	I/O	8mA	SDRAM/DDR2 Data bit #2

Pin	Name	I/O/IPU/IPD	Driving	Description
N3	MD1	I/O	8mA	SDRAM/DDR2 Data bit #1
M4	MD0	I/O	8mA	SDRAM/DDR2 Data bit #0
AD5	MA13	I/O , IPD	8mA	DDR2 Address bit #13
AD6	MA12	I/O , IPD	8mA	SDRAM/DDR2 Address bit #12
AC6	MA11	I/O , IPD	8mA	SDRAM/DDR2 Address bit #11
AB6	MA10	I/O , IPD	8mA	SDRAM/DDR2 Address bit #10
AD4	MA9	I/O , IPD	8mA	SDRAM/DDR2 Address bit #9
AC5	MA8	I/O , IPD	8mA	SDRAM/DDR2 Address bit #8
AD3	MA7	I/O , IPD	8mA	SDRAM/DDR2 Address bit #7
AC4	MA6	I/O , IPD	8mA	SDRAM/DDR2 Address bit #6
AB5	MA5	I/O , IPD	8mA	SDRAM/DDR2 Address bit #5
AA6	MA4	I/O , IPD	8mA	SDRAM/DDR2 Address bit #4
AD2	MA3	I/O , IPD	8mA	SDRAM/DDR2 Address bit #3
AC3	MA2	I/O , IPD	8mA	SDRAM/DDR2 Address bit #2
AA5	MA1	I/O , IPD	8mA	SDRAM/DDR2 Address bit #1
AB4	MA0	I/O , IPD	8mA	SDRAM/DDR2 Address bit #0
AC2	MBA2	I/O	8mA	DDR2 MBA #2
AC1	MBA1	I/O	8mA	SDRAM/DDR2 MBA #1
Y3	MBA0	I/O	8mA	SDRAM/DDR2 MBA #0
V4	MRAS_N	I/O	8mA	SDRAM/DDR2 MRAS_N
U4	MCAS_N	I/O	8mA	SDRAM/DDR2 MCAS_N
W4	MWE_N	I/O	8mA	SDRAM/DDR2 MWE_N
Y1	MCK_P	I/O	8mA	SDRAM MCK/DDR2 MCK_P
Y2	MCK_N	I/O	8mA	DDR2 MCK_N
AD9	MDQM3	I/O	8mA	SDRAM MDQM#3/DDR2 MDM#3
AA9	MDQM2	I/O	8mA	SDRAM MDQM#2/DDR2 MDM#2
T2	MDQM1	I/O	8mA	SDRAM MDQM#1/DDR2 MDM#1
P4	MDQM0	I/O	8mA	SDRAM MDQM#0/DDR2 MDM#0
AD1	MCS_N	I/O	8mA	SDRAM/DDR2 MCS_N
AC9	MDQS3	I/O	8mA	DDR2 MDQS#3
AB9	MDQS2	I/O	8mA	DDR2 MDQS#2
T1	MDQS1	I/O	8mA	DDR2 MDQS#1
R3	MDQS0	I/O	8mA	DDR2 MDQS#0
W3	MCKE	I/O	8mA	DDR2 MCKE
LDO pins: 17 pins				
AD15	DIS_SW			SW or LDO select (default floating-->enable the SW regulator)
AB14	DCDC_V33D	P		
AC14	LGATE			Gate drive for external lower MOSFET
AA14	DCDC_VSSD	GND		
AD14	UGATE			Gate drive for external upper MOSFET
AC15	DCDC_VSSA	GND		
AD16	FB			SW regulator feedback voltage (0.75v) and feedback compensation network of the error amplifier.
AC16	COMP			This pin is the error amplifier output and combination with the FB pin, to compensate the voltage-control
AA15	EXTMOS_LDO			Gate drive for external MOSFET or BJT
AA16	DCDC_V33A	P		3.3v analog power
AB16	VFB_1P2	P		1.2v regulation output feedback

Pin	Name	I/O/IPU/IPD	Driving	Description
AB15	LDO_V26A	P		2.6v power supply for DDR LDO (2.6v get from external diode by 3.3v supply)
AB17	OUT_1P8	P		LDO output voltage 1.8v
AC17,AD17	VOUT_1P2	P		1.2v regulation output
AC18,AD18	LDO_V15A	P		1.5v power input for internal MOS
PLL interface: 4 pins				
H10	CPLL_DVDD_V12D	P		1.2V digital power supply to PLL
C10	CPLL_AVDD_V12A	P		1..2V analog power supply to PLL
J11	BPLL_DVDD_V12D	P		1.2V digital power supply to PLL
D10	BPLL_AVDD_V12A	P		1..2V analog power supply to PLL
PCIe clock gen pins: 9 pins				
C13	PCIE_VCCA33DR	P		PCIECG Driver 3.3V analog power
A12	PCIE_VCCA33CG	P		PCIECG PLL/BIAS 3.3V analog power
D13	PCIE_VCCA12CG	P		PCIECG PLL 1.2V clean digital power
A13	PCIE_CGREXT	O		Connect external 11.8Kohm resistor with 1% mismatch to ground on package
D15	PCIE_CGTEST	O		Test analog output
B17	PCIE_PEXCLKPO	O		External positive PEXCLK #0
A17	PCIE_PEXCLKNO	O		External negative PEXCLK #0
B15	PCIE_PEXCLKP1	O		External positive PEXCLK #1
A15	PCIE_PEXCLKN1	O		External negative PEXCLK #1
RF pins: 56 pins				
D1	RF0_RF2G_INP	I		2.4GHz RX0 input (positive)
D2	RF0_RF2G_INN	I		2.4GHz RX0 input (negative)
E1	RF0_RF5G_INP	I		5GHz RX0 input (positive)
E2	RF0_RF5G_INN	I		5GHz RX0 input (negative)
F2	RF0_RF2G_OUTP	O		2.4GHz TX0 output (positive)
G3	RF0_RF_V12A	P		1.2V Supply for RF channel 0
F1	RF0_RF5G_OUTP	O		5GHz TX0 output (positive)
H3	RF1_IF_V12A	P		1.2V Supply for LO & IF
G1	RF1_RF2G_INP	I		2.4GHz RX1 input (positive)
G2	RF1_RF2G_INN	I		2.4GHz RX1 input (negative)
H1	RF1_RF5G_INP	I		5GHz RX1 input (positive)
H2	RF1_RF5G_INN	I		5GHz RX1 input (negative)
J2	RF1_RF2G_OUTP	O		2.4GHz TX1 output (positive)
J3	RF1_RF_V12A	P		1.2V Supply for RF channel 1
J1	RF1_RF5G_OUTP	O		5GHz TX1 output (positive)
K3	RF2_IF_V12A	P		1.2V Supply for LO & IF
K1	RF2_RF2G_INP	I		2.4GHz RX2 input (positive)
K2	RF2_RF2G_INN	I		2.4GHz RX2 input (negative)
L1	RF2_RF5G_INP	I		5GHz RX2 input (positive)
L2	RF2_RF5G_INN	I		5GHz RX2 input (negative)
L3	RF2_RF_V12A	P		1.2V Supply for RF channel 2
A10	ADC_V12D	P		1.2V supply for ADC digital logics
C9	RF0_PA5_PE	O		0~3.3V control for external PA0 for 5G BAND(20mA)
D9	RF0_TSSI5_IN	I		TX signal strength monitor input0 for 5G BAND (0 ~3.3V)
B9	RF0_PA_PE	O		0 ~ 3.3V control for external PA0 for 2.4G BAND(20mA)
A9	RF0_TSSI_IN	I		TX signal strength monitor input0 for 2.4G

Pin	Name	I/O/IPU/IPD	Driving	Description
				BAND (0 ~ 3.3V)
C8	RF1_PA5_PE	O		0 ~ 3.3V control for external PA1 for 5G BAND(20mA)
D8	RF1_TSSI5_IN	I		TX signal strength monitor input1 for 5G BAND (0 ~ 3.3V)
B8	RF1_PA_PE	O		0 ~ 3.3V control for external PA1 for 2.4G BAND(20mA)
C7	RF1_TSSI_IN	I		TX signal strength monitor input1 for 2.4G BAND (0 ~ 3.3V)
B7	RF2_TSSI5_IN	I		TX signal strength monitor input2 for 5G BAND (0 ~ 3.3V)
D6	RF2_TSSI_IN	I		TX signal strength monitor input2 for 2.4G BAND (0 ~ 3.3V)
B6	RF_IO_V33A	P		3.3V supply
A8	ADC_V12A	P		1.2V supply for ADC analog blocks
A7	ADC_VREF	O		Auxiliary ADC reference voltage (p)
C5	BASE_TRX_QN	I/O		Baseband Q 20Mhz debug I/O (negative)
D5	BASE_TRX_QP	I/O		Baseband Q 20Mhz debug I/O (positive)
C4	BASE_TRX_IN	I/O		Baseband I 20Mhz debug I/O (negative)
D4	BASE_TRX_IP	I/O		Baseband I 20Mhz debug I/O (positive)
F4	RF_BB2_V12A	P		1.2V Supply for analog baseband
A5	BG_RES_12K	I/O		External reference resistor (12K ohm)
A6	BG_V33A	P		3.3V supply for band gap reference
B5	LDO_OUT1_V12A	O		LDO 1.2V 200mA output for RF core
B4	LDO_OUT2_V12A	O		LDO 1.2V 50mA output for RF PLL
C3	LDO_IN12_VX	I		LDO 1.5 ~ 2V 300mA input for RF core and PLL
A3	PLL_X1	I		Crystal oscillator input
A4	PLL_X2	O		Crystal oscillator output
B3	PLL_V12A	P		1.2V Supply for PL
A2	PLL_VC_CAP	I/O		PLL external loop filter
B2	VCO_LO_V12A	P		1.2V Supply for VCO output buffer
E3	RF_BB1_V12A	P		1.2V Supply for analog baseband
F3	RFO_IF_V12A	P		1.2V Supply for LO & IF
Other power pins: 25 pins				
AC13,AD13,V14 ,G15,T17	SOC_IO_V33D	P		3.3v digital I/O power supply
U9,G11,AA12, T14,U14,H15,N 16,N17,	SOC_CO_V12D	P		1.2v digital core power supply
Y4,AD12	DDR_IOR_V09D	P		0.9v(GND) reference voltage power supply for DDR2(SDR)
AA4,AA13	DDR_IOL_V33D	P		1.8V(3.3V) level shifter power supply for DDR2(SDR)
AB1,AB2,AB3, AB13	DDR_IO_V33D	P		1.8V(3.3V) I/O power supply for DDR2(SDR)
U8,V8,AB12, AC12	DDR_IOC_V12D	P		1.2v I/O core power supply for DDR2 and SDR
Ground pins: 127 pins				
A1,A14,A16,A18 A20,B1,B13, B14,B16,B18,	GND	G		Ground pin

Pin	Name	I/O/IPU/IPD	Driving	Description
B20,B22,B23, B24,C1,C14,C15 C16,C17,C18,C1 9,C2,C21,D14, D16,D18,D19, D20,D21,D3, E4,G16,G4,G5, G6,H16,H17,H4, H5,H6,H8,H9, J10,J12,J13,J14, J15,J16,J21,J4,J5 J6,J9,K10,K11, K12,K13,K14, K15,K22,K23, K24,K4,K5, L10,L11,L12,L13 L14,L15,L4,L5, M10,M11,M12, M13,M14,M15, M16,M17,M3, N1,N10,N11, N12,N13,N14, N15,N2,P10,P11 P12,P13,P14,P1 5,P16,R10,R11, R12,R13,R14, R15,R16,R9, T10,T11,T12, T13,T15,T16,T8, T9,U10,U13, U15,U16,U17, V13,V15,V16, W1,W2,AA1, AA17,AA2,AA3, AB18,				
				Total: 444pins

**Note:**

1. IPD means internal pull-down; IPU means internal pull-up; P means power.
2. GPIO4/5/6/7 default is output direction.
3. While GPIO2 acts as an output “WATCH DOG RESET” pin to reset external component, a pull-high resistance is necessary.

### 1.3 Pins Sharing Scheme

Some pins are shared with GPIO to provide maximum flexibility for system designers. The RT3662 provides up to 94 GPIO pins. Users can configure SYSCFG and GPIO MODE registers in the System Control block to specify the pin function. Unless it is stated otherwise, all GPIO pins are in input mode after reset.

GPIO share scheme:

I/O Pad Group	Normal Mode	GPIO Mode
RGMII1	GE1_RXCLK	GPIO#95
	GE1_RXDV	GPIO#94
	GE1_RXD3	GPIO#93
	GE1_RXD2	GPIO#92
	GE1_RXD1	GPIO#91
	GE1_RXD0	GPIO#90
	GE1_TXCLK	GPIO#89
	GE1_TXEN	GPIO#88
	GE1_TXD3	GPIO#87
	GE1_TXD2	GPIO#86
	GE1_TXD1	GPIO#85
	GE1_TXD0	GPIO#84
	GE2_RXCLK	GPIO#83
	GE2_RXDV	GPIO#82
RGMII2	GE2_RXD3	GPIO#81
	GE2_RXD2	GPIO#80
	GE2_RXD1	GPIO#79
	GE2_RXD0	GPIO#78
	GE2_TXCLK	GPIO#77
	GE2_TXEN	GPIO#76
	GE2_TXD3	GPIO#75
	GE2_TXD2	GPIO#74
	GE2_TXD1	GPIO#73
	GE2_TXD0	GPIO#72
PCI	{AD31:AD0}	GPIO#71~GPIO#40
LNA	LNA_PE_G2	GPIO#37
	LNA_PE_G1	GPIO#36
	LNA_PE_G0	GPIO#35
	LNA_PE_A2	GPIO#34
	LNA_PE_A1	GPIO#33
	LNA_PE_A0	GPIO#32
GPIO	{GPIO7:GPIO1}	GPIO#30~24
MDIO	MDC	GPIO#23
	MDIO	GPIO#22
JTAG	JTAG_TRST_N	GPIO#21
	JTAG_TCLK	GPIO#20
	JTAG_TMS	GPIO#19
	JTAG_TDI	GPIO#18
	JTAG_TDO	GPIO#17
UARTL	RXD2	GPIO#16
	TXD2	GPIO#15
UARTF	RIN	GPIO#14
	DSR_N	GPIO#13
	DCD_N	GPIO#12
	DTR_N	GPIO#11
	RXD	GPIO#10
	CTS_N	GPIO#9
	TXD	GPIO#8
	RTS_N	GPIO#7

SPI	SPI_MISO	GPIO#6
	SPI_MOSI	GPIO#5
	SPI_CLK	GPIO#4
	SPI_CS0	GPIO#3
I2C	I2C_SCLK	GPIO#2
	I2C_SD	GPIO#1
GPIO	GPIO0	GPIO#0

UARTF\_SHARE\_MODE: UART full pin share scheme

Pin Name \ I/O	3'b000 UARTF	3'b001 PCM, UARTF	3'b010 PCM, I2S	3'b011 I2S UARTF	3'b100 PCM, GPIO	3'b101 GPIO, UARTF	3'b110 GPIO I2S	3'b111 GPIO
RIN	RIN	PCMDTX	PCMDTX	RXD	PCMDTX	GPIO#14	GPIO#14	GPIO#14
DSR_N	DSR_N	PCMDRX	PCMDRX	CTS_N	PCMDRX	GPIO#13	GPIO#13	GPIO#13
DCD_N	DCD_N	PCMCLK	PCMCLK	TXD	PCMCLK	GPIO#12	GPIO#12	GPIO#12
DTR_N	DTR_N	PCMFS	PCMFS	RTS_N	PCMFS	GPIO#11	GPIO#11	GPIO#11
RXD	RXD	RXD	I2SSDI	I2SSDI	GPIO#10	RXD	I2SSDI	GPIO#10
CTS_N	CTS_N	CTS_N	I2SSDO	I2SSDO	GPIO#9	CTS_N	I2SSDO	GPIO#9
TXD	TXD	TXD	I2SWS	I2SWS	GPIO#8	TXD	I2SWS	GPIO#8
RTS_N	RTS_N	RTS_N	I2SCLK	I2SCLK	GPIO#7	RTS_N	I2SCLK	GPIO#7

PCM/I2S IO direction:

Pin Name \ I/O	I/O
PCMDTX	O
PCMDRX	I
PCMCLK	I/O
PCMFS	I/O
I2SSDI	I
I2SSDO	O
I2SWS	I/O
I2SCLK	/O

{GE1\_GPIO\_MODE, GE2\_GPIO\_MODE}: RGMII pin share scheme:

Pin Name \ I/O	2'b00 RGMII1, RGMII2	2'b01 RGMII1, GPIO	2'b10 GPIO, RGMII2	2'b11 (default) GPIO
GE1_RXCLK	GE1_RXCLK	GE1_RXCLK	GPIO#95	GPIO#95
GE1_RXDV	GE1_RXDV	GE1_RXDV	GPIO#94	GPIO#94
GE1_RXD0~3	GE1_RXD0~3	GE1_RXD0~3	GPIO#93~90	GPIO#93~90
GE1_TXCLK	GE1_TXCLK	GE1_TXCLK	GPIO#89	GPIO#89
GE1_TXDV	GE1_TXDV	GE1_TXDV	GPIO#88	GPIO#88
GE1_RXD0~3	GE1_RXD0~3	GE1_RXD0~3	GPIO#87~84	GPIO#87~84
GE2_RXCLK	GE2_RXCLK	GPIO#83	GE2_RXCLK	GPIO#83
GE2_RXDV	GE2_RXDV	GPIO#82	GE2_RXDV	GPIO#82
GE2_RXD0~3	GE2_RXD0~3	GPIO#81~78	GE2_RXD0~3	GPIO#81~78
GE2_TXCLK	GE2_TXCLK	GPIO#77	GE2_TXCLK	GPIO#77
GE2_TXDV	GE2_TXDV	GPIO#76	GE2_TXDV	GPIO#76
GE2_RXD0~3	GE2_RXD0~3	GPIO#75~72	GE2_RXD0~3	GPIO#75~72

PCI\_SHARE\_MODE: PCI pin sharing scheme:

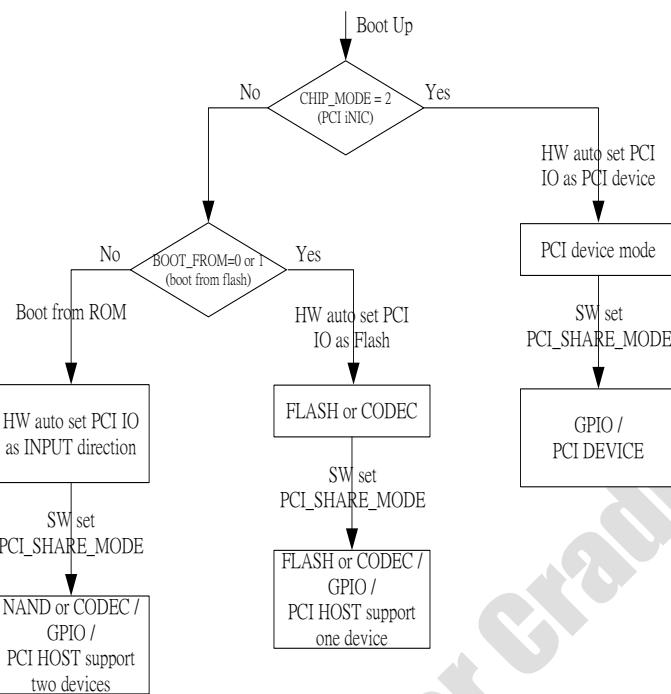


Fig. 1-3-1 PCI pin sharing scheme

Pin Name	3'b000 PCI Device	3'b001 PCI Host support two device	3'b010 PCI Host support one device	3'b011 FLASH/NAND/CODEC			3'b111 GPIO
				FLASH	NAND	CODEC	
PCICLK	PCICLK	PCICLK	PCICLK				CS0_N PCICLK
RST_N	RST_N	RST_N	RST_N				WR1_N RST_N
INTA_N	INTA_N	INTA_N	INTA_N				ACK0_N INTA_N
INTB_N	INTB_N	INTB_N	(FLASH_OE_N)	FLASH_OE_N	REN		INTB_N
REQ1_N	REQ1_N	REQ1_N	REQ1_N				ACK1_N REQ1_N
REQ2_N	REQ2_N	REQ2_N	(FLASH_CS_N)	FLASH_CS_N	NAND_CS_N		REQ2_N
GNT1_N	GNT1_N	GNT1_N	GNT1_N				CS1_N GNT1_N
GNT2_N	GNT2_N	GNT2_N	(FLASH_WE_N)	FLASH_WE_N	WEN		GNT2_N
CBE3_N	CBE3_N	CBE3_N	CBE3_N	ADDR12			DATA20 CBE3_N
CBE2_N	CBE2_N	CBE2_N	CBE2_N	ADDR13			DATA21 CBE2_N
CBE1_N	CBE1_N	CBE1_N	CBE1_N	ADDR14			DATA22 CBE1_N
CBE0_N	CBE0_N	CBE0_N	CBE0_N	ADDR15			DATA23 CBE0_N
IDSEL	IDSEL	IDSEL	IDSEL				DREQ0_N IDSEL
PAR	PAR	PAR	PAR	ADDR8			DATA16 PAR
IRDY_N	IRDY_N	IRDY_N	IRDY_N	ADDR20			DATA28 IRDY_N
FRAME_N	FRAME_N	FRAME_N	FRAME_N	ADDR21			DATA29 FRAME_N
TRDY_N	TRDY_N	TRDY_N	TRDY_N	ADDR18			DATA26 TRDY_N
SERR_N	SERR_N	SERR_N	SERR_N				WR0_N SERR_N
STOP_N	STOP_N	STOP_N	STOP_N	ADDR19			DATA27 STOP_N
PERR_N	PERR_N	PERR_N	PERR_N				RD0_N PERR_N
DEVSEL_N	DEVSEL_N	DEVSEL_N	DEVSEL_N				DACK0_N DEVSEL_N
AD31	AD31	AD31	AD31	DATA10			DATA10 GPIO#71
AD30	AD30	AD30	AD30	DATA9			DATA9 GPIO#70
AD29	AD29	AD29	AD29	DATA1	DATA1	DATA1	GPIO#69

AD28	AD28	AD28	AD28	DATA8		DATA8	GPIO#68
AD27	AD27	AD27	AD27	DATA0	DATA0	DATA0	GPIO#67
AD26	AD26	AD26	AD26	ADDR0		ADDR0	GPIO#66
AD25	AD25	AD25	AD25	ADDR1		ADDR1	GPIO#65
AD24	AD24	AD24	AD24	ADDR2		ADDR2	GPIO#64
AD23	AD23	AD23	AD23	ADDR3		ADDR3	GPIO#63
AD22	AD22	AD22	AD22	ADDR4	WPN	ADDR4	GPIO#62
AD21	AD21	AD21	AD21	ADDR5	CLE	ADDR5	GPIO#61
AD20	AD20	AD20	AD20	ADDR6	ALE	ADDR6	GPIO#60
AD19	AD19	AD19	AD19	ADDR22		DATA30	GPIO#59
AD18	AD18	AD18	AD18	ADDR7	RB		GPIO#58
AD17	AD17	AD17	AD17	DATA14		DATA14	GPIO#57
AD16	AD16	AD16	AD16	ADDR17		DATA25	GPIO#56
AD15	AD15	AD15	AD15	ADDR23		DATA31	GPIO#55
AD14	AD14	AD14	AD14	ADDR9		DATA17	GPIO#54
AD13	AD13	AD13	AD13	SRAM_CS_N			GPIO#53
AD12	AD12	AD12	AD12	ADDR11		DATA19	GPIO#52
AD11	AD11	AD11	AD11	DATA2	DATA2	DATA2	GPIO#51
AD10	AD10	AD10	AD10	ADDR16		DATA24	GPIO#50
AD9	AD9	AD9	AD9	ADDR10		DATA18	GPIO#49
AD8	AD8	AD8	AD8	DATA15		DATA15	GPIO#48
AD7	AD7	AD7	AD7	DATA7	DATA7	DATA7	GPIO#47
AD6	AD6	AD6	AD6	DATA13		DATA13	GPIO#46
AD5	AD5	AD5	AD5	DATA6	DATA6	DATA6	GPIO#45
AD4	AD4	AD4	AD4	DATA12		DATA12	GPIO#44
AD3	AD3	AD3	AD3	DATA5	DATA5	DATA5	GPIO#43
AD2	AD2	AD2	AD2	DATA11		DATA11	GPIO#42
AD1	AD1	AD1	AD1	DATA4	DATA4	DATA4	GPIO#41
AD0	AD0	AD0	AD0	DATA3	DATA3	DATA3	GPIO#40

FLASH/NAND/CODEC IO direction:

FLASH pin name	I/O	NAND pin name	I/O	CODEC pin name	I/O
FLASH_OE_N	O	NAND_CS_N	O	CS0_N	O
FLASH_CS_N	O	REN	O	WR0_N	O
FLASH_WE_N	O	WEN	O	RD0_N	O
SRAM_CS_N	O	WPN	O	ACK0_N	I
ADDR0~23	O	CLE	O	DREQ0_N	I
DATA0~15	I/O	ALE	O	DACK0_N	O
		RB	I	CS1_N	O
		DATA0~7	I/O	WR1_N	O
				ACK1_N	I
				ADDR0~6	O
				DATA0~31	I/O

LNA\_G\_SHARE\_MODE: LNA\_PE\_Gx share mode

Pin Name	2'b00 LNA_PE_Gx	2'b10 CODEC	2'b11 GPIO
LNA_PE_G0	LNA_PE_G0	RD1_N	GPIO#37
LNA_PE_G1	LNA_PE_G1	DREQ1_N	GPIO#36
LNA_PE_G2	LNA_PE_G2	DACK1_N	GPIO#35

## CODEC IO direction:

Pin Name	I/O
RD1_N	O
DREQ1_N	I
DACK1_N	O

## LNA\_A\_SHARE\_MODE: LNA\_PE\_Ax share mode

Pin Name	2'b00 LNA_PE_Ax	2'b10 CODEC	2'b11 GPIO
LNA_PE_A0	LNA_PE_A0	RD1_N	GPIO#34
LNA_PE_A1	LNA_PE_A1	DREQ1_N	GPIO#33
LNA_PE_A2	LNA_PE_A2	DACK1_N	GPIO#32

## :Notes:

1. All given GPIO are 4mA drive capable.
2. The default direction for GPIO pins are input (i.e. tri-state). Except these GPIO pins:  
- The GPIO17~21 shared with the JTAG interface. The default value for JTAG\_GPIO\_MODE is 0.

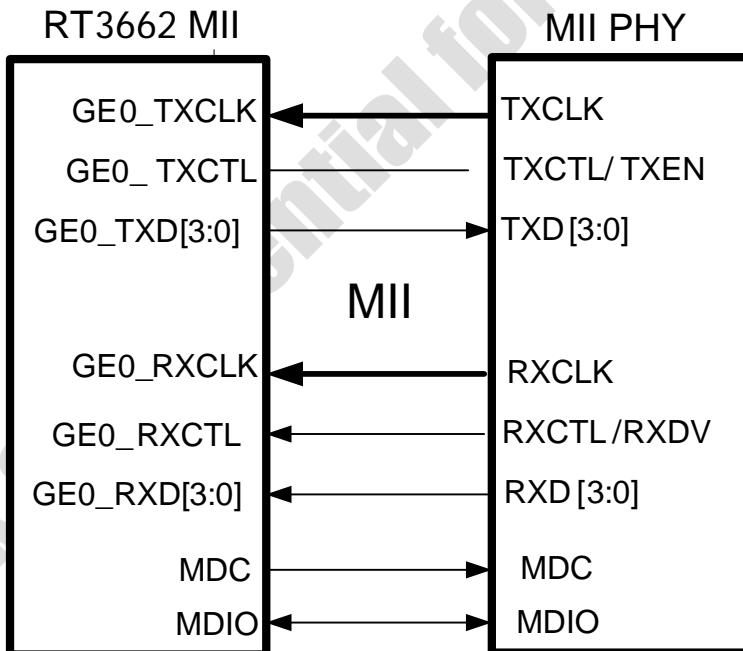


Fig. 1-3-2 RT3662 MII → MII PHY

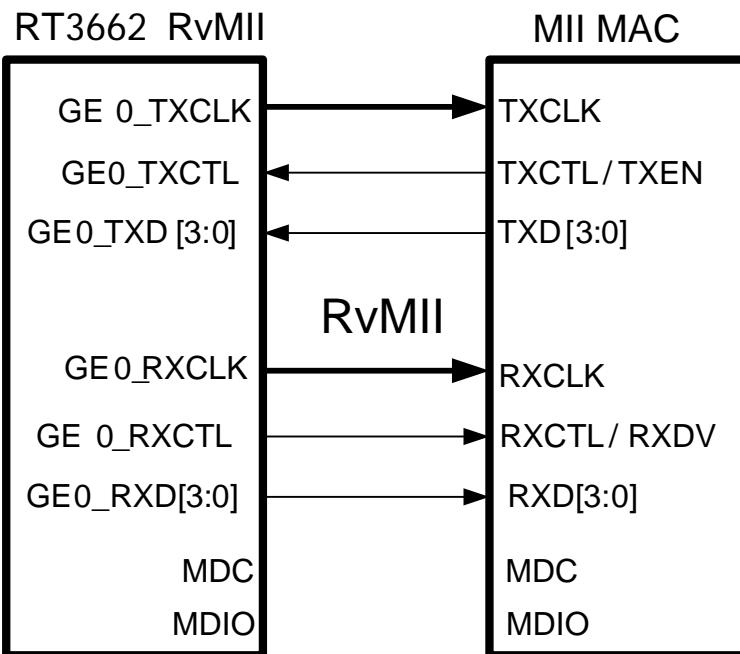


Fig. 1-3-3 RT3662 RvMII → MII MAC

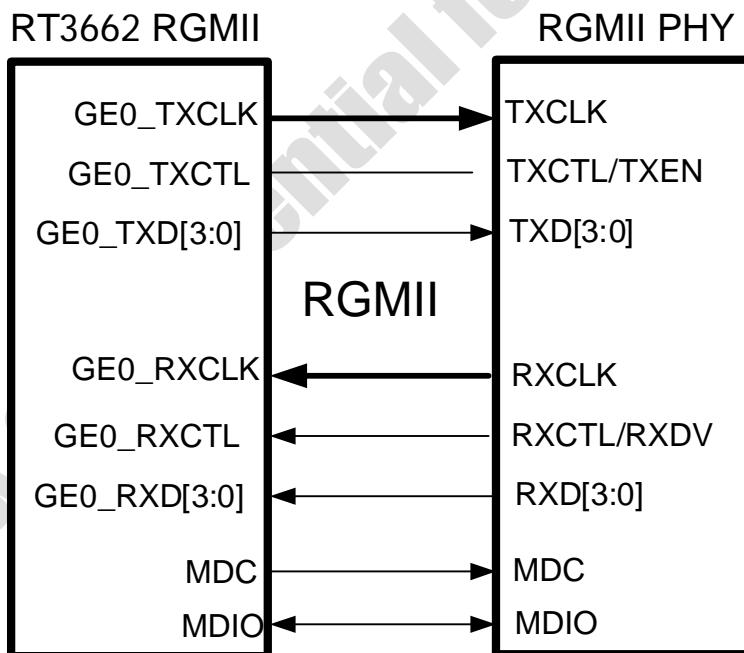


Fig. 1-3-4 RT3662 RGMII → RGMII PHY

### RT3662 RGMII                    RGMII MAC

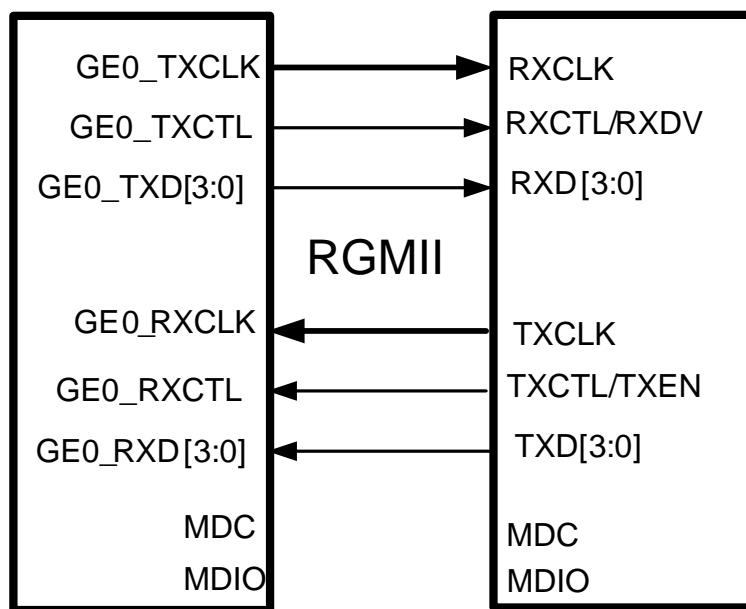


Fig. 1-3-5 RT3662 RGMII → RGMII MAC

### 1.4 Boot strapping description

From signal pad:

Pin Name	Boot Strapping Signal Name	Description
ANT_TRNB	BIGENDIAN	0: LITTLE ENDIAN 1: BIG ENDIAN
GPIO7	DRAM_FROM_EE	0: DRAM configuration from boot strapping. 1: DRAM configuration(size/width) from EEPROM
LNA_PE_A1	DRAM_TYPE	0: SDRAM 1: DDR2
LNA_PE_A0	DRAM_TOTAL_WIDTH	0: 16 1: 32
{LNA_PE_G2...LNA_PE_G0}	DRAM_SIZE (one dram cell)	0: 2MB 1: 8MB 2: 16MB 3: 32MB 4: 64MB 5: 128MB 6: 256MB
MDC	DRAM_WIDTH (one dram cell)	SDRAM(DDR2) 0: 16 (8) 1: 32 (16)
{GPIO5, GPIO4}	CPU_CLK_SEL[1:0]	3: 500 MHz (DDR2 166MHz / SDR 125MHz) (default) 2: 480 MHz (DDR2 160MHz / SDR 120MHz) 1: 384 MHz (DDR2 128MHz / SDR 96MHz) 0: 250 MHz (DDR2 125MHz / SDR 83MHz)
ANT_TRN	BYPASS_PLL	0: Do Not Bypass PLL (default) 1: Bypass PLL
{ GPIO6, WLAN_LED_N }	BOOT_FROM[1:0]	2'b00: boot from external 16-bit flash (default) 2'b01: boot from external 8-bit flash 2'b10/11: boot from internal ROM
{ SPI_CLK, SPI_MOSI , TXD2, TXD}	CHIP_MODE[3:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0: Normal mode (AP mode)(default) 1: iNIC-USB mode 2: iNIC-PCI mode 3: iNIC-PCIe mode 4: iNIC-RGMII mode (GE1) 5: iNIC-MII mode (GE1) 6: iNIC-RVMII mode (GE1) 7: AP – support boot from external serial flash 8: AP – support boot from external NAND flash 14:scan mode 15: test/debug mode

Note: 1. GE1/2 mode are defined in registers.

2. PCI/PCIe host/device mode are defined in registers.

3. SDRAM or DDR2 memory cell used is defined in a register bit.

4. When booting from 3'b000/3'b001/3'b010, all PCI I/O will be flash I/O only.  
(CHIP\_MODE should not be '2')

## 2 Maximum Ratings and Operating Conditions

### 2.1 Absolute Maximum Ratings

Supply Voltage .....	3.6V
Vcc to Vcc Decouple.....	-0.3 to +0.3V
Input, Output or I/O Voltage.....	GND -0.3V to Vcc+0.3V

### 2.2 Thermal Information

Maximum Junction Temperature (Plastic Package) .....	125°C
Maximum Lead Temperature (Soldering 10s).....	260°C

Thermal characteristics in still air condition

Thermal Resistance $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) for JEDEC 2L system PCB .....	54.3 $^{\circ}\text{C}/\text{W}$
Thermal Resistance $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) for JEDEC 4L system PCB .....	23.5 $^{\circ}\text{C}/\text{W}$
Thermal Resistance $\theta_{JC}$ ( $^{\circ}\text{C}/\text{W}$ ) for JEDEC 2L system PCB .....	6.9 $^{\circ}\text{C}/\text{W}$
Thermal Resistance $\theta_{JC}$ ( $^{\circ}\text{C}/\text{W}$ ) for JEDEC 4L system PCB .....	6.0 $^{\circ}\text{C}/\text{W}$
Thermal Characterization parameter $\Psi_{JT}$ ( $^{\circ}\text{C}/\text{W}$ ) for JEDEC 2L system PCB .....	2.1 $^{\circ}\text{C}/\text{W}$
Thermal Characterization parameter $\Psi_{JT}$ ( $^{\circ}\text{C}/\text{W}$ ) for JEDEC 4L system PCB .....	1.4 $^{\circ}\text{C}/\text{W}$

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4"x4.5")

### 2.3 Operating Conditions

Temperature Range .....	-10 to 70 $^{\circ}\text{C}$
Core Supply Voltage.....	1.2V +/- 5%
I/O Supply Voltage .....	3.3V +/- 10%

### 2.4 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0  $^{\circ}\text{C}$  and 40  $^{\circ}\text{C}$  at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- a) Mounted within 168-hours of factory conditions < 30  $^{\circ}\text{C} / 60\%$ RH
- b) Storage humidity needs to maintained at <10% RH
- c) Baking is necessary if customer expose the component to air over 168 hrs, baking condition: 125  $^{\circ}\text{C} / 8\text{hrs}$

### 2.5 External Xtal Specification

Frequency .....	40MHz
Frequency offset .....	+/- 20 ppm
VIH/VIL .....	Vcc-0.3V / 0.3V
Duty Cycle .....	45%~55%

### 2.6 DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc33		3.0	3.3	3.6	V
1.2V Supply Voltage	Vcc12		1.14	1.2	1.26	V
3.3V Current Consumption	Icc33			130		mA
1.5V Current Consumption	Icc15			1094		mA
1.8V Current Consumption	Icc18			182		mA

### 2.6.1 DC characteristics for GPIO pins with 4mA driving capability

Symbol	Parameter	Min	Normal	Max
VIH	Input High Voltage	2		5.5
VIL	Input Low Voltage	-0.3		0.8
VOH	Output High Voltage	2.4		
VOL	Output Low Voltage			0.4
IOH	High Level Output Current @VOH(min) (mA)	6.8	13.1	21.7
IOL	Low Level Output Current @VOL(max) (mA)	5.0	7.8	10.5

### 2.6.2 DC characteristics for GPIO pins with 8mA driving capability

Symbol	Parameter	Min	Normal	Max
VIH	Input High Voltage	2		5.5
VIL	Input Low Voltage	-0.3		0.8
VOH	Output High Voltage	2.4		
VOL	Output Low Voltage			0.4
IOH	High Level Output Current @VOH(min) (mA)	13.2	25.5	42.1
IOL	Low Level Output Current @VOL(max) (mA)	10.0	15.7	21.1

### 2.6.3 DC characteristics for RGMII related pins

Symbol	Parameter	Min	Normal	Max
VIH	Input High Voltage	2		5.5
VIL	Input Low Voltage	-0.3		0.8
VOH	Output High Voltage	2.4		
VOL	Output Low Voltage			0.4
IOH	High Level Output Current @VOH(min) (mA)	19.5	37.8	62.5
IOL	Low Level Output Current @VOL(max) (mA)	15.0	23.5	31.7

## 2.7 AC Electrical Characteristics

### 2.7.1 SDRAM Interface

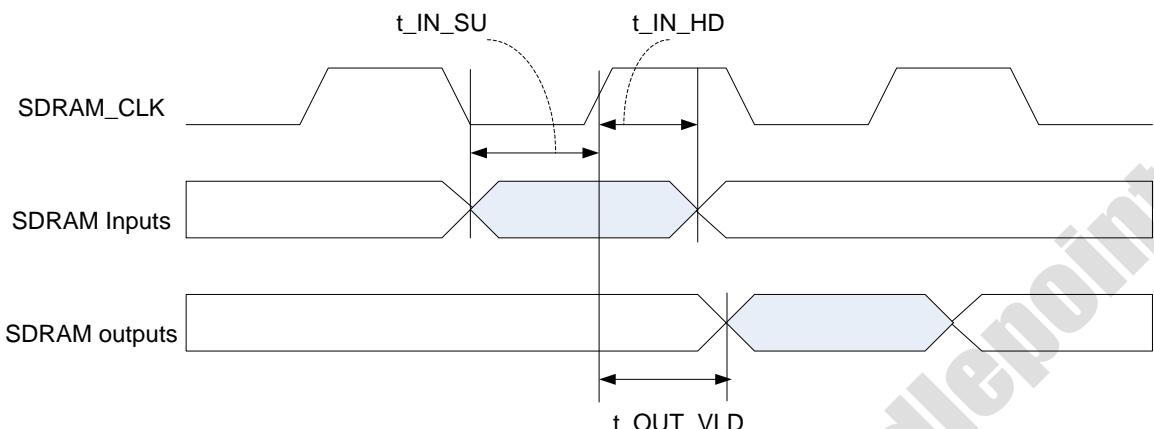


Fig. 2-7-1 SDRAM Interface

Symbol	Description	Min	Max	Unit	Remark
t_IN_SU	Setup time for Input signals (e.g. MD*)	1.5	-	ns	
t_IN_HD	Hold time for input signals	1.7	-	ns	
t_OUT_VLD	SDRAM_CLK to output signals (MA*, MD*, SDRAM_RAS_N,...) valid	0.8	5	ns	output load: 8pF

### 2.7.2 RGMII Interface

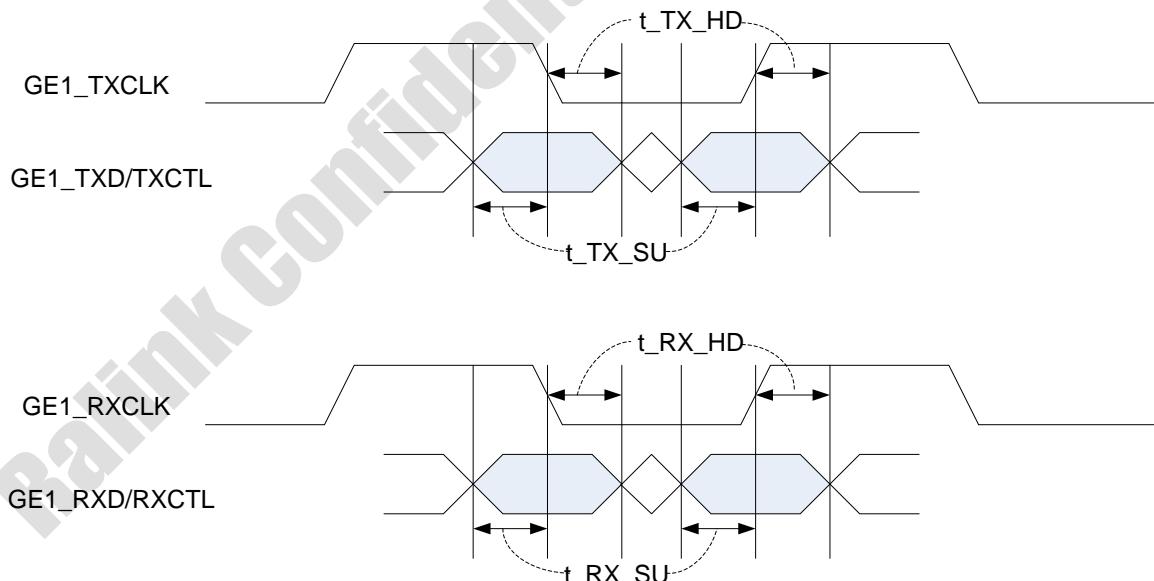
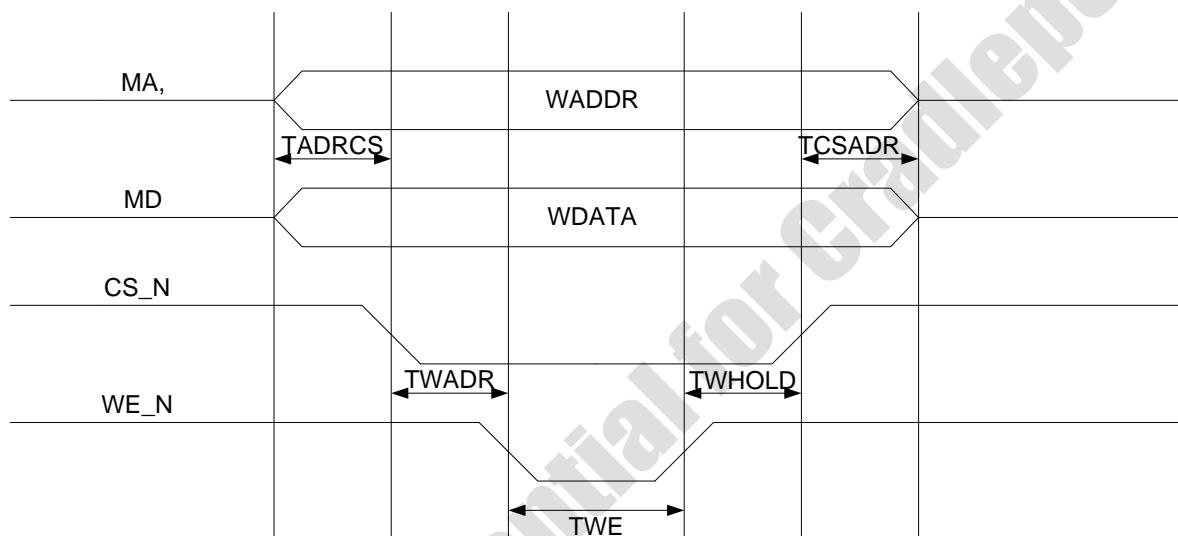


Fig. 2-7-2 RGMII Interface

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. GE1_TXD*, GE1_TXEN)	1.2	-	ns	output load : 5pF
t_RX_SU	Hold time for output signals	1.2	-	ns	output load : 5pF
t_RX_HD	Setup time for input signals (e.g. GE1_RXD*, GE1_RXDV)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

### 2.7.3 Flash/SRAM Interface

Flash, Async. SRAM Write Timing



Flash, Async. SRAM Read Timing

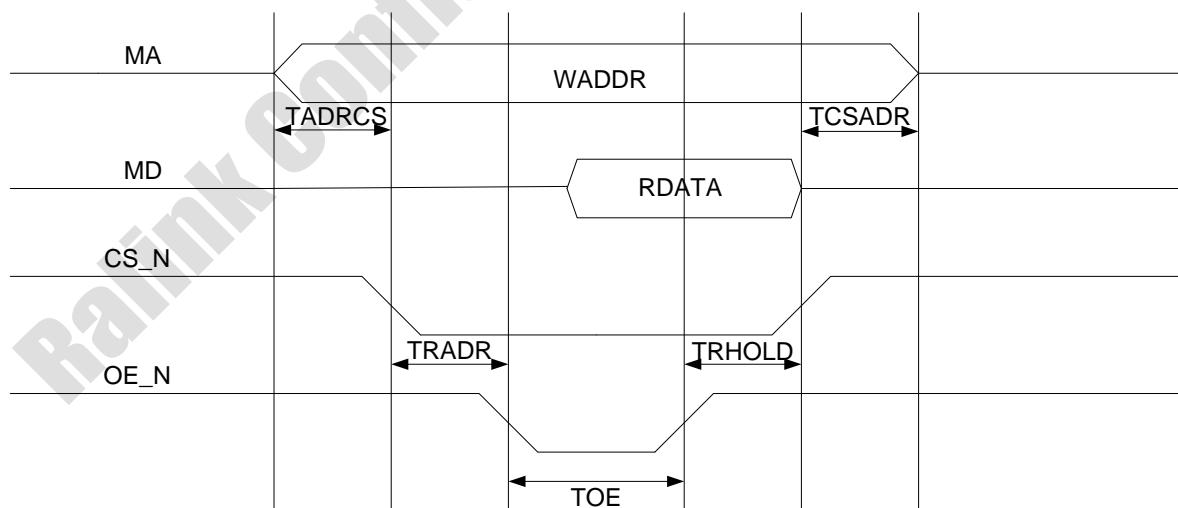


Fig. 2-7-3 Flash/SRAM Interface

Please refer to the "Memory Controller" section for more information about the timing set on the Flash/SRAM interface.

### 2.7.4 Power On Sequence

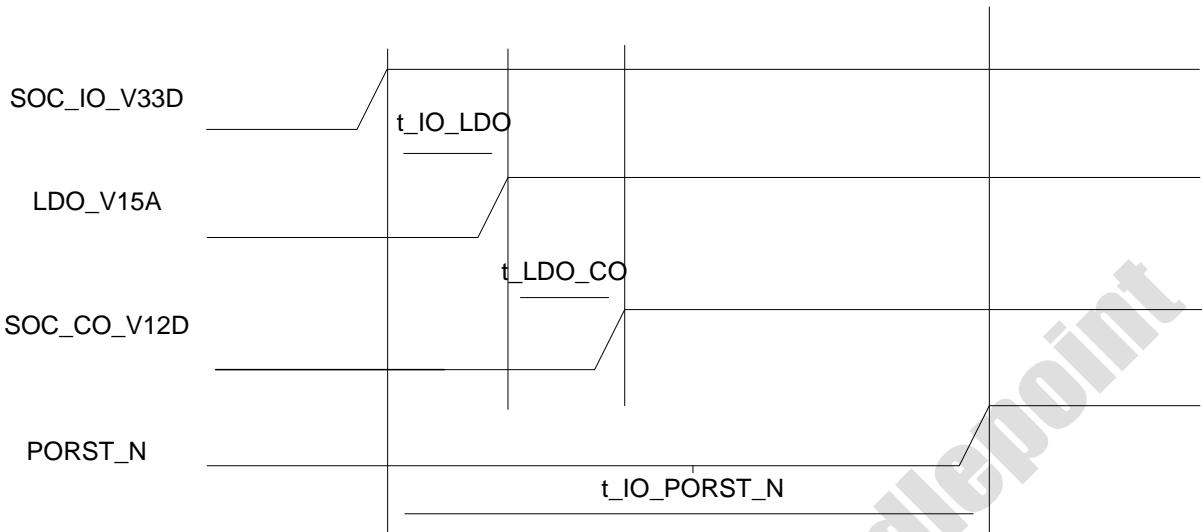


Fig. 2-7-4 Power ON Sequence

Symbol	Description	Min	Max	Unit	Remark
$t_{IO\_LDO}$	Time between ldo power on to io power on	1.5		ms	
$t_{LDO\_CO}$	Time between core power on to ldo power on	1.5		ms	
$t_{IO\_PORST\_N}$	Time between I/O power on to PORST_N de-assertion	10	-	ms	

### 3 Function Description

#### 3.1 Overview

The RT3662 SOC combines Ralink's 802.11n compliant 2T3R MAC/BBP/RF, a high performance 500-MHz MIPS74Kc CPU core and USB controller/PHY, , to enable a multitude of high performance, cost-effective 802.11n applications.

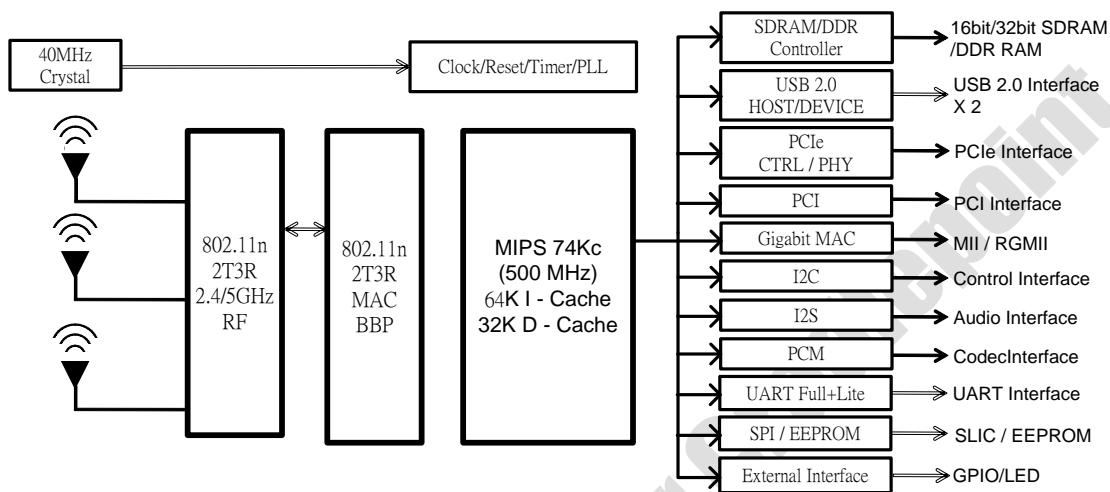


Fig. 3-1-1 RT3662 Block Diagram

There are x bus masters (MIPS 74K, USB , and 802.11n MAC/BBP/RF) in the RT3662 SoC on a high performance, low latency Rbus, (Ralink Bus). In addition, the RT3662 SoC supports lower speed peripherals such as UART, GPIO, and SPI via a low speed peripheral bus (Pbus).The Flash/SRAM/SDRAM controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

The RT3662 SoC embeds Ralink's market proven 802.11n 2T3R MAC/BBP/RF to provide a 450Mbps PHY rate on the wireless LAN interface. The MAC design employs a highly efficient DMA engine and hardware data processing accelerators, which free the CPU for user applications. The 802.11n 3TR MAC/BBP/RF is designed to support standards based features in the area of security, quality of service and international regulation resulting in an enhanced end user experience.

#### 3.2 Memory Map Summary

Start	End	Size	Description
0000.0000	-	0FFF.FFFF	256 M DDR2 256MB/SDRAM 128MB
1000.0000	-	1000.00FF	SYSCTL
1000.0100	-	1000.01FF	TIMER
1000.0200	-	1000.02FF	INTCTL
1000.0300	-	1000.03FF	MEM_CTRL (SDR/DDR2)
1000.0400	-	1000.04FF	<<Reserved>>
1000.0500	-	1000.05FF	UART
1000.0600	-	1000.06FF	PIO
1000.0700	-	1000.07FF	Flash Controller (NOR/SRAM)
1000.0800	-	1000.08FF	NAND Controller
1000.0900	-	1000.09FF	I2C
1000.0A00	-	1000.0AFF	I2S
1000.0B00	-	1000.0BFF	SPI

1000.0C00	-	1000.0CFF	256	UARTLITE
1000.0D00	-	1000.0DFF		<<Reserved>>
1000.2000	-	1000.27FF	2 K	PCM (up to 16 channel)
1000.2800	-	1000.2FFF	2 K	Generic DMA (up to 64 channel)
1000.3000	-	1000.37FF	2 K	CODEC 1
1000.3800	-	1000.3FFF	2 K	CODEC 2
1000.4000	-	100F.FFFF		<<Reserved>>
1010.0000	-	1010.FFFF	64 K	Frame Engine
1011.0000	-	1011.7FFF	32 K	<<Reserved>>
1011.8000		1011.BFFF	16 K	ROM
1011.C000	-	1011.FFFF	16 K	<<Reserved>>
1012.0000	-	1012.7FFF	16 K	USB Device
1012.8000	-	1012.FFFF	16 K	<<Reserved>>
1013.0000	-	1013.7FFF	32 K	<<Reserved>>
1013.8000	-	1013.FFFF	32 K	<<Reserved>>
1014.0000	-	1017.FFFF	256 K	PCI/ PCI Express
1018.0000	-	101B.FFFF	256 K	802.11n MAC/BBP
101C.0000	-	101F.FFFF	256 K	USB Host
1020.0000	-	1023.FFFF	256 K	<<Reserved>>
1024.0000	-	1027.FFFF	256 K	<<Reserved>>
1028.0000	-	1BFF.FFFF		<<Reserved>>
1C00.0000	-	1DFF.FFFF	16KB ROM or 32MB 16-bit Flash or 16MB 8-bit Flash	When BOOT_FROM = 3'b000, up-to 32MB external 16-bit flash is mapped.  When BOOT_FROM = 3'b001, up-to 16MB external 8-bit flash is mapped.  When BOOT_FROM = 3'b010/3'b011/3'b100, 16KB internal boot ROM is mapped.
1E00.0000	-	1FFF.FFFF		External SRAM/Flash
2000.0000	-	2FFF.FFFF	256 M	PCI/PCle Memory Space

Note:

### 3.3 MIPS 74K Processor

#### 3.3.1 Features

- 14-stage ALU and 15-stage AGEN pipelines
  - 12-stage ALU fetch and execution pipe
  - 13-stage AGEN fetch and execution pipe
  - Common 2-stage graduation pipe
- 32-bit address paths
- 128-bit data path for instruction cache and 64 or 128-bit data path for data cache
- 64-bit data paths to external interface
- MIPS32 Release2 Instruction Set and Privileged Resource Architecture
- MIPS16e Code Compression
- MIPS DSP ASE - Revision 2.0
  - 3 additional pairs of accumulator registers
  - Fractional data types (Q15, Q31)
  - Saturating arithmetic
  - SIMD instructions operate on 2×16 bit or 4×8 bit simultaneously
- Instruction Fetch Unit
  - 4 instruction fetch per cycle
  - 8-entry Return Prediction Stack
  - Combined Majority Branch Predictor using three 256-entry Branch History Tables (BHT)
  - Hardware prefetching of next 1 or 2 sequential cache lines on a miss. Number of prefetched lines (0, 1, or 2) controllable via configuration bits.
- Dual Out-of-Order Instruction Issue
  - Separate ALU and AGEN pipes
  - AGEN pipe executes load/store and control transfer instructions
  - ALU pipe executes all other instructions
  - 32 (18 ALU, 14 AGEN) completion buffers hold execution results until instructions are graduated in program order
- Programmable Memory Management Unit
  - 16/32/48/64 dual-entry, dual-ported TLB shared by Instruction and Data MMU
  - 4-entry ITLB (4KB, 1MB page size)
  - 4K, 16K, 64K, 256K, 1M, 4M, 16M, 64M, 256M byte page size supported in JTLB
  - Optional simple Fixed Mapping Translation (FMT) mechanism
- Programmable L1 Cache Sizes
  - Individually configurable instruction and data caches
  - Instruction Cache sizes of 0/16/32/64 KB
  - Data Cache sizes of 0/16/32/64 KB
  - 4-way set associative
  - 32-byte cache line size
  - Virtually indexed, physically tagged
  - Cache line locking support
  - Up to 4 outstanding I-cache misses
  - Virtual tag based hit prediction in data cache
  - Up to 4 unique outstanding D-cache misses and 9 total load misses
  - Write-back and write-through support in data cache
  - Non-blocking data cache prefetches
  - Optional parity support

- Scratchpad RAM support
  - Independent Instruction and Data Scratch- pad RAMs
  - Scratchpad RAM size from 4KB to 1MB
  - Independent of cache configuration
  - 64-bit OCP interfaces for external DMA
  - OCP port runs at the same core/bus clock ratio as the BIU interface
- Front-side L2 support
  - Support for inline L2 cache
  - L2 cache can be configured to be bypass- able
- Bus Interface
  - OCP version 2.1 interface with 32-bit address and 64-bit data
  - OCP version 2.1 interface runs at core/bus clock ratios of 1, 1.5, 2, 2.5, 3, 3.5, 4, 5, or 10 via a separate synchronous bus clock
  - Clock ratio can be changed dynamically
  - Burst size of four, 64-bit beats
  - 4-entry write buffer
  - “Simple” byte enable mode allows easier bridging to other bus standards
  - Extensions for front-side L2 cache
- Multiply/Divide Unit
  - Maximum issue rate of one 32x32 multi- ply per clock
  - 7-cycle multiply latency
  - Iterative SRT divide algorithm. Minimum 10 and maximum 50 clock latency (divided (rs) sign extension-dependent)
- CorExtend® User Defined Instruction Set Extensions
  - Allows user to define and add instructions to the core at build time
  - Maintains full MIPS32® compatibility
  - Includes access to GPRs and Accumulator registers
  - Instruction operand format (source/destination registers) and latency specified by a programmable template
  - Allows latencies of 3, 5, or >5 cycles when destination is a GPR/Accumulator. Single- cycle latency is allowed when there is no modification to the architectural state of the 74Kc core.
  - Allows in order issue of CorExtend instructions that do not modify the 74Kc core architectural state
  - Supported by industry-standard development tools
- Relocatable Reset Vector
  - Support for user (pin) programmable reset vector in a multi-core environment.
- Power Control
  - Minimum frequency: 0 MHz
  - Power-down mode (triggered by WAIT instruction)
  - Support for software-controlled clock divider
  - Support for top-level, block-level, fine- grained and data cache clock gating
- EJTAG Debug 4.14
  - Support for single-stepping
  - Instruction address and data address/value breakpoints
  - TAP controller is chainable for multi-CPU debug
  - Cross-CPU breakpoint support

- MIPS Trace
  - PC, data address, data value, performance counter value, processor pipeline inefficiency tracing with trace compression
  - Support for on-chip and off-chip trace memory
  - PDtrace version 6 compliant
- Testability
  - Full scan design achieves test coverage in excess of 99% (dependent on library and configuration options)
  - Optional memory BIST for internal SRAM arrays

### 3.3.2 Block Diagram

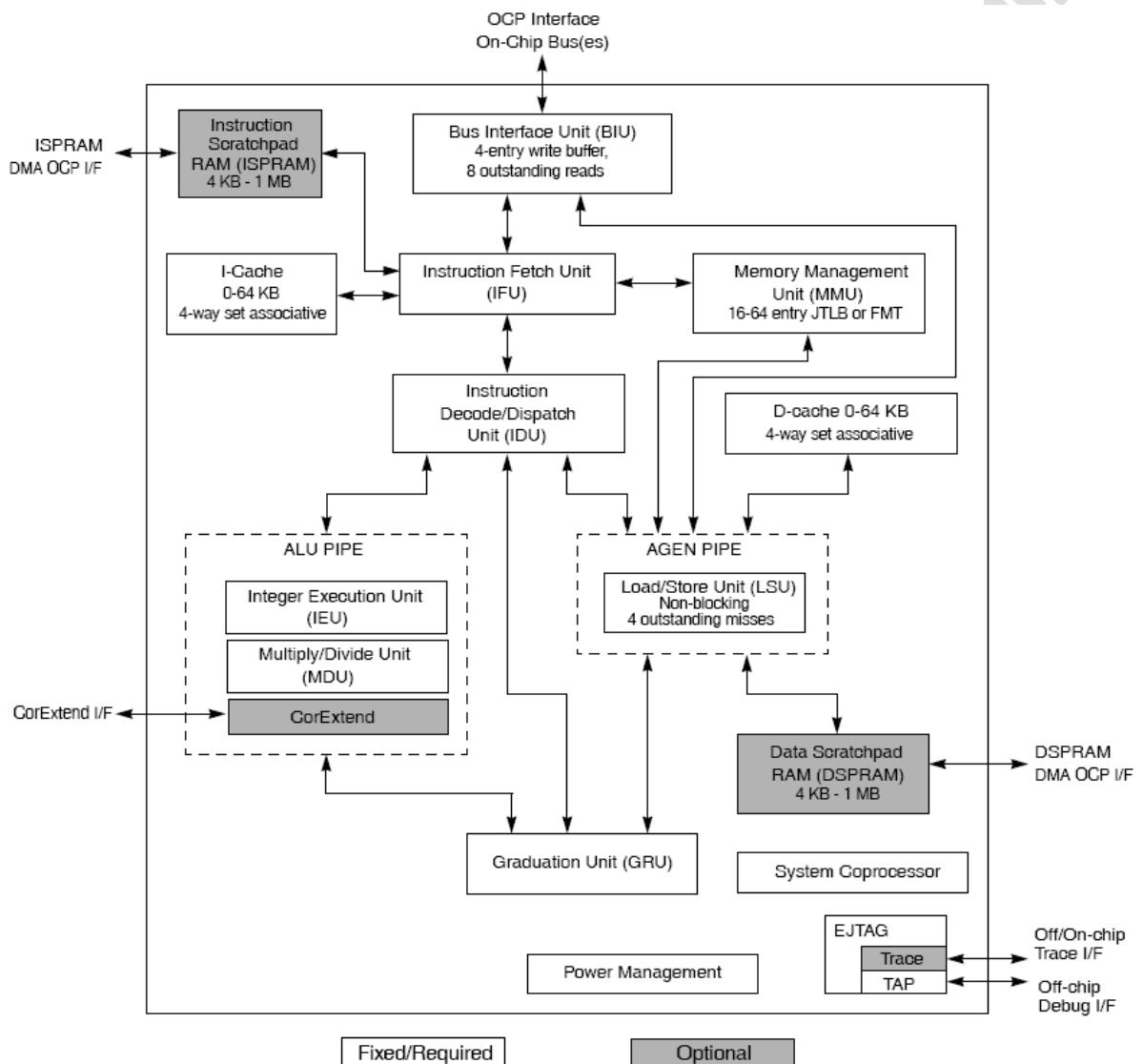


Fig. 3-3-1 MIPS74Kc Processor Diagram

### 3.3.3 Clock Plan

Unit: MHz

CPU	DDR2	SDR
500	166	125
480	160	120
384	128	96
250	125	83

### 3.4 System Control

#### 3.4.1 Features

- Provide read-only chip revision registers
- Provide a window to access boot-strapping signals
- Support memory remapping configurations
- Support software reset to each platform building block
- Provide registers to determine GPIO and other peripheral pin muxing schemes
- Provide some power-on-reset only test registers for software programmers
- Combine miscellaneous registers (such as clock skew control, status register, memo registers,...etc)

#### 3.4.2 Block Diagram

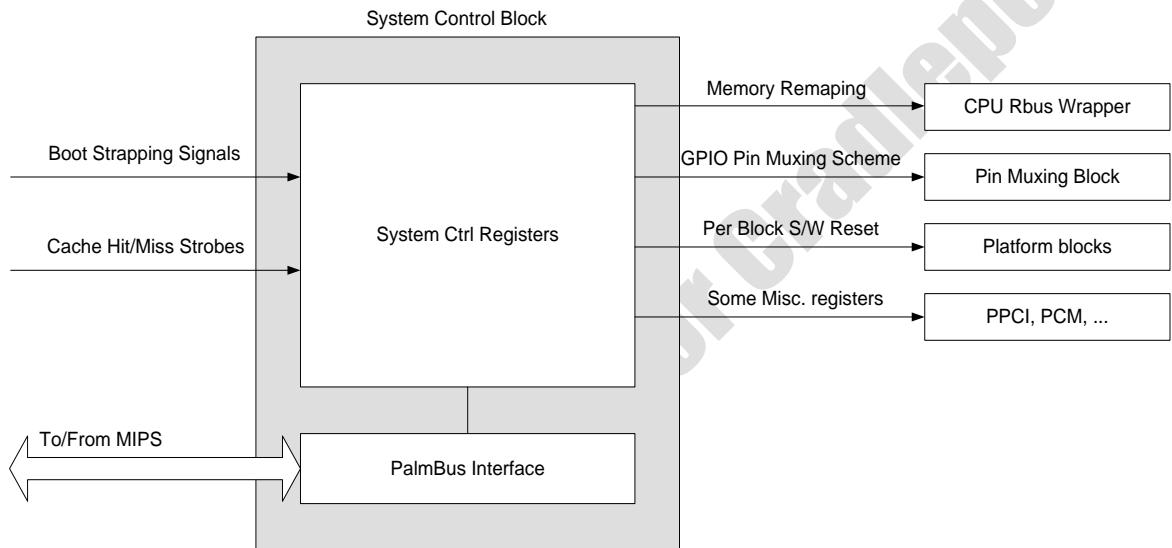


Fig. 3-4-1 System Control Block Diagram

#### 3.4.3 Register Description (base: 0x1000.0000)

SYSCFG0 : System Configuration Register1 (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:24	RW	TEST_CODE	Test code Default value is from bootstrap and can be modified by software	Bootstrap
23:19	-	-	Reserved	
19	RO	BIG_ENDIAN	0: LITTLE ENDIAN 1: BIG ENDIAN	Bootstrap
18	RO	DRAM_FROM_EE	0: DRAM configuration from boot strapping. 1: DRAM configuration(size/width) from EEPROM	Bootstrap
17	RO	DRAM_TYPE	0: SDRAM 1: DDR2	Bootstrap
16	-	-	-	0
15	RO	DRAM_TOTAL_WI_DTH	0:16 1:32	Bootstrap
14:12	RO	DRAM_SIZE	0: 2MB 1: 8MB 2: 16MB 3: 32MB	Bootstrap

			4: 64MB 5: 128MB 6: 256MB	
11	-	-	Reserved	
10	RO	DRAM_WIDTH	SDRAM (DDR2) 0: 16 (8) 1: 32 (16)	Bootstrap
9:8	RO	CPU_CLK_SEL	3: 500 MHz (default) 2: 480Mhz 1: 384 MHz 0: 250 MHz	Bootstrap
7	RO	BYPASS_PLL	0: Do Not Bypass PLL (default) 1: Bypass PLL	Bootstrap
6		-	-	0
5:4	RW	BOOT_FROM	2'b00: boot from external 16-bit flash (default) 2'b01: boot from external 8-bit flash 2'b10: boot from internal ROM 2'b11: boot from internal ROM	Bootstrap
3:0	RO	CHIP_MODE	A vector to set chip function/test/debug modes. In non-test/debug operation, 0: Normal mode (AP mode)(default) 1: iNIC-USB mode 2: iNIC-PCI mode 3: iNIC-PCle mode 4: iNIC-RGMII mode (GE1) 5: iNIC-MII mode (GE1) 6: iNIC-RVMII mode (GE1) 7: AP – support boot from external serial flash 8: AP – support boot from external NAND flash 14:scan mode 15:test/debug mode	Bootstrap

SYSCFG1 : System Configuration Register0 (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	
26	R/W	PULL_EN	PAD pull high/low enable 0: disable 1: enable	0
25	R/W	DDR_PAD_DS	selects input differential receiver under different supply voltage. 1'b0: DDR2 differential Rx mode 1'b1: DDR1 differential Rx mode (not support)	Bootstrap
24:23	R/W	DDR_PAD_ODT	Ondie termination 2'b00: disable (SDR/DDR2 default) 2'b01: 75 ohm 2'b10: 150 ohm 2'b11: reserved	Bootstrap
22	R/W	DDR_PAD_LVCMOS	select operation mode of receiver 1'b0: Differential receive 1'b1: Single-end receive. (SDR/DDR2 default)	Bootstrap
21:20	R/W	DDR_PAD_DRV	DDR2: 2'b00: Full drive 2'b10: Half drive (default) SDR: 2'b10: High drive	Bootstrap

			2'b11: Low drive (default)	
19:17	-	-	Reserved	0
16	R/W	DDR_DPAD_ODT_SEL	DDR2 data pad ODT enable control selection 1: use pad input mode as enable 0: use ddr controller odt control	0
15:14	R/W	GE2_MODE	Gigabit Port #2 Mode 2'b00: RGMII Mode (10/100/1000 Mbps) 2'b01: MII Mode (10/100M bps) 2'b10: Reverse MII Mode (10/100M bps) 2'b11: reserved	2'b00
13:12	R/W	GE1_MODE	Gigabit Port #1 Mode 2'b00: RGMII Mode (10/100/1000 Mbps) 2'b01: MII Mode (10/100M bps) 2'b10: Reverse MII Mode (10/100M bps) 2'b11: reserved	2'b00
11	-	-	Reserved	
10	R/W	USBO_HOST_MODE	0: Set USB#0 to Device Mode 1: Set USB#0 to Host Mode.	1'b0
9	-	-	Reserved	
8	R/W	PCIE_RC_MODE	PCIe RC/EP mode select 1'b0: set PCIe controller to EP mode 1'b1: set PCIe controller to RC mode	1'b0
7	R/W	PCI_HOST_MODE	0: Set PCI to Device Mode 1: Set PCI to Host Mode.	1'b0
6	R/W	PCI_66M_MODE	0: PCI in 33MHz mode 1: PCI in 66MHz mode	1'b0
5:4	R/W	PCI_PAD_DRV	2'b00 trise= 1.65v/ns; tfall= 1.29v/ns duty cycle=59% 2'b01 trise= 2.6v/ns; 2.28v/ns; duty cycle=54.5% 2'b10 trise=3.34v/ns; 3v/ns ; duty cycle=52.7% 2'b11 trise=3.98v/ns; 3.73v/ns; duty cycle= 52%	2'b00
3	-	-	Reserved	
2	RW	GPIO_AS_WD_TO_UT_MODE	GPIO2 as watch dog timeout 1'b0: GPIO2 1'b1: Watch dog reset output (active low for 3 system clocks)	1'b0
1	RW	GPIO_AS_BT_MODE	GPIO7~3 as BT 1'b0: GPIO7~3 1'b1: BT	1'b0
0	RW	DDR_CTL_DRV_SEL	DDR2 control pad driving strength selection 1: use DDR_CTL_PAD_DRV 0: use DDR_PAD_DRV	1'b0

TESTSTAT : Firmware Test Status Register (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:0	R/W	TSETSTAT[31:0]	Firmware Test Status :Note: This register is reset only by power on reset.	32'b0

TESTSTAT2 : Firmware Test Status Register 2 (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:0	R/W	TSETSTAT2[31:0]	Firmware Test Status 2 :Note: This register is reset only by power on reset.	32'b0

Reserved register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	32'b0

Reserved register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	32'b0

Reserved register (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	32'b0

CLKCFG0 : Clock Configuration Register 0 (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:30	R/W	SDRAM_CLK_SKEW	0: zero delay 1: delay 200ps 2: delay 400ps 3: delay 600ps	2'b01
29:22	-	-	Reserved	
21:16	R/W	OSC_1US_DIV	1 usec count for reference clock	6'd39
15:13	R/W	REFCLK1_RATE	0: 32K 1:12M 2:24M 3:31.25M 4:40M 5:62.5M 6:80M 7:Reserved	3'd1
12	-	-	Reserved	
11:9	R/W	REFCLK0_RATE	0: 32K 1:25M 2:50M 3:31.25M 4:40M 5:62.5M 6:80M 7:Reserved	3'd4
8	R/W	REFCLK0_IS_OUT	To control the GPIO1 as REFCLK0 output pin 0: GPIO1 1: Reference clock0 output	1'b0
7:4	-	-	Reserved	
3:0	R/W	CPU_FREQ_ADJ	Clock rate output for CPU. 15: CPU_CLK 14: CPU_CLK* 15/16 ... 1: CPU_CLK * 2/16 0: CPU_CLK * 1/16	4'b0

CLKCFG1 : Clock Configuration Register 1 (offset: 0x30)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	
31	R/W	PBUS_DIV2	0: Pbus clock is running at the same frequency as System clock 1: Pbus clock is running at 1/2 frequency of System clock	1'b0
29	R/W	SYS_TCK_EN	System tick enable	1'b0
28:23	-	-	Reserved	
22	R/W	FE_GDMA_PCLK_EN	0: FE's GDMA clock is gated (PCIe/PCI clock domain) 1: FE's GDMA clock is enabled (PCIe/PCI clock domain)	1'b1
21	R/W	PCIE_CLK_EN	0: PCIe clock is gated 1: PCIe clock is enabled	1'b1

20	R/W	UPHY1_CLK_EN	0: USB PHY1 clock is gated 1: USB PHY0 clock is enabled	1'b1
19	R/W	PCI_CLK_EN	0: PCI clock is gated 1: PCI clock is enabled	1'b1
18	R/W	UPHY0_CLK_EN	0: USB PHY0 clock is gated 1: USB PHY0 clock is enabled	1'b1
17	R/W	GE2_CLK_EN	0: GE2 clock is gated 1: GE2 clock is enabled	1'b1
16	R/W	GE1_CLK_EN	0: GE1 clock is gated 1: GE1 clock is enabled	1'b1
15:0	-	-	Reserved	1'b1

RSTCTRL : Reset Control Register (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	8'b0
27	RW	PCIE_PCI_PDMA_RST	Write 1 to this bit will reset PCIe/PCI PDMA block Write 0 to de-assert reset.	1'b0
26	RW	FLASH	Write 1 to this bit will reset FLASH block Write 0 to de-assert reset.	1'b0
25	RW	UDEV_RST	Write 1 to this bit will reset USB Device block Write 0 to de-assert reset.	1'b0
24	RW	PCI_RST	Write 1 to this bit will reset PCI block Write 0 to de-assert reset.	1'b0
23	RW	PCIE_RST	Write 1 to this bit will reset PCIe block Write 0 to de-assert reset.	1'b0
22	RW	UHST_RST	Write 1 to this bit will reset USB Host block Write 0 to de-assert reset.	1'b0
21	RW	FE_RST	Write 1 to this bit will reset Frame Engine block Write 0 to de-assert reset.	1'b0
20	RW	WLAN_RST	Write 1 to this bit will reset WLAN (MAC/BBP) block Write 0 to de-assert reset.	1'b0
19	RW	UARTL_RST	Write 1 to this bit will reset UART Lite block Write 0 to de-assert reset.	1'b0
18	RW	SPI	Write 1 to this bit will reset SPI block Write 0 to de-assert reset.	1'b0
17	RW	I2S	Write 1 to this bit will reset I2S block Write 0 to de-assert reset.	1'b0
16	RW	I2C	Write 1 to this bit will reset I2C block Write 0 to de-assert reset.	1'b0
15	RW	NAND	Write 1 to this bit will reset NAND block Write 0 to de-assert reset.	1'b0
14	RW	DMA	Write 1 to this bit will reset DMA block Write 0 to de-assert reset.	1'b0
13	RW	PIO	Write 1 to this bit will reset PIO block Write 0 to de-assert reset.	1'b0
12	RW	UART_RST	Write 1 to this bit will reset UART block Write 0 to de-assert reset.	1'b0
11	RW	PCM_RST	Write 1 to this bit will reset PCM block Write 0 to de-assert reset.	1'b0
10	RW	MC_RST	Write 1 to this bit will reset Memory Controller block Write 0 to de-assert reset.	1'b1
9	RW	INTC_RST	Write 1 to this bit will reset Interrupt Controller block Write 0 to de-assert reset.	1'b0
8	RW	TIMER_RST	Write 1 to this bit will reset Timer block Write 0 to de-assert reset.	1'b0

7:1	-	Reserved		7'b0
0	W1C	SYS_RST	Write 1 to this bit will reset Whole SoC	1'b0

**RSTSTAT : Reset Status Register (offset: 0x38)**

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/C	SWCPURST	Software CPU reset occurred This bit will be set if software reset the CPU by writing to the RSTCPU bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect.  :Note: This register is reset only by power on reset.	1'b0
2	R/C	SWSYSRST	Software system reset occurred This bit will be set if software reset the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect.  :Note: This register is reset only by power on reset.	1'b0
1	R/C	WDRST	Watchdog reset occurred This bit will be set if the watchdog timer reset the chip. Writing a '1' will clear this bit. Writing a '0' has not effect.  :Note: This register is reset only by power on reset.	1'b0
0	-	-	Reserved	1'b0

**USB\_PS : USB Power saving control (offset: 0x5C)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:8	R/W	USB_PS_DBC_CNT	USB Host debounce counter Set this field to adjust the debounce count done value, the unit is 256us, i.e. Set to 8 8*256us = 2048us	8'h08
7:6	-	-	Reserved	2'b00
5:4	RO	USB_PS_ST	USB Host power saving status USB_PS_ST[0]: Status of USB PHY0 USB_PS_ST[1]: Status of USB PHY1	Depend on suspend_n state
3:2	-	-	Reserved	2'b00
1:0	R/W	USB_PS_EN	USB Host power saving enable Set this bit will let USB PHY into suspend automatic if no device is connected USB_PS_EN[0]: control USB PHY0 USB_PS_EN[1]: control USB PHY1	2'b00

**GPIOMODE : GPIO Purpose Select (offset: 0x60)**

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	22'b0
19:18	R/W	LNA_G_SHARE_MOD_E	The detailed LNA_PE_GX Mode Pin Sharing is shown in previous session.	2'b11
17:16	R/W	LNA_A_SHARE_MOD_E	The detailed LNA_PE_AX Mode Pin Sharing is shown in previous session.	2'b11
15:14	-	-	Reserved	
13:11	R/W	PCI_SHARE_MODE	The detailed PCI Mode Pin Sharing is shown in previous session.	Bootstrap
10	R/W	GE2_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
9	R/W	GE1_GPIO_MODE	0:Normal Mode	1'b1

			1:GPIO Mode	
8	-	-	Reserved	0
7	R/W	MDIO_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
6	R/W	JTAG_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b0
5	R/W	UARTL_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
4:2	R/W	UARTF_SHARE_MODE	UARF Full interface is shared with PCM, I2S, and GPIO. The detailed UARTF Mode Pin Sharing is shown in previous session.	3'b111
1	R/W	SPI_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1
0	R/W	I2C_GPIO_MODE	0:Normal Mode 1:GPIO Mode	1'b1

PCIPDMA\_STAT : Control and Status of PDMA in PPCI (offset: 0x64)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/W	PCIPDMA_RX_EN	PDMA (the one inside PPCI block) RX DMA enable register.  In iNIC application, the external Host can enable the PDMA inside the RT2880's PPCI block to start RX (from the external host point of view) packet DMA. However, the actual PDMA RX enable signal is generated to PDMA RX block when: MIPS (internal CPU) writes 1 to PCIPDMA_RX_EN; and External Host writes 1 to RX_DMA_EN via BAR1	1'h0
2	R/W	PCIPDMA_TX_EN	PDMA (the one inside PPCI block) TX DMA enable register.  In iNIC application, the external Host can enable the PDMA inside the RT2880's PPCI block to start TX (from the external host point of view) packet DMA. However, the actual PDMA TX enable signal is generated to PDMA TX block when: 1. MIPS (internal CPU) writes 1 to PCIPDMA_TX_EN; and 2. External Host writes 1 to TX_DMA_EN via BAR1	1'h0
1	RO	PCIPDMA_RX_BUSY	Busy flag for PDMA RX in PPCI block 1:PDMA RX is busy 0:PDMA RX is idle	1'h0
0	RO	PCIPDMA_TX_BUSY	Busy flag for PDMA TX in PPCI block 1:PDMA TX is busy 0:PDMA TX is idle	1'h0

DRAM\_CTL\_PAD\_CFG: (offset: 0x68)

Bits	Type	Name	Description	Initial value
31:28	R/W		Reserved	0
27:26	R/W	DDR_CTL_PAD_ODT	DDR pad ODT setting 0: disabled 1: 75 ohm 2: 150 ohm 3: reserved	1'd0
25:24	R/W	DDR_CTL_PADDRV	DDR pad driving strength setting DDR2: 2'b00: Full drive 2'b10: Half drive (default)	2'd0

			SDR: 2'b10: High drive 2'b11: Low drive (default)	
23:0	R/W		Reserved	0

PCIE\_CLK\_GEN: (offset: 0x7C)

Bits	Type	Name	Description	Initial value
31	R/W	cgrstb	Clock generator reset timing control when low active. The clock generation configuration is re-latched and I2C is reset/real time system reset signal for watchdog timer timeout. The signal connects to (Power-On-ResetB or software ResetB)	1'b1
30	R/W	cgpdb	Clock generator global power down control when low active. (including BG BIAS) 0:power down 1:power up	7'b0010100
29	R/W	pexdrv1	PEXCLK 100MHz output driver #1 enable 0: driver disable 1: driver enable	7'b000_0100
28	R/W	pexdrv0	PEXCLK 100MHz output driver #0 enable 0: driver disable 1: driver enable	3'b001
27:24	R/W	pexdrvsel1	PEXDRV1 current output control (Default:0111) 0000: 10.84mA (540.7mV) 0001: 11.30mA (563.9mV) 0010: 11.76mA (587.1mV) 0011: 12.23mA (610.2mV) 0100: 12.69mA (633.3mV) 0101: 13.15mA (656.3mV) 0110: 13.61mA (679.3mV) 0111: 14.07mA (702.3mV) 1000: 14.53mA (725.2mV) 1001: 14.99mA (748mV) 1010: 15.45mA (770.8mV) 1011: 15.9mA (793.5mV) 1100: 16.36mA (816.1mV) 1101: 16.81mA (838.7mV) 1110: 17.26mA (861.2mV) 1111: 17.71mA (883.6mV)	2'b10
23:20	R/W	pexdrvsel0	PEXDRV current output control (Default:0000) 0000: 10.84mA (540.7mV) 0001: 11.30mA (563.9mV) 0010: 11.76mA (587.1mV) 0011: 12.23mA (610.2mV) 0100: 12.69mA (633.3mV) 0101: 13.15mA (656.3mV) 0110: 13.61mA (679.3mV) 0111: 14.07mA (702.3mV) 1000: 14.53mA (725.2mV) 1001: 14.99mA (748mV) 1010: 15.45mA (770.8mV) 1011: 15.9mA (793.5mV) 1100: 16.36mA (816.1mV) 1101: 16.81mA (838.7mV) 1110: 17.26mA (861.2mV)	2'b00

			1111: 17.71mA (883.6mV)	
19:17	R/W	cgtest_sel	Select test output to CGTESTP 000: PLL VCO control voltage 001: 010: 011: 100: 101: 110: 111:	2'b01
16	R/W	cgpdbtest	Test buffer circuit power down, 1: power up 0: power down	2'b00
15	R/W	cgpllrbstb	PLL reset control by register When low active 0: reset 1: non-reset	2'b00
14	R/W	cgpllpdb	PLL power up control by register 0:power down 1:power up	3'b111
13:12	R/W	bgsel	VBG Selection (Default:01) 00: 1.1236V 01: 1.1793V 10: 1.227V 11: 1.274V	1'd0
11:8	R/W	cgpll_vregsel	PLL VCO Regulator voltage control selection output (Default:0000) Sign Magnitude Code: 0 0 1 1 +0.15V 0 0 1 0 +0.10V 0 0 0 1 +0.05V 0 0 0 0 +0.00V (default=vbg) 0 1 0 0 -0.00V 0 1 0 1 -0.05V 0 1 1 0 -0.10V 0 1 1 1 -0.15	7'b0010100
7	R/W	pexclken	PEXCLK 100M output enable control 0: clock disable 1: clock enable	7'b000_0100
6:0	R/W	ref_div	PLL Reference input divider R=1~127. (Default:0000001) R=1 PCIECLK=(40MHz/ref_div)*(fb_div*2)/(out_div*2) Ex: 100MHz=(40M/1)*(20)/(8)	3'b001

**PCIE\_CLK\_GEN1: (offset: 0x80)**

Bits	Type	Name	Description	Initial value
31	R/W	tmode		1'd0
30:24	R/W	fb_div	PLL Feedback divider N=1~127. (Default:0001010) N=10 PCIECLK=(40MHz/ref_div)*(fb_div*2)/(out_div*2) Ex: 100MHz=(40M/1)*(10*2)/(8)	7'b0010100
23:17	R/W	out_div	PLL Output divider OD=1~127. (Default:0000100) OD=4 PCIECLK=(40MHz/ref_div)*(fb_div*2)/(out_div*2) Ex: 100MHz=(40M/1)*(20)/(4*2)	7'b000_0100
16:14	R/W	cgpll_ivco	PLL VCO fixed current control (Default: 001)	3'b001

			000: 500uA 001: 600uA 010: 700uA 011: 800uA 100: 900uA 101: 1mA 110: 1.1mA 110: 1.2mA	
13:12	R/W	cgpll_icp	PLL CP current control (Default: 10) 00: 10uA 01: 20uA 10: 30uA 11: 40uA	2'b10
11:10	R/W	cgpll_lpf_c1	PLL LPF C1 control (Default: 11) 00: 25pF 01: 50pF 10: 75pF 11: 100pF	2'b00
9:8	R/W	cgpll_lpf_c2	PLL LPF C2 control (Default: 01) 00: 2pF 01: 4pF 10: 6pF 11: 8pF	2'b01
7:6	R/W	pfd_dly	PLL PFD Delay control (Default: 00) 00: 393ps 01: 693ps 10: 1.16ns 11: 1.46ns	2'b00
5:3	R/W	ld_dly	PLL LockDetect window control (Default: 000) 000: 720ps 001: 1.44ns 010: Not used 011: Not used 100: Not used 101: Not used 110: Not used 111: Not used	2'b00
2:0	R/W	tod	PLL testing output divider TOD=1~8 (Default:111) TOD=8	3'b111
31	R/W	tmode		1'd0
30:24	R/W	fb_div	PLL Feedback divider N=1~127. (Default:0001010) N=10 PCIECLK=(40MHz/ref_div)*(fb_div*2)/(out_div*2) Ex: 100MHz=(40M/1)*(10*2)/(8)	7'b0010100

**PCIE\_CLK\_GEN2: (offset: 0x84)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:8	R/W	cg_reserve1	Reserved	8'b01010101
7:0	R/W	cg_reserve2	Reserved	8'b01010101

**PMU : (offset: 0x88)**

Bits	Type	Name	Description	Initial value
31:24	-	-		
23	R/W	a_sscperi	SSCG modulation period select (default:1)	1'b1

22	R/W	a_undisb	under voltage monitor function (default: 1)	1'b1
21:20	R/W	a_ssc	SSCG modulation frequency select (default:10)	2'b10
19:12	R/W	a_vtune	Programmable output voltage level (default: <10100100>)	8'b10100101
11				
10:8	R/W	a_dly	Output power MOSFET dead zone control (default: <011>).	3'b011
7:4	R/W	a_drven	Output power MOSFET driving control (default:<0100>).	4'b0100
3:1				
0	R/W	a_sscgen	Spread spectrum function enable (default: 0 (off))	1'b0

PMU1 : (offset: 0x8c)

Bits	Type	Name	Description	Initial value
31:16	-	-		
15:8	R/W	a_dig_Idolevel	Ido output level selection	7'b10011101
7:0	R/W	a_ddr_Idolevel	Ido output level selection	7'b11010110

(The remainder of this page is left blank intentionally)

### 3.5 Timer

#### 3.5.1 Features

- Independent clock pre-scale for each timer
- Independent interrupts for each timer
- Two General-purpose timers
- Periodic mode
- Free-running mode
- Time-out mode
- Second timer may be used as watchdog timer
- Watchdog timer resets system on time-out
- Timer Modes

##### Periodic:

In periodic mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. After reaching zero, the load value is reloaded into the timer and the timer counts down again. A load value of zero disables the timer.

##### Timeout:

In timeout mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. In this mode, the ENABLE bit is reset when the timer reaches zero, stopping the counter. After reaching zero, the load value is reloaded into the timer. A load value of zero disables the timer.

##### Free-running:

In free-running mode, the timer counts down to zero from FFFFh. An interrupt is generated when the count is zero. After reaching zero, FFFFh is reloaded into the timer. This mode is identical to the periodic mode with a load value of 65535. Though it is worth noting that if firmware writes to the load value register in this mode, the timer will still load that value even though that value will be ignored thereafter. Also note that when the timer is first enabled, it will begin counting down from its current value, not necessarily FFFFh.

##### Watchdog:

In watchdog mode, the timer counts down to zero from the load value. If the load value is not reloaded or the timer is not disabled before the count is zero, the chip will be reset. When this occurs, every register in the chip is reset except the watchdog reset status bit WDRST in the RSTSTAT register in the system control block; it remains set to alert firmware of the timeout event when it re-executes its bootstrap.

### 3.5.2 Block Diagram

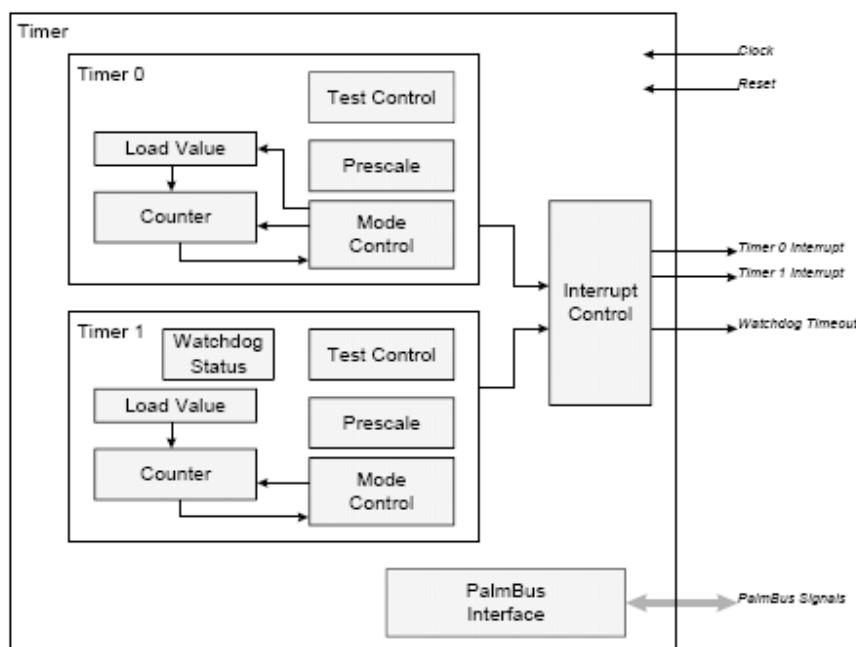


Fig. 3-5-1 Timer Block Diagram

### 3.5.3 Register Description (base: 0x1000.0100)

TMRSTAT: Timer Status Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	26'b0
5	W	TMR1RST	Timer 1 Reset Writing a '1' to this bit will reset the Timer 1 to 0xFFFF if in free-running mode, or the value specified in the TMR1LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit will return a '0'.	1'b0
4	W	TMR0RST	Timer 0 Reset Writing a '1' to this bit will reset Timer 0 to 0xFFFF if in free-running mode, or the value specified in the TMR0LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit will return a '0'.	1'b0
3:2	-	-	Reserved	2'b0
1	W/C	TMR1INT	Timer 1 Interrupt Status This bit is set if Timer 1 has expired. The Timer 1 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.	1'b0
0	W/C	TMROINT	Timer 0 Interrupt Status This bit is set if Timer 0 has expired. The Timer 0 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.	1'b0

TMR0LOAD: Timer 0 Load Value (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:16	R-	-	Reserved	16'b0

15:0	R/W	TMRLOAD[15:0]	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.	16'b0
------	-----	---------------	---	-------

**TMROVAL: Timer 0 Counter Value (offset: 0x14)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	RO	TMRVAL[15:0]	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	16'hffff

**TMROCTL: Timer 0 Control (offset: 0x18)**

Bits	Type	Name	Description	Initial value																		
31:16	-	-	Reserved	16'b0																		
15	R/W	TESTEN	Reserved for Test This bit should be written with a zero	1'b0																		
14:8	-	-	Reserved	15'b0																		
7	R/W	ENABLE	Timer Enable 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	1'b0																		
6	-	-	Reserved	1'b0																		
5:4	R/W	MODE[1:0]	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Time-out	1'b0																		
3:0	R/W	PRESCALE[3:0]	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below.  <table border="1"> <tr> <th>Value</th> <th>Timer Clock Frequency</th> </tr> <tr> <td>0</td> <td>System clock</td> </tr> <tr> <td>1</td> <td>System clock / 4</td> </tr> <tr> <td>2</td> <td>System clock / 8</td> </tr> <tr> <td>3</td> <td>System clock / 16</td> </tr> <tr> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>System clock / 32768</td> </tr> <tr> <td>14</td> <td>System clock /65536</td> </tr> <tr> <td>15</td> <td></td> </tr> </table> <p><b>Note:</b> The pre-scale value should not be changed unless the timer is disabled.</p>	Value	Timer Clock Frequency	0	System clock	1	System clock / 4	2	System clock / 8	3	System clock / 16	.	.	.	System clock / 32768	14	System clock /65536	15		4'b0
Value	Timer Clock Frequency																					
0	System clock																					
1	System clock / 4																					
2	System clock / 8																					
3	System clock / 16																					
.	.																					
.	System clock / 32768																					
14	System clock /65536																					
15																						

**TMR1LOAD: Timer 1 Load Value (offset: 0x20)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0

15:0	R/W	TMRLOAD[15:0]	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.	16'b0
------	-----	---------------	---	-------

TMR1VAL: Timer 1 Counter Value (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	RO	TMRVAL[15:0]	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	16'hffff

TMR1CTL: Timer 1 Control (offset: 0x28)

Bits	Type	Name	Description	Initial value																		
31:16	-	-	Reserved	16'b0																		
15	R/W	TESTEN	Reserved for Test This bit should be written with a zero	1'b0																		
14:8	-	-	Reserved	7'b0																		
7	R/W	ENABLE	Timer Enable 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	1'b0																		
6	R/W	WD_TIMEOUT_SRC	Watchdog timeout alarm source 0: From Timer 1 1: From PMU watch dog timer	1'b0																		
5:4	R/W	MODE[1:0]	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Watchdog	1'b0																		
2:0	R/W	PRESCALE[3:0]	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. <table border="1"> <tr> <th>Value</th> <th>Timer Clock Frequency</th> </tr> <tr> <td>0</td> <td>System clock</td> </tr> <tr> <td>1</td> <td>System clock / 4</td> </tr> <tr> <td>2</td> <td>System clock / 8</td> </tr> <tr> <td>3</td> <td>System clock / 16</td> </tr> <tr> <td>.</td> <td>.</td> </tr> <tr> <td>.</td> <td>.</td> </tr> <tr> <td>14</td> <td>System clock / 32768</td> </tr> <tr> <td>15</td> <td>System clock / 65536</td> </tr> </table>	Value	Timer Clock Frequency	0	System clock	1	System clock / 4	2	System clock / 8	3	System clock / 16	.	.	.	.	14	System clock / 32768	15	System clock / 65536	3'b0
Value	Timer Clock Frequency																					
0	System clock																					
1	System clock / 4																					
2	System clock / 8																					
3	System clock / 16																					
.	.																					
.	.																					
14	System clock / 32768																					
15	System clock / 65536																					
			Note: The pre-scale value should not be changed unless the timer is disabled.																			

### 3.6 Interrupt Controller

#### 3.6.1 Features

- Support a central point for interrupt aggregation for platform related blocks
- Separated interrupt enable and disable registers
- Support global disable function
- 2-level Interrupt priority selection
- Each interrupt source can be directed to IRQ#0 or IRQ#1

Note: RT3662 supports MIPS 74K's vector interrupt mechanism.

There are 6 hardware interrupts supported by MIPS 74K. The interrupt allocation is shown below:

MIPS H/W interrupt pins	Connect to	Remark
HW_INT#5	Timer interrupt	Highest priority
HW_INT#4	802.11n NIC	
HW_INT#3	FE	
HW_INT#2	PCIe/PCI	
HW_INT#1	Other high priority interrupts (IRQ#1)	
HW_INT#0	Other low priority interrupts (IRQ#0)	Lowest priority

#### 3.6.2 Block Diagram

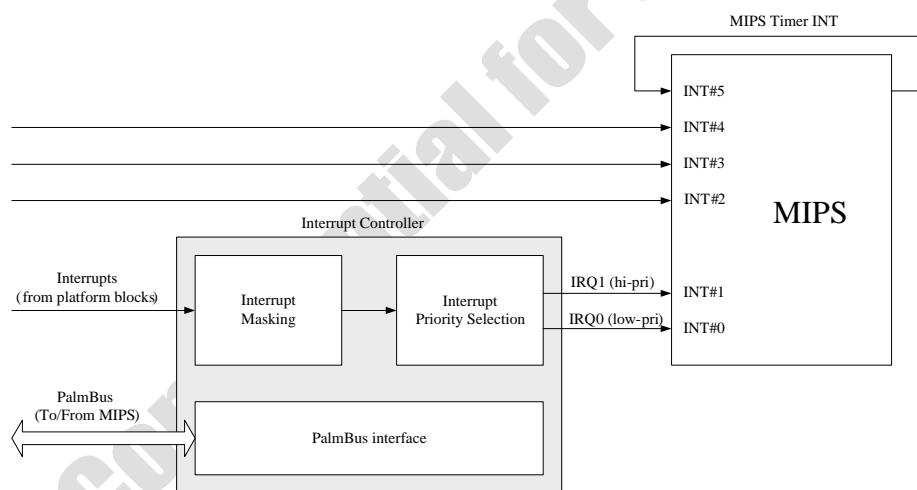


Fig. 3-6-1 Interrupt Controller Block Diagram

### 3.6.3 Register Description (base: 0x1000.0200)

IRQ0STAT: Interrupt Type 0 Status after Enable Mask (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	RO	UDEV	USB device interrupt status after mask	1'b0
18	RO	UHST	USB host interrupt status after mask	1'b0
17	-	-	Reserved	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	RO	UARTLITE	UARTLITE interrupt status after mask	1'b0
11	RO	-	Reserved	1'b0
10	RO	I2S	I2S interrupt status after mask	1'b0
9	RO	PC	MIPS performance counter interrupt status after mask	1'b0
8	RO	NAND	NAND flash controller interrupt status after mask	1'b0
7	RO	DMA	DMA interrupt status after mask	1'b0
6	RO	PIO	PIO interrupt status after mask	1'b0
5	RO	UART	UART interrupt status after mask	1'b0
4	RO	PCM	PCM interrupt status after mask	1'b0
3	RO	ILL_ACC	Illegal access interrupt status after mask	1'b0
2	RO	WDTIMER	Watch dog timer interrupt status after mask	1'b0
1	RO	TIMERO	Timer 0 interrupt status after mask	1'b0
0	RO	SYSCTL	System control interrupt status after mask	1'b0

These bits are set if the corresponding interrupt is asserted from the source and with following two conditions

- The interrupt is not masked (bit not set in the INTDIS register)
- The interrupt type is set to INT0 (in the INTTYPE register).

Note that write to these bits are ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

IRQ1STAT: Interrupt Type 1 Status after Enable Mask (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	RO	UDEV	USB device interrupt status after mask	1'b0
18	RO	UHST	USB host interrupt status after mask	1'b0
17	-	-	Reserved	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	RO	UARTLITE	UARTLITE interrupt status after mask	1'b0
11	-	-	Reserved	1'b0
10	RO	I2S	I2S interrupt status after mask	1'b0
9	RO	PC	MIPS performance counter interrupt status after mask	1'b0
8	RO	NAND	NAND flash controller interrupt status after mask	1'b0
7	RO	DMA	DMA interrupt status after mask	1'b0
6	RO	PIO	PIO interrupt status after mask	1'b0
5	RO	UART	UART interrupt status after mask	1'b0
4	RO	PCM	PCM interrupt status after mask	1'b0
3	RO	ILL_ACC	Illegal access interrupt status after mask	1'b0
2	RO	WDTIMER	Watch dog timer interrupt status after mask	1'b0
1	RO	TIMERO	Timer 0 interrupt status after mask	1'b0
0	RO	SYSCTL	System control interrupt status after mask	1'b0

These bits are set if the corresponding interrupt is asserted from the source and with following two conditions

- The interrupt is not masked (bit not set in the INTDIS register)
- The interrupt type is set to INT1 (in the INTTYPE register).

Note that writing to these bits is ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

**INTTYPE: Interrupt Type (offset: 0x20)**

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	R/W	UDEV	USB device interrupt status after mask	1'b0
18	R/W	UHST	USB host interrupt status after mask	1'b0
17	-	-	Reserved	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	R/W	UARTLITE	UARTLITE interrupt status type	1'b0
11	-	-	Reserved	1'b0
10	R/W	I2S	I2S interrupt status type	1'b0
9	R/W	PC	MIPS performance counter interrupt status type	1'b0
8	R/W	NAND	NAND flash controller interrupt status type	1'b0
7	R/W	DMA	DMA interrupt status after type	1'b0
6	R/W	PIO	PIO interrupt status after type	1'b0
5	R/W	UART	UART interrupt status type	1'b0
4	R/W	PCM	PCM interrupt status type	1'b0
3	R/W	ILL_ACC	Illegal access interrupt status type	1'b0
2	R/W	WDTIMER	Watch dog timer interrupt status type	1'b0
1	R/W	TIMERO	Timer 0 interrupt status type	1'b0
0	R/W	SYSCTL	System control interrupt status type	1'b0

These bits control whether an interrupt is IRQ0 or IRQ1. The interrupt type may be changed at any time; if the interrupt type is changed while the interrupt is active, the interrupt is immediately redirected.

**INTRAW: Raw Interrupt Status before Enable Mask (offset: 0x30)**

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0
19	RO	UDEV	USB device interrupt status after mask	1'b0
18	RO	UHST	USB host interrupt status after mask	1'b0
17	-	-	Reserved	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	RO	UARTLITE	UARTLITE interrupt status before mask	1'b0
11	RO	-	Reserved	1'b0
10	RO	I2S	I2S interrupt status before r mask	1'b0
9	RO	PC	MIPS performance counter interrupt status before mask	1'b0
8	RO	NAND	NAND flash controller interrupt status before mask	1'b0
7	RO	DMA	DMA interrupt status before mask	1'b0
6	RO	PIO	PIO interrupt status before mask	1'b0
5	RO	UART	UART interrupt status before mask	1'b0
4	RO	PCM	PCM interrupt status before mask	1'b0
3	RO	ILL_ACC	Illegal access interrupt status before mask	1'b0
2	RO	WDTIMER	Watch dog timer interrupt status before mask	1'b0
1	RO	TIMERO	Timer 0 interrupt status before mask	1'b0
0	RO	SYSCTL	System control interrupt status before mask	1'b0

These bits are set if the corresponding interrupt is asserted from the source. The status bit is set if the interrupt is active, even if it is masked, and regardless of the interrupt type. This provides a single-access snapshot of all active interrupts for implementation of a polling system.

**INTENA: Interrupt Enable (offset: 0x34)**

Bits	Type	Name	Description	Initial value
31	R/W	GLOBAL	Global interrupt enable Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual enable mask. A read returns the global status ('1' if enabled).	1'b0
30:20	-	-	Reserved	12'b0
19	R/W	UDEV	USB device interrupt status after mask	1'b0
18	R/W	UHST	USB host interrupt status after mask	1'b0
17	-	-	Reserved	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	R/W	UARTLITE	UARTLITE interrupt status after mask	1'b0
11	-	-	Reserved	1'b0
10	R/W	I2S	I2S interrupt enable	1'b0
9	R/W	PC	MIPS performance counter interrupt enable	1'b0
8	RW	NAND	NAND flash controller interrupt enable	1'b0
7	RW	DMA	DMA interrupt enable	1'b0
6	RW	PIO	PIO interrupt enable	1'b0
5	RW	UART	UART interrupt enable	1'b0
4	RW	PCM	PCM interrupt enable	1'b0
3	RW	ILL_ACC	Illegal access interrupt enable	1'b0
2	RW	WDTIMER	Watch dog timer interrupt enable	1'b0
1	RW	TIMERO	Timer 0 interrupt enable	1'b0
0	RW	SYSCTL	System control interrupt enable	1'b0

Writing a '1' to these bits (except the GLOBAL bit) will enable the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writes of '0' are ignored. Reading either the INTENA or INTDIS register will return the current mask, where an interrupt is masked (disabled) if the bit is 'zero', and unmasked (enabled) if the bit is 'one'.

**INTDIS: Interrupt Disable (offset: 0x38)**

Bits	Type	Name	Description	Initial value
31	R/W	GLOBAL	Global interrupt disable Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual Disable mask. A read returns the global status ('1' if Disabled).	1'b0
30:20	-	-	Reserved	12'b0
19	RW	UDEV	USB device interrupt status after mask	1'b0
18	RW	UHST	USB host interrupt status after mask	1'b0
17	-	-	Reserved	1'b0
16	-	-	Reserved	1'b0
15:13	-	-	Reserved	3'b0
12	R/W	UARTLITE	UARTLITE interrupt s disable	1'b0
11	-	-	Reserved	1'b0
10	R/W	I2S	I2S interrupt disable	1'b0
9	R/W	PC	MIPS performance counter interrupt disable	1'b0
8	RW	NAND	NAND flash controller interrupt disable	1'b0
7	RW	DMA	DMA interrupt disable	1'b0
6	RW	PIO	PIO interrupt disable	1'b0
5	RW	UART	UART interrupt disable	1'b0
4	RW	PCM	PCM interrupt disable	1'b0
3	RW	ILL_ACC	Illegal access interrupt disable	1'b0
2	RW	WDTIMER	Watch dog timer interrupt disable	1'b0

1	RW	TIMER0	Timer 0 interrupt disable	1'b0
0	RW	SYSCTL	System control interrupt disable	1'b0

Writing a '1' to these bits (except the GLOBAL bit) will disable the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writing '0' is ignored. Reading either the INTENA or INTDIS register will return the current mask, where an interrupt is masked (disabled) if the bit is 'zero', and unmasked (enabled) if the bit is 'one'.

Ralink confidential for cradlepoint

Draft

### 3.7 UART

#### 3.7.1 Features

- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

#### 3.7.2 Block Diagram

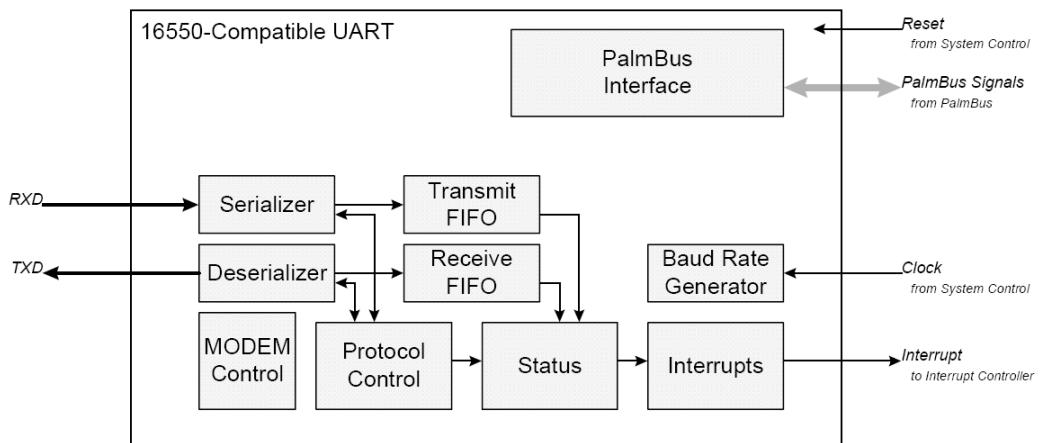


Fig. 3-7-1 UART block diagram

#### 3.7.3 Register Description (base: 0x1000.0500)

RBR : Receive Buffer Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	RO	RXD[7:0]	Receive Buffer Data Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received.	1'b0

**TBR : Transmit Buffer Register (offset: 0x04)**

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	RO	TXD[7:0]	Transmit Buffer Data Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	1'b0

**IER : Interrupt Enable Register (offset: 0x08)**

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/W	EDSSI	Enable Modem Interrupt 1: modem status (DCD, RI, DSR, CTS, DDCD, TERI, DDSR, and DCTS) interrupts. 0: Disable modem status (DCD, RI, DSR, CTS, DDCD, TERI, D and DCTS) interrupts.	1'b0
2	R/W	ELSI	Enable Receiver Line Status Interrupt 1: Enable line status (OE, PE, FE, and BI) interrupts. 0: Disable line status (OE, PE, FE, and BI) interrupts.	1'b0
1	R/W	ETBEI	Enable Transmitter Buffer Line Status Interrupt 1: Enable transmit buffer empty (THRE) interrupt. 0: Disable transmit buffer empty (THRE) interrupt.	1'b0
0	R/W	ERBFI	Enable Receiver Buffer Empty Interrupt 1: Enable data ready (DR) or character time-out interrupt. 0: Disable data ready (DR) or character time-out interrupt.	1'b0

**IIR : Interrupt Identification Register (offset: 0x0C)**

Bits	Type	Name	Description	Initial value																																				
31:8	-	-	Reserved	24'b0																																				
7:6	RO	FIFOENA[1:0]	FIFOs Enabled FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.	1'b0																																				
5:4	-	-	Reserved	2'b0																																				
3:1	RO	INTID[2:0]	Interrupt Identifier Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below. <table border="1"> <thead> <tr> <th>ID</th> <th>Priority</th> <th>Type</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td>7</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>6</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>5</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>4</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>3</td> <td>1</td> <td>Receiver Line Status</td> <td>OE,PE,FE,BI</td> </tr> <tr> <td>2</td> <td>2</td> <td>Receiver Buffer Full</td> <td>DR</td> </tr> <tr> <td>1</td> <td>3</td> <td>Transmit buffer Empty</td> <td>THRE</td> </tr> <tr> <td>0</td> <td></td> <td>Undefined</td> <td></td> </tr> </tbody> </table> If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be	ID	Priority	Type	Source	7		Undefined		6		Undefined		5		Undefined		4		Undefined		3	1	Receiver Line Status	OE,PE,FE,BI	2	2	Receiver Buffer Full	DR	1	3	Transmit buffer Empty	THRE	0		Undefined		3'b1
ID	Priority	Type	Source																																					
7		Undefined																																						
6		Undefined																																						
5		Undefined																																						
4		Undefined																																						
3	1	Receiver Line Status	OE,PE,FE,BI																																					
2	2	Receiver Buffer Full	DR																																					
1	3	Transmit buffer Empty	THRE																																					
0		Undefined																																						

			cleared when data is written to the TBR register. See also "Interrupt Priorities".	
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	1'b0

FCR : FIFO Control Register (offset: 0x10)

Bits	Type	Name	Description	Initial value										
31:8	-	-	Reserved	24'b0										
7:6	R/W	RXTRIG[1:0]	<p>Receiver Trigger Level The data ready interrupt (DR) will be asserted when the receive buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table border="1"> <tr> <th>RXTRIG</th> <th>Trigger Level</th> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>14</td> </tr> </table> <p>Note: This register is not used if the receive FIFO is disabled.</p>	RXTRIG	Trigger Level	0	1	1	4	2	8	3	14	2'b0
RXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	14													
5:4	R/W	TXTRIG[1:0]	<p>Transmitter Trigger Level The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table border="1"> <tr> <th>TXTRIG</th> <th>Trigger Level</th> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>12</td> </tr> </table>	TXTRIG	Trigger Level	0	1	1	4	2	8	3	12	2'b0
TXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	12													
3	R/W	DMAMODE	Enable DMA transfers This bit is writeable and readable, but has no other hardware function.	1'b0										
2	W	TXRST	Transmitter Reset Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.	1'b0										
1	W	RXRST	Receive Reset Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.	1'b0										
0	R/W	FIFOENA	0: The Transmit and Receive FIFOs have the effective depth of one character. 1: The Transmit and Receive FIFOs are enabled. Note: The FIFO status and data are automatically cleared when this bit is changed.	1'b0										

**LCR : Line Control Register (offset: 0x 14, 0x00000000, 0xfffff00, 00)**

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/W	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only	2'b0
6	R/W	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to '0'. Transmitter otherwise operates normally.	2'b0
5	R/W	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity is forced to '1'.	1'b0
4	R/W	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0'). Note: This bit is ignored if the PEN bit is '0'.	1'b0
3	R/W	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	1'b0
2	R/W	STB	Stop Bit Select 0: 1 stop bit is transmitted and received. 1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	1'b0
1:0:	R/W	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	2'b0

**MCR : Modem Control Register (offset: 0x18)**

Bits	Type	Name	Description	Initial value												
31:5	-	-	Reserved	24'b0												
			Loop-back Mode Enable 0: Normal Operation. 1: The UART is put into loop-back mode, used for self-test: TXD pin is driven high; the TXD signal connections are made internally													
4	R/W	LOOP	<table border="1"> <tr> <th>Signal</th> <th>Wrapped back through...</th> </tr> <tr> <td>TXD</td> <td>RXD</td> </tr> <tr> <td>DTRN</td> <td>DSRN</td> </tr> <tr> <td>RTSN</td> <td>CTSN</td> </tr> <tr> <td>OUT1N</td> <td>RIN</td> </tr> <tr> <td>OUT2N</td> <td>DCDN</td> </tr> </table>	Signal	Wrapped back through...	TXD	RXD	DTRN	DSRN	RTSN	CTSN	OUT1N	RIN	OUT2N	DCDN	1'b0
Signal	Wrapped back through...															
TXD	RXD															
DTRN	DSRN															
RTSN	CTSN															
OUT1N	RIN															
OUT2N	DCDN															
3	R/W	OUT2	Out2 Value 0: OUT2N pin is driven to a high level. 1: OUT2N pin is driven to a low level. Note: This bit is only functional in loop-back mode.	0												
2	R/W	OUT1	Out1 Value 0: OUT1N pin is driven to a high level. 1: OUT1N pin is driven to a low level. Note: This bit is only functional in loop-back mode.	0												

1	R/W	RTS	Out1 Value 0: RTSN pin is driven to a high level. 1: RTSN pin is driven to a low level.	1'b0
1	R/W	DTR	Reserved 0: DTRN pin is driven to a high level. 1: DTRN pin is driven to a low level.	1'b0

LSR : Line Status Register (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/C	ERINFIFO	The FIFO contains data which had a parity or framing error This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.	1'b0
6	R/C	TEMT	Transmitter Empty This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the <b>TBR</b> register.	1'b0
5	R/C	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the <b>TBR</b> register.	1'b0
4	R/C	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received.	1'b0
3	R/C	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.	1'b0
2	R/C	PE	Parity Error This bit is set if the received parity is different from the expected value.	1'b0
1	R/C	OE	Overrun Error This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.	1'b0
0	R/C	DR	Data Ready This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.	1'b0

MSR : Modem Status Register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/C	DCD	Data Carrier Detect This bit is set when the DCDN (Data Carrier Detect) pin is at a low value.	1'b0
6	R/C	RI	Ring Indicator This bit is set when the RIN (Ring Indicator) pin is at a low value.	1'b0
5	R/C	DSR	Data Set Ready This bit is set when the DSRN (Data Set Ready) pin is at a low value.	1'b0
4	R/C	CTS	Clear to Send	1'b0

			This bit is set when the CTSN (Clear to Send) pin is at a low value.	
3	R/C	DDCD	Delta Data Carrier Detect This bit is set when the DCDN (Data Carrier Detect) pin changes.	1'b0
2	R/C	TERI	Trailing Edge Ring Indicator This bit is set when the RIN (Ring Indicator) pin changes from a low to a high value.	1'b0
1	R/C	DDSR	Delta Data Set Ready This bit is set when the DSRN (Data Set Ready) pin changes.	1'b0
0	R/C	DCTS	Delta Clear to Send This bit is set when the CTSN (Clear to Send) pin changes.	1'b0

**SCRATCH** : Scratch Register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	SCRATCH[7:0]	Scratch This register is defined as a scratch register in 16550 application. It has no hardware function, and is retained for compatibility only.	8'b0

**DL** : Clock Divider Divisor Latch (offset: 0x28)

Bits	Type	Name	Description	Initial value																								
31:16	-	-	Reserved	16'b0																								
15:0	R/W	DL[15:0]	Divisor Latch This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: baud rate = 40MHz / (CLKDIV * 16). Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only. NOTE: DL[15:0] should be >= 4 <table border="1"> <tr> <th>Src clock(MHz)</th> <th>Req Baud rate</th> <th>DL[15:0]</th> <th>Err Rate (%)</th> </tr> <tr> <td>40000000</td> <td>57000</td> <td>44</td> <td>-0.32%</td> </tr> <tr> <td></td> <td>115200</td> <td>22</td> <td>-1.36%</td> </tr> <tr> <td></td> <td>230400</td> <td>11</td> <td>-1.36%</td> </tr> <tr> <td></td> <td>345600</td> <td>7</td> <td>3.34%</td> </tr> <tr> <td></td> <td>460800</td> <td>5</td> <td>8.51%</td> </tr> </table>	Src clock(MHz)	Req Baud rate	DL[15:0]	Err Rate (%)	40000000	57000	44	-0.32%		115200	22	-1.36%		230400	11	-1.36%		345600	7	3.34%		460800	5	8.51%	16'h0001
Src clock(MHz)	Req Baud rate	DL[15:0]	Err Rate (%)																									
40000000	57000	44	-0.32%																									
	115200	22	-1.36%																									
	230400	11	-1.36%																									
	345600	7	3.34%																									
	460800	5	8.51%																									

**DLLO** : Clock Divider Divisor Latch Low (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLLO[7:0]	This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	8'b1

**DLHI** : Clock Divider Divisor Latch High (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLHI[7:0]	This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility.	8'b0

			Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	
--	--	--	---	--

(The remainder of this page is left blank intentionally)

Ralink confidential for cradlepoint

Draft

### 3.8 UART Lite

#### 3.8.1 Features

- 2-pin UART
- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

#### 3.8.2 Block Diagram

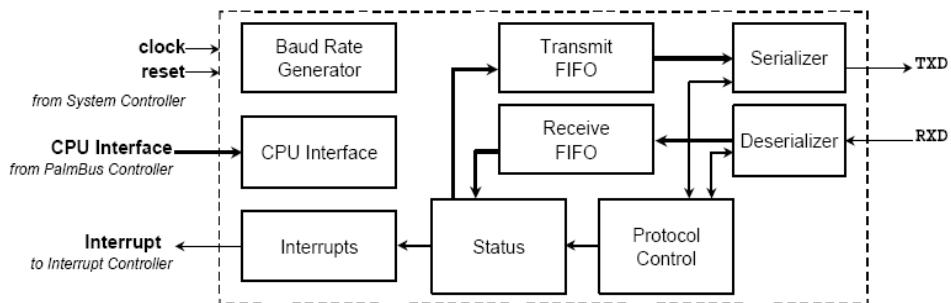


Fig. 3-8-1 UART Lite Block Diagram

#### 3.8.3 Register Description (base: 0x1000.0C00)

RBR: Receive Buffer Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	RO	RXD[7:0]	Receive Buffer Data Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received.	8'b0

TBR: Transmit Buffer Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	RO	TXD[7:0]	Transmit Buffer Data Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	8'b0

**IER: Interrupt Enable Register (offset: 0x08)**

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	29'b0
2	R/W	ELSI	Enable Receiver Line Status Interrupt 1: Enable line status (OE, PE, FE, and BI) interrupts. 0: Disable line status (OE, PE, FE, and BI) interrupts.	1'b0
1	R/W	ETBEI	Enable Transmitter Buffer Line Status Interrupt 1: Enable transmit buffer empty (THRE) interrupt. 0: Disable transmit buffer empty (THRE) interrupt.	1'b0
0	R/W	ERBFI	Enable Receiver Buffer Empty Interrupt 1: Enable data ready (DR) or character time-out interrupt. 0: Disable data ready (DR) or character time-out interrupt.	1'b0

**IIR: Interrupt Identification Register (offset: 0x0C)**

Bits	Type	Name	Description	Initial value																																								
31:8	-	-	Reserved	24'b0																																								
7:6	RO	FIFOENA [1:0]	FIFOs Enabled FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.	1'b0																																								
5:4	-	-	Reserved	2'b0																																								
3:1	RO	INTID[2:0]	Interrupt Identifier Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below.	3'b0																																								
			<table border="1"> <thead> <tr> <th>ID</th> <th>Priority</th> <th>Type</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td>7</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>6</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>5</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>4</td> <td></td> <td>Undefined</td> <td></td> </tr> <tr> <td>3</td> <td>1</td> <td>Receiver Line Status</td> <td>OE,PE,FE,BI</td> </tr> <tr> <td>2</td> <td>2</td> <td>Receiver Buffer Full</td> <td>DR</td> </tr> <tr> <td>1</td> <td>3</td> <td>Transmit buffer</td> <td>THRE</td> </tr> <tr> <td>0</td> <td>4</td> <td>Empty</td> <td>DCTD,DDSR, RI,</td> </tr> <tr> <td></td> <td></td> <td>Modem Status</td> <td>DCD</td> </tr> </tbody> </table> <p>If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be cleared when data is written to the TBR register. See also "Interrupt Priorities".</p>	ID	Priority	Type	Source	7		Undefined		6		Undefined		5		Undefined		4		Undefined		3	1	Receiver Line Status	OE,PE,FE,BI	2	2	Receiver Buffer Full	DR	1	3	Transmit buffer	THRE	0	4	Empty	DCTD,DDSR, RI,			Modem Status	DCD	
ID	Priority	Type	Source																																									
7		Undefined																																										
6		Undefined																																										
5		Undefined																																										
4		Undefined																																										
3	1	Receiver Line Status	OE,PE,FE,BI																																									
2	2	Receiver Buffer Full	DR																																									
1	3	Transmit buffer	THRE																																									
0	4	Empty	DCTD,DDSR, RI,																																									
		Modem Status	DCD																																									
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	1'b0																																								

**FCR: FIFO Control Register (offset: 0x10)**

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:6	R/W	RXTRIG [1:0]	Receiver Trigger Level The data ready interrupt (DR) will be asserted when the receiver buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding	2'b0

			is as follows:											
			<table border="1"> <thead> <tr> <th>RXTRIG</th> <th>Trigger Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>14</td> </tr> </tbody> </table>	RXTRIG	Trigger Level	0	1	1	4	2	8	3	14	
RXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	14													
			Note: This register is not used if the receive FIFO is disabled.											
5:4	R/W	TXTRIG[1:0]	<p>Transmitter Trigger Level The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table border="1"> <thead> <tr> <th>TXTRIG</th> <th>Trigger Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>12</td> </tr> </tbody> </table>	TXTRIG	Trigger Level	0	1	1	4	2	8	3	12	2'b0
TXTRIG	Trigger Level													
0	1													
1	4													
2	8													
3	12													
3	R/W	DMAMODE	Enable DMA transfers This bit is writeable and readable, but has no other hardware function.	1'b0										
2	W	TXRST	Transmitter Reset Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.	1'b0										
1	W	RXRST	Receive Reset Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.	1'b0										
0	R/W	FIFOENA	0: The Transmit and Receive FIFOs have the effective depth of one character. 1: The Transmit and Receive FIFOs are enabled. Note: The FIFO status and data are automatically cleared when this bit is changed.	1'b0										

LCR: Line Control Register (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/W	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only	2'b0
6	R/W	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to '0'. Transmitter otherwise operates normally.	2'b0
5	R/W	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity is forced to '1'.	1'b0
4	R/W	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0'). Note: This bit is ignored if the PEN bit is '0'.	1'b0
3	R/W	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	1'b0
2	R/W	STB	Stop Bit Select	1'b0

			0: 1 stop bit is transmitted and received. 1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	
1:0:	R/W	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	2'b0

MCR: Modem Control Register (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	24'b0
4	R/W	LOOP	Loop-back Mode Enable 0: Normal Operation. 1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal are connected to RXD internally.	1'b0
3:0	RO	-	Reserved	7'b0

LSR: Line Status Register (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/C	ERINFIFO	The FIFO contains data which had a parity or framing error This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.	2'b0
6	R/C	TEMT	Transmitter Empty This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the <b>TBR</b> register.	1'b0
5	R/C	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the <b>TBR</b> register.	1'b0
4	R/C	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received.	1'b0
3	R/C	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.	1'b0
2	R/C	PE	Parity Error This bit is set if the received parity is different from the expected value.	1'b0
1	R/C	OE	Overrun Error This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.	1'b0
0	R/C	DR	Data Ready This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.	1'b0

DL: Clock Divider Divisor Latch (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0

15:0	R/W	DL[15:0]	<p><b>Divisor Latch</b></p> <p>This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as:</p> <p>Baud rate = system clock frequency / (CLKDIV * 16).</p> <p>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.</p> <p>NOTE: DL[15:0] should be <math>\geq 4</math></p> <table border="1"> <thead> <tr> <th>Src clock(MHz)</th><th>Req Baud rate</th><th>DL[15:0]</th><th>Err Rate (%)</th></tr> </thead> <tbody> <tr> <td>40000000</td><td>57000</td><td>44</td><td>-0.32%</td></tr> <tr> <td></td><td>115200</td><td>22</td><td>-1.36%</td></tr> <tr> <td></td><td>230400</td><td>11</td><td>-1.36%</td></tr> <tr> <td></td><td>345600</td><td>7</td><td>3.34%</td></tr> <tr> <td></td><td>460800</td><td>5</td><td>8.51%</td></tr> </tbody> </table>	Src clock(MHz)	Req Baud rate	DL[15:0]	Err Rate (%)	40000000	57000	44	-0.32%		115200	22	-1.36%		230400	11	-1.36%		345600	7	3.34%		460800	5	8.51%	16'h0001
Src clock(MHz)	Req Baud rate	DL[15:0]	Err Rate (%)																									
40000000	57000	44	-0.32%																									
	115200	22	-1.36%																									
	230400	11	-1.36%																									
	345600	7	3.34%																									
	460800	5	8.51%																									

DLLO: Clock Divider Divisor Latch Low (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLLO[7:0]	<p>This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility.</p> <p>Note: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.</p>	8'b1

DLHI : Clock Divider Divisor Latch High (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLHI[7:0]	<p>This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility.</p> <p>Note: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.</p>	8'b0

IFCTL : Interface Control (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	31'b0
0	R/W	IFCTL	<p>Open Collector Mode Control. This register controls if the UART Lite TXD output functions in open collector mode or is always driven. When set to '0', the output is always driven with the value of the transmit data signal. When set to a '1', the TXD output functions in open collector mode, where the TXD output is either driven low (when the transmit data output is active low) or tri-stated (when the transmit data output is active high).</p>	1'b0

### 3.9 Programmable I/O

#### 3.9.1 Features

- Support 94 programmable I/Os
- Parameterized numbers of independent inputs, outputs, and inputs
- Independent polarity controls for each pin
- Independently masked edge detect interrupt on any input transition
- Programmable I/O pins are shared pin with DRAM, PCI, MDIO, JTAG, UART-Lite, UART, SPI, PCM, I2C, GE1 and GE2.

#### 3.9.2 Block Diagram

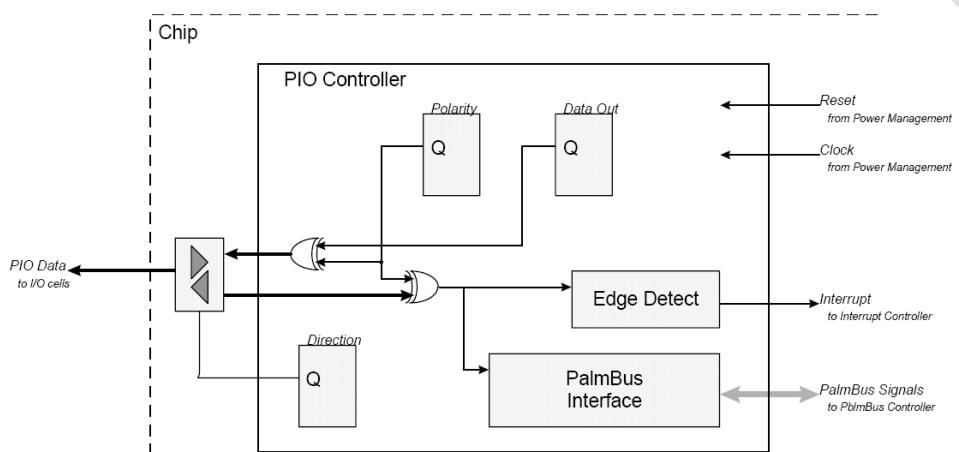


Fig. 3-9-1 Program I/O Block Diagram

#### 3.9.3 Register Description (base: 0x1000.0600)

GPIO23\_00\_INT: Programmed I/O Interrupt Status (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOINT[23:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register.  Note: Changes to the PIO pins can only be detected when the clock is running.	24'b0

GPIO23\_00\_EDGE: Programmed I/O Edge Status (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOEDGE[23:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register.	24'b0

			Note: Changes to the PIO pins can only be detected when the clock is running.	
--	--	--	---	--

**GPIO23\_00\_RENA: Programmed I/O Rising Edge Interrupt Enable (offset: 0x08)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIORENA[23:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	24'b0

**GPIO23\_00\_FENA: Programmed I/O Falling Edge Interrupt Enable (offset: 0x0C)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOFMASK [23:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	24'b0

**GPIO23\_00\_DATA: Programmed I/O Data (offset: 0x20)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODATA[23:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	24'b0

**GPIO23\_00\_DIR: Programmed I/O Direction (offset: 0x24)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODIR[23:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	24'b0

**GPIO23\_00\_POL: Programmed I/O Pin Polarity (offset: 0x28)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOPOL[23:0]	Program I/O Pin Polarity	24'b0

			These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data.  Note: The polarity controls affect both input and output modes.	
--	--	--	--	--

GPIO23\_00\_SET: Set PIO Data Bit (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOSET[23:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO23\_00\_RESET: Clear PIO Data bit (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIORESET[23:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO23\_00\_TOG: Toggle PIO Data bit (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOTOG[23:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO39\_24\_INT : Program I/O Interrupt (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOINT[15:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register.  Note: Changes to the PIO pins can only be detected when the clock is running.	16'b0

GPIO39\_24\_EDGE : Program I/O Edge Status (offset: 0x3c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOEDGE [15:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register.  Note: Changes to the PIO pins can only be detected when the clock is running.	16'b0

**GPIO39\_24\_RENA : Program I/O Rising Edge Interrupt Enable (offset: 0x40)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIORENA[15:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	16'b0

**GPIO39\_24\_FENA : Program I/O Falling Edge Interrupt Enable (offset: 0x44)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIOFENA[15:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set. Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	16'b0

**GPIO39\_24\_DATA : Program I/O Data (offset: 0x48)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIODATA[15:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	16'b0

**GPIO39\_24\_DIR : Program I/O Direction (offset: 0x4c)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIODATA[15:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	16'b0

**GPIO39\_24\_POL : Program I/O Pin Polarity (offset: 0x50)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	PIOPOL[15:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data	16'b0

			at any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data. Note: The polarity controls affect both input and output modes.	
--	--	--	---	--

**GPIO39\_24\_SET : Set PIO Data Bit (offset: 0x54)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOSET[15:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	16'b0

**GPIO39\_24\_RESET : Clear PIO Data bit [39:24](offset: 0x58)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIORESET[15:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	16'b0

**GPIO39\_24\_TOG : Toggle PIO Data bit (offset: 0x5c)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/C	PIOTOG[15:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	16'b0

**GPIO71\_40\_INT : Program I/O Interrupt Status (offset: 0x60)**

Bits	Type	Name	Description	Initial value
31:0	R/C	PIOINT[31:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register. Note: Changes to the PIO pins can only be detected when the clock is running.	32'b0

**GPIO71\_40\_EDGE : Program I/O Edge Status (offset: 0x64)**

Bits	Type	Name	Description	Initial value
31:0	R/C	PIOEDGE[31:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register. Note: Changes to the PIO pins can only be detected when the clock is running.	32'b0

**GPIO71\_40\_RENA : Program I/O Rising Edge Interrupt Enable (offset: 0x68)**

Bits	Type	Name	Description	Initial value
31:0	R/W	PIORENA[31:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.	32'b0

			Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	
--	--	--	---	--

**GPIO71\_40\_FENA : Program I/O Falling Edge Interrupt Enable (offset: 0x6C)**

Bits	Type	Name	Description	Initial value
31:0	R/W	PIORENA[31:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.  Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	32'b0

**GPIO71\_40\_DATA : Program I/O Data (offset: 0x70 )**

Bits	Type	Name	Description	Initial value
31:0	R/W	PIODATA[31:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins.  Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes.  Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	32'b0

**GPIO71\_40\_DIR : Program I/O Direction (offset: 0x74)**

Bits	Type	Name	Description	Initial value
31:0	R/W	PIODIR [31:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	32'b0

**GPIO71\_40\_POL : Program I/O Pin Polarity(offset: 0x78)**

Bits	Type	Name	Description	Initial value
31:0	R/W	PIOPOL [31:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value will not modify the pin data.  Note: The polarity controls affect both input and output modes.	32'b0

**GPIO71\_40\_SET : Set PIO Data Bit (offset: 0x7C)**

Bits	Type	Name	Description	Initial value
31:0	R/C	PIOSET [31:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	32'b0

**GPIO71\_40\_RESET : Clear PIO Data bit (offset: 0x80)**

Bits	Type	Name	Description	Initial value
31:0	R/C	PIORESET [31:0]	These bits are used for setting bits in the PIODATA output	32'b0

			register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	
--	--	--	--	--

**GPIO71\_40\_TOG : Toggle PIO Data bit (offset: 0x84)**

Bits	Type	Name	Description	Initial value
31:0	R/C	PIOTOG [31:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	32'b0

**GPIO95\_72\_INT : Program I/O Interrupt (offset: 0x88)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOINT[23:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register.  Note: Changes to the PIO pins can only be detected when the clock is running.	24'b0

**GPIO95\_72\_EDGE : Program I/O Edge Status (offset: 0x8c)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOEDGE [23:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register.  Note: Changes to the PIO pins can only be detected when the clock is running.	24'b0

**GPIO95\_72\_RENA : Program I/O Rising Edge Interrupt Enable (offset: 0x90)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIORENA[23:0]	Rising edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.  Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.	24'b0

**GPIO95\_72\_FENA : Program I/O Falling Edge Interrupt Enable (offset: 0x94)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOFENA[23:0]	Falling edge mask for individual Programmed I/O pin The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.  Note: Edge detection is done after polarity is adjusted according	24'b0

			to the PIOPOL register.	
--	--	--	-------------------------	--

**GPIO95\_72\_DATA : Program I/O Data (offset: 0x98 )**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODATA[23:0]	<p>Data Pin for Program I/O</p> <p>These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins.</p> <p>Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes.</p> <p>Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.</p>	24'b0

**GPIO95\_72\_DIR : Program I/O Direction (offset: 0x9c)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODATA[23:0]	<p>Program I/O Pin Direction</p> <p>These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.</p>	24'b0

**GPIO95\_72\_POL : Program I/O Pin Polarity (offset: 0xa0)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOPOL[23:0]	<p>Program I/O Pin Polarity</p> <p>These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data.</p> <p>Note: The polarity controls affect both input and output modes.</p>	24'b0

**GPIO95\_72\_SET : Set PIO Data Bit (offset: 0xa4)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOSET[23:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

**GPIO95\_72\_RESET : Clear PIO Data bit [39:24](offset: 0xa8)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIORESET[23:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

**GPIO95\_72\_TOG : Toggle PIO Data bit (offset: 0xac)**

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0

23:0	R/C	PIOTOG[23:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0
------	-----	--------------	---	-------

Ralink confidential for cradlepoint

Draft

### 3.10 I2C Controller

### 3.10.1 Features

- Two I2C Host Controllers
  - Programmable I2C bus clock rate
  - Supports the Synchronous Inter Integrated Circuits (I2C) serial protocol
  - Bi-directional data transfer
  - Programmable address width up to 8 bits
  - Sequential byte read or write capability
  - Device address and data address can be transmitted for device, page and address selection
  - Supports Standard mode and Fast mode

### 3.10.2 Block Diagram

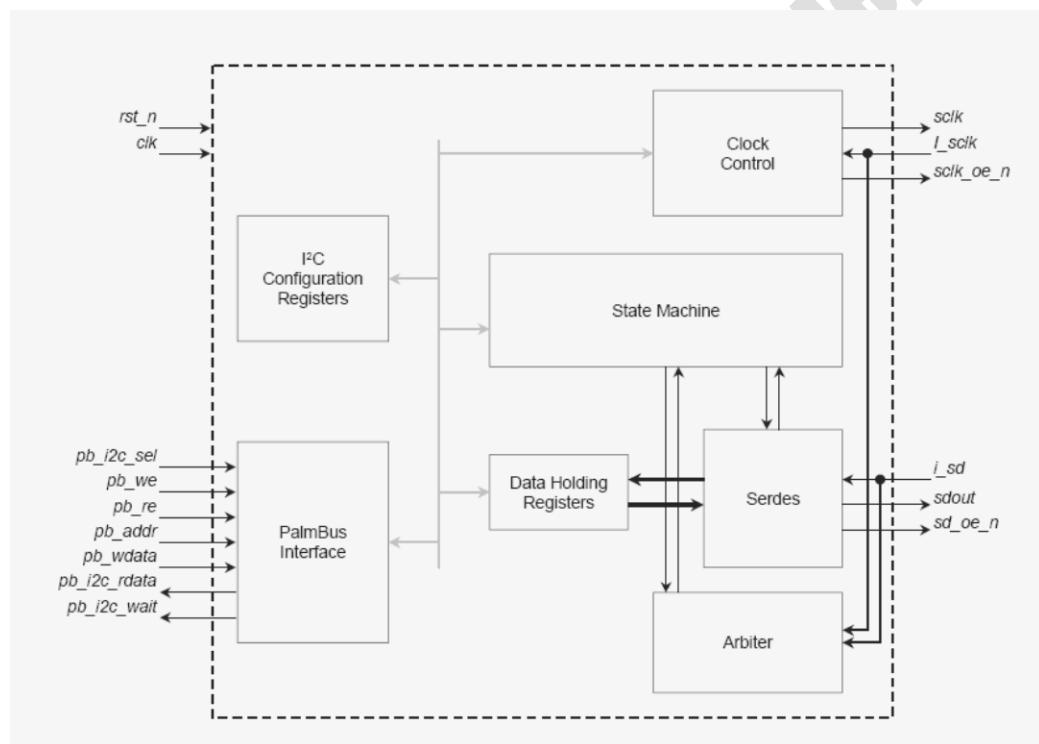


Fig. 3-10-1I2C Controller Block Diagram

### 3.10.3 Register Description (base: 0x1000.0900)

## CONFIG: I2C Configuration Register (offset: 0x00)

CONVLEN Configuration Register (Offset: 0x00)				
Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:5	R/W	ADDRLEN [2:0]	Address Length The value written to this register plus one will indicate the number of address bits to be transferred from the I2C <b>ADDR</b> register. Program '0' for a 1-bit address, '1' for a 2-bit address, etc.)	3'b0
4:2	R/W	DEVADLEN [2:0]	Device Address Length The value written to this register plus one indicates the number of device address bits to be transferred from the	3'b0

			<b>DEVADDR</b> register. This field should be programmed to '6' for compliance with I2C bus protocol.	
1	R/W	ADDRDIS	0: Normal transfers will occur with the address being Transmitted, followed by read or write data. 1: The controller will read or write serial data without transferring the address.	1'b0
0	R/W	DEVADDIS	0: The device address will be transmitted before the data address. 1: The controller will not transfer the device address.  Note: if this bit is set, the ADDRDIS bit is ignored, and an address is always transmitted.  Note: most I2C slave devices require a device address to be transmitted; this bit should typically be set to '0'.	1'b0

CLKDIV: I2C Clock Divisor Register (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	CLKDIV[15:0]	Clock Divisor  The value written to this register is used to generate the I2C bus SCLK signal by applying the following equation: SCLK frequency = 40MHz / ( 2 x CLKDIV ) Note: Only values of 8 and above are valid.  Note: Due to synchronization between the I2C internal clock and the system clock, the exact equation is actually SCLK frequency = pb_clk frequency / ((2 x CLKDIV) + 5). For most systems, CLKDIV is usually programmed to very larger numbers since the system clock frequency should be orders of magnitude faster than the I2C bus clock. These results in the synchronization errors being insignificant and the exact equation approximating the simpler one given above.	16'b0

DEVADDR: I2C Device Address Register (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:7	-	-	Reserved	25'b0
6:0	R/W	DEVADDR[6:0]	I2C Device Address  This value is transmitted as the device address, if <b>DEVADDIS</b> bit in the <b>CONFIG</b> register is not set to '1'.	7'b0

ADDR: I2C Address Register (offset: 0x0c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	ADDR[7:0]	I2C Address  These bits store the 8-bits of address to be sent to the external I2C slave devices when the <b>ADDRDIS</b> bit is '0'.	8'b0

DATAOUT: I2C Data Out Register (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DATAOUT [7:0]	I2C Data Out  These bits store the 8-bits of data to be written to the external I2C slave devices during a write transfer.	8'b0

DATAIN: I2C Data In Register (offset: 0x14)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0

7:0	RO	DATAIN[7:0]	I2C Data In These bits store the 8-bits of data received from the external I2C slave devices during a read transaction. The <b>DATARDY</b> bit in the <b>STATUS</b> register is set to '1' when data is valid in this register.	8'b0
-----	----	-------------	--	------

**STATUS:** I2C Status Register (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	27'b0
4	RO	STARTERR	Start Overflow Error This bit is set when the <b>STARTXFR</b> register is written and a transfer is in progress. When this occurs, the write to the <b>STARTXFR</b> register is ignored. This bit is automatically cleared if firmware writes to the <b>STARTXFR</b> register when the <b>BUSY</b> bit cleared.	1'b0
3	RO	ACKERR	I2C Acknowledge Error Detect This bit is set when the Host controller did not receive a proper acknowledge from the I2C slave device after the transmission of a device address, address, or data out. This bit is automatically cleared when firmware writes to the <b>STARTXFR</b> register.	1'b0
2	RO	DATARDY	I2C Data Ready for Read This bit indicates that the receive buffer contains valid data. It is set when data is received from an I2C slave device and is transferred from the interface shift register to the <b>DATAIN</b> register. This bit is automatically cleared when firmware reads the <b>DATAIN</b> register.	1'b0
1	RO	SDOEMPTY	I2C Serial Data Out Register Empty This bit indicates that the transmit data buffer is empty. It is cleared when the <b>DATAOUT</b> register is written to by software, and set to '1' when transmit data is transferred from the <b>DATAOUT</b> register to the interface shift register. Firmware may write to the <b>DATAOUT</b> register when this bit is '1'.	1'b1
0	RO	BUSY	I2C State Machine Busy This bit is '1' when the I2C interface is active, and '0' when it is idle. Firmware may initiate an I2C transfer when this bit is '0', and should not modify any I2C host controller registers while it is '1'.	1'b0

**STARTXFR:** I2C Transfer Start Register (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	30'b0
1	R/W	NODATA	Initiate transfer without transferring data When this register is written with this bit set, an address-only transaction is initiated. If <b>DEVADDIS</b> is '0', the device address, direction, address and stop condition are transmitted to the I2C slave device. If <b>DEVADDIS</b> is '1', the address and stop condition are transmitted to the I2C slave device. This bit should be written with a '0' for normal I2C bus accesses. Note: <b>ADDRDIS</b> is ignored if this bit is set for a transaction.	1'b0
0	R/W	RWDIR	Read/Write Direction When this register is written with this bit set, a read transaction is initiated; when written with this bit reset, a write transaction is initiated. Note: this bit is shifted out to the I2C slave device after the device address; if <b>DEVADDIS</b> is '1', this bit is not shifted out to the device.	1'b0

**BYTECNT: I2C Byte Counter Register (offset: 0x20)**

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	26'b0
5:0	R/W	BYTCNT[5:0]	Byte Count used for sequential reads/writes The value written to this register plus one indicates the number of data bytes to be written to or read from the external I2C slave device. If its value is non-zero, multiple sequential read or write cycles will be issued with a single address (and/or device address).	6'b0

Ralink confidential for cradlepoint

Draft

### 3.11 PCM Controller

#### 3.11.1 Features

- PCM module provides PBUS interface for register configuration and data transfer
- Two clock sources are reserved for PCM circuit. (From internal clock generator, int\_pcm\_clk, and from external clock source, ext\_pcm\_clk)
- PCM module can drive a clock out to external codec ( $\text{out\_clk\_freq} = \text{int\_pcm\_clk}/n$ ,  $n = \text{configurable by register}, 1 \leq n \leq 64$ ).
- 2 channels PCM are available. 4~128 slots are configurable.
- Each channel supports a-law(8-bits)/u-law(8-bits)/raw-PCM(16-bits) transfer.
- Hardware converter of a-law?raw-16 and u-law ? raw-16 are implemented in design.
- Support long(8 cycle)/short(1 cycles)/configurable(interval & start point are configurable) FSYNC.
- All signals are driven by rising edge and latched by falling edge.
- Last bit of DTX will be tri-stated on falling edge.
- Begin of slot is configurable by 10 bits registers each channel.
- 32 bytes FIFO are available for each channel
- PCM interface can emulate I2S interface (16-bits data-width only).
- MSB/LSB order is configurable.
- support both of a-law/u-law(8-bits) → linear PCM(16-bits) and linear PCM(16bits) → a-law/u-law(8-bits)

#### 3.11.2 Block Diagram

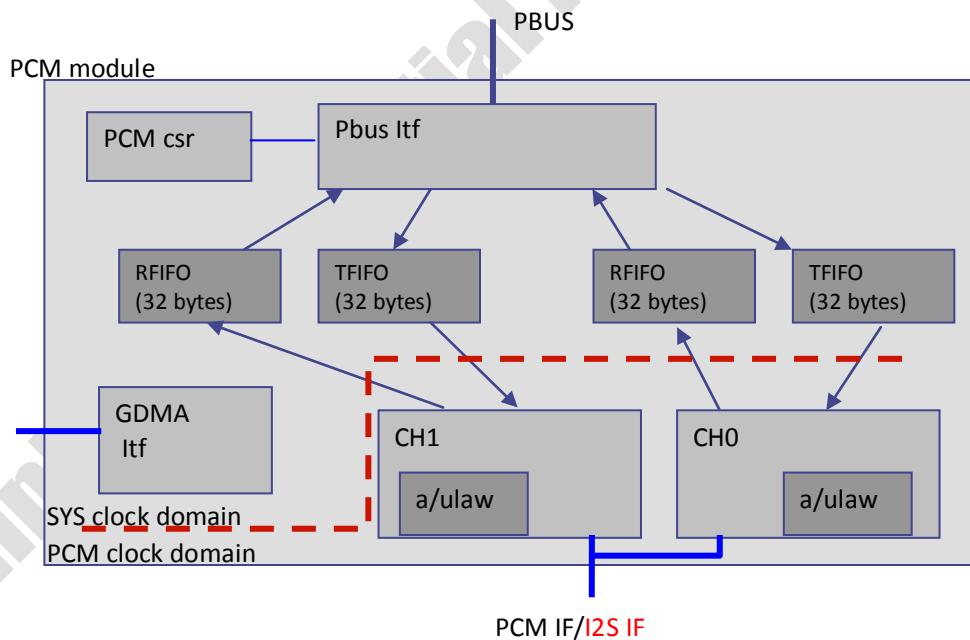


Fig. 3-11-1 PCM Controller Block Diagram

Two clocks domains are partitioned in this design. PCM converter (ulaw?raw-16bit and alaw?raw-16bit) are implemented in PCM mxDmx. The threshold of FIFO is configurable. As the threshold reaches, PCM will (a) trigger the DMA interface to notify external DMA engine to transfer data. (b) trigger the interrupts to host.

The interrupt sources include:

- threshold is reached
- FIFO under run or overrun.

- fault is detected at DMA interface.

The A-law and u-law converter is implemented base on ITU-G.711 A-law and u-law table. In this design, support both of a-law/u-law(8-bits) → linear PCM(16-bits) and linear PCM(16bits) → a-law/u-law(8-bits)

The data-flow from codec to PCM-controller (RX-flow) is shown as below:

- PCM-controller latches the data from DRX at indicated time slot and then writes it to FIFO. If FIFO full, the data will be lost.
- As the RX-FIFO reach the threshold, two actions may be taken
- As DMA\_ENA=1, DMA\_REQ will be asserted to request a burst transfer. And it will re-check the FIFO threshold after DMA\_END is asserted by GDMA. (GDMA should be configured before channel is enabled.)
- Assert the Interrupt source to notify HOST. HOST can check RFIFO\_AVAIL information then get back the data from FIFO.

The data-flow from PCM-controller to codec (TX-flow) is shown as below:

- After GDMA is configured, software should configure and enable the PCM channel.
- The empty FIFO should
- As DMA\_ENA=1, DMA\_REQ will be triggered to request a burst transfer. And it will re-check the FIFO threshold after DMA\_END is asserted by GDMA (a burst is completed.).
- Assert the Interrupt source to notify HOST. HOST will write down the data to TX-FIFO. After that, HOST will recheck TFIFO\_EMPTY information then write more data if available.

NOTICE: As DMA\_ENA=1, the burst size of GDMA should less than the threshold value.

### 3.11.3 Register Description (base: 0x1000.2000)

GLB\_CFG: GLB\_CFG Register (offset: 0x00)

Bits	Type	Name	Description	Initial value
31	RW	PCM_EN	PCM enable, 1: enable 0: disable, all FSM and control register of PCM_mxDmx will be clear to default value.	0
30	RW	DMA_EN	DMA enable 1: enable DMA interface, transfer data with DMA 0: disable DMA interface, transfer data with software.	0
29:23	-	-	Reserved	0
22:20	RW	RFF_THRES	RXFIFO threshold, As threshold reach, host/dma will be notified to fill FIFO. (unit = word) It should be >2 and <6 As data in FIFO under the threshold, interrupt & DMA will be triggered.	4
19	-	-	Reserved	0
18:16	RW	TFF_THRES	TXFIFO threshold, As threshold reach, host/dma will be notified to fill FIFO. (unit = word) It should be >2 and <6. As data in FIFO over the threshold, interrupt & DMA will be triggered.	4
15:10	-	-	Reserved	0
9	RW	CH1-TX_EN	Channel-1 TX enable	0
8	RW	CH0-TX_EN	Channel-0 TX enable	0
7:2	-	-	Reserved	0
1	RW	CH1-RX_EN	Channel-1 RX enable	0

0	RW	CHO-RX_EN	Channel-0 RX enable 1: enable 0:disable	0
---	----	-----------	---	---

**PCM\_CFG: PCM\_CFG Register (offset: 0x04)**

Bits	Type	Name	Description	Initial value
31	RW	-	Reserved for future.	0
30	RW	CLKOUT_EN	Enable the PCM_CLK_OUT 1: PCM clock is provide from internal divider. 0: PCM clock is provide from external Codec/OSC (NOTE: Normally, the register should be asserted to '1'. And it should be asserted after divider cfg & divider clock enable)	0
29:28	-	-	Reserved	
27	RW	EXT_FSYNC	FSYNC is provided by external. 1: FSYNC is provided by external 0: FSYNC is generated by internal circuit.	0
26	RW	LONG_FSYNC	FSYNC mode: 1: long FSYNC 0: short FSYNC	0
25	RW	FSYNC_POL	Polarity of FSYNC 1: FSYNC is high active 0: FSYNC is low active	1
24	RW	DTX_TRI	Tristate the DTX as fall edge as last bit. 1: Tristate the DTX 0: non-Tristate the DTX	1
23:3	-	-	Reserved	0
2:0	RW	SLOT_MODE	How many slot each PCM frame 0: 4 slots, PCM clock out/in should be 256KHz. 1: 8 slots, PCM clock out/in should be 512KHz. 2:16 slots, PCM clock out/in should be 1.024MHz. 3:32 slots, PCM clock out/in should be 2.048MHz. 4:64 slots, PCM clock out/in should be 4.096MHz. 5:128 slots, PCM clock out/in should be 8.192MHz. other: reserved.  Note: When using the external clock, the frequency clock should be equal to PCM_clock out. Otherwise, the PCM_CLKin should be 8.192 MHz.	0

**INT\_STATUS: INT\_STATUS Register (offset: 0x08)**

Bits	Type	Name	Description	Initial value
31:16	RO	-	Reserved	0
15	RW	CH1T_DMA_FAULT	Found any fault of the CH1-TX's DMA signals. (Write '1' to clear)	0
14	RW	CH1T_OVRUN	The FIFO of CH1-TX overrun(Write '1' to clear)	
13	RW	CH1T_UNRUN	The FIFO of CH1-TX underrun(Write '1' to clear)	0
12	RW	CH1T_THRES	The FIFO of CH1-TX lower than the defined threshold. (Write '1' to clear)	0
11	RW	CH1R_DMA_FAULT	Found any fault of the CH1-RX's DMA signals. (Write '1' to clear)	0
10	RW	CH1R_OVRUN	The FIFO of CH1-RX overrun(Write '1' to clear)	
9	RW	CH1R_UNRUN	The FIFO of CH1-RX underrun(Write '1' to clear)	0
8	RW	CH1R_THRES	The FIFO of CH1-RX lower than the defined threshold. (Write '1' to clear)	0
7	RW	CH0T_DMA	Found any fault of the CHO-TX's DMA signals. (Write '1' to clear)	0

		FAULT	
6	RW	CHOT_OVRUN	The FIFO of CH0-TX overrun(Write '1' to clear)
5	RW	CHOT_UNRUN	The FIFO of CH0-TX underrun(Write '1' to clear)
4	RW	CHOT_THRES	The FIFO of CH0-TX lower than the defined threshold. (Write '1' to clear)
3	RW	CHOR_DMA_FAULT	Found any fault of the CH0-RX's DMA signals. (Write '1' to clear)
2	RW	CHOR_OVRUN	The FIFO of CH0-RX overrun(Write '1' to clear)
1	RW	CHOR_UNRUN	The FIFO of CH0-RX underrun(Write '1' to clear)
0	RW	CHOR_THRES	The FIFO of CH0-RX lower than the defined threshold. (Write '1' to clear)

INT\_EN: INT\_EN Register (offset: 0x0c)

Bits	Type	Name	Description	Initial value
31:16	RO	-	Reserved	0
15	RW	INT15_EN	Enable INT_STATUS[15]	0
14	RW	INT14_EN	Enable INT_STATUS[14]	0
13	RW	INT13_EN	Enable INT_STATUS[13]	0
12	RW	INT12_EN	Enable INT_STATUS[12]	0
11	RW	INT11_EN	Enable INT_STATUS[11]	0
10	RW	INT10_EN	Enable INT_STATUS[10]	0
9	RW	INT9_EN	Enable INT_STATUS[9]	0
8	RW	INT8_EN	Enable INT_STATUS[8]	0
7	RW	INT7_EN	Enable INT_STATUS[7]	0
6	RW	INT6_EN	Enable INT_STATUS[6]	0
5	RW	INT5_EN	Enable INT_STATUS[5]	0
4	RW	INT4_EN	Enable INT_STATUS[4]	0
3	RW	INT3_EN	Enable INT_STATUS[3]	0
2	RW	INT2_EN	Enable INT_STATUS[2]	0
1	RW	INT1_EN	Enable INT_STATUS[1]	0
0	RW	INT0_EN	Enable INT_STATUS[0]	0

FF\_STATUS: FF\_STATUS Register (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:12	RO	CH1RFF_AVCNT	CH1, Available FIFO space can be read (unit=word)	0
11:8	RO	CH1TFF_EPCNT	CH1, Available FIFO space can be written (unit=word)	8
7:4	RO	CH0RFF_AVCNT	CH0, Available FIFO space can be read (unit=word)	0
3:0	RO	CH0TFF_EPCNT	CH0, Available FIFO space can be written (unit=word)	8

CH0\_CFG: CH0\_CFG Register (offset: 0x020)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback enable 1: loopback (Asyn-TXFIFO → DTX → DRX → Asyn-RXFIFO) 0: normal mode	0
30	RW	EXT_LBK_EN	External loopback enable 1: external loopback enable (Ext-Codec → DRX → DTX → Ext-Codec) 0: normal mode	0
29:27	RW	CMP_MODE	Compress type select 000: disable HW converter, linear raw-data (16-bits) 010: disable HW converter, linear raw-data(8-bits), A-law or U-law (8-bits) 011: reserved 100: enable HW converter, raw-data(16-bits) → U-law mode (8-	0

			bits) (PCM bus be compress format) 101: enable HW converter, U-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format) 110: enable HW converter, raw-data(16-bits) → A-law mode (8-bits) (PCM bus be compress format) 111: enable HW converter, A-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format)	
26:10	-	-	Reserved	0
9:0	RW	TS_START	Timeslot Starting location	1

CH1\_CFG: CH1\_CFG Register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback enable 1: loopback (Asyn-TXFIFO → DTX → DRX → Asyn-RXFIFO) 0: normal mode	0
30	RW	EXT_LBK_EN	External loopback enable 1: external loopback enable (Ext-Codec → DRX → DTX → Ext-Codec) 0: normal mode	0
29:27	RW	CMP_MODE	Compress type select 000: disable HW converter, linear raw-data (16-bits) 010: disable HW converter, linear raw-data(8-bits), A-law or U-law (8-bits) 011: reserved 100: enable HW converter, raw-data(16-bits) → U-law mode (8-bits) (PCM bus be compress format) 101: enable HW converter, U-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format) 110: enable HW converter, raw-data(16-bits) → A-law mode (8-bits) (PCM bus be compress format) 111: enable HW converter, A-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format)	0
26:10	-	-	Reserved	
9:0	RW	TS_START	Timeslot Starting location	1

FSYNC\_CFG:: FSYNC configuration Register (offset:0x30)

Bits	Type	Name	Description	Initial value
31	RW	Cfg_fsync_en	Enable configurable FSYNC	0
30	RW	Pos_sample	Controller sample data with 1: positive edge of PCM clock 0: negative edge of PCM clock  Notice: This configuration should be "0" if DTX_TRI=1	0
29:22	-	-	Reserved	0
21:12	RW	Fsync_start	Start point of configurable FSYNC	0
11:10	-	-	Reserved	0
9:0	RW	Fsync_intv	Interval of configurable FSYNC	0

CH\_CFG2:: Extended channel configuration Register (offset:0x34)

Bits	Type	Name	Description	Initial value
31:20	-	-	-	-
19	RW	CH1_RXFF_CLR	CH1 RXFIFO clear, set 1 for clear, 0 for normal operation.	0
18	RW	CH1_TXFF_CLR	CH1 TXFIFO clear, set 1 for clear, 0 for normal operation.	0
17	RW	-	Reserved	0

16	RW	CH1_LSB	Enable CH1 transmit in LSB order	0
15:4	-	-	Reserved	0
3	RW	CHO_RXFF_CLR	CHO RXFIFO clear, set 1 for clear, 0 for normal operation.	0
2	RW	CHO_TXFF_CLR	CHO TXFIFO clear, set 1 for clear, 0 for normal operation.	0
1	RW	-	Reserved	0
0	RW	CHO_LSB	Enable CHO transmit in LSB order	0

**RSV\_REG16: RSV\_REG16 Register (offset: 0x38)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0
15:0	RW	SPARE_REG	Spare Register for future	0

**DIVCOMP\_Cfg: Integer part of Divider Register (offset: 0x50)**

Bits	Type	Name	Description	Initial value
31	RW	CLK_EN	Enable the clock divider.	0
30:8	-	-	Reserved	0
7:0	RW	DIVCOMP	fraction part of divider.	0

**DIVINT\_Cfg: Integer part of Divider Register (offset: 0x54)**

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	0
9:0	RW	DIVINT	Integer part of divider. Formula: $FreqOut = 1/(FreqIn * 2 * (DIVINT + DIVCOMP) / (2^{10}))$ FreqIn is always fixed to 40MHz.	0

**CHO\_FIFO: CHO\_FIFO Register (offset: 0x80)**

Bits	Type	Name	Description	Initial value
31:0	RW	CHO_FIFO	FIFO access point	0

**CH1\_FIFO:: CH1\_FIFO Register (offset:0x84)**

Bits	Type	Name	Description	Initial value
31:0	RW	CH1_FIFO	FIFO access point	0

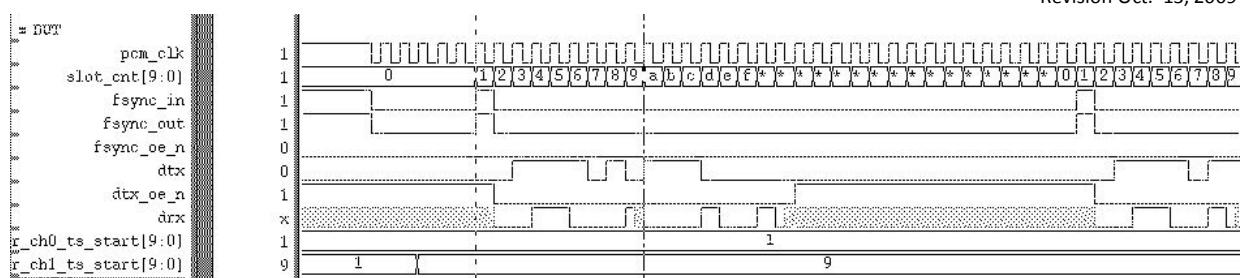
PCM initialization flow:

- Step #1: Set PCM\_CFG
- Step #2: Set CH0/1\_CFG
- Step #3: Write PCM data to FIFO CH0/1\_FIFO
- Step #4: Set GLB\_CFG to enable the PCM and channel.
- Step #5: Set divider clock
- Step #6: enable clock
- Step #7: Monitor FF\_STATUS to receive/transmit the other PCM data.

**Example of PCM configuration**

Case1:

```
Cfg_fsync Register: Cfg_fsync_en = 0 (PS: fsync is always driven at slot_cnt=1)
CHO_CFG Register: ts_start=1
CH1_CFG Register: ts_start=9
PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b1, DRX_TRI=1'b0, SLOT_MODE=3'b0
```

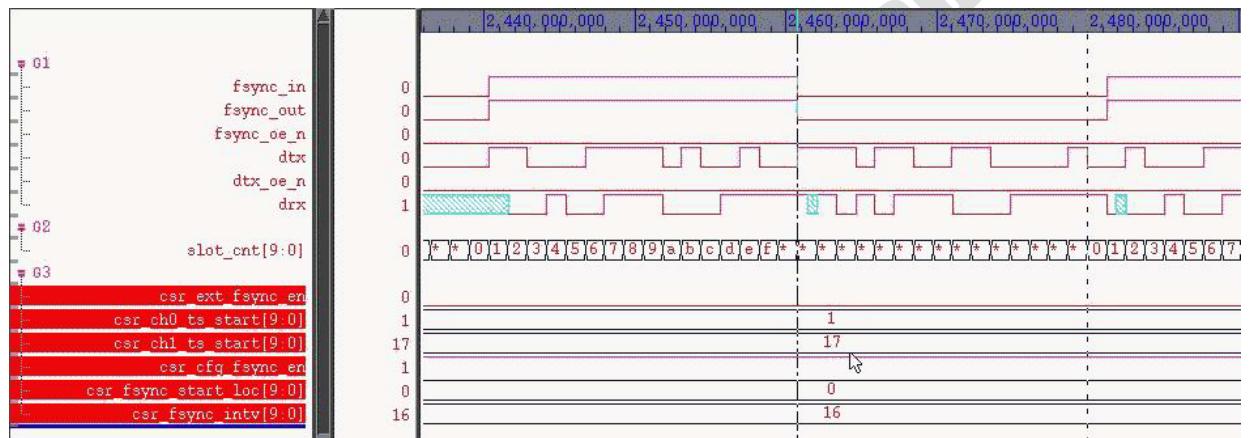

**Case2:**

Cfg\_fsync Register: Cfg\_fsync\_en = 1, start\_loc=0, interval=16

CHO\_CFG Register: ts\_start=1

CH1\_CFG Register: ts\_start=17

PCM\_CFG Register: LONG\_FSYNC=1'b0, FSYNC\_POL=1'b1, DRX\_TRI=1'b0, SLOT\_MODE=3'b0, RAW16-bits

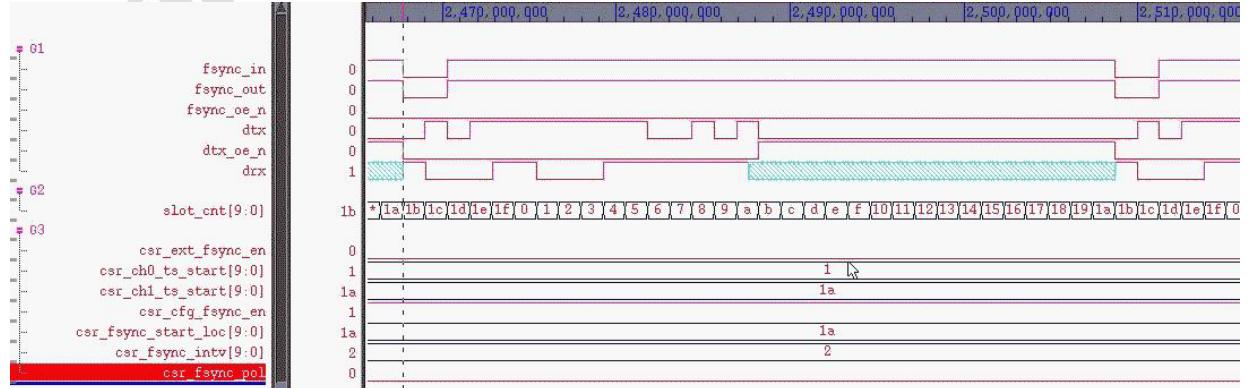

**Case3:**

Cfg\_fsync Register: Cfg\_fsync\_en = 1, start\_loc=0x1A, interval=2

CHO\_CFG Register: ts\_start=1 (disable)

CH1\_CFG Register: ts\_start=0x1A

PCM\_CFG Register: LONG\_FSYNC=1'b0, FSYNC\_POL=1'b0 (LOW active), DRX\_TRI=1'b0, SLOT\_MODE=3'b0, RAW16-bits



### 3.12 Generic DMA Controller

#### 3.12.1 Features

- Support 16 DMA channels
- Support 16 DMA requests
- Programmable hardware channel priority
- Programmable DMA Burst Size (1,2,4,8,16 burst transfer)
- Support 32 bit wide transaction
- Big-endian and Little-endian support
- Support memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral transfers.
- Interrupts for each channel. They also can be masked, independently.
- Each channel transaction can be masked temporarily by the software, and released by the hardware automatically

#### 3.12.2 Block Diagram

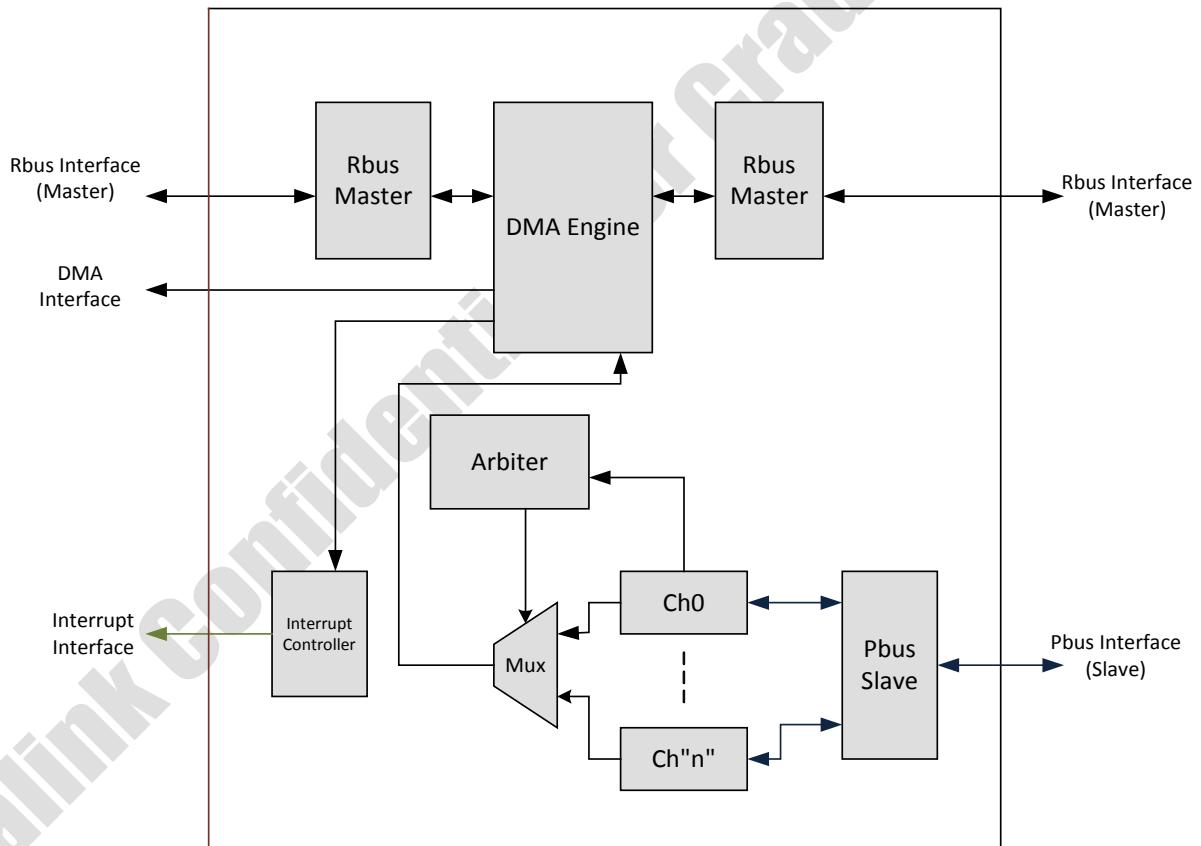


Fig.3-12-1 Generic DMA controller block diagram

#### 3.12.3 Peripheral Channel Connection

Channel number	Peripheral
1	NAND Flash Controller
2	I2S Controller (TXDMA)
3	I2S Controller (RXDMA)
4	PCM Controller (RDMA, channel-0)

5	PCM Controller (RDMA, channel-1)
6	PCM Controller (TDMA, channel-0)
7	PCM Controller (TDMA, channel-1)
8	Codec Interface-0
9	Codec Interface-1

### 3.12.4 Register Description (Base: 0x1000.2800)

GDMA\_SAN: GDMA Channel n Source Address

(offset: 0x000, 0x010, 0x020, 0x030, 0x040, 0x050, 0x060, 0x070, 0x080, 0x090, 0x0A0, 0x0B0, 0x0C0, 0x0D0, 0x0E0, 0x0F0)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:0	R/W	CHANNEL SOURCE ADDRESS	Channel Source Address: This register contains the source address information	32'b0

GDMA\_DAn: GDMA Channel n Destination Address

(offset: 0x004, 0x014, 0x024, 0x034, 0x044, 0x054, 0x064, 0x074, 0x084, 0x094, 0x0A4, 0x0B4, 0x0C4, 0x0D4, 0x0E4, 0x0F4)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:0	R/W	CHANNEL DESTINATION ADDRESS	Channel Destination Address: This register contains the destination address information	32'b0

GDMA\_CTOn: GDMA Channel n Control Register 0

(offset: 0x008, 0x018, 0x028, 0x038, 0x048, 0x058, 0x068, 0x078, 0x088, 0x098, 0x0A8, 0x0B8, 0x0C8, 0x0D8, 0x0E8, 0x0F8)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:24	--	-	Reserved	8'b0
23:16	R/W	Transfer Count	These registers contain the number of the data bytes needed to be transfer.	8'b0
15:8	--	-	Reserved	8'b0
7	R/W	Source Burst Mode	The value represents the source burst mode 'b0: incremental mode 'b1: fix mode	1'b0
6	R/W	Destination Burst Mode	The value represents the destination burst mode 'b0: incremental mode 'b1: fix mode	1'b0
5:3	R/W	Burst Size	The number of the transfer for burst transaction. 'b000: 1 transfer 'b001: 2 transfer 'b010: 4 transfer 'b011: 8 transfer 'b100: 16 transfer others: undefined	3'b0
2	R/W	Transmit Done Interrupt Enable	Transmit done interrupt enable. 'b1:Enable 'b0:Disable	1'b0

1	R/W	Channel Enable	Enable the channel 'b1: Enable 'b0: Disable This bit will be de-asserted by the hardware when the transaction is done.	1'b0
0	R/W	Hardware/Software Mode Select	Hardware/Software Mode Select 'b1: Software Mode 'b0: Hardware Mode In software mode, the data transfer will start when the Channel Enable bit is set. In hardware mode, the data transfer will start when the DMA Request is asserted.	1'b0

**GDMA\_CT1n: GDMA Channel n Control Register 1**

(offset: 0x00C, 0x01C, 0x02C, 0x03C, 0x04C, 0x05C, 0x06C, 0x07C, 0x08C, 0x09C, 0x0AC, 0x0BC, 0x0CC, 0x0DC, 0x0EC, 0x0FC)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:22	--	-	Reserved	10'b0
21:16	R/W	Source DMA Request	The value represents the source DMA request. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 ... n: DMA_REQn n+1: The source of the transfer is memory others: undefined	6'b0
15:14	--	-	Reserved	2'b0
13:8	R/W	Destination DMA Request	The value represents the destination DMA request. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 ... n: DMA_REQn n+1: The destination of the transfer is memory others: undefined	6'b0
7:3	R/W	Next Unmasked Channel	The value represents the next unmasked channel. When the transaction is done, the hardware will clear the Channel Mask bit of the next unmasked channel. 0: Channel 0 1: Channel 1 2: Channel 2 ... n: Channel n If the hardware doesn't need to clear any Channel Mask bit, these bits must be set to their own channel.	5'b0
2	--	-	Reserved	1'b0
1	R/W	Channel Unmasked Interrupt Enable	Channel unmasked interrupt enable. 'b1:Enable 'b0:Disable When this bit is set, an interrupt will be asserted when the hardware wants to clear the Channel Mask bit and the Channel Mask bit is 0 originally.	1'b0

0	R/W	Channel Mask	Channel Mask 'b1: This channel is masked 'b0: This channel is not masked When this channel mask is set, the GDMA transaction will not start until this bit is clear by the hardware.	1'b0
---	-----	--------------	---	------

GDMA\_UNMASKINT: GDMA Unmasked Interrupt Status Register (offset: 0x200)

Bits	Type	Name	Description	Initial value
31:0	R/W1C	Unmasked Interrupt Status	This register contains the unmasked interrupt status. This bit will be set when the hardware wants to clear the Channel Mask bit and the Channel Mask bit is 0 originally. Bitn~bit0 is for channel-n ~ channel-0, respectively.	32'b0

GDMA\_DONEINT: GDMA Interrupt Status Register (offset: 0x204)

Bits	Type	Name	Description	Initial value
31:0	R/W1C	Transmit Done Interrupt Status	This register contains the transmit-done interrupt status. Bitn~bit0 is for channel-n ~ channel-0, respectively.	32'b0

GDMA\_GCT: GDMA Global Control Register (offset: 0x220)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	-
4:3	RO	Total channel number	2'b0: 8 channel 2'b1: 16 channel 2'b2: 32 channel 2'b3: Reserved	2'b1
2:1	RO	IP version	Version of GDMA core	2'b1
0	R/W	Arbitration Selection	Select the channel arbitration method. 1'b0: Channel-0 has the highest priority. Channel-1~ Channel-n are round-robin. 1'b1: Channel-0 doesn't have the highest priority. Channel-0~Channel-n are round-robin.	1'b0

GDMA\_REQSTS: GDMA Request Status Register (offset: 0x2A0)

Bits	Type	Name	Description	Initial value
31:0	R	GDMA Request Signal Status	This register contains the GDMA Request Signals status Bitn~bit0 is for GDMA_REQn ~ GDMA_REQ0, respectively.	32'b0

GDMA\_ACKSTS: GDMA Acknowledge Status Register (offset: 0x2A4)

Bits	Type	Name	Description	Initial value
31:0	R	GDMA Acknowledge Signal Status	This register contains the GDMA Acknowledge Signals status Bitn~bit0 is for GDMA_ACKn ~ GDMA_ACK0, respectively.	32'b0

GDMA\_FINSTS: GDMA Finish Status Register (offset: 0x2A8)

Bits	Type	Name	Description	Initial value
31:0	R	GDMA Finish Signal Status	This register contains the GDMA Finish Signals status Bitn~bit0 is for GDMA_FINISHn ~ GDMA_FINISH0, respectively.	32'b0

### 3.13 SPI Controller

#### 3.13.1 Features

- Supports up to 2 SPI master operations
- Programmable clock polarity
- Programmable interface clock rate
- Programmable bit ordering
- Firmware-controlled SPI enable
- Programmable payload (address + data) length

#### 3.13.2 Block Diagram

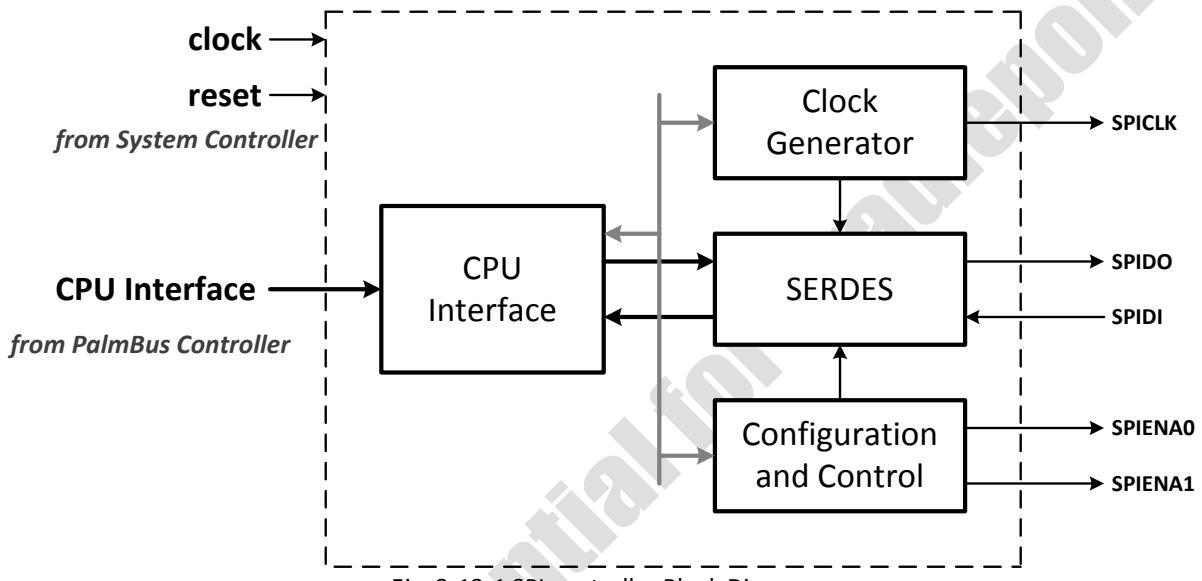


Fig. 3-13-1 SPI controller Block Diagram

#### 3.13.3 Register Description (base: 0x1000.0B00)

SPISTAT0: SPI Interface 0 Status (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	31'b0
0	RO	BUSY	SPI transfer in progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. Note: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is a '1'.	1'b0

SPICFG0: SPI Interface 0 Configuration (offset: 0x10)

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	23'b0
8	R/W	MSBFIRST	Bit transfer order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. Note: This bit applies to both the command and data.	1'b1
7	-	-	Reserved	1'b0
6	R/W	SPICLKPOL	SPI clock default state 0: The default state of the SPICLK is logic '0'. 1: The default state of the SPICLK is logic '1'. Note: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	1'b0

5	R/W	RXCKEDGE	SPI clock default state 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	1'b0
4	R/W	TXCKEDGE	SPI clock default state 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	1'b0
3	R/W	HIZSPI	Tri-state all SPI pin 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. Note: This bit overrides all normal functionality.	1'b0
2:0	R/W	SPICLK[2:0]	SPI clock divide control (the rate in following table should be change in the future) 0: SPICLK rate is system clock rate / 2 1: SPICLK rate is system clock rate / 4 2: SPICLK rate is system clock rate / 8 3: SPICLK rate is system clock rate / 16 4: SPICLK rate is system clock rate / 32 5: SPICLK rate is system clock rate / 64 6: SPICLK rate is system clock rate / 128 7: SPICLK is disabled	3'b0

**SPICTL0: SPI Interface 0 Control (offset: 0x14)**

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/W	HIZSDO	Tri-state data out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. Note: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	1'b0
2	W	STARTWR	Start SPI write transfer When this bit is written with a '1', the contents of the SPIDATA register are transferred to the SPI slave device. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
1	W	STARTRD	When this bit is written with a '1', a read from the SPI slave is started; the read data is placed in the SPIDATA register. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
0	R/W	SPIENA	0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	1'b0

**SPIDATA0: SPI Interface 0 Data (offset: 0x20)**

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	SPIDATA[7:0]	This register is used for command/data transfers on the SPI interface. The use of this register is given below: Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most	8'b0

			significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA[0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	
--	--	--	---	--

**SPISTAT1: SPI Interface 1 Status (offset: 0x40)**

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	30'b0
0	RO	BUSY	SPI transfer in progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. Note: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is a '1'.	1'b0

**SPICFG1: SPI Interface 1 Configuration (offset: 0x50)**

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	23'b0
8	R/W	MSBFIRST	Bit transfer order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. Note: This bit applies to both the command and data.	1'b1
7	-	-	Reserved	1'b0
6	R/W	SPICLKPOL	SPI clock default state 0: The default state of the SPICLK is logic '0'. 1: The default state of the SPICLK is logic '1'. Note: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	1'b0
5	R/W	RXCKEDGE	SPI clock default state 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	1'b0
4	R/W	TXCKEDGE	SPI clock default state 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	1'b0
3	R/W	HIZSPI	Tri-state all SPI pin 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. Note: This bit overrides all normal functionality.	1'b0
2:0	R/W	SPICLK[2:0]	SPI clock divide control (the rate in following table should be change in the future) 0: SPICLK rate is system clock rate / 2 1: SPICLK rate is system clock rate / 4 2: SPICLK rate is system clock rate / 8 3: SPICLK rate is system clock rate / 16 4: SPICLK rate is system clock rate / 32 5: SPICLK rate is system clock rate / 64 6: SPICLK rate is system clock rate / 128 7: SPICLK is disabled	3'b0

**SPICTL1: SPI Interface 1 Control (offset: 0x54)**

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	28'b0
3	R/W	HIZSDO	Tri-state data out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. Note: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	1'b0
2	W	STARTWR	Start SPI write transfer When this bit is written with a '1', the contents of the SPIDATA register are transferred to the SPI slave device. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
1	W	STARTRD	When this bit is written with a '1', a read from the SPI slave is started; the read data is placed in the SPIDATA register. Writing a '0' to this register has no effect. Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	1'b0
0	R/W	SPIENA	0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	1'b0

**SPIDATA1: SPI Interface 1 Data (offset: 0x60)**

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	SPIDATA[7:0]	This register is used for command/data transfers on the SPI interface. The use of this register is given below: Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA[0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	8'b0

**SPIARB SPI Interface ARBITER (offset: 0xF0) (Note: This register must be configured when SPI interface 1 want to be activated)**

Bits	Type	Name	Description	Initial value
31	R/W	ARB_EN	Arbiter Enable 0: Only SPI interface 0 will work. 1: SPI Interface 0/1 will work concurrently.	1'b0
30:2	-	-	Reserved	29'b0
1	R/W	SPI1_POR	The chip enable polarity indicator for SPI interface 1 0: Indicate the chip enable is low active 1: Indicate the chip enable is high active	1'b0
0	R/W	SPI0_POR	The chip enable polarity indicator for SPI interface 0	1'b0

<input type="checkbox"/>	<input type="checkbox"/>		0: Indicate the chip enable is low active 1: Indicate the chip enable is high active	<input type="checkbox"/>
--------------------------	--------------------------	--	---	--------------------------

Ralink confidential for cradlepoint

Draft

### 3.14 I<sup>2</sup>S Controller

#### 3.14.1 Features

- I<sup>2</sup>S transmitter, which can be configured as master or slave.
- Support 16-bit data, sample rate 48Khz
- Support stereo audio data transfer.
- 32 bytes FIFO are available for data transmission.
- Support GDMA access

#### 3.14.2 Block Diagram

The block diagram of I<sup>2</sup>S Transmitter is shown as below.

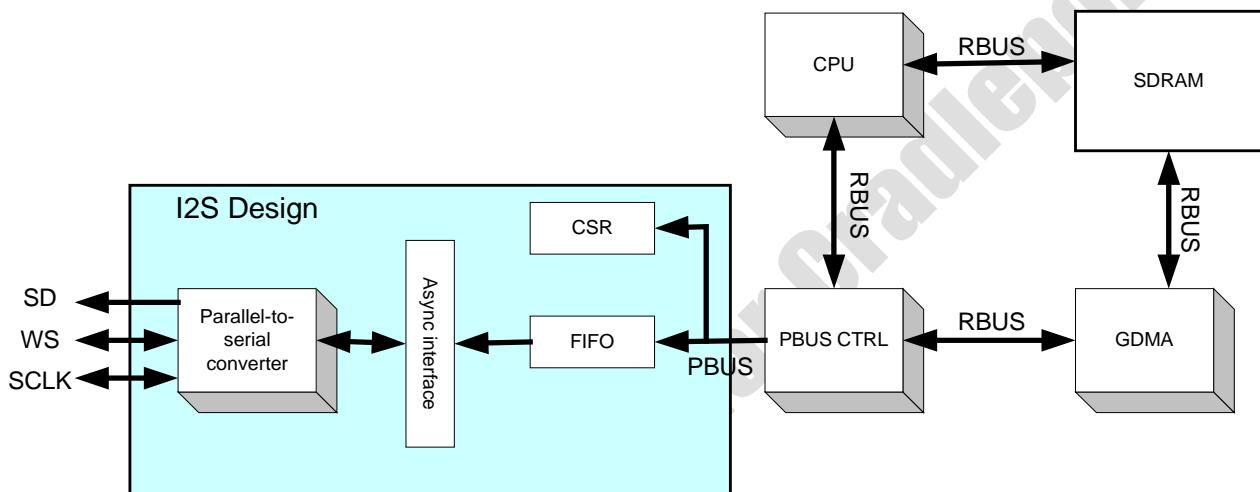


Fig. 3-14-1 The block diagram of I<sup>2</sup>S Transmitter

The I<sup>2</sup>S interface consists of two separate cores, a transmitter and a receiver. Both can operate in either master or slave mode. Here we will design only the transmitter in master or slave mode.

I<sup>2</sup>S signal timing:

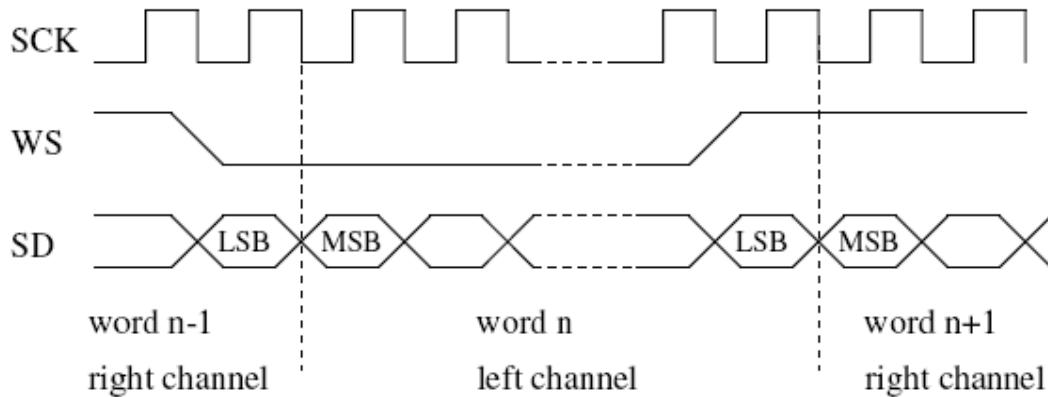


Fig. 3-14-2 I<sup>2</sup>S Transmitter

Serial data is transmitted in 2's complement with the MSB first. The transmitter always sends the MSB of the next word one clock period after the WS changes. Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must

be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next Word.

### **3.14.3 Register Description of I2S (base:1000.0A00)**

I2S\_CFG (offset: 0x00, default: 0x0000\_0840)

Bits	Type	Name	Description	Init Value
31	RW	I2S_EN	I <sup>2</sup> S enable, 1: enable 0: disable, all control registers of I <sup>2</sup> S will be clear to default value.	0
30	RW	DMA_EN	DMA Enable 1: enable dma access 0: disable dma access	0
29:25		Reserved	Reserved	
24	RW	TX_EN	Transmitter on/off control 1: Enable transmitter 0: Disable transmitter	0
23:21		Reserved	Reserved	
20	RW	RX_EN	Receiver on/off control 1: Enable receiver 0: Disable receiver	0
19:17	-	Reserved	Reserved	
16	RW	SLAVE_MODE	Master or Slave 0: Master: using internal clock 1: Slave: using external clock	1
15		Reserved	Reserved	
14:12	RW	RX_FF_THRES	FIFO threshold, As threshold reach, host/dma will notify to fill FIFO. (Unit = word) It should be >2 and <6	4
11	RW	RX_CH_SWAP	Channel swap control 0: No swapping 1: Swap CH0 and CH1	0
10	RW	RX_CH1_OFF	Channel 1 ON/OFF control 0: Channel 1 is ON 1: Channel 1 is OFF	0
9	RW	RX_CH0_OFF	Channel 0 ON/OFF control 0: Channel 0 is ON 1: Channel 0 is OFF	0
8:7	-	Reserved	Reserved	
6:4	RW	TX_FF_THRES	FIFO threshold, As threshold reach, host/dma will notify to fill FIFO. (Unit = word) It should be >2 and <6	4
3	RW	TX_CH_SWAP	Channel swap control 0: No swapping 1: Swap CH0 and CH1	0

2	RW	TX_CH1_OFF	Channel 1 ON/OFF control 0: Channel 1 is ON 1: Channel 1 is OFF	0
1	RW	TX_CH0_OFF	Channel 0 ON/OFF control 0: Channel 0 is ON 1: Channel 0 is OFF	0
0	RW	WS_INV	I <sup>2</sup> S ws signal direction. 1: opposite to SCLK 0: same as SCLK	0

**INT\_STATUS (offset: 0x04, default: 0x0)**

Bits	Type	Name	Description	Init Value
31:8	RO	Reserved	Reserved	0
7	RW	RX_DMA_FAULT	Find any fault in RX's DMA signals	0
6	RW	RX_OVRUN	The RX FIFO is overflow (Write '1' to clear)	0
5	RW	RX_UNRUN	The RX FIFO is underflow (Write '1' to clear)	0
4	RW	RX_THRES	The RX FIFO is lower than the defined threshold. (Write '1' to clear)	0
3	RW	TX_DMA_FAULT	Find any fault in TX's DMA signals	0
2	RW	TX_OVRUN	The TX FIFO is overflow (Write '1' to clear)	0
1	RW	TX_UNRUN	The TX FIFO is underflow (Write '1' to clear)	0
0	RW	TX_THRES	The FIFO is lower than the defined threshold. (Write '1' to clear)	0

**INT\_EN (offset: 0x08, default: 0x0)**

Bits	Type	Name	Description	Init Value
31:9	RO	Reserved	Reserved	0
7	RW	RX_INT3_EN	Enable INT_STATUS[7]	0
6	RW	RX_INT2_EN	Enable INT_STATUS[6]	0
5	RW	RX_INT1_EN	Enable INT_STATUS[5]	0
4	RW	RX_INTO_EN	Enable INT_STATUS[4]	0
3	RW	TX_INT3_EN	Enable INT_STATUS[3]	0
2	RW	TX_INT2_EN	Enable INT_STATUS[2]	0
1	RW	TX_INT1_EN	Enable INT_STATUS[1]	0
0	RW	TX_INTO_EN	Enable INT_STATUS[0]	0

**FF\_STATUS (offset: 0xc, default: 0x0)**

Bits	Type	Name	Description	Init Value
31:8	-	Reserved	Reserved	0
7:4	RO	RX_EPCNT	Available FIFO space can be written	8
3:0	RO	TX_EPCNT	Available FIFO space can be written	8

**TX\_FIFO\_WREG(offset: 0x10, default:0x0)**

Bits	Type	Name	Description	Init Value
31:0	W	TX_FIFO_WDATA	Write data buffer	0

**RX\_FIFO\_RREG(offset: 0x14, default:0x0)**

Bits	Type	Name	Description	Init Value
31:0	R	RX_FIFO_WDATA	Read data buffer	0

**I2S\_CFG1 (offset: 0x18, default:0x0)**

Bits	Type	Name	Description	Init Value
31	RW	LBK_EN	Loop Back Enable 0: normal mode 1: loop back mode Async_txFifo → Tx → Rx → Async_rxFifo	0
30	RW	EXT_LBK_EN	External Loop Back Enable	0

			0: normal mode 1: external loop back enable External A/D → Rx → Tx → External D/A	
29:2	-	Reserved	Reserved	
1:0	RW	DATA_FMT	0: I2S Format 1: Left Justified 2: Right Justified	0

**DIVCOMP\_Cfg:** Integer part of Divider Register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31	RW	CLK_EN	Enable the clock divider.	0
30:9	-	-	Reserved	0
8:0	RW	DIVCOMP	fraction part of divider.	0

**DIVINT\_Cfg:** Integer part of Divider Register (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	0
9:0	RW	DIVINT	Integer part of divider. Formula: $FreqOut = FreqIn * (1/2) * \{1 / [DIVINT + DIVCOMP / (512)]\}$ FreqIn is always fixed to 40MHz.	0

### 3.15 Memory Controller

#### 3.15.1 Features

- Support 1 SDRAM/DDR2 (16b/32b) chip selects
- Support 128MB(SDRAM)/256MB(DDR2) per chip select
- Support SDRAM transaction overlapping by early active and hidden pre-charge
- Support user SDRAM Init commands
- Support 4 banks per SDRAM chip select
- SDRAM burst length: 4 (fixed)
- DDR2 burst length: 4/8(programmable)
- Support Wrap-4 transfer
- Support Bank-Raw-Column and Raw-Bank-Column address mapping

#### 3.15.2 Block Diagram

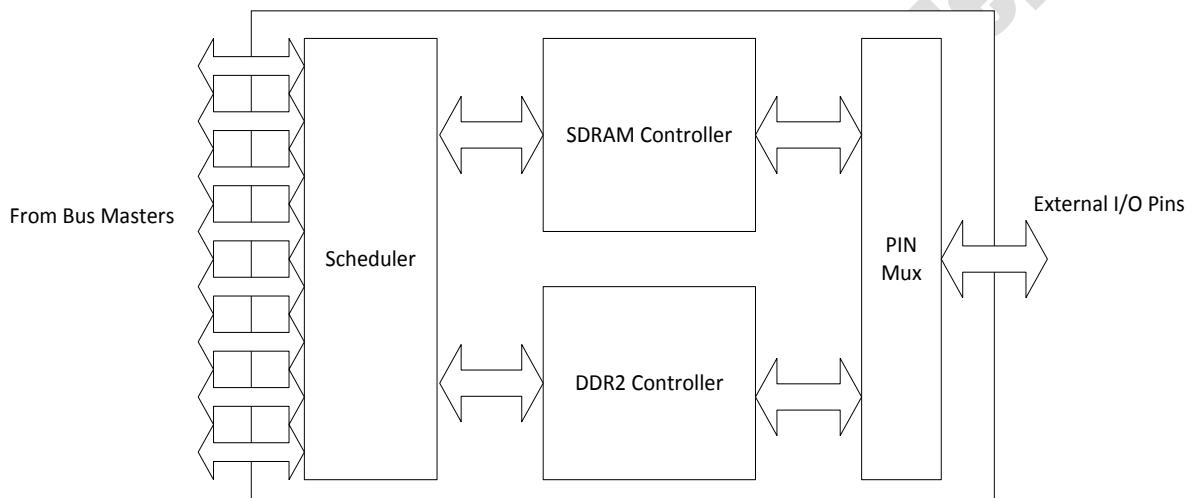


Fig. 3-15-1 Flash/SRAM/SDRAM controller Block Diagram

##### 3.15.2.1 SDRAM Initialization Sequence

SDRAMs require an initialization sequence before they are ready for reading and writing. The initialization sequence is described below.

- Step #1: setting SDRAM related timing in SDRAM\_CFG0
- Step#2: setting SDRAM size and refresh time in SDRAM\_CFG1 register with  
SDRAM\_INIT\_START = 1
- Step#3: Read SDRAM\_INIT\_DONE in SDRAM\_CFG1 register
- Step#4: if SDRAM\_INIT\_DONE !=1, go to Step#3, else SDRAM initialization sequence finished

##### Turn off power saving

Size	DRAM width (16bit), total bus width 16	DRAM width (16bit), total bus width 32	DRAM width (32bit), total bus width 32
<b>16Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xA0000600	SDRAM0: 0xD1825272, SDRAM1: 0xA1000600	N/A
<b>64Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xA0010600	SDRAM0: 0xD1825272, SDRAM1: 0xA1010600	SDRAM0: 0xD1825272, SDRAM1: 0xA1000600
<b>128Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xA0110600	SDRAM0: 0xD1825272, SDRAM1: 0xA1110600	SDRAM0: 0xD1825272, SDRAM1: 0xA1010600

<b>256Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xA0120600	SDRAM0: 0xD1825272, SDRAM1: 0xA1120600	SDRAM0: 0xD1825272, SDRAM1: 0xA1110600
<b>512Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xA0220600	SDRAM0: 0xD1825272, SDRAM1: 0xA1220600	SDRAM0: 0xD1825272, SDRAM1: 0xA1120600
<b>1024Mb</b>	N/A	N/A	N/A
<b>2048Mb</b>	N/A	N/A	N/A

**Turn on power saving with pre-charge power down mode**

Size	DRAM width (16bit), total bus width 16	DRAM width (16bit), total bus width 32	DRAM width (32bit), total bus width 32
<b>16Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB0000600	SDRAM0: 0xD1825272, SDRAM1: 0xB1000600	N/A
<b>64Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB0010600	SDRAM0: 0xD1825272, SDRAM1: 0xB1010600	SDRAM0: 0xD1825272, SDRAM1: 0xB1000600
<b>128Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB0110600	SDRAM0: 0xD1825272, SDRAM1: 0xB1110600	SDRAM0: 0xD1825272, SDRAM1: 0xB1010600
<b>256Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB0120600	SDRAM0: 0xD1825272, SDRAM1: 0xB1120600	SDRAM0: 0xD1825272, SDRAM1: 0xB1110600
<b>512Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB0220600	SDRAM0: 0xD1825272, SDRAM1: 0xB1220600	SDRAM0: 0xD1825272, SDRAM1: 0xB1120600
<b>1024Mb</b>	N/A	N/A	N/A
<b>2048Mb</b>	N/A	N/A	N/A

**Turn on power saving with active power down mode**

Size	DRAM width (16bit), total bus width 16	DRAM width (16bit), total bus width 32	DRAM width (32bit), total bus width 32
<b>16Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB8000600	SDRAM0: 0xD1825272, SDRAM1: 0xB9000600	N/A (ISSI have no this size)
<b>64Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB8010600	SDRAM0: 0xD1825272, SDRAM1: 0xB9010600	SDRAM0: 0xD1825272, SDRAM1: 0xB9000600
<b>128Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB8110600	SDRAM0: 0xD1825272, SDRAM1: 0xB9110600	SDRAM0: 0xD1825272, SDRAM1: 0xB9010600
<b>256Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB8120600	SDRAM0: 0xD1825272, SDRAM1: 0xB9120600	SDRAM0: 0xD1825272, SDRAM1: 0xB9110600
<b>512Mb</b>	SDRAM0: 0xD1825272, SDRAM1: 0xB8220600	SDRAM0: 0xD1825272, SDRAM1: 0xB9220600	SDRAM0: 0xD1825272, SDRAM1: 0xB9120600
<b>1024Mb</b>	N/A	N/A	N/A
<b>2048Mb</b>	N/A	N/A	N/A

**3.15.2.2 DDR2 Initialization Sequence**

DDR2 require an initialization sequence before they are ready for reading and write.

Initialization sequence is described below.

Step #1: Wait for 200us to set "0" in bit10 in address "0x1000\_0034"

Step #2: Read bit[21] of DDR\_CFG1 and wait for it become "1"

Step #3: Set DDR2 size and data width in DDR\_CFG1 (Please refer the table)

DDR2 SIZE	DDR2 WIDTH	DDR2 Total Width	DDR_CFG1
64Mb	8	16	32'h22252323
64Mb	8	32	32'h22253323
64Mb	16	16	32'h22262323
64Mb	16	32	32'h22263323
128Mb	8	16	32'h22292323

128Mb	8	32	32'h22293323
128Mb	16	16	32'h222A2323
128Mb	16	32	32'h222A3323
256Mb	8	16	32'h222D2323
256Mb	8	32	32'h222D3323
256Mb	16	16	32'h222E2323
256Mb	16	32	32'h222E3323
512Mb	8	16	32'h22312323
512Mb	8	32	32'h22313323
512Mb	16	16	32'h22322323
512Mb	16	32	32'h22323323
1Gb	8	16	32'h22352323
1Gb	16	16	32'h22362323
1Gb	16	32	32'h22363323
2Gb	16	16	32'h223A3323

For DDR2 Performance, need to follow this CFG0 table for different DDR2 size

DDR2 Frequency: 166MHz (500MHz/3)

<b>DDR SIZE</b>	<b>DDR WIDTH</b>	<b>DDR Total Width</b>	<b>DDR_CFG0(tRFC/tREFI)</b>
64Mb	8	16	32'h2498E4F0
64Mb	8	32	32'h2498E4F0
64Mb	16	16	32'h2498E4F0
64Mb	16	32	32'h2498E4F0
128Mb	8	16	32'h2498E4F0
128Mb	8	32	32'h2498E4F0
128Mb	16	16	32'h2498E4F0
128Mb	16	32	32'h2498E4F0
256Mb	8	16	32'h2498E4F0
256Mb	8	32	32'h2498E4F0
512Mb	8	16	32'h249924F0
512Mb	8	32	32'h249924F0
512Mb	16	16	32'h249924F0
512Mb	16	32	32'h249924F0
1Gb	8	16	32'h249964F0
1Gb	16	16	32'h249964F0
1Gb	16	32	32'h249964F0
2Gb	16	16	32'h249A24F0

DDR2 Frequency: 160MHz (480MHz/3)

<b>DDR SIZE</b>	<b>DDR WIDTH</b>	<b>DDR Total Width</b>	<b>DDR_CFG0(tRFC/tREFI)</b>
64Mb	8	16	32'h2498E4C0
64Mb	8	32	32'h2498E4C0
64Mb	16	16	32'h2498E4C0
64Mb	16	32	32'h2498E4C0
128Mb	8	16	32'h2498E4C0
128Mb	8	32	32'h2498E4C0
128Mb	16	16	32'h2498E4C0
128Mb	16	32	32'h2498E4C0
256Mb	8	16	32'h2498E4C0
256Mb	8	32	32'h2498E4C0
256Mb	16	16	32'h2498E4C0
256Mb	16	32	32'h2498E4C0

512Mb	8	16	32'h249924C0
512Mb	8	32	32'h249924C0
512Mb	16	16	32'h249924C0
512Mb	16	32	32'h249924C0
1Gb	8	16	32'h249964C0
1Gb	16	16	32'h249964C0
1Gb	16	32	32'h249964C0
2Gb	16	16	32'h249A24C0

DDR2 Frequency: 125MHz (500MHz/4)

<b>DDR SIZE</b>	<b>DDR WIDTH</b>	<b>DDR Total Width</b>	<b>DDR_CFG0(tRFC/tREFI)</b>
64Mb	8	16	32'h2498A3B0
64Mb	8	32	32'h2498A3B0
64Mb	16	16	32'h2498A3B0
64Mb	16	32	32'h2498A3B0
128Mb	8	16	32'h2498A3B0
128Mb	8	32	32'h2498A3B0
128Mb	16	16	32'h2498A3B0
128Mb	16	32	32'h2498A3B0
256Mb	8	16	32'h2498A3B0
256Mb	8	32	32'h2498A3B0
256Mb	16	16	32'h2498A3B0
256Mb	16	32	32'h2498A3B0
512Mb	8	16	32'h2498C3B0
512Mb	8	32	32'h2498C3B0
512Mb	16	16	32'h2498C3B0
512Mb	16	32	32'h2498C3B0
1Gb	8	16	32'h249903B0
1Gb	16	16	32'h249903B0
1Gb	16	32	32'h249903B0
2Gb	16	16	32'h2499A3B0

<b>DDR2 SIZE</b>	<b>DDR2 WIDTH</b>	<b>DDR2 Total Width</b>	<b>DDR_CFG0(tRFC)</b>
64Mb	8	16	32'h2498E130
64Mb	8	32	32'h2498E130
64Mb	16	16	32'h2498E130
64Mb	16	32	32'h2498E130
128Mb	8	16	32'h2498E130
128Mb	8	32	32'h2498E130
128Mb	16	16	32'h2498E130
128Mb	16	32	32'h2498E130
256Mb	8	16	32'h2498E130
256Mb	8	32	32'h2498E130
256Mb	16	16	32'h2498E130
256Mb	16	32	32'h2498E130
512Mb	8	16	32'h24992130
512Mb	8	32	32'h24992130
512Mb	16	16	32'h24992130
512Mb	16	32	32'h24992130
1Gb	8	16	32'h24996130
1Gb	16	16	32'h24996130
1Gb	16	32	32'h24996130
2Gb	16	16	32'h249A2130

Note: The system only have 256MB(2Gb) memory space for DRAM, so there are no some types of combination of DDR2 (Please refer the list table)

<b>DDR2 SIZE</b>	<b>DDR2 WIDTH</b>	<b>DDR2 Total Width</b>
1Gb	8	32
2Gb	8	16
2Gb	8	32
2Gb	16	32

### 3.15.3 Register Description (base: 0x1000.0300)

SDRAM\_CFG0: SDRAM Configuration 0 (offset: 0x00)

Bits	Type	Name	Description	Initial value
31	RO	ALWAYS_ONE	Use as an identification for Rbus controller	1'b1
30-29	-	-	Reserved	2'b00
28	R/W	TWR	Write Recovery time number of system clock cycles – 1.	1'b1
27:24	R/W	TMRD	LOAD MODE to any other command delay number of system clock cycles – 1.	4'b0001
23:20	R/W	TRFC	AUTO REFRESH period number of system clock cycles – 1.	4'b1001
19:18	-	-	Reserved	2'b00
17:16	R/W	TCAS	READ command to data valid delay (CAS latency) in number of system clock cycles – 1.	2'b10
15:12	R/W	TRAS	ACTIVE to PRECHARGE command delay in number of system clock cycles – 1.	4'b0101
11:10	-	-	Reserved	2'b00
9:8	R/W	TRCD	ACTIVE to READ or WRITE delay in number of system clock cycles – 1.	2'b10
7:4	R/W	TRC	ACTIVE to ACTIVE command period in number of system clock cycles -1	4'b1000
3:2	-	-	Reserved	2'b00
1:0	R/W	TRP	PRECHARGE command period in number of system clock cycles –1.	2'b10

SDRAM\_CFG1: SDRAM Configuration 1 (offset: 0x04)

Bits	Type	Name	Description	Initial value
31	R/W	SDRAM_INIT_START	Write 1 to perform SDRAM initialization sequence. Cannot set it to zero after initialization.	1'b0
30	RO	SDRAM_INIT_DONE	0: SDRAM has not been initialized 1: SDRMA has been initialized	1'b0
29	R/W	RBC_MAPPING	1: {ROW ADDR, BANK ADDR, COL ADDR} address mapping scheme 0: {BANK ADDR, ROW ADDR, COL ADDR} address mapping scheme	1'b0
28	R/W	PWR_DOWN_EN	1: Enable SDRAM pre-charge power down mode to save standby power. When enabled, SDRAM will go 0: Disable SDRAM pre-charge power down mode	1'b0
27	R/W	PWR_DOWN_MODE	1: Active power down mode 0: Pre-charge power down mode	1'b0
26:25	-	-	Reserved	4'b0
24	R/W	SDRAM_WIDTH	Number of SDRAM data bus bits: (#TBD##) 0: 16 bits 1: 32 bits (default)	1'b1
23:22	-	-	Reserved	2'b0

21:20	R/W	NUMCOLS	Number of Column address bits: 0: 8 Column address bits 1: 9 Column address bits (default) 2: 10 Column address bits 3: 11 Column address bits	2'b01
19:18	-	-	Reserved	2'b00
17:16	R/W	NUMROWS	Number of Row address bits: 0: 11 Row address bits 1: 12 Row address bits (default) 2: 13 Row address bits 3: 14 Row address bits (not allocable if boot from NAND flash is enabled)	2'b10
15:0	R/W	TREFR	AUTO REFRESH period in number of SDRAM clock cycles – 1.	16'h0600

\*PS: SDRAM Self Refresh Mode and Power Down will be supported later.

DRAM\_ARB\_CFG: DRAM arbiter configuration (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	2'b0
29	R/W	CPU_POST_LOCK_EN	Enable arbiter to lock CPU for a while after service CPU 0: Disable 1: Enable	1'b0
28	R/W	CPU_PRE_LOCK_EN	Enable arbiter to lock CPU when detect the CPU command present in OCP bus 0: Disable 1: Enable	1'b0
27:16	-	0	Reserved	12'b0
15:8	R/W	DMA_PENDING_CNT	The counter is used to cancel the CPU lock when DMA request was pending for specified period clock count. The valid value is 1~255, "0" means to cancel the CPU pre/post lock function	8'b0
7:4	-	-	Reserved	
3:0	R/W	CPU_LOCK_CNT	The counter is used to count the period of CPU post lock after service the CPU. The valid value is 1~15. "0" means post lock is 0 cycles	4'b0

Reserved (offset: 0x0C)

ILL\_ACC\_ADDR: Illegal Access Address Capture (offset: 0x10)

Bits	Type	Name	Description	Initial value
31: 0	RO	ILL_ACC_ADDR	If any bus masters (including CPU) issue illegal accesses (e.g. accessing to reserved memory space, non-double-word accessing to configuration registers), the address of the illegal transaction is captured in this register. An illegal interrupt will generate to indicate this exception.	32'b0

ILL\_ACC\_TYPE: Illegal Access TYPE Capture (offset: 0x14)

Bits	Type	Name	Description	Initial value
31	RO, W1C	ILL_INT_STATUS	1: Indicate the illegal access interrupt is pending 0: Indicate the illegal access interrupt is cleared Write 1 to this bit will clear both ILL_ACC_ADDR and ILL_ACC_TYPE registers and thus clear the ILL_INT_STATUS.	1'b0
30	RO	ILL_ACC_WR	Indicate the access type of the illegal access 1: illegal access is write 0: illegal access is read This value is reset to 0 when ILL_ACC_ADDR is written	1'b0
29:20	-	-	Reserved	1'b0
19:16	RO	ILL_ACC_BSEL	Indicate the byte select of the illegal access This value is reset to 0 when ILL_ACC_ADDR is written	1'b0

15:11	-	-	Reserved	1'b0
10:8	RO	ILL_IID	Indicate the initiator ID of the illegal access. 0: CPU 1: DMA 2: PPE 3: Ethernet PDMA RX 4: Ethernet PDMA TX 5: PCI/PCIE 6: Embedded WLAN MAC/BBP 7: USB  This value is reset to 0 when ILL_ACC_ADDR is written	3'b0
7:0	RO	ILL_ACC_LEN	Indicate the access size of the illegal access. The unit is byte  This value is reset to 0 when ILL_ACC_ADDR is written.	8'b0

DDR\_SELF\_REFRESH: (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	27'b0
4	R/W	SR_AUTO_EN	Auto self-refresh enable for power saving 0: Disable auto self-refresh feature 1: Enable auto self-refresh feature	1'b0
3:2	-	-	Reserved	2'b0
1	RO	SRACK_B	Self refresh acknowledge status. 0: The DDR2 is under self refresh mode 1: The DDR2 has been exit from the self refresh mode (when DDR2 from self refresh mode to normal mode, it will take about 200 clock cycles)	1'b1
0	R/W	SRREQ_B	Self refresh request control. It is low active. 0: Request DDR2 to enter into self refresh mode. 1: Request DDR2 to exit the self refresh mode.	1'b1

DDR\_SR\_TARGET\_CNT: (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:24	RO	PD_CNT	A counter to show the times of entering self-refresh mode This counter only was referenced when the SR_AUTO_EN is set. This counter is use to count the period of the DDR2 IDLE status. When the IDLE period reach to the specified time period (SR_TAR_CNT*256/SYS_CLK_FREQ), the DDR2 will be automatically enter self-refresh mode. Software can configure it for suitable value.	8'h00
23:0	R/W	SR_TAR_CNT	Here is reference table 166MHz: 24'h03FFFF * 256* 6.02ns ~= 404ms 160MHz: 32'h03FFFF * 256* 6.25ns ~= 419ms 125MHz: 32'h03FFFF * 256* 8.0ns ~=536ms	24'h03FFFF

Reserved: (offset: 0x20~3C)

DDR\_CFG0: (offset: 0x40)

Bits	Type	Name	Description	Initial value
31:28	R/W	Active-to-Active delay of different banks[3:0]	The minimum number of clock cycles from an active command to the next active command for different banks ( $T_{RRD}$ ). For DDR2 devices, this is required to be a minimum of 2 regardless of the cycle time.	4'b0010
27:23	R/W	Active to Pre-charge time [4:0]	It is the number of clock cycles from an active command until a pre-charge command is allowed. To obtain this value, one should divide the minimum RAS# to pre-charge delay of the SDRAM by the clock cycle time ( $T_{RAS}$ ). The sum of Active-to-	5'b01001

			Pre-charge and Pre-charge-to-Active should be equal or larger than active-to-active delay of the same bank ( $T_{RC}$ )	
22:19	R/W	Pre-charge to Active command time [3:0]	The number of clock cycles needed for the SDRAM to recover from a pre-charge command and ready to accept the next active command. To obtain this value, one should divide the RAS# pre-charge time of the SDRAM ( $T_{RP}$ ) by the clock cycle time. The sum of Active-to-Pre-charge and Pre-charge-to-Active should be equal or larger than active-to-active delay of the same bank ( $T_{RC}$ )	4'b0011
18:13	R/W	Refresh to Refresh or Active command delay [5:0]	This field is half the number of clock cycles needed for the SDRAM to recover from a refresh signal to be ready to take the next command. To obtain this value, one should divide the SDRAM row cycle time ( $T_{RFC}$ ) by the clock cycle time.	6'b011010
12:0	R/W	Refresh Interval [12:0]	The number of clock cycles from one refresh command to the next refresh command. To obtain this value, one should divide the periodic refresh interval ( $T_{REFI}$ ) by the clock cycle time. The actual timing of issuing a pre-charge command may be delayed by if the SDRAM is processing a normal access. However, the delay is not accumulative so there is no need to shorten the refresh interval to account for memory access time. The non-accumulative refresh delay typically increases memory bandwidth by a few percentage points.	13'b000100 1011000

DDR\_CFG1: (offset: 0x44)

Bits	Type	Name	Description	Initial value
31:28	R/W	Write-to-Read delay [3:0]	The write-to-read delay ( $T_{WTR}$ ) (last write data to the next read command) as specified by the DDR2 data sheet	4'b0010
27:24	R/W	Read-to-Pre-charge delay	The read-to-pre-charge delay ( $T_{RTP}$ ) as specified by the DDR2 data sheet. Note that this is a DDR2 requirement, and requires a minimum of 2 cycles.	4'b0010
23:22	-	-	Reserved	2'b00
21	R/W	User data width	This bit is 1 to indicate 64-bit user data width and 0 to indicate 32-bit user data width. When user data width is 32-bits, DDR2 width (bit 13:12) must be "10" to indicate DDR2 data width "16". Note: Our system is always 64-bits. Don't modify it.	1'b1
20:18	R/W	DDR2 size	000: Reserved, 001: individual DDR2 is 64Mbit 010: individual DDR2 is 128Mbit 011: individual DDR2 is 256Mbit. 100: individual DDR2 is 512Mbit. 101: individual DDR2 is 1Gbit. 110: individual DDR2 is 2Gbit 111: Reserved	3'b101
17:16	R/W	DDR2 width	00: Reserved 01: individual DDR2 is 8-bit wide 10: individual DDR2 is 16-bit wide 11: Reserved	2'b01
15:14	R/W	External banks	00: 1 external bank, 1 module. (CS#[0]) 01: 2 external bank, 1 module. (CS#[1:0]), 10: Reserved 11: 2 external banks, 2 modules. (CS#[1:0]) Note: In RT3883, we only have one CS pin.	2'b00
13:12	R/W	Total DDR2 data path	00: Reserved 01: Reserved	2'b10

		width	10: 16-bits 11: 32-bits. Allowed only when user data width is 64-bits (bit 21 is "1").  This field specifies the total data width to the DDR2. For example, if four 8-bit wide DDR2 chips are used in parallel to form a 32-bit DDR2 data width, this field should be defined as "11" to indicate 32-bit width. In this case, bit 17:16 should define as "01".	
11:8	R/W	Write Recovery Time [3:0]	The clock cycles needed for the DDR2 to recover from a write command and be able to accept a pre-charge command. To obtain this value, one should divide the SDRAM write recovery time by the clock cycle time ( $T_{WR}$ )	4'b0011
7:4	R/W	Mode register set to active [3:0]	The number of clock cycles after the setting of the mode registers in the DDR2 and before the issue of the next command. To obtain this value, one should divide the Mode Register Set Cycle time ( $T_{MRD}$ ) by the clock cycle time.	4'b0010
3:0	R/W	RAS# to CAS# delay time[3:0]	The number of clock cycles from an active command to a read/write assertion. To obtain this value, one should divide the RAS# to CAS# delay time ( $T_{RCD}$ ) by the clock cycle time.	4'b0011

DDR\_CFG2: (offset: 0x48)

Bits	Type	Name	Description	Initial value
31	R/W	REGE	This bit should be high when external registers are inserted in the control and address signals between the controller and the DDR2 SDRAM. One example of such instance is when register mode SDRAM DIMM is used. This bit should be low when the control and address signals from the controller is connected to the SDRAM without register delay	1'b0
30	R/W	DDR2 Mode	This bit determines whether the controller is in DDR1 or DDR2 mode 0: DDR1 mode 1: DDR2 mode	1'b1
29:28	R/W	DQS window control for DQSO	Control the mask of DQSO window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	2'b00
27:26	R/W	DQS window control for DQS1	Control the mask of DQS1 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	2'b00
25:24	R/W	DQS window control for DQS2	Control the mask of DQS2 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	2'b00
23:22	R/W	DQS window control for DQS3	Control the mask of DQS3 window leading and trailing edge 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window)	2'b00

			01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No any extended cycle for leading and trailing edge of DQS window (minimum window)	
21:13	-	-	Reserved	9'b0
12	R/W	PD	Active Power Down Exit Time 0: Fast exit time ( $T_{XARD}$ ) 1: Slow exit time( $T_{XARDS}$ )	1'b0
11:9	R/W	WR	Auto Pre-charge Write Recovery ( $T_{DAL}$ ).	3'b010
8	R/W	DLLRESET	0: Normal operation. 1: Normal operation with DLL reset.	1'b0
7	R/W	TESTMODE	0: Normal operation. 1: Test mode. The user must keep this bit at "0" if the SDRAM does not support the TESTMODE bit.	1'b0
6:4	R/W	CAS Latency [2:0]	This register specifies the number of the clock cycles from the assertion of a read/write signal to the SDRAM until the first valid data on the output from the SDRAM. The valid numbers are: "101": 5 "010": 2 "110": Reserved "011": 3 "100": 4	3'b011
3	RO	Burst Type	This register is hardwired to "0" to indicate sequential burst type.	1'b0
2:0	R/W	Burst Length [2:0]	This register indicates the burst length of the read/write transaction. "010" is a burst of 4. "011" is a burst of 8. Burst of 4 is not allowed when user data is 64-bit while SDRAM data is 16-bit. Burst of 8 is allowed in all user/SDRAM data width combination. Other values of burst length are not allowed.	3'b011

**DDR\_CFG3: (offset: 0x4C)**

Bits	Type	Name	Description	Initial value
31:13	-	-	Reserved	19'b0
12	R/W	Qoff	Output buffer disable 0: output buffer is enabled 1: output buffer is disabled	1'b0
11	R/W	RDQS	This bit enables the redundant DQS function if supported by the SDRAM. This bit is used for DDR2 SDRAM only.	1'b0
10	R/W	Differential DQS	0: enable differential DQS 1: disable differential DQS This bit is used for DDR2 SDRAM only.	1'b1
9:7	R/W	OCD	These bits support the OCD function if supported by the SDRAM. Value programmed in these register bits will be programmed into the SDRAM at EMR1 programming. This bit is used for DDR2 SDRAM only.	3'b000
6	R/W	RTT bit 1	Used together with bit 2 (RTT0) to control ODT. RTT1, RTT0 00 ODT disabled. 01 75 ohm 10 150 ohm 11 Reserved This bit is used for DDR2 SDRAM only.	1'b0
5:3	R/W	Additive Latency	Additive Latency. 000: 0 cycle	3'b010

			001: 1 cycle 010: 2 cycles 011: 3 cycles 100: 4 cycles 101: 5 cycles others: reserved This bit is used for DDR2 SDRAM only.	
2	R/W	RTT bit 0	Used together with bit 6 (RTT1) to control ODT. This bit is used for DDR2 SDRAM only.	1'b0
1	R/W	DS	Drive Strength 0: 100% drive strength. 1: 60% drive strength.	1'b1
0	R/W	DLL	0: Enable. 1: Disable.	1'b0

DDR\_CFG4: (offset: 0x50)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	27'b0
4:0	R/W	FAW	DDR2 devices imposes a restriction in that no more than 4 ACTIVE commands may be issued in a given FAW period. To obtain this value, one should divide the Four Bank Activate period ( $T_{FAW}$ ) of the DDR by the clock cycle time. These bits are ignored in 4 bank devices.	5'b10100

Reserved: (offset: 0x54~0x5C)

DDR\_CFG8: (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:24	R/W	DQ_GROUP3_DELAY_SEL	Data output delay path selection for group3(MD24~MD31) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111
23:16	R/W	DQ_GROUP2_DELAY_SEL	Data output delay path selection for group2(MD16~MD23) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111
15:8	R/W	DQ_GROUP1_DELAY_SEL	Data output delay path selection for group1(MD8~MD15) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns	8'b0000_1111

			8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	
7:0	R/W	DQ_GROUP0_DELAY_SEL	Data output delay path selection for group0(MD0~MD7) 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0000_1111

DDR\_CFG9: (offset: 0x64)

Bits	Type	Name	Description	Initial value
31:24	R/W	DQS3_DELAY_SEL	DQS3 input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_1111
23:16	R/W	DQS2_DELAY_SEL	DQS2 input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_1111
15:8	R/W	DQS1_DELAY_SEL	DQS1 input delay path selection 8'b0000_0000: 0.4ns (typical case) 8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	8'b0001_1111
7:0	R/W	DQSO_DELAY_SEL	DQSO input delay path selection 8'b0000_0000: 0.4ns (typical case)	8'b0001_1111

		8'b0000_0001: 0.5 ns 8'b0000_0011: 0.6 ns 8'b0000_0111: 0.7 ns 8'b0000_1111: 0.8 ns 8'b0001_1111: 0.9 ns 8'b0011_1111: 1.0 ns 8'b0111_1111: 1.1 ns 8'b1111_1111: 1.1 ns	
--	--	--	--

Ralink confidential for cradlepoint

Draft

### **3.16 Flash/SRAM/Codec Controller**

#### **3.16.1 Features**

- Support 2 Flash(SRAM)(8/16b) chip selects with independent timing parameters
- Support 2 SRAM-like Codec(16b/32b) with independent timing parameter
- Support up to two DMA channel for SRAM-like Codec
- Support 32MB/Flash(SRAM) per chip select
- Support 128B memory space for SRAM-like Codec per chip select
- Support Wrap-4 transfer

#### **3.16.2 Register Description (base: 0x1000.0700)**

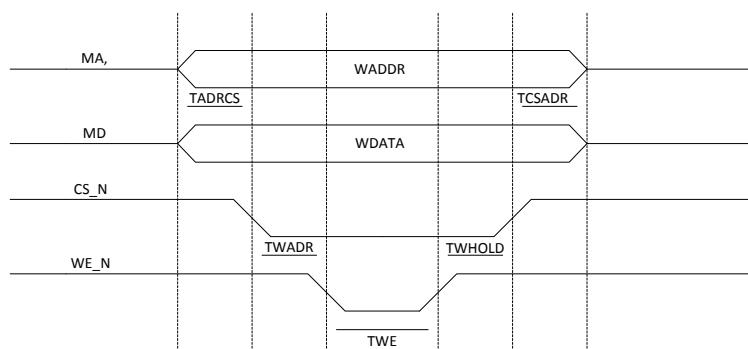
FLASH\_CFG0: Flash Bank 0 Configuration (offset: 0x00)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:26	RO	FLASH_WIDTH0	Number of Flash Chip Select0 data bus bits: 0: 8 bits 1: 16 bits (default) 2: reserved 3: reserved Note: This value is from boot strapping.	2'b01
25	-	-	Reserved	1'b0
24	R/W	CSADRO	Address hold time from Chip Select in number of system clock cycles	1'b1
23:22	-	-	Reserved	2'b0
21:20	R/W	TWHOLD0	Chip select and Data hold time from Write Enable in number of system clock cycles	2'b01
19:18	-	-	Reserved	2'b0
17:16	R/W	TRHOLD0	Chip select hold time from Output Enable in number of system clock cycles	2'b01
15:12	R/W	TWE0	Write Enable duration in number of system clock cycles	4'b1111
11:8	R/W	TOE0	Output Enable duration in number of system clock cycles	4'b1111
7:6	R/W	TRADRO	Read address setup in number of system clock cycles	2'b10
5:4	R/W	TWADRO	Write address setup in number of system clock cycles	2'b10
3:2	-	-	Reserved	2'b0
1:0	R/W	TADRC0	Address setup time prior to Chip Select in number of system clock cycles	2'b01

\*PS: Flash\_Width0 (8/16/32 bits) is configured by power on pin capture.

Note: Total of width specified by TADRC0 + TWADRO/TRADRO + TWE/TOE + TWHOLD/TRHOLD + TCSADR may not be fewer than 3 clock cycles.

Flash, Async. SRAM Write Timing



Flash, Async. SRAM Read Timing

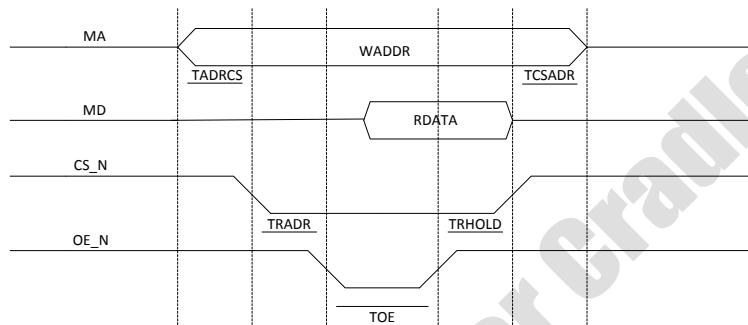


Fig. 3-16-1 Flash/SRAM/SDRAM Controller R/W waveform

Note: Total of width specified by TADRCS + TWADR/TRADR + TWE/TOE + TWHOLD/TRHOLD + TCSADR may not be fewer than 3 clock cycles

**FLASH\_CFG1: Flash Bank 1 Configuration (offset: 0x04)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:26	RW	FLASH_WIDTH1	Number of Flash Chip Select1 data bus bits: 0: 8 bits 1: 16 bits (default) 2: 32bits	2'b01
25	-	-	Reserved	1'b0
24	R/W	CSADR1	Address hold time from Chip Select in number of system clock cycles	1'b1
23:22	-	-	Reserved	2'b0
21:20	R/W	TWHOLD1	Chip select and Data hold time from Write Enable in number of system clock cycles	2'b01
19:18	-	-	Reserved	2'b0
17:16	R/W	TRHOLD1	Chip select hold time from Output Enable in number of system clock cycles	2'b01
15:12	R/W	TWE1	Write Enable duration in number of system clock cycles	4'b1111
11:8	R/W	TOE1	Output Enable duration in number of system clock cycles	4'b1111
7:6	R/W	TRADR1	Read address setup in number of system clock cycles	2'b10
5:4	R/W	TWADR1	Address setup in number of system clock cycles	2'b10
3:2	-	-	Reserved	2'b0
1:0	R/W	TADRC1	Address setup time prior to Chip Select in number of system clock cycles	2'b01

**Codec\_CFG0: Codec Bank 0 Configuration (offset: 0x40)**

Bits	Type	Name	Description	Initial value
31	RW	Codec0_EN	Codec bank0 memory access enable 0: Disable 1: Enable	1'b0
30:28	-	-	Reserved	3'b0
27:26	RW	Codec_WIDTH0	Number of Flash Chip Select1 data bus bits: 0: Reserved 1: 16 bits (default) 2: 32bits	2'b01
25	-	-	Reserved	1'b0
24	R/W	CSADRO	Address hold time from Chip Select in number of system clock cycles	1'b1
23:22	-	-	Reserved	2'b0
21:20	R/W	TWHOLD0	Chip select and Data hold time from Write Enable in number of system clock cycles	2'b01
19:18	-	-	Reserved	2'b0
17:16	R/W	TRHOLD0	Chip select hold time from Output Enable in number of system clock cycles	2'b01
15:12	R/W	TWE0	Write Enable duration in number of system clock cycles	4'b1111
11:8	R/W	TOE0	Output Enable duration in number of system clock cycles	4'b1111
7:6	R/W	TRADRO	Read address setup in number of system clock cycles	2'b10
5:4	R/W	TWADRO	Address setup in number of system clock cycles	2'b10
3:2	-	-	Reserved	2'b0
1:0	R/W	TADRC0	Address setup time prior to Chip Select in number of system clock cycles	2'b01

**Codec\_CFG1: Codec Bank 1 Configuration (offset: 0x44)**

Bits	Type	Name	Description	Initial value
31	RW	Codec1_EN	Codec bank1 memory access enable 0: Disable 1: Enable	1'b0
30:28	-	-	-	3'b0
27:26	RW	Codec_WIDTH1	Number of Flash Chip Select1 data bus bits: 0: Reserved 1: 16 bits (default) 2: 32bits	2'b01
25	-	-	Reserved	1'b0
24	R/W	CSADR1	Address hold time from Chip Select in number of system clock cycles	1'b1
23:22	-	-	Reserved	2'b0
21:20	R/W	TWHOLD1	Chip select and Data hold time from Write Enable in number of system clock cycles	2'b01
19:18	-	-	Reserved	2'b0
17:16	R/W	TRHOLD1	Chip select hold time from Output Enable in number of system clock cycles	2'b01
15:12	R/W	TWE1	Write Enable duration in number of system clock cycles	4'b1111
11:8	R/W	TOE1	Output Enable duration in number of system clock cycles	4'b1111
7:6	R/W	TRADR1	Read address setup in number of system clock cycles	2'b10
5:4	R/W	TWADR1	Address setup in number of system clock cycles	2'b10
3:2	-	-	Reserved	2'b0
1:0	R/W	TADRC1	Address setup time prior to Chip Select in number of system clock cycles	2'b01

**Codec\_DMA\_CFG: Codec DMA Configuration (offset: 0x48)**

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	10'b0
21:20	R/W	TWHOLD	Data hold time from inactive of Write Enable in number of system clock cycles	2'b01
19:16	-	-	Reserved	4'b0
15:12	R/W	TWE	Write Enable duration in number of system clock cycles	4'b1111
11:8	R/W	TOE	Output Enable duration in number of system clock cycles	4'b1111
7:5	-	-	Reserved	2'b0
4	R/W	DMA_MODE	DMA mode selection 0: Both of DMA channel 0/1 use to RD0_N/WR0_N control signal 1: DMA channel 0 use RD0_N/WR0_N and DMA channel 1 use RD1_N/WR1_N	1'b0
3:1	-	-	Reserved	3'b0
0	R/W	DMA_EN	DMA function enable	1'b0

### 3.16.3 Codec0 Memory Space (base: 0x1000.3000)

Codec0\_Memory(offset: 0x00~0x7F) → 128Byte only

Codec\_DMA\_CH0(offset: 0x100)

### 3.16.4 Codec1 Memory Space (base: 0x1000.3800)

Codec1\_Memory(offset: 0x00~0x7F) → 128Byte only

Codec\_DMA\_CH1(offset: 0x100)

## 3.17 NAND Flash Controller

### 3.17.1 Introduction

In price, the NAND flash memory is much close to NOR flash memory. So some users start to execute the boot code on a NAND flash and execute the main code on a DRAM.

### 3.17.2 Specification

#### 3.17.2.1 Features

1. Support read / erase / page program NAND flash memory.
2. Hardware ECC engine. (Hardware generating and software correcting)
3. Only supports NAND flash memory with 512-bytes page size and 8-bits data.
4. Indirect access for special command.
5. Configurable write protect register.
6. Little / bit ending operation.
7. Flash pin share with PCI interface. (Under PCI host mode)

#### 3.17.2.2 Normal Mode Flow

Under this mode, CPU must first configure the command register of the controller register. After configuration of the command register, the controller will send serial command and address to NAND flash memory. And then a byte data will be read (write) from data buffer (NAND flash) to NAND flash (data buffer). At the same time, CPU or GDMA is responsible to write (read) data into (from) data buffer.

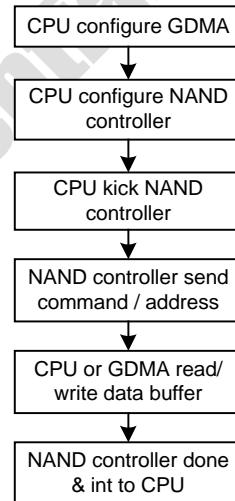


Fig. 3-17-1 Normal Mode Flow

### 3.17.2.3 ECC

The ECC engine uses Hamming code. The Hamming code will generate a 24-bit ECC per 512 bytes in order to perform a 2-bit detection and a 1-bit correction.

In our application, hardware will perform ECC error detection, and software will perform 1-bit ECC error correction.

Following table shows how the 24-bit ECC was generated from 512-byte data.

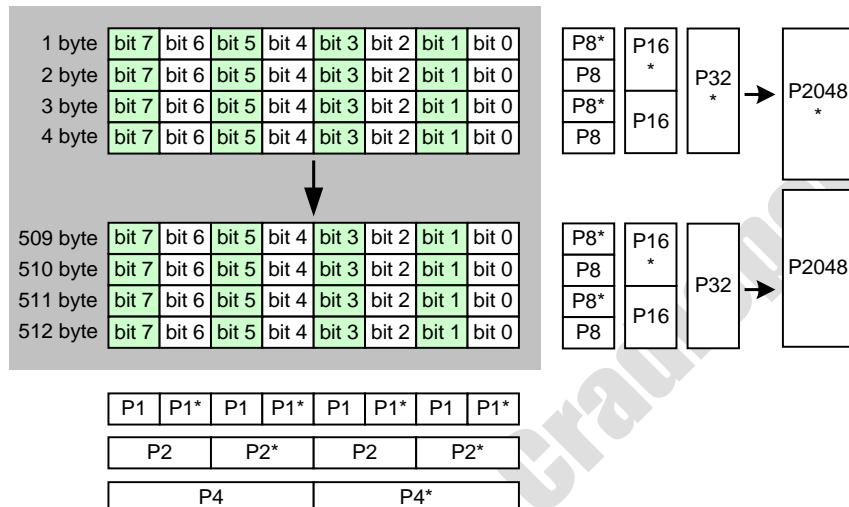


Fig. 3-17-2 24-bit ECC was generated from 512-byte data

$$P1 = \text{bit}7 \wedge \text{bit}5 \wedge \text{bit}3 \wedge \text{bit}1 \wedge P1$$

$$P2 = \text{bit}7 \wedge \text{bit}6 \wedge \text{bit}3 \wedge \text{bit}2 \wedge P2$$

$$P4 = \text{bit}7 \wedge \text{bit}6 \wedge \text{bit}5 \wedge \text{bit}4 \wedge P4$$

$$P8 = \text{bit}7 \wedge \text{bit}6 \wedge \text{bit}5 \wedge \text{bit}4 \wedge P4 \wedge \text{bit}3 \wedge \text{bit}2 \wedge \text{bit}1 \wedge \text{bit}0 \wedge P8$$

$$P1^* = \text{bit}8 \wedge \text{bit}6 \wedge \text{bit}4 \wedge \text{bit}2 \wedge P1^*$$

$$P2^* = \text{bit}5 \wedge \text{bit}4 \wedge \text{bit}1 \wedge \text{bit}0 \wedge P2^*$$

$$P4^* = \text{bit}3 \wedge \text{bit}2 \wedge \text{bit}1 \wedge \text{bit}0 \wedge P4^*$$

$$P8^* = \text{bit}7 \wedge \text{bit}6 \wedge \text{bit}5 \wedge \text{bit}4 \wedge P4 \wedge \text{bit}3 \wedge \text{bit}2 \wedge \text{bit}1 \wedge \text{bit}0 \wedge P8^*$$

Following table shows how the 24-bit ECC bits are arranged in three bytes. The first and second ECC byte contains row parity bits. The third ECC byte contains six column parity bits, plus two row parity bits.

ECC	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECC 0	P64	P64*	P32	P32*	P16	P16*	P8	P8*
ECC 1	P1024	P1024*	P512	P512*	P256	P256*	P128	P128*
ECC 2	P4	P4*	P2	P2*	P1	P1*	P2048	P2048*

The figure shows the hardware ECC detection flowchart.

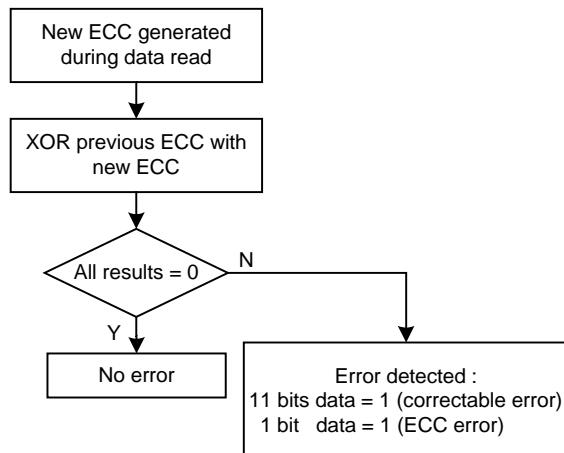


Fig. 3-17-3 hardware ECC detection flowchart

#### 3.17.2.4 Interfaces

#### 3.17.2.5 Major interfaces

The major interfaces of NAND flash controller are illustrated below.

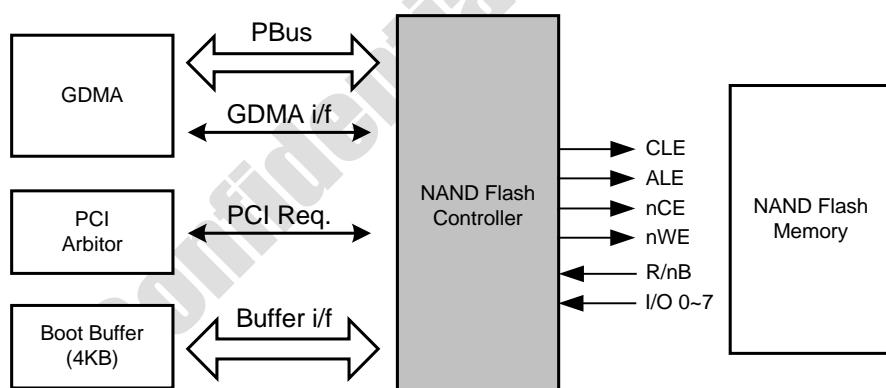


Fig. 3-17-4 Interfaces of NAND flash controller

#### 3.17.2.6 In/Out ports

The input/output ports of the NAND flash controller are listed in the table below.

Port Name	I/O	Width	Description
<b>Clock and Reset</b>			
clk	I	1	Operate clock
rst_n	I	1	Asynchronous reset (act low)
<b>Pbus interface</b>			
init_rd	I	1	Read request from initiator
init_wr	I	1	Write request from initiator
init_req	I	1	Access request from initiator

init_addr	I	32	Transaction address from initiator
init_bsel	I	4	Transaction length in byte
init_wdata	I	32	Write data from initiator
tg_rdy	I	1	Ready from target
tg_rdata	I	32	Read data from target
Buffer interface			
PCI arbiter interface			
GDMA interface			
DMA_NAND_REQ	O	1	DMA request
DMA_NAND_ACK	I	1	DMA acknowledge
DMA_NAND_FINISH	I	1	DMA finish
NAND flash interface			
CLE	O	1	Command latch enable
ALE	O	7	Address latch enable
nCE	O	7	Chip enable (active low)
nRE	O	1	Read enable (active low)
nWE	O	1	Write enable (active low)
R/nB	I	1	Ready / Busy (active low)
I/O	B	8	Data in/out

### 3.17.3 Register Description (base: 1000.0800)

CTRL (offset: 0x04, default: 0x00)

Bits	Type	Name	Description	Init Value
31:24			Reserved	
23:16	RW	TWAITB	Dummy time period to wait busy signal = clock * (TWAIT+1)	0
15:12	RW	THOLD	Hold time duration = clock * (THOLD+1)	0
11:8	RW	TPERIOD	Period time duration = clock * (TPERIOD+1)	0
7:4	RW	TSETUP	Setup time duration = clock * (TSETUP+1)	0
3:2	RW	BURST_SIZE	0: 1 DW 1: 2 DW 2: 4 DW 3: 8 DW	0
1	RW	DBUF_CLR	Clear data buffer	0
0	RW	WP	Write protect	0

TRANS\_CFG (offset: 0x00, default: 0x00)

Bits	Type	Name	Description	Init Value
31:30			Reserved	
29:20	RW	BNUM_DATA	Byte number of data to be transferred	528
19			Reserved	
18:16	RW	BNUM_ADDR	Byte number of address Note: maximum number is 4	3
15:14			Reserved	
13:12	RW	BNUM_CMD3	Byte number of command 3	0
11:10	RW	BNUM_CMD2	Byte number of command 2	0
9:8	RW	BNUM_CMD1	Byte number of command 1	1
7	RW	RESPB_DATA	Respect busy signal after data phase	0
6	RW	RESPB_ADDR	Respect busy signal after address phase	0
5	RW	RESPB_CMD3	Respect busy signal after command 3 phase	0

4	RW	RESPB_CMD2	Respect busy signal after command 2 phase	0
3	RW	ECC_ENA	ECC enable 0: disable 1: enable  Note: In read transfer, HW ECC check function will be active. In write transfer, HW ECC generate function will be active.	0
2	RW	DMA_ENA	Issue a request to generic DMA when data read/write. 0: CPU will get/put data from/to data buffer. 1: GDMA will get/put data from/to data buffer.	0
1	RW	WR_TRANS	The transfer is read / write. 0: read 1: write	0
0	WC	KICK_TRANS	Kick the a NAND flash transfer 0: no transfer 1: kick a transfer  Note: this bit will auto clear	0

CMD1 (offset: 0x04, default: 0x00)

Bits	Type	Name	Description	Init Value
31:24			Reserved	
23:16	RW	CMD1_BYTE3	3rd byte of command 1	0
15:8	RW	CMD1_BYTE2	2nd byte of command 1	0
7:0	RW	CMD1_BYTE1	1st byte of command 1	0

CMD2 (offset: 0x08, default: 0x00)

Bits	Type	Name	Description	Init Value
31:24			Reserved	
23:16	RW	CMD2_BYTE3	3rd byte of command 2	0
15:8	RW	CMD2_BYTE2	2nd byte of command 2	0
7:0	RW	CMD2_BYTE1	1st byte of command 2	0

CMD3 (offset: 0x0c, default: 0x00)

Bits	Type	Name	Description	Init Value
31:24			Reserved	
23:16	RW	CMD3_BYTE3	3rd byte of command 3	0
15:8	RW	CMD3_BYTE2	2nd byte of command 3	0
7:0	RW	CMD3_BYTE1	1st byte of command 3	0

ADDR (offset: 0x0c, default: 0x00)

Bits	Type	Name	Description	Init Value
31:24	RW	ADD_BYTE4	4th byte of address	
23:16	RW	ADD_BYTE3	3rd byte of address	0
15:8	RW	ADD_BYTE2	2nd byte of address	0
7:0	RW	ADD_BYTE1	1st byte of address	0

DATA (offset: 0x0c, default: 0x00)

Bits	Type	Name	Description	Init Value
31:0	RW	DATA	Data for read / write	0

ECC\_ENC (offset: 0x0c, default: 0x00)

Bits	Type	Name	Description	Init Value
31:24			Reserved	
23:16	R	ENC_BYTE2	3rd byte of ECC encode	0
15:8	R	ENC_BYTE1	2nd byte of ECC encode	0
7:0	R	ENC_BYTE0	1st byte of ECC encode	0

**STATUS (offset: 0x0c, default: 0x00)**

Bits	Type	Name	Description	Init Value
31:17			Reserved	
16:8	R	DEC_BYTE	ECC decode fail byte address	0
7			Reserved	
6:4	R	DEC_BIT	ECC decode fail bit address	0
3			Reserved	
2	R	ND_RB_N	NAND flash ready 0: busy 1: ready	1
1	R	DEC_ERR	ECC decode check status 0: no error 1: correctable error or ecc error	0
0	R	BUSY	NAND flash controller is in busy. 0: idle 1: busy	0

### 3.18 USB Host Controller & PHY

#### 3.18.1 Features

- Complies with the USB 2.0 Specification
- Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports ping and split transactions
- Descriptor and data prefetching.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- UTMI (legacy), UTMI+ to the PHY

#### 3.18.2 Block Diagram

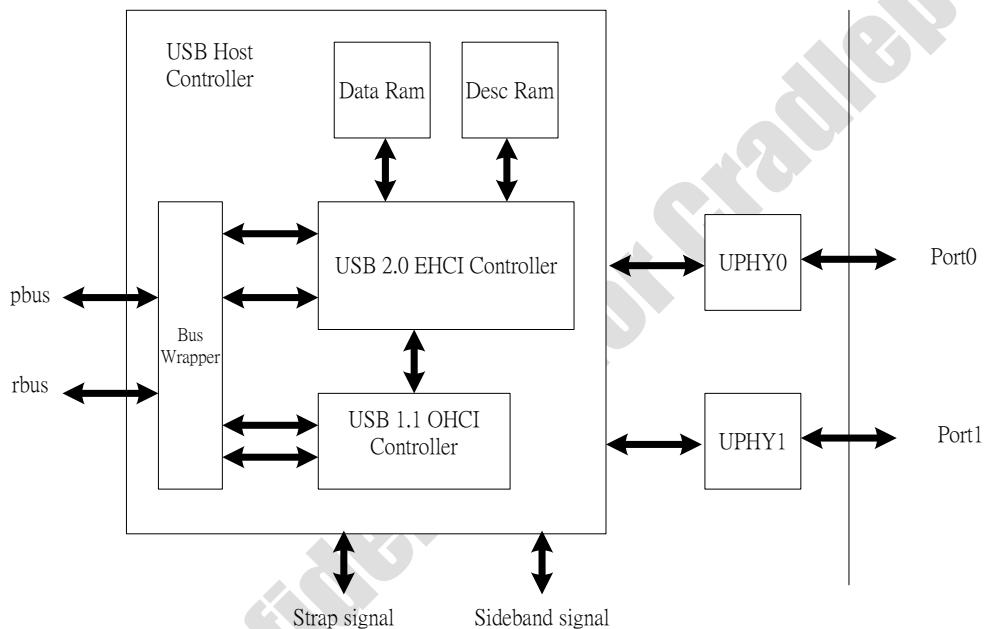


Fig. 3-18-1 USB Host Controller & PHY Block Diagram

### 3.18.3 Register Description (base: 0x101C.0000)

NOTE: To program EHCI and OHCI registers and initialize the core, refer to the Enhanced Host Controller Interface Specification for Universal Serial Bus and Open Host Controller Interface Specification for USB, respectively.

#### 3.18.3.1 EHCI Operation register (BASE: 0x101C.0000)

##### EHCI Capability Register

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address	Default Value
HCCAPBASE	Capability Register	USBBASE <sup>1</sup> + 00h	32'h01000010
HCSPARAMS	Structural Parameter	USBBASE + 04h	32'h00001116
HCCPARAMS	Capability Parameter	USBBASE + 08h	32'h0000A010 <b>Note:</b> The Isochronous Scheduling Threshold value is set to 1 by default. If Descriptor/Data Prefetch is selected, the value is set 2.

USBBASE is fixed to EHCI slave start address = 0x101C.0000

##### EHCI Operational Registers

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address <sup>1</sup>	Default Value
USBCMD	USB Command	USBOPBASE <sup>1</sup> + 00h	32'h00080000 or 32'h00080B00 <sup>2</sup>
USBSTS	USB Status	USBOPBASE + 04h	32'h00001000
USBINTR	USB Interrupt Enable	USBOPBASE + 08h	32'h00000000
FRINDEX	USB Frame Index	USBOPBASE + 0ch	32'h00000000
CTRLDSSSEGMENT	4G Segment Selector	USBOPBASE + 10h	32'h00000000
PERIODICLISTBASE	Periodic Frame List Base Address Register	USBOPBASE + 14h	32'h00000000
ASYNCLISTADDR	Asynchronous List Address	USBOPBASE + 18h	32'h00000000

1. USBOPBASE is fixed to the EHCI slave start address + 'h10 (offset = 'h10).

2. The default value depends on whether Async park capability is enabled. Disabled = 32'h0008\_0000 and enabled = 32'h0008\_0B00.

The default value is:

32'h0008\_0000 if Async park capability is disabled (through coreConsultant)

32'h0008\_0B00 if Async park capability is enabled.

##### EHCI Auxiliary Power Well Registers

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address	Default Value
CONFIGFLAG	Configured Flag Register	USBOPBASE + 40h	32'h00000000
PORSC_1 to PORSC_15	Port Status/Control	USBOPBASE + 44h	32'h00002000

### 3.18.3.2 OHCI Operation register (BASE: 0x101C.1000)

Offset		
0	HcRevision	0
4	HcControl	0
8	HcCommandStatus	
C	HcInterruptStatus	
10	HcInterruptEnable	
14	HcInterruptDisable	
18	HcHCCA	
1C	HcPeriodCurrentED	
20	HcControlHeadED	
24	HcControlCurrentED	
28	HcBulkHeadED	
2C	HcBulkCurrentED	
30	HcDoneHead	
34	HcFmInterval	
38	HcFmRemaining	
3C	HcFmNumber	
40	HcPeriodicStart	
44	HcLSThreshold	
48	HcRhDescriptorA	
4C	HcRhDescriptorB	
50	HcRhStatus	
54	HcRhPortStatus[1]	
...	...	
54+4*NDP	HcRhPortStatus[NDP]	

Ralink confidential

Draft

### 3.19 USB Device Controller

#### 3.19.1 Features

- the USB 2.0 Specification (Revision 1.0a), operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports up to 2 bulk-in and bulk out endpoints, including control endpoint 0
- Packet DMA (PDMA) is integrated for efficient data transfer.
- Support bulk-out aggregation features. More than one packet can be aggregated to single bulk transfer.
- Support two RX descriptor rings and two TX descriptor rings for QoS service.

##### 3.19.1.1 PDMA descriptor format

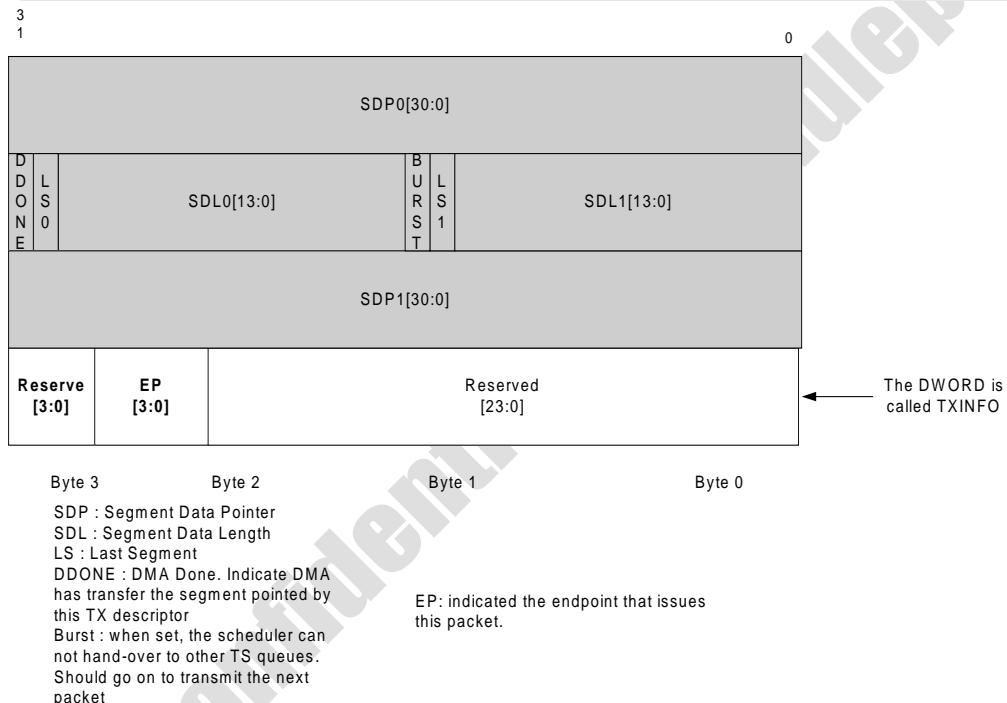
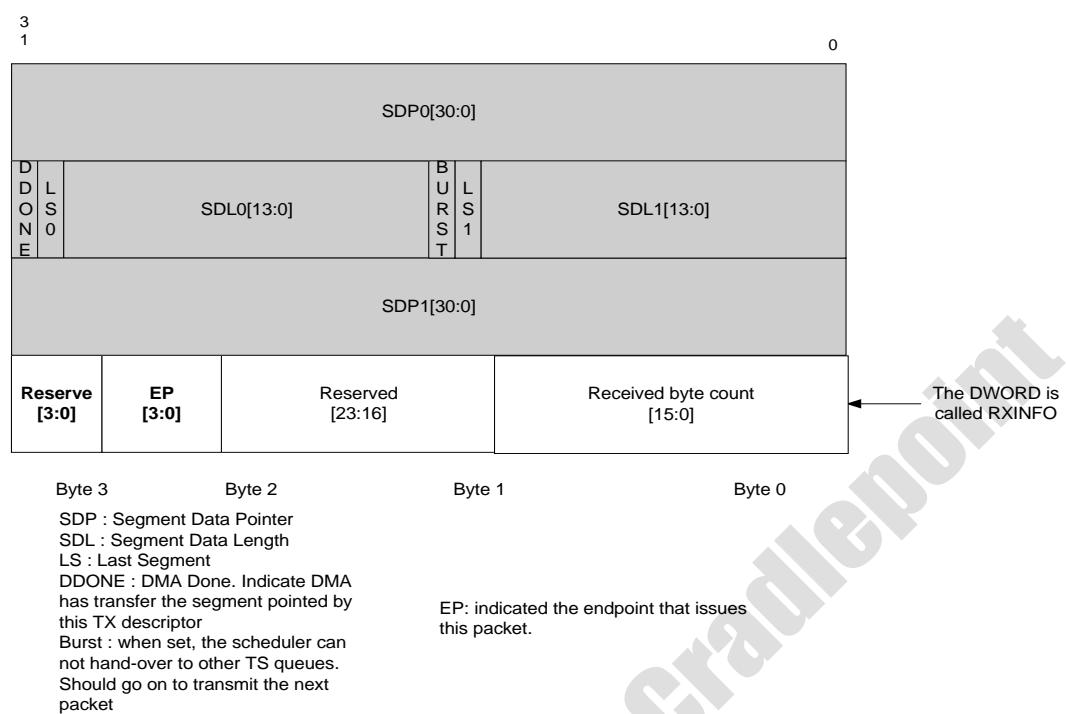


Fig. 3-19-1 PDMA TX descriptor format



### 3.19.2 Register Description (base: 0x1012.0000)

#### 3.19.2.1 USB control registers

Refer to *case\_cusb2\_spec.pdf*.

Registers address = Byte address \* 4.

#### 3.19.2.2 UDMA registers

UDMA\_CTRL (offset: 0x0800, default: 0x00000000)

Bits	Type	Name	Description	Init Value
31:26			Reserved	
25	R/W	EPOUT1_DMAEN	EPOUT1 UDMA enable.	0
24	R/W	EPOUT0_DMAEN	EPOUT0 UDMA enable.	0
23:18				
17	R/W	EPOUT1_AGGEN	EPOUT1 UDMA de-aggregation enable.	0
16	R/W	EPOUT0_AGGEN	EPOUT0 UDMA de-aggregation enable.	0
15:10	-	-	Reserved	-
9	R/W	EPOUT1_QSEL	EPOUT1 Rx ring mapping.	0
8	R/W	EPOUT0_QSEL	EPOUT0 Rx ring mapping.	0
7:5	-	-	Reserved	-
4	R/W	WAKEUP_EN	USB wakeup host enable.	0
3:2	-	-	Reserved	0
1	R/W	UDMA_RX_EN	UDMA Rx enable.	0
0	R/W	UDMA_TX_EN	UDMA Tx enable.	0

UDMA\_WRR (offset: 0x0804, default: 0x00000000)

Bits	Type	Name	Description	Init Value
31:30	-	-	RESERVED	-
29:28	R/W	SCH_MODE	Scheduling mode 00: WRR 01: strict priority, EP1 > EP2 > EP3 > EP4 > EP5 > EP6 10: mixed mode, EP1 > EP2 > WRR(EP3, EP4, EP5, EP6)	2'b00
27:23	-	-	Reserved	-
22:20	R/W	SCH_WT_EP6	Scheduling weight of EPOUT6	0
19	-	-	Reserved	-
18:16	R/W	SCH_WT_EP5	Scheduling weight of EPOUT5	0
15	-	-	Reserved	-
14:12	R/W	SCH_WT_EP4	Scheduling weight of EPOUT4	0
11	-	-	Reserved	-
10:8	R/W	SCH_WT_EP3	Scheduling weight of EPOUT3	0
7	-	-	Reserved	-
6:4	R/W	SCH_WT_EP2	Scheduling weight of EPOUT2	0
3	-	-	Reserved	-
2:0	R/W	SCH_WT_EP1	Scheduling weight of EPOUT1	0

#### 3.19.2.3 PDMA registers

TX\_BASE\_PTR0 (offset: 0x1000, default: 0x00000000)

Bits	Type	Name	Description	Init Value
31:16	-	-	Reserved	-
15:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	0

TX\_MAX\_CNT0 (offset: 0x1004, default: 0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	0

**TX\_CTX\_IDX0** (offset:0x1008,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	TX_CTX_IDX0	Point to the next TXD CPU wants to use	0

**TX\_DTX\_IDX0** (offset:0x100C,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	Reserved	-0
7:0	RO	TX_DTX_IDX0	Point to the next TXD DMA wants to use	0

**TX\_BASE\_PTR1** (offset:0x1010,default:0x00000000)

**TX\_MAX\_CNT1** (offset:0x1014,default:0x00000000)

**TX\_CTX\_IDX1** (offset:0x1018,default:0x00000000)

**TX\_DTX\_IDX1** (offset:0x101C,default:0x00000000)

**RX\_BASE\_PTR0** (offset:0x1100,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:16	-	-	Reserved	-
15:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address	0

**RX\_MAX\_CNT0** (offset:0x1104,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

**RX\_CALC\_IDX0** (offset:0x1108,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

**FS\_DRX\_IDX0** (offset:0x110C,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	R/W	RX_DRX_IDX0	Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address.	0

**RX\_BASE\_PTR1** (offset:0x1110,default:0x00000000)

**RX\_MAX\_CNT1** (offset:0x1114,default:0x00000000)

**RX\_CALC\_IDX1** (offset:0x1118,default:0x00000000)

**RX\_DRX\_IDX1** (offset:0x111C,default:0x00000000)

**PDMA\_INFO** (offset:0x1200,default:0x1008020E)

Bits	Type	Name	Description	Init Value
31:28	RO	VERSION	PDMA controller version.	0x1
27:24	RO	INDEX_WIDTH	Ring index width	0xC
23:16	RO	BASE_PTR_WIDTH	Base pointer width, x Base_addr[31:32-x] is shared with all ring base addr. Only ring0's base address [31:32-x] field is writable.	0x10
15:8	RO	RX_RING_NUM	Rx ring number	0x2
7:0	RO	TX_RING_NUM	Tx ring number	0x2

**PDMA\_GLO\_CFG (offset:0x1204,default:0x00000050)**

Bits	Type	Name	Description	Init Value
31:29			Reserved	
28:16		HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	8'b0
15:8	-	-	Reserved	-
7	R/W	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.	0
6	R/W	TX_WB_DDONE	0:Disable TX_DMA writing back DDONE into TXD 1: Enable TX_DMA writing back DDONE into TXD	1'b1
5	-	-	Reserved	-
4	R/W	WPDMA_BT_SIZE	Define the burst size of WPDMA 0: 4 DWORD (16bytes) 1: 8 DWORD (32 bytes)	1'b1
3	RO	RX_DMA_BUSY	1: RX_DMA is busy 0: RX_DMA is not busy	0
2	R/W	RX_DMA_EN	1: Enable RX_DMA 0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	0
1	RO	TX_DMA_BUSY	1: TX_DMA is busy 0: TX_DMA is not busy	0
0	R/W	TX_DMA_EN	1: Enable TX_DMA 0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	0

**PDMA\_RST\_IDX (offset:0x1208,default:0x00000000)**

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	W1C	RST_DRX_IDX1	Write 1 to reset to RX_DMARX_IDX1 to 0	1'b0
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DMARX_IDX0 to 0	1'b0
15:2	-	-	Reserved	-
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DMATX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DMATX_IDX0 to 0	1'b0

**DELAY\_INT\_CFG (offset:0x120C,default:0x00000000)**

Bits	Type	Name	Description	Init Value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (See below), an Final TX_DLY_INT is generated.  Set to 0 will disable pending interrupt count check	7'b0
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INTO-5. When the pending time equal or greater TXMAX_PTIME x 20us or the # of pended TX_DONE_INTO-5 equal or greater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated  Set to 0 will disable pending interrupt time check	8'b0

15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or greater than the value specified here or interrupt pending time reach the limit (See below), an Final RX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or greater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or greater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0

INT\_STATUS (offset: 0x1220, default: 0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
30	R/W	RX_DLY_INT	Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
29	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
28	R/W	TX_DLY_INT	Summary of the whole WPDMA TX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
27:18	-	-	Reserved	-
17	R/W	RX_DONE_INT1	RX Queue#1 packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
16	R/W	RX_DONE_INTO	RX Queue#0 packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
15:2	-	-	Reserved	-
1	R/W	TX_DONE_INT1	TX Queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
0	R/W	TX_DONE_INTO	TX Queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0

INT\_MASK (offset: 0x1228, default: 0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	RX_COHERENT_INT_MSK	Interrupt enable for RX_DMA data coherent event.. 1: Enable the interrupt 0: Disable the interrupt	0
30	R/W	RX_DLY_INT_MSK	Summary of the whole WPDMA RX related interrupts 1: Enable the interrupt 0: Disable the interrupt	0
29	R/W	TX_COHERENT_INT_MSK	Interrupt enable for TX_DMA data coherent event.. 1: Enable the interrupt	0

			0: Disable the interrupt	
28	R/W	TX_DLY_INT_MSK	Summary of the whole WPDMA TX related interrupts 1: Enable the interrupt 0: Disable the interrupt	0
27:18	-	-	Reserved	-
17	R/W	RX_DONE_INT_MSK1	RX Queue#1 packet receive interrupt 1: Enable the interrupt 0: Disable the interrupt	0
16	R/W	RX_DONE_INT_MSK0	RX Queue#0 packet receive interrupt 1: Enable the interrupt 0: Disable the interrupt	0
15:2	-	-	Reserved	-
1	R/W	TX_DONE_INT_MSK1	TX Queue#1 packet transmit interrupt 1: Enable the interrupt 0: Disable the interrupt	0
0	R/W	TX_DONE_INT_MSK0	TX Queue#0 packet transmit interrupt 1: Enable the interrupt 0: Disable the interrupt	0

PDMA\_WRR (offset: 0x1280, default:0x00000000)

Bits	Type	Name	Description	Init Value
31:30	-	-	RESERVED	-
29:28	R/W	SCH_MODE	SCHEDULING MODE 00: WRR 01: strict priority, Q0 > Q1 > Q2 > Q3 10: mixed mode, Q0 > Q1 > WRR(Q2, Q3)	2'b00
27:15	-	-	RESERVED	-
14:12	R/W	SCH_WT_Q3	SCHEDULING WEIGHT OF TX Q3	0
11	-	-	RESERVED	-
10:8	R/W	SCH_WT_Q2	SCHEDULING WEIGHT OF TX Q2	0
7	-	-	RESERVED	-
6:4	R/W	SCH_WT_Q1	SCHEDULING WEIGHT OF TX Q1	0
3	-	-	RESERVED	-
2:0	R/W	SCH_WT_Q0	SCHEDULING WEIGHT OF TX Q0	0

## 3.20 Frame Engine

### 3.20.1 Features

- Wire-speed (1000Mbps) Ethernet LAN/WAN NAT/NAPT routing
- L1-L7(content aware) policy table
- Stateful packet inspection firewall
- QoS support for multimedia traffic
- Support per flow/rule accounting/rate limiting
- Checksum/VLAN/PPPoE offload

#### 3.20.1.1 Network Interface

- One 10/100/1000Mbps Ethernet MACs with RGMII/MII interfaces
- One Scatter-Gather packet DMA with Rbus master interface  

(Note: Although there are two gigabit Ethernet ports, only one packet DMA is existed. From software point of view, only one software driver instance is used. The software driver could assign the TX packet destination by assign the PN filed in the TX descriptor)
- One special port for packet processing engine

#### 3.20.1.2 PSE (Packet Switch Engine) Features

- 
- Four external ports and one special PPE port (for packet bridging/routing)
- Efficient page-based buffer management (256 pages, each page is 128 bytes)
- QoS-aware queue management
- Supports 4 output queues per gigabit Ethernet port
- WRR/Strict priority scheduling
- Egress rate limiting/shaping
- Non-blocking, wire-speed packet switching
- Supports Jumbo frames up-to 12KB
- Flow control for no-packet-loss guarantee
- Emulated multicast support (can mirror a TX packet to CPU)
- Checksum offload, VLAN & PPPOE header insertion (by CDMA)
- Auto-Padding for sub-64B packets

#### 3.20.1.3 PPE Features

- Supports 512 policy rules for ACL, accounting and rate limiting
- The policy rules can base on pre-route/post-route L1-L7 headers & contents (up-to 16 bytes)
- DDoS avoidance by rate limiting
- Supports stateful packet filtering (SPI)
- Supports IPv4 NAT/NAPT and IPv6 NAT routing
- Supports 1/2/4/8/16K IPv4 NAPT flows
- Supports virtual server, port-triggering & port forwarding
- Supports any kind of IPv4 NAT(NAPT, Twice NAT)
- Supports 16 PPPoE sessions
- Supports cone-NAT, port-restricted NAT & Symmetric NAT
- Supports per rule or per flow accounting or rate limiting

- Patent-pending Flow Offloading technology for flexible/high performance packet L3/L4 packet processing
- Supports double VLAN tagging (Q-in-Q)
- Support VID Swapping
- Support multi-WAN load balancing with H/W S/W cooperation
- PS: All the PPE features mentioned above require software porting to enable

#### 3.20.1.4 QoS Related Features

- Packets can be classified based on L1-L7 headers/content
- Supports 4 TX queues
- Supports WRR scheduling for GE ports
- Supports egress rate limiting for each network port
- Powerful buffer reservation scheme to reserve packet buffer resources for multi-media traffic

#### 3.20.1.5 Packet DMA (PDMA) Features

- Supports 2 TX descriptor rings and one RX descriptor ring
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8/16 32-bit word burst length

### 3.20.2 Block Diagram

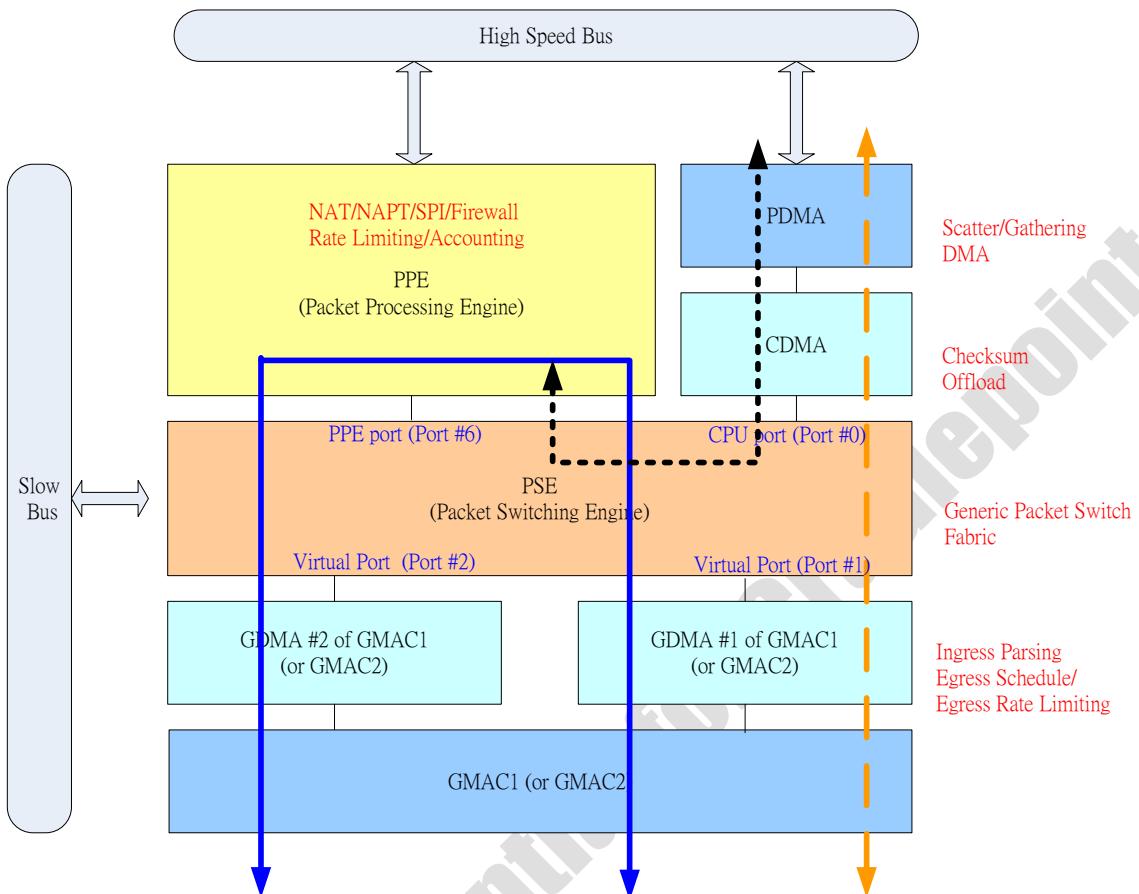
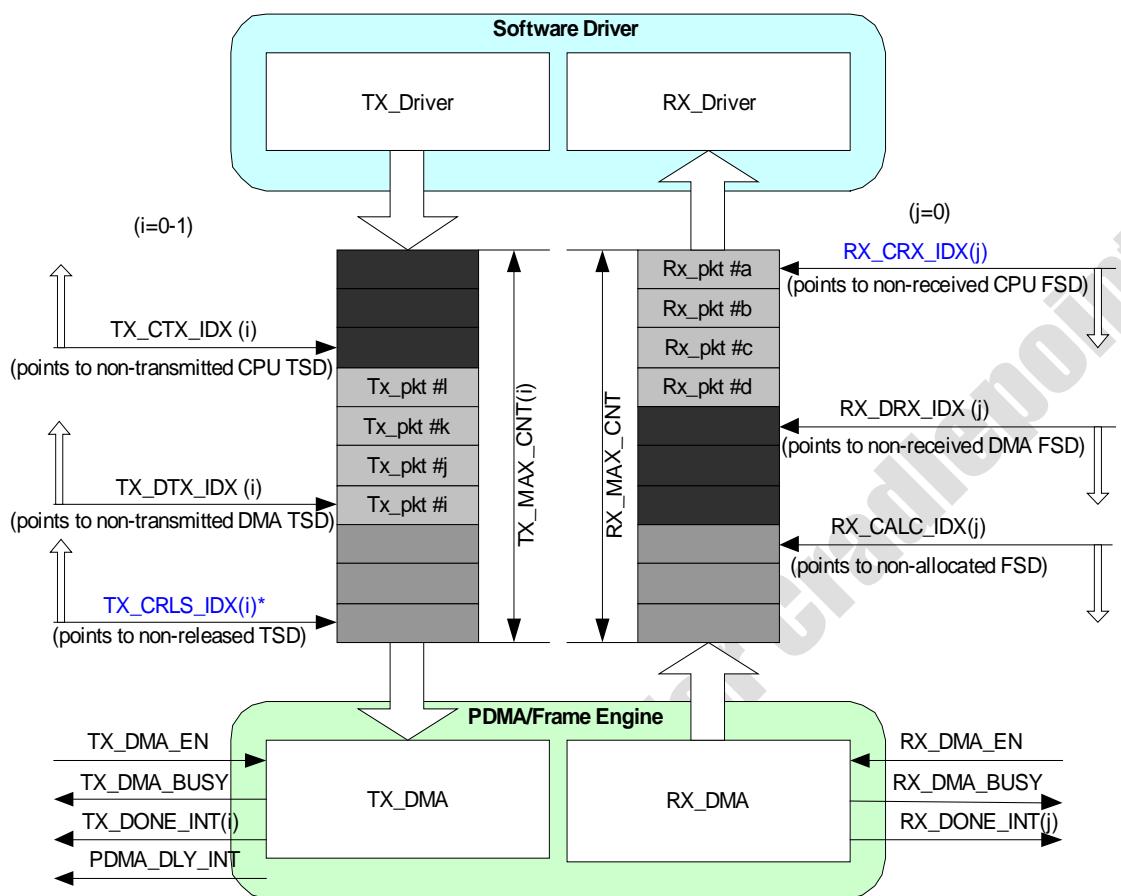


Fig. 3-20-1 Frame Engine block diagram

### 3.20.2.1 PDMA FIFO-like Ring Concept



Note 1 : TX\_CRLS\_IDX(i) and RX\_CRX\_IDX (j) are not in  
PDMA hardware, they are resident in CPU local memory

Note 2:

TXQ0 : GE MAC low priority queue  
TXQ1 : GE MAC high priority queue

RXQ0 : For GE MAC receive

Fig. 3-20-2 PDMA FIFO-like ring concept

### 3.20.2.2 PDMA Descriptor Format

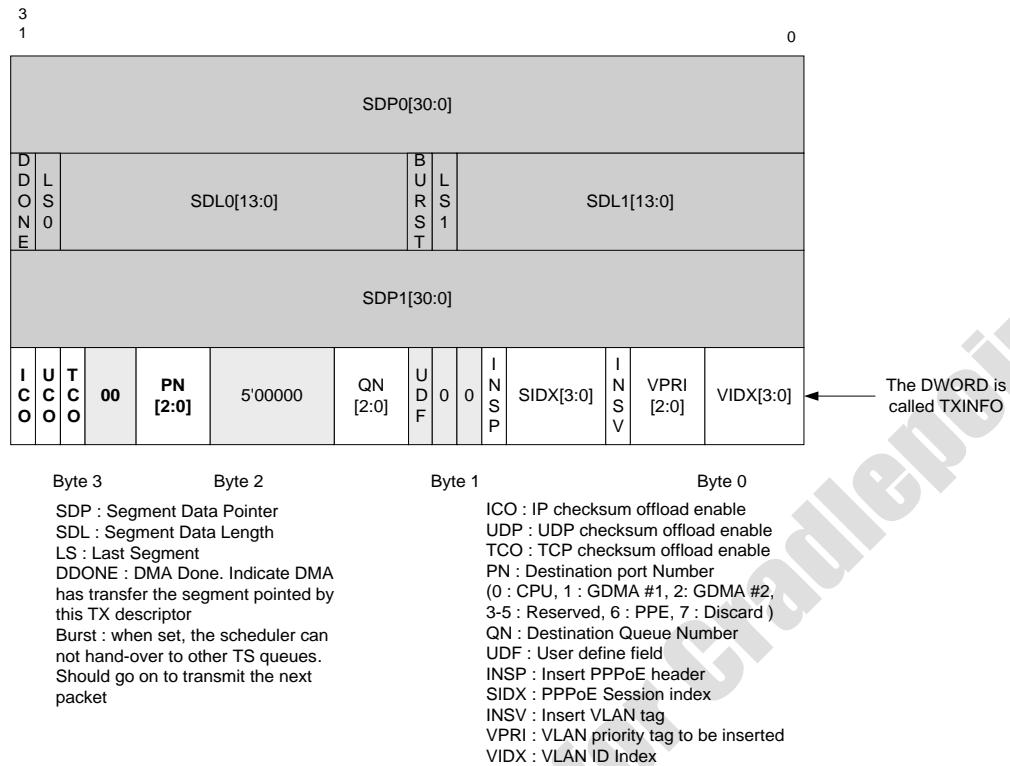


Fig. 3-20-3 PDMA TX descriptor format

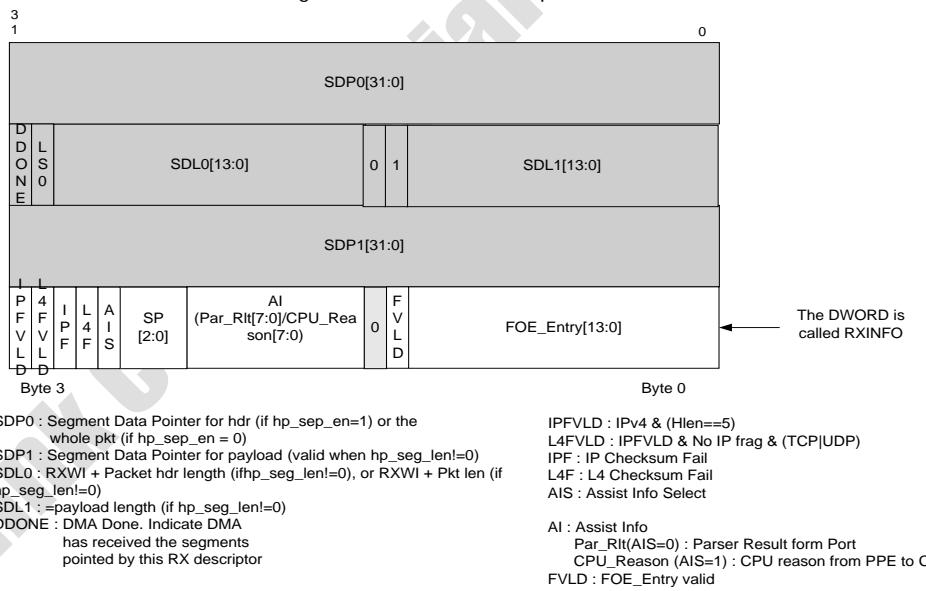


Fig. 3-20-4 PDMA RX descriptor format

### 3.20.3 Register Description (base: 0x1010.0000)

MDIO\_ACCESS : MDIO Access (offset: 0x00)

Bits	Type	Name	Description	Initial value
31	WSC	MD_CMD_TRG	MDIO command trigger. This bit is cleared by hardware after command is completed. 1: Read/write operation ongoing 0: Read/write operation complete	1'b0
30	WO	MD_WR	When set, this bit tells the PHY that this will be a Write operation using MD_DATA register. If this bit is not set, this will be a Read operation, placing the data in MD_DATA register. 1: Write operation. 0: Read operation.	1'b0
29	-	-	Reserved	1'b0
28:24	R/W	MD_PHY_ADDR	Address of PHY device	5'b0
23:21	-	-	Reserved	3'b0
20:16	R/W	MD_REG_ADDR	Register addresses within PHY device	5'b0
15:0	R/W	MD_DATA	PHY register read/write data	16'b0

MDIO\_CFG1 : MDIO Configuration for GE port#1 (offset: 0x04)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	2'b0
29	R/W	GE1_AUTO_POLL_EN	0: Disable GE1 MDC/MDIO auto polling 1: Enable GE1 MDC/MDIO auto polling	1'b1
28:24	R/W	MD_PHY1ADDR	Address of PHY device #1. This register is used for PHY auto-polling function.	5'h01
23:17	-	-	Reserved	1'b0
16	T/W	GE1_BP_EN	Set to one to enable backpressure in half-duplex mode. Set to 0 disable backpressure function in half-duplex mode	1'b1
15	R/W	GE1_FRC_EN	GMAC1 force link status enable. When set, hardware will force GMAC link status according to bit[14:9]. When reset, bit[14:9] will be ignored, and hardware will auto-polling PHY link status and set it to GMAC1.	1'b0
14:13	R/W	GE1_SPEED	Force GE1 speed. When bit[15] is reset, this register will reflect current link status. 00: 10 M 01: 100M 10: 1000M 11: reserved	2'b00
12	R/W	GE1_DUPLEX	Force GE1 duplex mode. When bit[15] is 0, this register will reflect current link status. 1: full duplex 0: half duplex	1'b0
11	R/W	GE1_FC_TX	Force GE1 transmitting flow control ability. When bit[15] is 0, this register will reflect current link status. 1: enable transmitting flow control ability 0: disable transmitting flow control ability	1'b1
10	R/W	GE1_FC_RX	Force GE1 receiving flow control ability. When bit[15] is 0, this register will reflect current link status. 1: enable receiving flow control ability 0: disable receiving flow control ability	1'b0
9	R/W	GE1_LNK_DWN	Force GE1 link down. When bit[15] is 0, this register will reflect current link status. 1: link down. 0: link up.	1'b1
8	RO	GE1_AN_DONE	Auto-negotiation done. When bit[15] is set, this register will	1'b0

			always be zero.	
7:6	R/W	MDC_CLK_DIV	00: 4 MHz 01: 2MHz 10: 1Mhz 11: 512Khz	2'b01
5	R/W	GE1_TBO_MII_FREQ	0: MII clock speed for TURBO_MII Mode is 31.25Mhz 1: MII clock speed for TURBO_MII Mode is 50 MHz	1'b0
4	R/W	GE1_TBO_MII_MODE	0: disable TURBO_MII_MODE 1: Generate a 50Mhz TX_CLK when MAC speed is 100Mbps	1'b0
3:2	R/W	GE1_RX_CLK_SKEW	0: zero delay 1: delay 200ps 2: delay 400ps 3: clock inversion	2'b01
1	-	-	reserved	1'b0
0	R/W	GE1_TX_CLK_MODE	0: HP Mode (clk and data are in-phase) 1: 3COM mode (clk and data are 90 degree diff.)	1'b1

**FE\_GLO\_CFG** : Frame Engine Global Configuration (offset: 0x08)

Bits	Type	Name	Description	Initial value
31:16	R/W	EXT_VLAN	Extended VLAN type	16'h8100
15:8	R/W	US_CYC_CNT	1us timer count in unit of clock cycle. For example, if frame engine is running at 133MHz, set this register to 8'd132.	8'd132
7:4	R/W	L2_SPACE	L2 space. Unit is 8 bytes	4'h8
3:0	-	-	Reserved	1'b0

**FE\_RST\_GLO** : Frame Engine Global Reset (offset: 0x0C)

Bits	Type	Name	Description	Initial value
31:16	RC	FC_DROP_CNT	Flow control drop packet count.	16'b0
15:1	-	-	Reserved	15'b0
0	WO	PSE_RESET	PSE reset Write 1 to reset PSE Write 0 to disable reset PSE	1'b0

**FE\_INT\_STATUS** : Frame Engine Interrupt Status (offset: 0x10)

Bits	Type	Name	Description	Initial value
31	R/W	CNT_PPE_AF	PPE Counter Table Almost Full Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
30	-	-	Reserved	1'b0
29	R/W	CNT_GDM1_AF	GDMA1 Counter Table Almost Full Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
28:26	-	-	Reserved	3'b000
25	R/W	GE1_CRC_DROP	GE1 discards a packet due to CRC error Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
24	R/W	PSE_BUF_DROP	PSE discards a packet due to buffer sharing limitation (flow control) Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
23	R/W	GE1_OTHER_DROP	GE1 discards a packet due to other reason (e.g. too short, too long, FIFO overflow, checksum error,.., etc.) Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
22	R/W	PSE_P1_FC	PSE port1 (GDMA1) flow control asserted. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0

21	R/W	PSE_P0_FC	PSE port0 (CDMA) flow control asserted. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
20	R/W	PSE_FQ_EMPTY	PSE free Q empty threshold reached & forced drop condition occurred. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
19	-	-	Reserved	1'b0
18	R/W	GE1_STA_CHG	GE port #1 link status changes (link, speed, flow control) Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
15:12	-	-	Reserved	4'b0
11	R/W	TX_DONE_INT3	Tx queue#3 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
10	R/W	TX_DONE_INT2	Tx queue#2 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
9	R/W	TX_DONE_INT1	Tx queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
8	R/W	TX_DONE_INT0	Tx queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
7:3	-	-	Reserved	5'b0
2	R/W	RX_DONE_INT0	Packet receive interrupt. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
1	R/W	TX_DLY_INT	Delayed version of TX_DONE_INT0 and TX_DONE_INT1. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
0	R/W	RX_DLY_INT	Delayed version of RX_DONE_INT0. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0

**FE\_INT\_ENABLE : Frame Engine Interrupt Enable (offset: 0x14)**

Bits	Type	Name	Description	Initial value
31	R/W	CNT_PPE_AF	PPE Counter Table Almost Full 1: Enable the interrupt 0: Disable the interrupt	1'b0
30	-	-	Reserved	1'b0
29	R/W	CNT_GDM1_AF	GDMA1 Counter Table Almost Full Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
28:26	-	-	Reserved	3'b0
25	R/W	GE1_CRC_DROP	GE1discards a packet due to CRC error 1: Enable the interrupt 0: Disable the interrupt	1'b0
24	R/W	PSE_BUF_DROP	PSE discards a packet due to buffer sharing limitation (flow	1'b0

			control) 1: Enable the interrupt 0: Disable the interrupt	
23	R/W	GE1_OTHER_DROP	GE1 discards a packet due to other reason (e.g. too short, too long, FIFO overflow, checksum error,.., etc.) 1: Enable the interrupt 0: Disable the interrupt	1'b0
22	R/W	PSE_P1_FC	PSE port1 (GDMA1) flow control asserted. 1: Enable the interrupt 0: Disable the interrupt	1'b0
21	R/W	PSE_P0_FC	PSE port0 (CDMA) flow control asserted. 1: Enable the interrupt 0: Disable the interrupt	1'b0
20	R/W	PSE_FQ_EMPTY	PSE free Q empty threshold reached & forced drop condition occurred. 1: Enable the interrupt 0: Disable the interrupt	1'b0
19	-	-	Reserved	1'b0
18	R/W	GE1_STA_CHG	GE port #1 link status changes (link, speed, flow control) 1: Enable the interrupt 0: Disable the interrupt	1'b0
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. 1: Enable the interrupt 0: Disable the interrupt	1'b0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. 1: Enable the interrupt 0: Disable the interrupt	1'b0
15:12	-	-	Reserved	4'b0
11	R/W	TX_DONE_INT3	Tx queue#3 packet transmit interrupt 1: Enable the interrupt 0: Disable the interrupt	1'b0
10	R/W	TX_DONE_INT2	Tx queue#2 packet transmit interrupt 1: Enable the interrupt 0: Disable the interrupt	1'b0
9	R/W	TX_DONE_INT1	Tx queue#1 packet transmit interrupt 1: Enable the interrupt 0: Disable the interrupt	1'b0
8	R/W	TX_DONE_INT0	Tx queue#0 packet transmit interrupt 1: Enable the interrupt 0: Disable the interrupt	1'b0
7:3	-	-	Reserved	5'b0
2	R/W	RX_DONE_INT0	Packet receive interrupt. 1: Enable the interrupt 0: Disable the interrupt	1'b0
1	R/W	TX_DLY_INT	Delayed version of TX_DONE_INT0 and 1: Enable the interrupt 0: Disable the interrupt	1'b0
0	R/W	RX_DLY_INT	Delayed version of RX_DONE_INT0. 1: Enable the interrupt 0: Disable the interrupt	1'b0

FOE\_TS\_T : Time Stamp (offset: 0x1C)

Bits	Type	Name	Description	Initial value
31:24	R	PSE_FQ_PCNT	PSE free Q page count	8'hff
23:16	-		Reserved	8'b0

15:0	R/W	FOE_TS_T	Time stamp Note: Time Stamp unit is 1 sec.	16'b0
------	-----	----------	---	-------

### 3.20.3.1 Register Description – GDMA1

GDMA1\_FWD\_CFG : GDMA1 Forwarding Configuration (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:28	-	GDM1_JMB_LEN	When GDM1_JMB_EN=1, this parameter define the maximum packet length(including CRC) that GDMA1 could receive in 1024-byte unit. The valid value is from 0 ~12.	4'd12
27:26			Reserved	0
25	R/W	GDM1_20US_TICK_LT	0: GDM1 shaper add token every 1ms. 1: GDM1 shaper add token every 20us. Please refer to GDM1_TK_RATE in GDMA1_SHPR_CFG register.	1'b0
24	R/W	GDM1_TCI_81xx	0: Check VLAN tag with EXT_VLAN[15:0] 1: Check VLAN tag with EXT_VLAN[15:8] only	1'b0
23	R/W	GDM1_DROP_256B	A Special mode to drop packets with payload > 256 bytes. 0: Drop packets according to standard Ethernet frame length limitation. 1: Drop packets with payload >256 bytes	1'b0
22	R/W	GDM1_ICS_EN	IPv4 header checksum check enable	1'b1
21	R/W	GDM1_TCS_EN	TCP checksum check enable	1'b1
20	R/W	GDM1_UCS_EN	UDP checksum check enable	1'b1
19	R/W	GDM1_JMB_EN	0: Drop received frames if length is great than 1518 (1522 for VLAN frames, and 1526 for double VLAN frames) 1: Allow receiving jumbo frames length up to 12kB.	1'b0
18	R/W	GDM1_DISPAD	0: Enable GMAC1 Tx padding function. 1: Disable GMAC1 Tx padding function.	1'b0
17	R/W	GDM1_DISCRC	0: Enable GMAC1 Tx CRC generation. 1: Disable GMAC1 Tx CRC generation.	1'b0
16	R/W	GDM1_STRPCRC	0: Disable GDMA1 automatic Rx CRC stripping 1: Enable GDMA1 automatic Rx CRC stripping	1'b1
15	-	-	Reserved	1'b0
14:12	R/W	GDM1_UFRC_P	GDMA1 My MAC unicast frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111
11	-	-	Reserved	1'b0
10:8	R/W	GDM1_BFRC_P	GDMA1 broad-cast MAC address frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111
7	-	-	Reserved	1'b0
6:4	R/W	GDM1_MFRC_P	GDMA1 multi-cast MAC address frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2	3'b111

			3'd6: PPE 3'd7: Discard Others: Reserved	
3	-	-	Reserved	1'b0
2:0	R/W	GDM1_OFRC_P	GDMA1 other MAC address frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111

**GDMA1\_SCH\_CFG : GDMA1 Scheduling Configuration (offset: 0x24)**

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	7'b0
25:24	R/W	GDM1_SCH_MOD	2'b00: WRR 2'b01: Strict Priority, Q3>Q2>Q1>Q0 2'b10: Mixed, Q3>WRR(Q2,Q1,Q0) 2'b11: Reserved	2'b00
23:15	-	-	Reserved	1'b0
14:12	R/W	GDM1_WT_Q3	Q3's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b011
11	-	-	Reserved	1'b0
10:8	R/W	GDM1_WT_Q2	Q2's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b010
7	-	-	Reserved	1'b0
6:4	R/W	GDM1_WT_Q1	Q1's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b001
3	-	-	Reserved	1'b0
2:0	R/W	GDM1_WT_Q0	Q0's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b0

**GDMA1\_SHPR\_CFG : GDMA1 Output Shaper Configuration (offset: 0x28)**

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	7'b0
24	R/W	GDM1_SHPR_EN	GDMA1 output shaper enable. 0: Disable 1: Enable	1'b0
23:16	R/W	GDM1_BK_SIZE	GDMA1 output shaper maximum bucket size. Unit is 1kB.	8'b0
15:14	-	-	Reserved	2'b0

13:0	R/W	GDM1_TK_RATE	GDMA1 output shaper token rate. Unit is 8B/ms or 8B/20us. According To GDM1_20US_TICK_SLT	14'b0
------	-----	--------------	--	-------

GDMA1\_MAC\_ADRL : GDMA1 MAC Address LSB (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:0	R/W	GDM1_MY_MAC_L	GMAC1 MAC address bit 31-0	32'b0

GDMA1\_MAC\_ADRH : GDMA1 MAC Address MSB (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	GDM1_MY_MAC_H	GMAC1 MAC address bit 47-32	16'b0

### 3.20.3.2 Register Description - PSE

PSE\_FQ\_CFG (offset:0x40)

Bits	Type	Name	Description	Initial value
31:24	R/W	FQ_MAX_PCNT	Maximum free Q page count. Please reset PSE after re-programming this register.	8'hFF
23:16	R/W	FQ_FC_RLS	Free Q flow control release threshold.	8'h6C
15:8	R/W	FQ_FC_ASRT	Free Q flow control assertion threshold.	8'h4C
7:0	R/W	FQ_FC_DROP	Free Q empty threshold. If one input port is FC asserted and this threshold is reached, PSE will drop any new coming frame from this port.	8'h10

CDMA\_FC\_CFG (offset:0x44)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	3'b0
28	R/W	P0_SHARING	Allows high priority Q to share low priority Q's reserved pages. 1: enable 0: disable	1'b1
27:24	R/W	P0_HQ_DEF	Bit map definition of high priority Q. '1' presents high priority Q, and '0' presents low priority Q. bit 27: Q3 priority definition bit 26: Q2 priority definition bit 25: Q1 priority definition bit 24: Q0 priority definition	4'b1100
23:16	R/W	P0_HQ_RESV	Reserved page count for high priority Q.	8'h08
15:8	R/W	P0_LQ_RESV	Reserved page count for low priority Q.	8'h08
7:0	R/W	P0_IQ_ASRT	Virtual input Q FC assertion threshold.	8'h08

GDMA1\_FC\_CFG (offset:0x48)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	3'b0
28	R/W	P1_SHARING	Allows high priority Q to share low priority Q's reserved pages. 1: enable 0: disable	1'b1
27:24	R/W	P1_HQ_DEF	Bit map definition of high priority Q. '1' presents high priority Q, and '0' presents low priority Q. bit 27: Q3 priority definition bit 26: Q2 priority definition bit 25: Q1 priority definition bit 24: Q0 priority definition	4'b1100
23:16	R/W	P1_HQ_RESV	Reserved page count for high priority Q.	8'h08
15:8	R/W	P1_LQ_RESV	Reserved page count for low priority Q.	8'h08
7:0	R/W	P1_IQ_ASRT	Virtual input Q FC assertion threshold.	8'h08

**GDMA2\_FC\_CFG (offset:0x4C)**

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	3'b0
28	R/W	P2_SHARING	Allows high priority Q to share low priority Q's reserved pages. 1: enable 0: disable	1'b1
27:24	R/W	P2_HQ_DEF	Bit map definition of high priority Q. '1' presents high priority Q, and '0' presents low priority Q. bit 27: Q3 priority definition bit 26: Q2 priority definition bit 25: Q1 priority definition bit 24: Q0 priority definition	4'b1100
23:16	R/W	P2_HQ_RESV	Reserved page count for high priority Q.	8'h08
15:8	R/W	P2_LQ_RESV	Reserved page count for low priority Q.	8'h08
7:0	R/W	P2_IQ_ASRT	Virtual input Q FC assertion threshold.	8'h08

**CDMA\_OQ\_STA (offset:0x50)**

Bits	Type	Name	Description	Initial value
31:24	RO	P0_OQ3_PCNT	CDMA output Q3 page count.	8'b0
23:16	RO	P0_OQ2_PCNT	CDMA output Q2 page count.	8'b0
15:8	RO	P0_OQ1_PCNT	CDMA output Q1 page count.	8'b0
7:0	RO	P0_OQ0_PCNT	CDMA output Q0 page count.	8'b0

**GDMA1\_OQ\_STA (offset:0x54)**

Bits	Type	Name	Description	Initial value
31:24	RO	P1_OQ3_PCNT	GDMA1 output Q3 page count.	8'b0
23:16	RO	P1_OQ2_PCNT	GDMA1 output Q2 page count.	8'b0
15:8	RO	P1_OQ1_PCNT	GDMA1 output Q1 page count.	8'b0
7:0	RO	P1_OQ0_PCNT	GDMA1 output Q0 page count.	8'b0

**GDMA2\_OQ\_STA (offset:0x58)**

Bits	Type	Name	Description	Initial value
31:24	RO	P2_OQ3_PCNT	GDMA2 output Q3 page count.	8'b0
23:16	RO	P2_OQ2_PCNT	GDMA2 output Q2 page count.	8'b0
15:8	RO	P2_OQ1_PCNT	GDMA2 output Q1 page count.	8'b0
7:0	RO	P2_OQ0_PCNT	GDMA2 output Q0 page count.	8'b0

**PSE\_IQ\_STA (offset:0x5C)**

Bits	Type	Name	Description	Initial value
31:24	RO	P6_OQ0_PCNT	PPE output Q0 page count.	8'b0
23:16	RO	P2_IQ_PCNT	GDMA2 virtual input Q page count.	8'b0
15:8	RO	P1_IQ_PCNT	GDMA1 virtual input Q page count.	8'b0
7:0	RO	P0_IQ_PCNT	CDMA virtual input Q page count.	8'b0

### 3.20.3.3 Register Description – GDMA2

**GDMA2\_FWD\_CFG : GDMA2 Forwarding Configuration (offset: 0x60)**

Bits	Type	Name	Description	Initial value
31:28	R/W	GDM2_JMB_LEN	When GDM2_JMB_EN=1, this parameter define the maximum packet length(including CRC) that GDMA2 could receive in 1024-byte unit. The valid value is from 0 ~12.	4'd12
27:26			Reserved	0
25	R/W	GDM2_20US_TICK_LT	0: GDM2 shaper add token every 1ms. 1: GDM2 shaper add token every 20us. Please refer to GDM2_TK_RATE in GDMA2_SHPR_CFG register	0
24	R/W	GDM2_TCI_81xx	0: Check VLAN tag with EXT_VLAN[15:0] 1: Check VLAN tag with EXT_VLAN[15:8] only	1'd0
23	R/W	GDM2_DROP_256B	A Special mode to drop packets with payload > 256 bytes.	1'b0

			0: Drop packets according to standard Ethernet frame length limitation. 1: Drop packets with payload >256 bytes	
22	R/W	GDM2_ICS_EN	IPv4 header checksum check enable	1'b1
21	R/W	GDM2_TCS_EN	TCP checksum check enable	1'b1
20	R/W	GDM2_UCS_EN	UDP checksum check enable	1'b1
19	R/W	GDM2_JMB_EN	0: Drop received frames if length is great than 1518 (1522 for VLAN frames, and 1526 for double VLAN frames) 1: Allow receiving jumbo frames length up to 12kB.	1'b0
18	R/W	GDM2_DISPAD	0: Enable GDMA2 Tx padding function. 1: Disable GDMA2 Tx padding function.	1'b0
17	R/W	GDM2_DISCRC	0: Enable GDMA2 Tx CRC generation. 1: Disable GDMA2 Tx CRC generation.	1'b0
16	R/W	GDM2_STRPCRC	0: Disable GDMA2 automatic Rx CRC stripping 1: Enable GDMA2 automatic Rx CRC stripping	1'b1
15	-	-	Reserved	1'b0
14:12	R/W	GDM2_UFRC_P	GDMA2 My MAC unicast frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111
11	-	-	Reserved	1'b0
10:8	R/W	GDM2_BFRC_P	GDMA2 broad-cast MAC address frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111
7	-	-	Reserved	1'b0
6:4	R/W	GDM2_MFRC_P	GDMA2 multi-cast MAC address frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111
3	-	-	Reserved	1'b0
2:0	R/W	GDM2_OFRC_P	GDMA2 other MAC address frames destination port 3'd0: CPU 3'd1: GDMA1 3'd2: GDMA2 3'd6: PPE 3'd7: Discard Others: Reserved	3'b111

**GDMA2\_SCH\_CFG : GDMA2 Scheduling Configuration (offset: 0x64)**

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	7'b0
25:24	R/W	GDM2_SCH_MOD	2'b00: WRR 2'b01: Strict Priority, Q3>Q2>Q1>Q0 2'b10: Mixed, Q3>WRR(Q2,Q1,Q0) 2'b11: Reserved	2'b00

23:15	-	-	Reserved	1'b0
14:12	R/W	GDM2_WT_Q3	Q3's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b011
11	-	-	Reserved	1'b0
10:8	R/W	GDM2_WT_Q2	Q2's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b010
7	-	-	Reserved	1'b0
6:4	R/W	GDM2_WT_Q1	Q1's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b001
3	-	-	Reserved	1'b0
2:0	R/W	GDM2_WT_Q0	Q0's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b0

**GDMA2\_SHPR\_CFG : GDMA2Output Shaper Configuration (offset: 0x68)**

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	7'b0
24	R/W	GDM2_SHPR_EN	GDMA2 output shaper enable. 0: Disable 1: Enable	1'b0
23:16	R/W	GDM2_BK_SIZE	GDMA2 output shaper maximum bucket size. Unit is 1kB.	8'b0
15:14	-	-	Reserved	2'b0
13:0	R/W	GDM2_TK_RATE	GDMA2 output shaper token rate. Unit is 8B/ms or 8B/20us. According to GDM2_20US_TICK_SLT.	14'b0

**GDMA2\_MAC\_AdRL : GDMA2 MAC Address LSB (offset: 0x6C)**

Bits	Type	Name	Description	Initial value
31:0	R/W	GDM2_MY_MAC_L	GMAC2 MAC address bit 31-0	32'b0

**GDMA2\_MAC\_AdRH : GDMA1 MAC Address MSB (offset: 0x70)**

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	GDM2_MY_MAC_H	GMAC2 MAC address bit 47-32	16'b0

### 3.20.3.4 Register Description - CPU Port

**CDMA\_CSG\_CFG (offset: 0x80)**

Bits	Type	Name	Description	Initial value
31:16	R/W	INS_VLAN_	Inserted VLAN type	16'h8100
15:3	-	-	Reserved	13'b0
2	R/W	ICS_GEN_EN	IPv4 header checksum generation enable	1'b0
1	R/W	UCS_GEN_EN	UDP checksum generation enable	1'b0
0	R/W	TCS_GEN_EN	TCP checksum generation enable	1'b0

**CDMA\_SCH\_CFG (offset: 0x84)**

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	6'b0
25:24	R/W	CDM_SCH_MOD	2'b00: WRR 2'b01: Strict Priority, Q3>Q2>Q1>Q0 2'b10: Mixed, Q3>WRR(Q2,Q1,Q0) 2'b11: Reserved	2'b00
23:15	-	-	Reserved	9'b0
14:12	R/W	CDM_WT_Q3	Q3's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b011
11	-	-	Reserved	1'b0
10:8	R/W	CDM_WT_Q2	Q2's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b010
7	-	-	Reserved	1'b0
6:4	R/W	CDM_WT_Q1	Q1's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b001
3	-	-	Reserved	1'b0
2:0	R/W	CDM_WT_Q0	Q0's weight 3'd0: weight = 1 3'd1: weight = 2 3'd2: weight = 4 3'd3: weight = 8 3'd4: weight = 16	3'b000

**PPPOE\_SID\_0001 (offset: 0x88)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID1	PPPoE Session ID for SID INDEX#1	16'b0
15:0	R/W	PPPOE_SID0	PPPoE Session ID for SID INDEX#0	16'b0

**PPPOE\_SID\_0203 (offset: 0x8C)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID3	PPPoE Session ID for SID INDEX#3	16'b0
15:0	R/W	PPPOE_SID2	PPPoE Session ID for SID INDEX#2	16'b0

**PPPOE\_SID\_0405 (offset: 0x90)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID5	PPPoE Session ID for SID INDEX#5	16'b0
15:0	R/W	PPPOE_SID4	PPPoE Session ID for SID INDEX#4	16'b0

**PPPOE\_SID\_0607 (offset: 0x94)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID7	PPPoE Session ID for SID INDEX#7	16'b0
15:0	R/W	PPPOE_SID6	PPPoE Session ID for SID INDEX#6	16'b0

**PPPOE\_SID\_0809 (offset: 0x98)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID9	PPPoE Session ID for SID INDEX#9	16'b0
15:0	R/W	PPPOE_SID8	PPPoE Session ID for SID INDEX#8	16'b0

**PPPOE\_SID\_1011 (offset: 0x9C)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID11	PPPoE Session ID for SID INDEX#11	16'b0
15:0	R/W	PPPOE_SID10	PPPoE Session ID for SID INDEX#10	16'b0

**PPPOE\_SID\_1213 (offset: 0xa0)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID13	PPPoE Session ID for SID INDEX#13	16'b0
15:0	R/W	PPPOE_SID12	PPPoE Session ID for SID INDEX#12	16'b0

**PPPOE\_SID\_1415 (offset: 0xa4)**

Bits	Type	Name	Description	Initial value
31:16	R/W	PPPOE_SID15	PPPoE Session ID for SID INDEX#15	16'b0
15:0	R/W	PPPOE_SID14	PPPoE Session ID for SID INDEX#14	16'b0

**VLAN\_ID\_0001 (offset: 0xa8)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID0	VLAN ID of VLAN1	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID1	VLAN ID of VLAN0	12'b0

**VLAN\_ID\_0203 (offset: 0xaC)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID2	VLAN ID of VLAN2	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID3	VLAN ID of VLAN3	12'b0

**VLAN\_ID\_0405 (offset: 0xb0)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID4	VLAN ID of VLAN4	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID5	VLAN ID of VLAN5	12'b0

**VLAN\_ID\_0607 (offset: 0xb4)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID6	VLAN ID of VLAN6	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID7	VLAN ID of VLAN7	12'b0

**VLAN\_ID\_0809 (offset: 0xb8)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID8	VLAN ID of VLAN8	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID9	VLAN ID of VLAN9	12'b0

**VLAN\_ID\_1011 (offset: 0xc0)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID10	VLAN ID of VLAN10	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID11	VLAN ID of VLAN11	12'b0

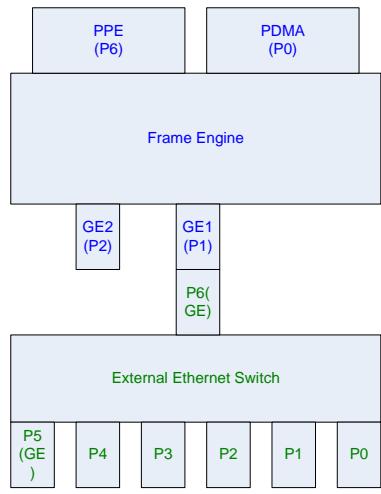
**VLAN\_ID\_1213 (offset: 0xd0)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:16	R/W	VLAN_ID12	VLAN ID of VLAN12	12'b0
15:12	-	-	Reserved	4'b0
11:0	R/W	VLAN_ID13	VLAN ID of VLAN13	12'b0

**VLAN\_ID\_14\_15 (offset: 0xd4)**

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
276	R/W	VLAN_ID_14	VLAN ID of VLAN14	12'b0
15:12	-	-	Reserved	4'b0
110	R/W	VLAN_ID_15	VLAN ID of VLAN15	12'b0

**FE\_COS\_MAP : Frame engine class of service mapping (offset: 0xd8)**

Bits	Type	Name	Description	Initial value																														
31	R/W	PORT_PRI_EN	0: use VLAN priority 1: use source port priority	1'b0																														
30	R/W	EXT_SW_EN	<p>0: There is no external Ethernet switch which supports Ralink special tag on the frame engine's GE port #1.      1: There is an external Ethernet switch which supports Ralink special tag on the frame engine's GE port #1.</p> <p>If both EXT_SW_EN and GDM1_TCI_81xx are set to 1, the frame engine will apply the following mapping to for identifying the source port of an incoming frame. This source port (SP[2:0]) will be attached to the RX descriptor when the frame's destination port is CPU. It is also used for PPE's policy engine process to classify frames based frame headers and source port.</p> <table border="1"> <thead> <tr> <th>Incoming port</th> <th>Frame Engine SP[2:0] (when EXT_SW_EN=1)</th> <th>Frame Engine SP[2:0] (when EXT_SW_EN=0)</th> </tr> </thead> <tbody> <tr> <td>Ethernet SW P0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Ethernet SW P1</td> <td>1</td> <td>1</td> </tr> <tr> <td>Ethernet SW P2</td> <td>2</td> <td>1</td> </tr> <tr> <td>Ethernet SW P3</td> <td>3</td> <td>1</td> </tr> <tr> <td>Ethernet SW P4</td> <td>4</td> <td>1</td> </tr> <tr> <td>Ethernet SW P5</td> <td>5</td> <td>1</td> </tr> <tr> <td>Frame Engine PDMA</td> <td>6</td> <td>0</td> </tr> <tr> <td>Frame Engine GE1</td> <td>N/A</td> <td>1</td> </tr> <tr> <td>Frame Engine GE2</td> <td>5</td> <td>2</td> </tr> </tbody> </table> 	Incoming port	Frame Engine SP[2:0] (when EXT_SW_EN=1)	Frame Engine SP[2:0] (when EXT_SW_EN=0)	Ethernet SW P0	0	1	Ethernet SW P1	1	1	Ethernet SW P2	2	1	Ethernet SW P3	3	1	Ethernet SW P4	4	1	Ethernet SW P5	5	1	Frame Engine PDMA	6	0	Frame Engine GE1	N/A	1	Frame Engine GE2	5	2	
Incoming port	Frame Engine SP[2:0] (when EXT_SW_EN=1)	Frame Engine SP[2:0] (when EXT_SW_EN=0)																																
Ethernet SW P0	0	1																																
Ethernet SW P1	1	1																																
Ethernet SW P2	2	1																																
Ethernet SW P3	3	1																																
Ethernet SW P4	4	1																																
Ethernet SW P5	5	1																																
Frame Engine PDMA	6	0																																
Frame Engine GE1	N/A	1																																
Frame Engine GE2	5	2																																

			Porting issues for software: 1. In this external switch mode, packets come from CPU (PDMA) and loop backed by PPE back to CPU will be denoted as coming from port "6" (see the mapping table above) 2. In this external switch mode, packets come from GE2 will be denoted as coming from port "6" (see the mapping table above) 3. There are two port #5 in the mapping table. It is because we just assume if customers want to use port#5 of the external switch, they might not want to use the GE2 of the frame engine. The reason for not using "port #7" to denote GE2 is we reserve "7" as "don't care source port" in the policy table of the PPE.	
29:28	-	-	Reserved	
27:26	R/W	Port5_QUEUE	Dest. queue # for frames with source port=5	2'b00
25:24	R/W	Port4_QUEUE	Dest. queue # for frames with source port=4	2'b00
23:22	R/W	Port3_QUEUE	Dest. queue # for frames with source port=3	2'b00
21:20	R/W	Port2_QUEUE	Dest. queue # for frames with source port=2	2'b00
19:18	R/W	Port1_QUEUE	Dest. queue # for frames with source port=1	2'b00
17:16	R/W	Port0_QUEUE	Dest. queue # for frames with source port=0	2'b00
15:14	R/W	VPRI7_QUEUE	Dest. queue # for frames with VLAN priority=7	2'b00
13:12	R/W	VPRI6_QUEUE	Dest. queue # for frames with VLAN priority=6	2'b00
11:10	R/W	VPRI5_QUEUE	Dest. queue # for frames with VLAN priority=5	2'b00
9:8	R/W	VPRI4_QUEUE	Dest. queue # for frames with VLAN priority=4	2'b00
7:6	R/W	VPRI3_QUEUE	Dest. queue # for frames with VLAN priority=3	2'b00
5:4	R/W	VPRI2_QUEUE	Dest. queue # for frames with VLAN priority=2	2'b00
3:2	R/W	VPRI1_QUEUE	Dest. queue # for frames with VLAN priority=1	2'b00
1:0	R/W	VPRI0_QUEUE	Dest. queue # for frames with VLAN priority=0	2'b00

### 3.20.3.5 Register Description - PDMA

PDMA\_GLO\_CFG (offset:0x100)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	2'b0
29:16	R/W	HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	14'b0
15:8	-	-	Reserved	8'b0
7	-	-	Reserved	1'b0
6	R/W	TX_WB_DDONE	0:Disable TX_DMA writing back DDONE into TXD 1: Enable TX_DMA writing back DDONE into TXD	1'b1
5:4	R/W	PDMA_BT_SIZE	Define the burst size of PDMA 0: 4 DWORD (16bytes) 1: 8 DWORD (32 bytes) 2: 16 DWORD (64 bytes) 3: Reserved	2'd2
3	RO	RX_DMA_BUSY	1: RX_DMA is busy 0: RX_DMA is not busy	1'b0
2	R/W	RX_DMA_EN	1: Enable RX_DMA 0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	1'b0

1	RO	TX_DMA_BUSY	1: TX_DMA is busy 0: TX_DMA is not busy	1'b0
0	R/W	TX_DMA_EN	1: Enable TX_DMA 0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	1'b0

**PDMA\_RST\_IDX (offset:0x104)**

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	15'b0
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DRX_IDX0 to 0	1'b0
15:4	-	-	Reserved	12'b0
3	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DTX_IDX3 to 0	1'b0
2	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DTX_IDX2 to 0	1'b0
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DTX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DTX_IDX0 to 0	1'b0

**DLY\_INT\_CFG (offset 0x10C)**

Bits	Type	Name	Description	Initial value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or greater than the value specified here or interrupt pending time reach the limit (See below), an Final TX_DLY_INT is generated. Set to 0 will disable this feature	7'b0
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INT0 and TX_DONE_INT1. When the pending time equal or greater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0 and TX_DONE_INT1 equal or greater than TXMAX_PINT (see above), Final TX_DLY_INT is generated Set to 0 will disable this feature	8'b0
15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or greater than the value specified here or interrupt pending time reach the limit (See below), an Final RX_DLY_INT is generated. Set to 0 will disable this feature	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or greater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or greater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable this feature.	8'b0

**TX\_BASE\_PTR0 (offset: 0x110)**

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	32'b0

**TX\_MAX\_CNT0 (offset: 0x114)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	12'b0

**TX\_CTX\_IDX0 (offset:0x118)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX0	Point to the next TXD in TXD_Ring0 CPU wants to use	12'b0

**TX\_DTX\_IDX0 (offset:0x11C)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX0	Point to the next TXD in TXD_Ring0 DMA wants to use	12'b0

**TX\_BASE\_PTR1(offset:0x120)**

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR1	Point to the base address of TX_Ring1 (4-DWORD aligned address)	32'b0

**TX\_MAX\_CNT1 (offset:0x124)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT1	The maximum number of TXD count in TXD_Ring1.	12'b0

**TX\_CTX\_IDX1(offset:0x128)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX1	Point to the next TXD in TXD_Ring1 CPU wants to use	12'b0

**TX\_DTX\_IDX1 (offset:0x12C)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX1	Point to the next TXD in TXD_Ring1 DMA wants to use	0

**RX\_BASE\_PTR0 (offset:0x130)**

Bits	Type	Name	Description	Initial value
31:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0. It should be a 4-DWORD aligned address	0

**RX\_MAX\_CNT0 (offset:0x134)**

Bits	Type	Name	Description	Initial value
31:12	R-	-	Reserved	0
11:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

**ALC\_IDX0 (offset:0x138)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0
11:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

**RX\_DRX\_IDX0 (offset:0x13C)**

Bits	Type	Name	Description	Initial value
31:12	RO	Reserved	Reserved	0
11:0	RO	RX_DRX_IDX0	Point to the next RXD DMA wants to use in RXD Ring#0. It should be a 4-DWORD aligned address.	0

**TX\_BASE\_PTR2(offset:0x140)**

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR2	Point to the base address of TX_Ring2 (4-DWORD aligned address)	32'b0

**TX\_MAX\_CNT2 (offset:0x144)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT2	The maximum number of TXD count in TXD_Ring2.	12'b0

**TX\_CTX\_IDX2(offset:0x148)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX2	Point to the next TXD in TXD_Ring2 CPU wants to use	12'b0

**TX\_DTX\_IDX2 (offset:0x14C)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX2	Point to the next TXD in TXD_Ring2 DMA wants to use	0

**TX\_BASE\_PTR3(offset:0x150)**

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_BASE_PTR3	Point to the base address of TX_Ring3 (4-DWORD aligned address)	32'b0

**TX\_MAX\_CNT3 (offset:0x154)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_MAX_CNT3	The maximum number of TXD count in TXD_Ring3.	12'b0

**TX\_CTX\_IDX3(offset:0x158)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	R/W	TX_CTX_IDX3	Point to the next TXD in TXD_Ring3 CPU wants to use	12'b0

**TX\_DTX\_IDX3 (offset:0x15C)**

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	20'b0
11:0	RO	TX_DTX_IDX3	Point to the next TXD in TXD_Ring3 DMA wants to use	0

**PDMA\_FC\_CFG (offset:0x1F0)**

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	2'b00
29:24	R/W	PDM_FC_DEF_Q3	Q3 flow control pause condition Bit[5]: pause Q3 when PSE P2 high Q full Bit[4]: pause Q3 when PSE P2 low Q full Bit[3]: pause Q3 when PSE P1 high Q full Bit[2]: pause Q3 when PSE P1 low Q full Bit[1]: pause Q3 when PSE P0 high Q full Bit[0]: pause Q3 when PSE P0 low Q full	6'b111111
23:22	-	-	Reserved	2'b00
21:16	R/W	PDM_FC_DEF_Q2	Q2 flow control pause condition Bit[5]: pause Q2 when PSE P2 high Q full Bit[4]: pause Q2 when PSE P2 low Q full Bit[3]: pause Q2 when PSE P1 high Q full Bit[2]: pause Q2 when PSE P1 low Q full Bit[1]: pause Q2 when PSE P0 high Q full Bit[0]: pause Q2 when PSE P0 low Q full	6'b111111
15:14	-	-	Reserved	2'b00
13:8	R/W	PDM_FC_DEF_Q1	Q1 flow control pause condition Bit[5]: pause Q1 when PSE P2 high Q full Bit[4]: pause Q1 when PSE P2 low Q full Bit[3]: pause Q1 when PSE P1 high Q full Bit[2]: pause Q1 when PSE P1 low Q full Bit[1]: pause Q1 when PSE P0 high Q full Bit[0]: pause Q1 when PSE P0 low Q full	6'b111111
7:6	-	-	Reserved	
5:0	R/W	PDM_FC_DEF_Q0	Q0 flow control pause condition Bit[5]: pause Q0 when PSE P2 high Q full Bit[4]: pause Q0 when PSE P2 low Q full Bit[3]: pause Q0 when PSE P1 high Q full Bit[2]: pause Q0 when PSE P1 low Q full Bit[1]: pause Q0 when PSE P0 high Q full Bit[0]: pause Q0 when PSE P0 low Q full	6'b111111

**SCH\_Q01\_CFG: Scheduler configuration for queue #0 and #1 (offset: 0x1F4)**

Bits	Type	Name	Description	Initial value
31	R/W	MAX_BKT_SIZE1	When set to 0, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us.  When set to 1, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
30	R/W	MAX_RATE_ULMT1	When set to 1, the max rate limitation function for queue #1 is disabled. The max rate for queue #1 is unlimited. The scheduler would allocate bandwidth to queue #1 based on MAX_WEIGHT1.  When set to 0, the max rate limitation function for queue #1 is enabled. The max rate for queue #1 is defined by MAX_RATE1.	1'b1
29:28	R/W	MAX_WEIGHT1	Define the auto-reload bucket size if MAX_RATE_ULMT1 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #1.  2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	2'd1
27:26	R/W	MIN_RATE_RATIO1	Define the guaranteed Min rate based on MAX_RATE1.  2'b00: MIN_RATE1 = MAX_RATE1 2'b01: MIN_RATE1 = 1/2 MAX_RATE1 2'b10: MIN_RATE1 = 1/4 MAX_RATE1 2'b11: MIN_RATE1 = 0	2'd3
25:16	R/W	MAX_RATE1	Define the limited Max rate for queue # 1 if MAX_RATE_ULMT1 is 0.  The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us.  For example,  If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125\mu\text{s} = 16.384\text{M bytes/sec or } 131\text{Mbps}$	10'd0
15	R/W	MAX_BKT_SIZE0	When set to 0, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us.  When set to 1, the max bucket size (burst size allowed in byte) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
14	R/W	MAX_RATE_ULMT0	When set to 1, the max rate limitation function for queue #0 is disabled. The max rate for queue #0 is unlimited. The scheduler would allocate bandwidth to queue #0 based on MAX_WEIGHT0.  When set to 0, the max rate limitation function for queue #0 is enabled. The max rate for queue #0 is defined by MAX_RATE0.	1'b1
13:12	R/W	MAX_WEIGHT0	Define the auto-reload bucket size if MAX_RATE_ULMT0 is set to 1. It is also served as excess bandwidth allocation ratio for	2'd0

			servicing queue #0. 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	
11:10	R/W	MIN_RATE_RATIO0	Define the guaranteed Min rate based on MAX_RATE0. 2'b00: MIN_RATE0 = MAX_RATE0 2'b01: MIN_RATE0 = 1/2 MAX_RATE0 2'b10: MIN_RATE0 = 1/4 MAX_RATE0 2'b11: MIN_RATE0 = 0	2'd3
9:0	R/W	MAX_RATE0	Define the limited Max rate for queue #0 if MAX_RATE_ULMT0 is 0. The value specified represents the amount of 4-byte quota to be added into the queue #0 bucket per 125us. For example, If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125\mu\text{s} = 16.384\text{M bytes/sec or } 131\text{Mbps}$	10'd0

SCH\_Q23\_CFG: Scheduler configuration for queue #2 and #3 (offset: 0x1f8)

Bits	Type	Name	Description	Initial value
31	R/W	MAX_BKT_SIZE3	When set to 0, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us. When set to 1, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
30	R/W	MAX_RATE_ULMT3	When set to 1, the max rate limitation function for queue #3 is disabled. The max rate for queue #3 is unlimited. The scheduler would allocate bandwidth to queue #3 based on MAX_WEIGHT3. When set to 0, the max rate limitation function for queue #3 is enabled. The max rate for queue #3 is defined by MAX_RATE3.	1'b1
29:28	R/W	MAX_WEIGHT3	Define the auto-reload bucket size if MAX_RATE_ULMT3 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #3. 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	2'd3
27:26	R/W	MIN_RATE_RATIO3	Define the guaranteed Min rate based on MAX_RATE3. 2'b00: MIN_RATE3 = MAX_RATE3 2'b01: MIN_RATE3 = 1/2 MAX_RATE3 2'b10: MIN_RATE3 = 1/4 MAX_RATE3 2'b11: MIN_RATE3 = 0	2'd3
25:16	R/W	MAX_RATE3	Define the limited Max rate for queue #3 if MAX_RATE_ULMT3 is 0.	10'd0

			The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us.  For example,: If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec or } 131\text{Mbps}$	
15	R/W	MAX_BKT_SIZE2	When set to 0, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us.  When set to 1, the max bucket size (burst size allowed) for both max and min buckets are equal to one max size packet + the associated max or min rate per 125us + 2048 bytes.	1'b0
14	R/W	MAX_RATE_ULMT2	When set to 1, the max rate limitation function for queue #2 is disabled. The max rate for queue #2 is unlimited. The scheduler would allocate bandwidth to queue #2 based on MAX_WEIGHT2.  When set to 0, the max rate limitation function for queue #2 is enabled. The max rate for queue #2 is defined by MAX_RATE0.	1'b1
13:12	R/W	MAX_WEIGHT2	Define the auto-reload bucket size if MAX_RATE_ULMT0 is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue #2.  2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	2'd2
11:10	R/W	MIN_RATE_RATI02	Define the guaranteed Min rate based on MAX_RATE0.  2'b00: MIN_RATE2 = MAX_RATE2 2'b01: MIN_RATE2 = 1/2 MAX_RATE2 2'b10: MIN_RATE2 = 1/4 MAX_RATE2 2'b11: MIN_RATE2 = 0	2'd3
9:0	R/W	MAX_RATE2	Define the limited Max rate for queue # 2 if MAX_RATE_ULMT2 is 0.  The value specified represents the amount of 4-byte quota to be added into the queue #0 bucket per 125us.  For example: If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125\text{us} = 16.384\text{M bytes/sec or } 131\text{Mbps}$	10'd0

### 3.20.3.6 Register Description – Frame Engine Counters (base: 0x1010.0400)

0x700	GDMA_TX_GBCNT1	Transmit good byte count for GDMA port#1
0x704	GDMA_TX_GPCNT1	Transmit good pkt count for GDMA port#1 (not including flow control frames)
0x708	GDMA_TX_SKIPCNT1	Transmit skip count for GDMA port#1
0x70C	GDMA_TX_COLCNT1	Transmit collision count for GDMA port#1
0x710 – 0x71C	Reserved	
0x720	GDMA_RX_GBCNT1	Received good byte count for GDMA port#1
0x724	GDMA_RX_GPCNT1	Received good pkt count for GDMA port#1

		(not including flow control frames)
0x728	GDMA_RX_OERCNT1	Received overflow error pkt count for GDMA port#1
0x72C	GDMA_RX_FERCNT1	Received FCS error pkt count for GDMA port#1
0x730	GDMA_RX_SERCNT1	Received too short error pkt count for GDMA port#1
0x734	GDMA_RX_LERCNT1	Received too long error pkt count for GDMA port#1
0x738	GDMA_RX_CERCNT1	Received ip/tcp/udp checksum error pkt count for GDMA port#1
0x73C	GDMA_RX_FCCNT1	Received flow control pkt count for GDMA port#1
0x740	GDMA_TX_GBCNT2	Transmit good byte count for GDMA port#2
0x744	GDMA_TX_GPCNT2	Transmit good pkt count for GDMA port#2 (not including flow control frames)
0x748	GDMA_TX_SKIPCNT2	Transmit skip count for GDMA port#2
0x74C	GDMA_TX_COLCNT2	Transmit collision count for GDMA port#2
0x750 – 0x75C	Reserved	
0x760	GDMA_RX_GBCNT2	Received good byte count for GDMA port#2
0x764	GDMA_RX_GPCNT2	Received good pkt count for GDMA port#2 (not including flow control frames)
0x768	GDMA_RX_OERCNT2	Received overflow error pkt count for GDMA port#2
0x76C	GDMA_RX_FERCNT2	Received FCS error pkt count for GDMA port#2
0x760	GDMA_RX_SERCNT2	Received too short error pkt count for GDMA port#2
0x764	GDMA_RX_LERCNT2	Received too long error pkt count for GDMA port#2
0x768	GDMA_RX_CERCNT2	Received ip/tcp/udp checksum error pkt count for GDMA port#2
0x76C	GDMA_RX_FCCNT2	Received flow control pkt count for GDMA port#2

### 3.21 802.11n 2T3R MAC/BBP

#### 3.21.1 Features

- 1x1/1x2/1x3/2x1/2x2/2x3/3x1/3x2/3x3 modes
- 450MHz PHY Rate Support
- Legacy and High Throughput Modes
- 20MHz/40MHz bandwidth
- Reverse Direction Data Flow and Frame Aggregation
- WEP 64/128, WPA, WPA2 Support
- QoS – WMM, WMM-PS
- Wake on Wireless LAN
- Multiple BSSID Support
- International Regulation - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 Compliance
- Bluetooth Co-existence
- Low Power with Advanced Power Management

#### 3.21.2 Block Diagram

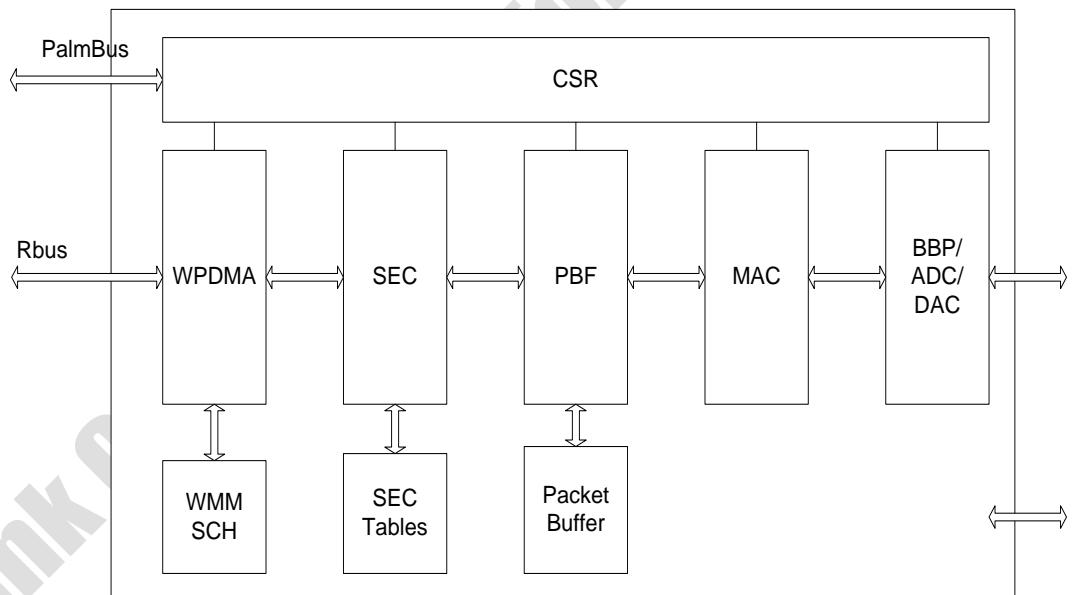


Fig. 3-21-1 802.11n 2T3R MAC/BBP block diagram

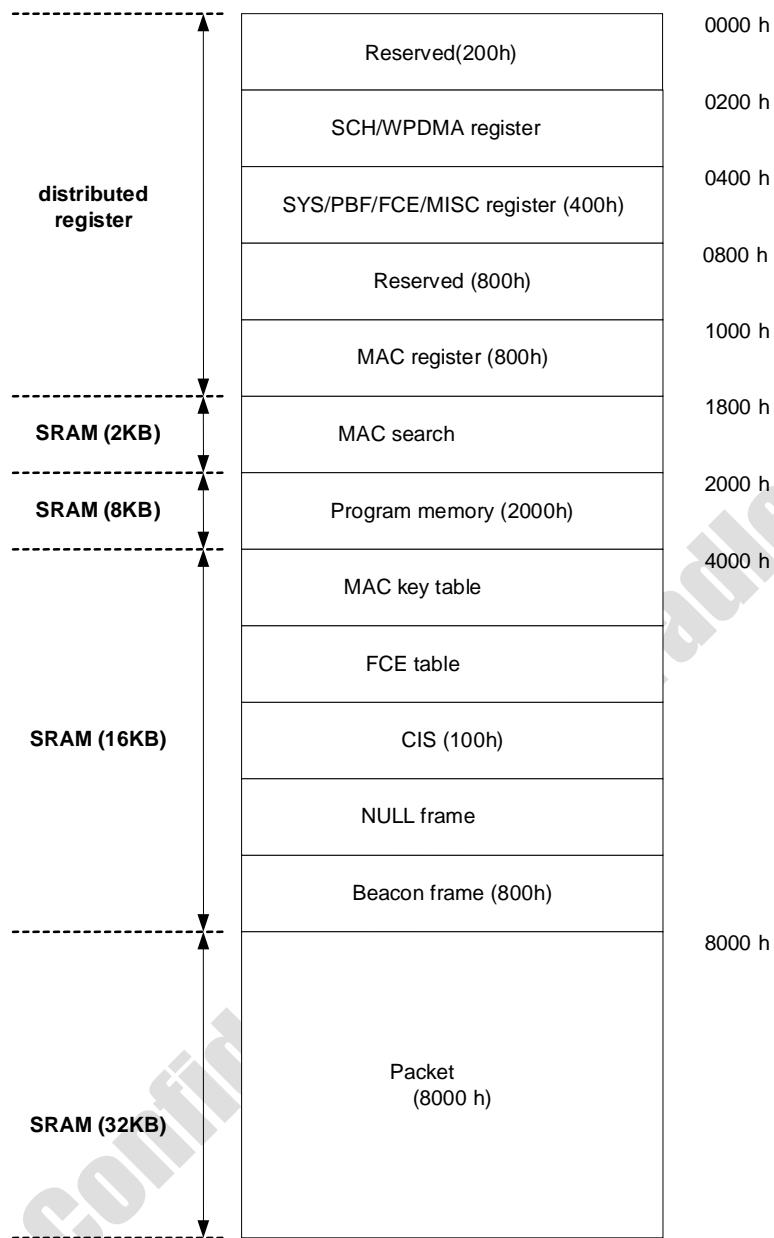


Fig. 3-21-2 802.11n 2T3R MAC/BBP register map

### 3.21.3 Register Description - SCH/WPDMA (base: 1018.0000)

INT\_STATUS (offset: 0x0200)

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	R/W	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
16	R/W	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	0
15	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0

14	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0
13	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
12	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
11	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
10	RO	TX_RX_COHERENT	When TX_COHERENT or RX_COHERENT is on, this bit is set	0
9	R/W	MCU_CMD_INT	MCU command interrupt	0
8	R/W	TX_DONE_INT5	TX Queue#5 packet transmit interrupt Write 1 to clear the interrupt.	0
7	R/W	TX_DONE_INT4	TX Queue#4 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
6	R/W	TX_DONE_INT3	TX Queue#3 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
5	R/W	TX_DONE_INT2	TX Queue#2 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
4	R/W	TX_DONE_INT1	TX Queue#1 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
3	R/W	TX_DONE_INT0	TX Queue#0 packet transmit interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
2	R/W	RX_DONE_INT	RX packet receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	0
1	R/W	TX_DLY_INT	Summary of the whole WPDMA TX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0
0	R/W	RX_DLY_INT	Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt. Read to get the raw interrupt status	0

**INT\_MASK (offset:0x0204)**

Bits	Type	Name	Description	Init Value
31:18			Reserved	
17	R/W	TX_COHERENT_EN	Enable for TX_DMA data coherent interrupt	0
16	R/W	RX_COHERENT_EN	Enable for RX_DMA data coherent interrupt	0
15	R/W	MAC_INT4_EN	MAC interrupt 4: GP timer interrupt	0
14	R/W	MAC_INT3_EN	MAC interrupt 3: Auto wakeup interrupt	0
13	R/W	MAC_INT2_EN	MAC interrupt 2: TX status interrupt	0
12	R/W	MAC_INT1_EN	MAC interrupt 1: Pre-TBTT interrupt	0
11	R/W	MAC_INT0_EN	MAC interrupt 0: TBTT interrupt	0
10			Reserved	
9	R/W	MCU_CMD_INT_MSK	MCU command interrupt enable	0
8	R/W	TX_DONE_INT_MSK5	TX Queue#5 packet transmit interrupt	0
7	R/W	TX_DONE_INT_MSK4	TX Queue#4 packet transmit interrupt	0
6	R/W	TX_DONE_INT_MSK3	TX Queue#3 packet transmit interrupt	0
5	R/W	TX_DONE_INT_MSK2	TX Queue#2 packet transmit interrupt	0
4	R/W	TX_DONE_INT_MSK1	TX Queue#1 packet transmit interrupt	0
3	R/W	TX_DONE_INT_MSK0	TX Queue#0 packet transmit interrupt	0
2	R/W	RX_DONE_INT_MSK	RX packet receive interrupt	0
1	R/W	TX_DLY_INT_MSK	Summary of the whole WPDMA TX related interrupts	0
0	R/W	RX_DLY_INT_MSK	Summary of the whole WPDMA RX related interrupts	0

**WPDMA\_GLO\_CFG (offset:0x0208)**

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:8		HDR_SEG_LEN	Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value. When set to zero, the header/payload scattering feature is disabled.	8'b0
7	R/W	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.	0
6	R/W	TX_WB_DDONE	0 : Disable TX_DMA writing back DDONE into TXD 1 : Enable TX_DMA writing back DDONE into TXD	1'b1
5:4	R/W	WPDMA_BT_SIZE	Define the burst size of WPDMA 0 : 4 DWORD (16bytes)                            1 : 8 DWORD (32 bytes) 2 : 16 DWORD (64 bytes)    3 : 32 DWORD (128 bytes)	2'd2
3	RO	RX_DMA_BUSY	1 : RX_DMA is busy 0 : RX_DMA is not busy	0
2	R/W	RX_DMA_EN	1 : Enable RX_DMA 0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	0
1	RO	TX_DMA_BUSY	1 : TX_DMA is busy 0 : TX_DMA is not busy	0
0	R/W	TX_DMA_EN	1 : Enable TX_DMA 0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	0

**WPDMA\_RST\_IDX (offset:0x020C)**

Bits	Type	Name	Description	Init Value
31:17			Reserved	
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DMARX_IDX0 to 0	1'b0
15:6			Reserved	
5	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX5 to 0	1'b0
4	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX4 to 0	1'b0
3	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX3 to 0	1'b0
2	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX2 to 0	1'b0
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DMATX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DMATX_IDX0 to 0	1'b0

**DELAY\_INT\_CFG (offset:0x0210)**

Bits	Type	Name	Description	Init Value
31	RW	TXDLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism.	1'b0
30:24	RW	TXMAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See below), an Final TX_DLY_INT is generated.  Set to 0 will disable pending interrupt count check	7'b0
23:16	RW	TXMAX_PTIME	Specified Max pending time for the internal TX_DONE_INTO-5. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INTO-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated	8'b0

			Set to 0 will disable pending interrupt time check	
15	RW	RXDLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'b0
14:8	RW	RXMAX_PINT	Specified Max # of pended interrupts.  When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final RX_DLY_INT is generated.  Set to 0 will disable pending interrupt count check	7'b0
7:0	RW	RXMAX_PTIME	Specified Max pending time for the internal RX_DONE_INT.  When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated  Set to 0 will disable pending interrupt time check	8'b0

WMM\_AIFSN\_CFG (offset:0x0214,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:12	RW	AIFSN3	WMM parameter AIFSN3	4'h0
11:8	RW	AIFSN2	WMM parameter AIFSN2	4'h0
7:4	RW	AIFSN1	WMM parameter AIFSN1	4'h0
3:0	RW	AIFSN0	WMM parameter AIFSN0	4'h0

## WMM\_CWMIN\_CFG (offset:0x0218)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:12	RW	CW_MIN3	WMM parameter Cw_min3	4'h0
11:8	RW	CW_MIN2	WMM parameter Cw_min2	4'h0
7:4	RW	CW_MIN1	WMM parameter Cw_min1	4'h0
3:0	RW	CW_MIN0	WMM parameter Cw_min0	4'h0

## WMM CWMAX CFG (offset:0x021C)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:12	RW	CW_MAX3	WMM parameter Cw_max3	4'h0
11:8	RW	CW_MAX2	WMM parameter Cw_max2	4'h0
7:4	RW	CW_MAX1	WMM parameter Cw_max1	4'h0
3:0	RW	CW_MAX0	WMM parameter Cw_max0	4'h0

WMM TXOP0 CFG (offset:0x0220)

Bits	Type	Name	Description	Init Value
31:16	RW	TXOP1	WMM parameter TXOP1	16'h0
15:0	RW	TXOP0	WMM parameter TXOP0	16'h0

## WMM\_TXOP1\_CFG (offset:0x0224)

Bits	Type	Name	Description	Init Value
31:16	RW	TXOP3	WMM parameter TXOP3	16'h0
15:0	RW	TXOP2	WMM parameter TXOP2	16'h0

## GPIO\_CTRL (offset:0x0228)

Bits	Type	Name	Description	Init Value
31	R		Reserved	1'b0
30:24	RW	GPIO14_8_D	GPIO14~8 direction 0: Output                    1: Input	7'h7F
23	R		Reserved	1'b0
22:16	RW	GPIO14_8_O	GPIO14~8 data	7'b0
15:8	RW	GPIO7_0_D	GPIO7~0 direction 0: Output                    1: Input	8'hFF
7:0	RW	GPIO7_0_O	GPIO7~0 data	8'h00

**MCU\_CMD\_REG (offset:0x022C)**

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	RW	MCU_CMD	MCU command register. Internal 8051 write this register will trigger MCU command interrupt (0x0200 bit 9) to host.	8'h0

**TX\_BASE\_PTR0 (offset:0x0230)**

Bits	Type	Name	Description	Init Value
31:0	R/W	TX_BASE_PTR0	Point to the base address of TX_Ring0 (4-DWORD aligned address)	0

**TX\_MAX\_CNT0 (offset:0x0234)**

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	0

**TX\_CTX\_IDX0 (offset:0x0238,default :0x00000000)**

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	TX_CTX_IDX0	Point to the next TXD CPU wants to use	0

**TX\_DTX\_IDX0 (offset:0x023C)**

Bits	Type	Name	Description	Init Value
11:0	RO	TX_DTX_IDX0	Point to the next TXD DMA wants to use	0

TX\_BASE\_PTR2 (offset:0x0250,default :0x00000000)

TX\_MAX\_CNT2 (offset:0x0254,default :0x00000000)

TX\_CTX\_IDX2 (offset:0x0258,default :0x00000000)

TX\_DTX\_IDX2 (offset:0x025C,default :0x00000000)

TX\_BASE\_PTR3 (offset:0x0260,default :0x00000000)

TX\_MAX\_CNT3 (offset:0x0264,default :0x00000000)

TX\_CTX\_IDX3 (offset:0x0268,default :0x00000000)

TX\_DTX\_IDX3 (offset:0x026C,default :0x00000000)

TX\_BASE\_PTR4 (offset:0x0270,default :0x00000000)

TX\_MAX\_CNT4 (offset:0x0274,default :0x00000000)

TX\_CTX\_IDX4 (offset:0x0278,default :0x00000000)

TX\_DTX\_IDX4 (offset:0x027C,default :0x00000000)

TX\_BASE\_PTR5 (offset:0x0280,default :0x00000000)

TX\_MAX\_CNT5 (offset:0x0284,default :0x00000000)

TX\_CTX\_IDX5 (offset:0x0288,default :0x00000000)

TX\_DTX\_IDX5 (offset:0x028C,default :0x00000000)

**RX\_BASE\_PTR (offset:0x0290,default :0x00000000)**

Bits	Type	Name	Description	Init Value
31:0	R/W	RX_BASE_PTR0	Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address	0

**RX\_MAX\_CNT (offset:0x0294,default :0x00000000)**

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	RX_MAX_CNT0	The maximum number of RXD count in RXD Ring #0.	0

**RX\_CALC\_IDX (offset:0x0298,default :0x00000000)**

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	RX_CALC_IDX0	Point to the next RXD CPU wants to allocate to RXD Ring #0.	0

**FS\_DRX\_IDX (offset:0x029C,default :0x00000000)**

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11:0	R/W	RX_DRX_IDX0	Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address.	0

**USB\_DMA\_CFG (offset:0x02A0,default :0x00000000)**

Bits	Type	Name	Description	Init Value
31	R	TX_BUSY	USB DMA TX FSM busy	0
30	R	RX_BUSY	USB DMA RX FSM busy	0
29:24	R	EPOUT_VLD	OUT endpoint data valid	0
23	R/W	UDMA_TX_EN	USB DMA TX enable	0
22	R/W	UDMA_RX_EN	USB DMA RX enable	0
21	R/W	RX_AGG_EN	RX bulk aggregation enable	0
20	R/W	TXOP_HALT	Halt TXOP count down when TX buffer is full. 0: disable 1: enable	0
19	R/W	TX_CLEAR	Clear USB DMA TX path	0
18:17			Reserved	
16	R/W	PHY_WD_EN	USB PHY watch-dog enable	0
15:8	RW	RX_AGG_LMT	RX bulk aggregation limit. Unit is 1024 bytes	00
7:0	RW	RX_AGG_TO	RX bulk aggregation time-out count. Unit is 1us	00

**US\_CYC\_CNT (offset:0x02A4,default :0x00F00021)**

Bits	Type	Name	Description	Init Value
31:29			Reserved	
28			Edt_bypass (for DFT scan compression)	0
27:25			Reserved	0
24	R/W	TEST_EN	Test mode enable	0
23:16	R/W	TEST_SEL	Test mode selection	8'hf0
15:10			Reserved	
9	R/W	MAC_BT_SW_en	Enable function of single antenna switch for mac / blue-tooth	0
8	R/W	BT_MODE_EN	Blue-tooth mode enable	0
7:0	RW	US_CYC_CNT	Clock cycle count in 1us. It's dependent on the interface clock rate. For PCI 33, set 8'h21. For PCI express, set 8'h7D. For USB, set 8'h1E.	8'h21

**3.21.3.1 Register Description - PBF (base: 1018.0000)**
**SYS\_CTRL (offset: 0x0400)**

Bits	Type	Name	Description	Init Value
31:20			Reserved	
19	R/W	SHR_MSEL	Shared memory access selection. 0: address 0x4000 – 0x7FFF mapping to lower 16kB of shared memory 1: address 0x4000 – 0x4FFF mapping to higher 4kB of shared memory	0
18:17	R/W	PBF_MSEL	Packet buffer memory access selection. 00: address 0x8000 – 0xFFFF mapping to 1 <sup>st</sup> 32kB of packet buffer. 01: address 0x8000 – 0xFFFF mapping to 2 <sup>nd</sup> 32kB of packet buffer. 10: address 0x8000 – 0xBFFF mapping to higher 16kB of packet buffer.	0
16	R/W	HST_PM_SEL	Host program ram write selection. This bit is only for PCI/PCIe mode.	0

15			Reserved	
14	R/W	CAP_MODE	Packet buffer capture mode. 0: packet buffer in normal mode. 1: packet buffer in BBP capture mode.	0
13	R/W	PME_OEN	PCI and PCIE mode: PCI PME OEN USB mode: 1: force TR_PE=0, RF_PE = 0. 0: normal function.	1
12	R/W	CLKSELECT	MAC/PBF clock source selection. 0: from PLL 1: from 40MHz clock input	0
11	R/W	PBF_CLKEN	PBF clock enable.	1
10	R/W	MAC_CLK_EN	MAC clock enable.	1
9	R/W	DMA_CLK_EN	DMA clock enable.	1
8			Reserved	
7	R/W	MCU_READY	MCU ready. 8051 writes '1' to this bit to inform host internal MCU is ready.	0
6:5			Reserved	
4	R/W	ASY_RESET	ASYNC interface reset. Write '1' to put ASYNC into reset state.	0
3	R/W	PBF_RESET	PBF hardware reset. Write '1' to put PBF into reset state.	0
2	R/W	MAC_RESET	MAC hardware reset. Write '1' to put MAC into reset state.	0
1	R/W	DMA_RESET	DMA hardware reset. Write '1' to put DMA into reset state.	0
0	W1C	MCU_RESET	MCU hardware reset. This bit will be auto-cleared after several clock cycles.	0

**HOST\_CMD (offset: 0x0404)**

Bits	Type	Name	Description	Init Value
31:0	R/W	HST_CMD	Host command code. Host write this register will trigger interrupt to 8051.	0

**PBF\_CFG (offset: 0x0408)**

Bits	Type	Name	Description	Init Value
31:27			Reserved	
26:24	R/W	NULL2_SEL	NULL2 frame buffer selection (reuse beacon buffer). 0: use beacon #0 buffer (address set by 0x42C[7:0]) 1: use beacon #1 buffer (address set by 0x42C[15:8]) 2: use beacon #2 buffer (address set by 0x42C[23:16]) 3: use beacon #3 buffer (address set by 0x42C[31:24]) 4: use beacon #4 buffer (address set by 0x430[7:0]) 5: use beacon #5 buffer (address set by 0x430[15:8]) 6: use beacon #6 buffer (address set by 0x430[23:16]) 7: use beacon #7 buffer (address set by 0x430[31:24])	3'h0
23:21	R/W	TX1Q_NUM	Queue depth of Tx1Q. The maximum number is 7.	3'h3
20:16	R/W	TX2Q_NUM	Queue depth of Tx2Q. The maximum number is 20.	5'h10
15	R/W	NULL0_MODE	NULL0 frame auto mode. In this mode, all TXQ2 will be enabled after NULL0 frame transmitted. 0: disable 1: enable	0
14	R/W	NULL1_MODE	NULL1 frame auto mode. In this mode, all TXQ (0/1/2) will be disabled after NULL1 frame transmitted. 0: disable 1: enable	0
13	R/W	RX_DROP_MODE	Rx drop mode. When set, PBF will drop Rx packet before into DMA. 0: normal mode 1: drop mode	0
12	R/W	TX0Q_MODE	Tx0Q operation mode.	0

			0: auto mode 1: manual mode	
11	R/W	TX1Q_MODE	Tx1Q operation mode. 0: auto mode 1: manual mode	0
10	R/W	TX2Q_MODE	Tx2Q operation mode. 0: auto mode 1: manual mode	0
9	R/W	RX0Q_MODE	Rx0Q operation mode. 0: auto mode 1: manual mode	0
8	R/W	HCCA_MODE	HCCA auto mode. In this mode, TXQ1 will be enabled when CF-POLL arriving. 0: disable 1: enable	0
7:5			Reserved	
4	R/W	TX0Q_EN	Tx0Q enable	1
3	R/W	TX1Q_EN	Tx1Q enable	0
2	R/W	TX2Q_EN	Tx2Q enable	1
1	R/W	RX0Q_EN	Rx0Q enable	1
0			Reserved	

**MAX\_PCNT (offset: 0x040C)**

Bits	Type	Name	Description	Init Value
31:24	R/W	MAX_TX0Q_PCNT	Maximum buffer page count of Tx0Q.	8'h1f
23:16	R/W	MAX_TX1Q_PCNT	Maximum buffer page count of Tx1Q.	8'h3f
15:8	R/W	MAX_TX2Q_PCNT	Maximum buffer page count of Tx2Q.	8'h9f
7:0	R/W	MAX_RX0Q_PCNT	Maximum buffer page count of Rx0Q.	8'h9f

**BUF\_CTRL (offset: 0x0410)**

Bits	Type	Name	Description	Init Value
31:12			Reserved	
11	W1C	WRITE_TX0Q	Manual write Tx0Q.	0
10	W1C	WRITE_TX1Q	Manual write Tx1Q.	0
9	W1C	WRITE_TX2Q	Manual write Tx2Q	0
8	W1C	WRITE_RX0Q	Manual write Rx0Q	0
7	W1C	NULL0_KICK	Kick out NULL0 frame. This bit will be cleared after NULL0 frame is transmitted.	0
6	W1C	NULL1_KICK	Kick out NULL1 frame. This bit will be cleared after NULL1 frame is transmitted.	0
5	W1C	BUF_RESET	Buffer reset.	0
4	W1C	NULL2_KICK	Kick out NULL2 frame. This bit will be cleared after NULL2 frame is transmitted.	0
3	W1C	READ_TX0Q	Manual read Tx0Q.	0
2	W1C	READ_TX1Q	Manual read Tx1Q.	0
1	W1C	READ_TX2Q	Manual read Tx2Q	0
0	W1C	READ_RX0Q	Manual read Rx0Q	0

**MCU\_INT\_STA (offset: 0x0414)**

Bits	Type	Name	Description	Init Value
31:28			Reserved	
27	R/W	MAC_INT_11	MAC interrupt 11: Reserved	0
26	R/W	MAC_INT_10	MAC interrupt 10: Reserved	0
25	R/W	MAC_INT_9	MAC interrupt 9: Reserved	0
24	R/W	MAC_INT_8	MAC interrupt 8: RX QoS CF-Poll interrupt	0
23	R/W	MAC_INT_7	MAC interrupt 7: TXOP early termination interrupt	0
22	R/W	MAC_INT_6	MAC interrupt 6: TXOP early timeout interrupt	0
21	R/W	MAC_INT_5	MAC interrupt 5: Reserved	0
20	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0
19	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0

18	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
17	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
16	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
15:13			Reserved	
12	R/W	N2TX_INT	NULL2 frame Tx complete interrupt.	0
11	R/W	DTX0_INT	DMA to TX0Q frame transfer complete interrupt.	0
10	R/W	DTX1_INT	DMA to TX1Q frame transfer complete interrupt.	0
9	R/W	DTX2_INT	DMA to TX2Q frame transfer complete interrupt.	0
8	R/W	DRX0_INT	RX0Q to DMA frame transfer complete interrupt.	0
7	R/W	HCMD_INT	Host command interrupt.	0
6	R/W	NOTX_INT	NULL0 frame Tx complete interrupt.	0
5	R/W	N1TX_INT	NULL1 frame Tx complete interrupt.	0
4	R/W	BCNTX_INT	Beacon frame Tx complete interrupt.	0
3	R/W	MTX0_INT	TX0Q to MAC frame transfer complete interrupt.	0
2	R/W	MTX1_INT	TX1Q to MAC frame transfer complete interrupt.	0
1	R/W	MTX2_INT	TX2Q to MAC frame transfer complete interrupt.	0
0	R/W	MRX0_INT	MAC to RX0Q frame transfer complete interrupt.	0

\*This register is only for 8051

#### MCU\_INT\_ENA (offset:0x0418)

Bits	Type	Name	Description	Init Value
31:28			Reserved	
27	R/W	MAC_INT11_EN	MAC interrupt 11 enable	0
26	R/W	MAC_INT10_EN	MAC interrupt 10 enable	0
25	R/W	MAC_INT9_EN	MAC interrupt 9 enable	0
24	R/W	MAC_INT8_EN	MAC interrupt 8 enable	0
23	R/W	MAC_INT7_EN	MAC interrupt 7 enable	0
22	R/W	MAC_INT6_EN	MAC interrupt 6 enable	0
21	R/W	MAC_INT5_EN	MAC interrupt 5 enable	0
20	R/W	MAC_INT4_EN	MAC interrupt 4 enable	0
19	R/W	MAC_INT3_EN	MAC interrupt 3 enable	0
18	R/W	MAC_INT2_EN	MAC interrupt 2 enable	0
17	R/W	MAC_INT1_EN	MAC interrupt 1 enable	0
16	R/W	MAC_INT0_EN	MAC interrupt 0 enable	0
15:13			Reserved	
12	R/W	N2TX_INT_EN	NULL2 frame Tx complete interrupt enable.	0
11	R/W	DTX0_INT_EN	DMA to TX0Q frame transfer complete interrupt enable.	0
10	R/W	DTX1_INT_EN	DMA to TX1Q frame transfer complete interrupt enable.	0
9	R/W	DTX2_INT_EN	DMA to TX2Q frame transfer complete interrupt enable.	0
8	R/W	DRX0_INT_EN	RX0Q to DMA frame transfer complete interrupt enable.	0
7	R/W	HCMD_INT_EN	Host command interrupt enable.	0
6	R/W	NOTX_INT_EN	NULL0 frame Tx complete interrupt enable.	0
5	R/W	N1TX_INT_EN	NULL1 frame Tx complete interrupt enable.	0
4	R/W	BCNTX_INT_EN	Beacon frame Tx complete interrupt enable.	0
3	R/W	MTX0_INT_EN	TX0Q to MAC frame transfer complete interrupt enable.	0
2	R/W	MTX1_INT_EN	TX1Q to MAC frame transfer complete interrupt enable.	0
1	R/W	MTX2_INT_EN	TX2Q to MAC frame transfer complete interrupt enable.	0
0	R/W	MRX0_INT_EN	MAC to RX0Q frame transfer complete interrupt enable.	0

\*This register is only for 8051

#### TX0Q\_IO (offset: 0x041C)

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	TX0Q_IO	TX0Q IO port. This register is used in manual mode.	0

**TX1Q\_IO (offset: 0x0420)**

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	TX1Q_IO	TX1Q IO port. This register is used in manual mode.	0

**TX2Q\_IO (offset: 0x0424)**

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	TX2Q_IO	TX2Q IO port. This register is used in manual mode.	0

**RX0Q\_IO (offset: 0x0428)**

Bits	Type	Name	Description	Init Value
31:16			Reserved	
15:0	R/W	RX0Q_IO	RX0Q IO port. This register is used in manual mode.	0

**BCN\_OFFSET0 (offset: 0x042C0)**

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN3_OFFSET	Beacon #3 address offset in shared memory. Unit is 64 byte.	8'hec
23:16	R/W	BCN2_OFFSET	Beacon #2 address offset in shared memory. Unit is 64 byte.	8'he8
15:8	R/W	BCN1_OFFSET	Beacon #1 address offset in shared memory. Unit is 64 byte.	8'he4
7:0	R/W	BCN0_OFFSET	Beacon #0 address offset in shared memory. Unit is 64 byte.	8'he0

**BCN\_OFFSET1 (offset: 0x0430)**

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN7_OFFSET	Beacon #7 address offset in shared memory. Unit is 64 byte.	8'hfc
23:16	R/W	BCN6_OFFSET	Beacon #6 address offset in shared memory. Unit is 64 byte.	8'hf8
15:8	R/W	BCN5_OFFSET	Beacon #5 address offset in shared memory. Unit is 64 byte.	8'hf4
7:0	R/W	BCN4_OFFSET	Beacon #4 address offset in shared memory. Unit is 64 byte.	8'hf0

**TXRXQ\_STA (offset: 0x0434, default :0x22020202)**

Bits	Type	Name	Description	Init Value
31:24	RO	RX0Q_STA	RxQ status	8'h22
23:16	RO	TX2Q_STA	Tx2Q status	8'h02
15:8	RO	TX1Q_STA	Tx1Q status	8'h02
7:0	RO	TX0Q_STA	Tx0Q status	8'h02

**TXRXQ\_PCNT (offset: 0x0438)**

Bits	Type	Name	Description	Init Value
31:24	RO	RX0Q_PCNT	Page count in RxQ	8'h00
23:16	RO	TX2Q_PCNT	Page count in Tx2Q	8'h00
15:8	RO	TX1Q_PCNT	Page count in Tx1Q	8'h00
7:0	RO	TX0Q_PCNT	Page count in Tx0Q	8'h00

**PBF\_DBG (offset: 0x043C)**

Bits	Type	Name	Description	Init Value
31:8			Reserved	24'h840080
7:0	RO	FREE_PCNT	Free page count	8'hFE

**CAP\_CTRL (offset: 0x0440)**

Bits	Type	Name	Description	Init Value
31	R/W	CAP_ADC_FEQ	Data source. 0: data from the ADC output 1: Data from the FEQ output	0
30	WC	CAP_START	Data capture start	0

			0: No action 1: Start data capture (cleared automatically after capture finished)	
29	W1C	MAN_TRIGGER	Manual capture trigger	0
28:16	R/W	TRIG_OFFSET	Starting address offset before trigger point.	13'h140
15:13			Reserved	
12:0	RO	START_ADDR	Starting address of captured data.	13'h000

### 3.21.3.2 Register Description - MAC (base: 1018.0000)

### 3.21.3.2.1 MAC System configuration registers (offset:0x1000)

MAC\_SYS\_CTRL (offset:0x1004)

**Note:** MAC hard-reset is outside the scope of MAC registers.

#### MAC\_ADDR\_DW0 (offset:0x1008)

Bits	Type	Name	Description	Initial value
31:24	R/W	MAC_ADDR_3	MAC address byte3	0
23:16	R/W	MAC_ADDR_2	MAC address byte2	0
15:8	R/W	MAC_ADDR_1	MAC address byte1	0
7:0	R/W	MAC_ADDR_0	MAC address byte0	0

#### MAC\_ADDR\_DW1 (offset:0x100C)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	MAC_ADDR_5	MAC address byte5	0
7:0	R/W	MAC_ADDR_4	MAC address byte4	0

**Note:** Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

#### MAC\_BSSID\_DW0 (offset:0x1010, default :0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	BSSID_3	BSSID byte3	0
23:16	R/W	BSSID_2	BSSID byte2	0
15:8	R/W	BSSID_1	BSSID byte1	0
7:0	R/W	BSSID_0	BSSID byte0	0

#### MAC\_BSSID\_DW1 (offset: 0x1014, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23	R/W	MULTI_BCN_NUM_BIT3	Multiple BSSID Beacon number (extension bit3) Use together with MULTI_BCN_MUM: (MULTI_BCN_NUM_BIT3 * 8) + MULTI_BCN_MUM = 0: one back-off beacon 1-15: SIFS-burst beacon count	0
22	R/W	MULTI_BSSID_MODE_BIT4	Multiple BSSID mode (extension bit4) Use together with MULTI_BSSID_MODE: (MULTI_BSSID_MODE_BIT4 * 4) + MULTI_BSSID_MODE = 0: 1-BSSID mode 1: 2-BSSID mode 2: 4-BSSID mode 3: 8-BSSID mode 4: 16-BSSID mode	0
21	R/W	NEW_MULTI_BSSID_MODE	New multiple BSSID mode  0: use MAC address Byte5 to distinguish different BSSID  1: use MAC address Byte0 to distinguish different BSSID, New BSSID numbering rule: a. Bit0 of MAC address Byte0 is broadcast/multicast bit. b. Bit1 of MAC address Byte0 is local administration bit and should be set to 1 in extended multiple BSSIDs'. c. Bit4:Bit3 of MAC address Byte0 is extended multiple BSSID index.  For example: in 4-BSSID mode and MAC address is 00:0c:43:28:60:01, by new rule, the extended 3-BSSID is 02:0c:43:28:60:01 and 06:0c:43:28:60:01 and 0a:0c:43:28:60:01.	0
20:18	R/W	MULTI_BCN_NUM	Multiple BSSID Beacon number	0

			0: one back-off beacon 1-7: SIFS-burst beacon count	
17:16	R/W	MULTI_BSSID_MODE	Multiple BSSID mode In multiple-BSSID AP mode, BSSID shall be the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode.  The multiple MAC_ADDR/BSSID are distinguished by [bit2:bit0] of byte5. 0: 1-BSSID mode (BSS index = 0) 1: 2-BSSID mode (byte5.bit0 as BSS index) 2: 4-BSSID mode (byte5.bit1:0 as BSS index) 3: 8-BSSID mode (byte5.bit2:0 as BSS index)	0
15:8	R/W	BSSID_5	BSSID byte5	0
7:0	R/W	BSSID_4	BSSID byte4	0

**Note:** RXINFO bit17 is extension BSS\_INDEX bit 3, it is used together with RXWI BSS\_INDEX bit2:bit0 to represent 16 multiple BSS.

#### MAX\_LEN\_CFG (offset: 0x1018, default: 0x000A\_0FFF)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	MIN_MPDU_LEN	Minimum MPDU length (unit: bytes) MAC will drop the MPDU if the length is less than this limitation. Applied only in MAC RX.	10
15:14	R		Reserved	0
13:12	R/W	MAX_PSDU_LEN	Maximum PSDU length (power factor) 0: $2^{13} = 8K$ bytes 1: $2^{14} = 16K$ bytes 2: $2^{15} = 32K$ bytes 3: $2^{16} = 64K$ bytes  MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC TX.	0
11:0	R/W	MAX_MPDU_LEN	Maximum MPDU length (unit: bytes)  MAC will drop the MPDU if the length is greater than this limitation. Applied only in MAC RX.	4095

#### BBP\_CSR\_CFG (offset: 0x101C, default: 0x0008\_0000)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19	R/W	BBP_RW_MODE	BBP Register R/W mode 1: parallel mode 0: serial mode	1
18	R/W	BBP_PAR_DUR	BBP Register parallel R/W pulse width 0: pulse width = 62.5ns 1: pulse width = 112.5ns  Note: Please set BBP_PAR_DUR=1 in 802.11J mode	0
17	R/W	BBP_CSR_KICK	Write - kick BBP register read/write 0: do nothing 1: kick read/write process Read - Polling BBP register read/write progress 0: idle 1: busy	0
16	R/W	BBP_CSR_RW	0: Write 1: Read	0
15:8	R/W	BBP_ADDR	BBP register ID	0

			0 for R0, 1 for R1, and so on.	
7:0	R/W	BBP_DATA	Write - Data written to BBP Read - Data read from BBP	0

**RF\_CSR\_CFG0** (offset: 0x1020, default: 0x1600\_0000)

Bits	Type	Name	Description	Initial value
31	R/W	RF_REG_CTRL	Write: 1 - RF_REG0/1/2 to RF chip Read: 0 – idle, 1 - busy	0
30	R/W	RF_LE_SEL	RF_LE selection 0:RF_LE0 activate 1:RF_LE1 activate	0
29	R/W	RF_LE_STBY	RF_LE standby mode 0: RF_LE is high when standby 1: RF_LE is low when standby	0
28:24	R/W	RF_REG_WIDTH	RF register bit width	22
23:0	R/W	RF_REG_0	RF register0 ID and content	0

**RF\_CSR\_CFG1** (offset: 0x1024, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	RF_DUR	Gap between BB_CONTROL_RF and RF_LE 0: 3 system clock cycle (37.5usec) 1: 5 system clock cycle (62.5usec)	0
23:0	R/W	RF_REG_1	RF register1 ID and content	0

**RF\_CSR\_CFG2** (offset: 0x1028, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:0	R/W	RF_REG_2	RF register2 ID and content	0

**Note:** Software should make sure the first bit (MSB in the specified bit number) written to RF is 0 for RF chip mode selection.

**LED\_CFG** (offset: 0x102C, default: 0x0003\_1E46)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30	R/W	LED_POL	LED polarity 0: active low 1: active high	0
29:28	R/W	Y_LED_MODE	Yellow LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
27:26	R/W	G_LED_MODE	Green LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
25:24	R/W	R_LED_MODE	Red LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
23:22	R		Reserved	0
21:16	R/W	SLOW_BLK_TIME	Slow blinking period (unit: 1sec)	3
15:8	R/W	LED_OFF_TIME	TX blinking off period (unit: 1ms)	30
7:0	R/W	LED_ON_TIME	TX blinking on period (unit: 1ms)	70

**AMPDU\_MAX\_LEN\_20M1S** (offset: 0x1030, default: 0x7777\_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW20_MCS7	Maximum AMPDU for BW20 MCS7*	7
27:24	R/W	AMPDU_MAX_BW20_MCS6	Maximum AMPDU for BW20 MCS6*	7
23:20	R/W	AMPDU_MAX_BW20_MCS5	Maximum AMPDU for BW20 MCS5*	7
19:16	R/W	AMPDU_MAX_BW20_MCS4	Maximum AMPDU for BW20 MCS4*	7
15:12	R/W	AMPDU_MAX_BW20_MCS3	Maximum AMPDU for BW20 MCS3*	7
11:08	R/W	AMPDU_MAX_BW20_MCS2	Maximum AMPDU for BW20 MCS2*	7
07:04	R/W	AMPDU_MAX_BW20_MCS1	Maximum AMPDU for BW20 MCS1*	7
03:00	R/W	AMPDU_MAX_BW20_MCS0	Maximum AMPDU for BW20 MCS0*	7

Note1\*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K

Note2: The value applied together with 0x1018 MAX\_PSDU\_LEN.

**AMPDU\_MAX\_LEN\_20M2S** (offset: 0x1034, default: 0x7777\_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW20_MCS15	Maximum AMPDU for BW20 MCS15*	7
27:24	R/W	AMPDU_MAX_BW20_MCS14	Maximum AMPDU for BW20 MCS14*	7
23:20	R/W	AMPDU_MAX_BW20_MCS13	Maximum AMPDU for BW20 MCS13*	7
19:16	R/W	AMPDU_MAX_BW20_MCS12	Maximum AMPDU for BW20 MCS12*	7
15:12	R/W	AMPDU_MAX_BW20_MCS11	Maximum AMPDU for BW20 MCS11*	7
11:08	R/W	AMPDU_MAX_BW20_MCS10	Maximum AMPDU for BW20 MCS10*	7
07:04	R/W	AMPDU_MAX_BW20_MCS9	Maximum AMPDU for BW20 MCS9*	7
03:00	R/W	AMPDU_MAX_BW20_MCS8	Maximum AMPDU for BW20 MCS8*	7

Note1\*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K

Note2: The value applied together with 0x1018 MAX\_PSDU\_LEN.

**AMPDU\_MAX\_LEN\_40M1S** (offset: 0x1038, default: 0x7777\_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW40_MCS7	Maximum AMPDU for BW40 MCS7*	7
27:24	R/W	AMPDU_MAX_BW40_MCS6	Maximum AMPDU for BW40 MCS6*	7
23:20	R/W	AMPDU_MAX_BW40_MCS5	Maximum AMPDU for BW40 MCS5*	7
19:16	R/W	AMPDU_MAX_BW40_MCS4	Maximum AMPDU for BW40 MCS4*	7
15:12	R/W	AMPDU_MAX_BW40_MCS3	Maximum AMPDU for BW40 MCS3*	7
11:08	R/W	AMPDU_MAX_BW40_MCS2	Maximum AMPDU for BW40 MCS2*	7
07:04	R/W	AMPDU_MAX_BW40_MCS1	Maximum AMPDU for BW40 MCS1*	7
03:00	R/W	AMPDU_MAX_BW40_MCS0	Maximum AMPDU for BW40 MCS0*	7

Note1\*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K

Note2: The value applied together with 0x1018 MAX\_PSDU\_LEN.

**AMPDU\_MAX\_LEN\_40M2S** (offset: 0x103C, default: 0x7777\_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW40_MCS15	Maximum AMPDU for BW40 MCS15*	7
27:24	R/W	AMPDU_MAX_BW40_MCS14	Maximum AMPDU for BW40 MCS14*	7
23:20	R/W	AMPDU_MAX_BW40_MCS13	Maximum AMPDU for BW40 MCS13*	7
19:16	R/W	AMPDU_MAX_BW40_MCS12	Maximum AMPDU for BW40 MCS12*	7
15:12	R/W	AMPDU_MAX_BW40_MCS11	Maximum AMPDU for BW40 MCS11*	7
11:08	R/W	AMPDU_MAX_BW40_MCS10	Maximum AMPDU for BW40 MCS10*	7
07:04	R/W	AMPDU_MAX_BW40_MCS9	Maximum AMPDU for BW40 MCS9*	7
03:00	R/W	AMPDU_MAX_BW40_MCS8	Maximum AMPDU for BW40 MCS8*	7

Note1\*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K

Note2: The value applied together with 0x1018 MAX\_PSDU\_LEN.

**AMPDU\_MAX\_LEN\_40M2S** (offset: 0x1040, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:07	R	Reserved		0

06	R/W	FORCE_BA_WINSIZE_EN	Enable forced BA window size over BA window size value in TXWI 0: disable, 1: enable	0
05:00	R/W	FORCE_BA_WINSIZE	Forced BA window size	0

TX\_CHAIN\_ADDR0\_L (offset: 0x1044, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_CHAIN_ADDR0_L	Destination MAC address bit31:bit0 of TX chain0	0

TX\_CHAIN\_ADDR0\_H (offset: 0x1048, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	TX_CHAIN_SEL0	Selection value of TX chain0	0
15:0	R/W	TX_CHAIN_ADDR0_H	Destination MAC address bit47:32 of TX chain0	0

TX\_CHAIN\_ADDR1\_L (offset: 0x104C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_CHAIN_ADDR1_L	Destination MAC address bit31:bit0 of TX chain1	0

TX\_CHAIN\_ADDR1\_H (offset: 0x1050, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	TX_CHAIN_SEL1	Selection value of TX chain1	0
15:0	R/W	TX_CHAIN_ADDR1_H	Destination MAC address bit47:32 of TX chain1	0

TX\_CHAIN\_ADDR2\_L (offset: 0x1054, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_CHAIN_ADDR2_L	Destination MAC address bit31:bit0 of TX chain2	0

TX\_CHAIN\_ADDR2\_H (offset: 0x1058, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	TX_CHAIN_SEL2	Selection value of TX chain2	0
15:0	R/W	TX_CHAIN_ADDR2_H	Destination MAC address bit47:32 of TX chain2	0

TX\_CHAIN\_ADDR3\_L (offset: 0x105C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_CHAIN_ADDR3_L	Destination MAC address bit31:bit0 of TX chain3	0

TX\_CHAIN\_ADDR3\_H (offset: 0x1060, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	TX_CHAIN_SEL3	Selection value of TX chain3	0
15:0	R/W	TX_CHAIN_ADDR3_H	Destination MAC address bit47:32 of TX chain3	0

AMPDU\_MAX\_LEN\_20M3S (offset: 0x1064, default: 0x7777\_7777)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW20_MCS23	Maximum AMPDU for BW20 MCS23*	7
27:24	R/W	AMPDU_MAX_BW20_MCS22	Maximum AMPDU for BW20 MCS22*	7
23:20	R/W	AMPDU_MAX_BW20_MCS21	Maximum AMPDU for BW20 MCS21*	7
19:16	R/W	AMPDU_MAX_BW20_MCS20	Maximum AMPDU for BW20 MCS20*	7
15:12	R/W	AMPDU_MAX_BW20_MCS19	Maximum AMPDU for BW20 MCS19*	7
11:08	R/W	AMPDU_MAX_BW20_MCS18	Maximum AMPDU for BW20 MCS18*	7
07:04	R/W	AMPDU_MAX_BW20_MCS17	Maximum AMPDU for BW20 MCS17*	7
03:00	R/W	AMPDU_MAX_BW20_MCS16	Maximum AMPDU for BW20 MCS16*	7

Note1\*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K

Note2: The value applied together with 0x1018 MAX\_PSDU\_LEN.

AMPDU\_MAX\_LEN\_40M3S (offset: 0x1068, default: 0x7777\_7777)

Bits	Type	Name	Description	Initial value
31:0	R/W			

31:28	R/W	AMPDU_MAX_BW40_MCS23	Maximum AMPDU for BW40 MCS23*	7
27:24	R/W	AMPDU_MAX_BW40_MCS22	Maximum AMPDU for BW40 MCS22*	7
23:20	R/W	AMPDU_MAX_BW40_MCS21	Maximum AMPDU for BW40 MCS21*	7
19:16	R/W	AMPDU_MAX_BW40_MCS20	Maximum AMPDU for BW40 MCS20*	7
15:12	R/W	AMPDU_MAX_BW40_MCS19	Maximum AMPDU for BW40 MCS19*	7
11:08	R/W	AMPDU_MAX_BW40_MCS18	Maximum AMPDU for BW40 MCS18*	7
07:04	R/W	AMPDU_MAX_BW40_MCS17	Maximum AMPDU for BW40 MCS17*	7
03:00	R/W	AMPDU_MAX_BW40_MCS16	Maximum AMPDU for BW40 MCS16*	7

Note1\*: **0-2:** 2K bytes, **3:** 4K bytes, **4:** 8K, **5:** 16K, **6:** 32K, **7:** 64K

Note2: The value applied together with 0x1018 MAX\_PSDU\_LEN.

**TX\_WCID\_DROP\_MASK0** (offset: 0x106C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK0-31	Directly drop TX frame of specific WCID Bit0=WCID0, bit1=WCID1,... bit31=WCID31 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x1070, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK32-63	Directly drop TX frame of specific WCID Bit0=WCID32, bit1=WCID33,... bit31=WCID63 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x1074, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK64-95	Directly drop TX frame of specific WCID Bit0=WCID64, bit1=WCID65,... bit31=WCID95 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x1078, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK96-127	Directly drop TX frame of specific WCID Bit0=WCID96, bit1=WCID97,... bit31=WCID127 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x107C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK128-159	Directly drop TX frame of specific WCID Bit0=WCID128, bit1=WCID129,... bit31=WCID159 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x1080, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK160-191	Directly drop TX frame of specific WCID Bit0=WCID160, bit1=WCID161,... bit31=WCID191 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x1084, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK192-223	Directly drop TX frame of specific WCID Bit0=WCID192, bit1=WCID193,... bit31=WCID223 0: disable, 1:enable	0

**TX\_WCID\_DROP\_MASK0** (offset: 0x1088, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK224-255	Directly drop TX frame of specific WCID Bit0=WCID224, bit1=WCID225,... bit31=WCID255 0: disable, 1:enable	0

**TX\_BCN\_BYPASS\_MASK** (offset: 0x108C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R/W		Reserved	0
15:0	R/W	TX_BCN_DROP_MASK0-15	Directly bypass TX Beacon frame of specific Beacon Bit0=1 <sup>st</sup> Beacon, bit1=2 <sup>nd</sup> Beacon,... bit15=16 <sup>th</sup> Beacon 0: disable, 1:enable	0

AP\_CLIENT\_BSSID0\_L (offset: 0x1090, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID0_3	AP client BSSID0 byte3	0
23:16	R/W	APC_BSSID0_2	AP client BSSID0 byte2	0
15:8	R/W	APC_BSSID0_1	AP client BSSID0 byte1	0
7:0	R/W	APC_BSSID0_0	AP client BSSID0 byte0	0

AP\_CLIENT\_BSSID0\_H (offset: 0x1094, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	APC_BSSID_EN	Enable AP client mode (occupy BSSIDX8-16 of multiple BSSID mode) 0: disable, 1:enable	0
15:8	R/W	APC_BSSID0_5	AP client BSSID0 byte5	0
7:0	R/W	APC_BSSID0_4	AP client BSSID0 byte4	0

AP\_CLIENT\_BSSID1\_L (offset: 0x1098, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID1_3	AP client BSSID1 byte3	0
23:16	R/W	APC_BSSID1_2	AP client BSSID1 byte2	0
15:8	R/W	APC_BSSID1_1	AP client BSSID1 byte1	0
7:0	R/W	APC_BSSID1_0	AP client BSSID1 byte0	0

AP\_CLIENT\_BSSID1\_H (offset: 0x109C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID1_5	AP client BSSID1 byte5	0
7:0	R/W	APC_BSSID1_4	AP client BSSID1 byte4	0

AP\_CLIENT\_BSSID2\_L (offset: 0x10A0, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID2_3	AP client BSSID2 byte3	0
23:16	R/W	APC_BSSID2_2	AP client BSSID2 byte2	0
15:8	R/W	APC_BSSID2_1	AP client BSSID2 byte1	0
7:0	R/W	APC_BSSID2_0	AP client BSSID2 byte0	0

AP\_CLIENT\_BSSID2\_H (offset: 0x10A4, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID2_5	AP client BSSID2 byte5	0
7:0	R/W	APC_BSSID2_4	AP client BSSID2 byte4	0

AP\_CLIENT\_BSSID3\_L (offset: 0x10A8, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID3_3	AP client BSSID3 byte3	0
23:16	R/W	APC_BSSID3_2	AP client BSSID3 byte2	0
15:8	R/W	APC_BSSID3_1	AP client BSSID3 byte1	0
7:0	R/W	APC_BSSID3_0	AP client BSSID3 byte0	0

**AP\_CLIENT\_BSSID3\_H** (offset: 0x10AC, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID3_5	AP client BSSID3 byte5	0
7:0	R/W	APC_BSSID3_4	AP client BSSID3 byte4	0

**AP\_CLIENT\_BSSID4\_L** (offset: 0x10B0, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID4_3	AP client BSSID4 byte3	0
23:16	R/W	APC_BSSID4_2	AP client BSSID4 byte2	0
15:8	R/W	APC_BSSID4_1	AP client BSSID4 byte1	0
7:0	R/W	APC_BSSID4_0	AP client BSSID4 byte0	0

**AP\_CLIENT\_BSSID4\_H** (offset: 0x10B4, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID4_5	AP client BSSID4 byte5	0
7:0	R/W	APC_BSSID4_4	AP client BSSID4 byte4	0

**AP\_CLIENT\_BSSID5\_L** (offset: 0x10B8, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID5_3	AP client BSSID5 byte3	0
23:16	R/W	APC_BSSID5_2	AP client BSSID5 byte2	0
15:8	R/W	APC_BSSID5_1	AP client BSSID5 byte1	0
7:0	R/W	APC_BSSID5_0	AP client BSSID5 byte0	0

**AP\_CLIENT\_BSSID5\_H** (offset: 0x10BC, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID5_5	AP client BSSID5 byte5	0
7:0	R/W	APC_BSSID5_4	AP client BSSID5 byte4	0

**AP\_CLIENT\_BSSID6\_L** (offset: 0x10C0, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID6_3	AP client BSSID6 byte3	0
23:16	R/W	APC_BSSID6_2	AP client BSSID6 byte2	0
15:8	R/W	APC_BSSID6_1	AP client BSSID6 byte1	0
7:0	R/W	APC_BSSID6_0	AP client BSSID6 byte0	0

**AP\_CLIENT\_BSSID6\_H** (offset: 0x10C4, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID6_5	AP client BSSID6 byte5	0
7:0	R/W	APC_BSSID6_4	AP client BSSID6 byte4	0

**AP\_CLIENT\_BSSID7\_L** (offset: 0x10C8, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID7_3	AP client BSSID7 byte3	0
23:16	R/W	APC_BSSID7_2	AP client BSSID7 byte2	0
15:8	R/W	APC_BSSID7_1	AP client BSSID7 byte1	0
7:0	R/W	APC_BSSID7_0	AP client BSSID7 byte0	0

**AP\_CLIENT\_BSSID7\_H** (offset: 0x10CC, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID7_5	AP client BSSID7 byte5	0
7:0	R/W	APC_BSSID7_4	AP client BSSID7 byte4	0

**BT\_WINDOW\_CFG** (offset: 0x10D0, default: 0x04E2\_00FA)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26:16	R/W	BT_WIN_SIZE	Bluetooth slot window size for Bluetooth slot phase tracking (unit: usec)	1250
15:11	R		Reserved	0
10:0	R/W	PRE_BT_WIN_SIZE	Pre-Bluetooth slot window size (unit: usec) Pre-Bluetooth slot window will block WLAN TX	250

BT\_COEX\_CFG (offset: 0x10D4, default: 0x0010\_D3FF)

Bits	Type	Name	Description	Initial value
31:22	R		Reserved	0
21:16	R/W	BT_RPI_WIN_SIZE	Bluetooth priority indication window in 3-wire/4-wire mode (unit: usec)	16
15:8	R/W	WLAN_BT_DIS	WLAN high priority event (higher priority than Bluetooth) Bit8: non-Beacon TX event Bit9: Beacon TX event Bit10: RX event Bit11: ACK RX event Bit12: ACK TX event Bit13: CTS TX event Bit14: implicit BA TX event Bit15: explicit BA TX event	0xD3
7:0	R/W	WLAN_BT_EN	Truth table of Bluetooth halt WLAN activity condition {BT_AUX_IN, BT_HIGH_PRIORITY, BT_TX_STATE}	0xFF

### 3.21.3.2.2 MAC Timing Control Registers (offset:0x1100)

XIFS\_TIME\_CFG (offset:0x1100)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	
29	R/W	BB_RXEND_EN	BB_RX_END signal enable Refer BB_RX_END signal from BBP RX logic to start SIFS defer. 0: disable 1: enable	1
28:20	R/W	EIFS_TIME	EIFS time (unit: 1us) EIFS is the defer time after reception of a CRC error packet. After deferring EIFS, the normal back-off process may proceed.	314
19:16	R/W	OFDM_XIFS_TIME	Delayed OFDM SIFS time compensator (unit: 1us) When BB_RX_END from BBP is a delayed version the SIFS deferred will be (OFDM_SIFS_TIME - OFDM_XIFS_TIME)	4
15:8	R/W	OFDM_SIFS_TIME	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_TIME	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note1: EIFS = SIFS + ACK @ 1Mbps + DIFS = 10us (SIFS) + 192us (long preamble) + 14\*8us (ACK) + 50us (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).

Note2: EIFS is not applied if MAC is a TXOP initiator that owns the channel.

Note3: EIFS is not started if AMPDU is only partial corrupted.

**Caution:** It is recommended that both (CCK\_SIFS\_TIME) and (OFDM\_SIFS\_TIME) are no less than TX/RX transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst one.

BKOFF\_SLOT\_CFG (offset:0x1104, default : 0x0000\_0214)

Bits	Type	Name	Description	Initial value
31:12	R/W		Reserved	
11:8	R/W	CC_DELAY_TIME	Channel clear delay (unit: 1-us) This value specifies TX guard time after channel is clear.	2
7:0	R/W	SLOT_TIME	Slot time (unit: 1-us) This value specifies the slot boundary after deferring SIFS time. Note: Default 20us is for 11b/g. 11a and 11g-short-slot-mode is 9us.	20

NAV\_TIME\_CFG (offset:0x1108, default : 0x0000\_8000)

Bits	Type	Name	Description	Initial value
31	WC	NAV_UPD	NAV timer manual update command 0: Do nothing 1: Update NAV timer with NAV_UPD_VAL	0
30:16	R/W	NAV_UPD_VAL	NAV timer manual update value (unit: 1us)	0
15	R/W	NAV_CLR_EN	NAV timer auto-clear enable When enabled, MAC will auto clear NAV timer after the reception of CF-End frame from previous NAV holder STA. 0: disable 1: enable	1
14:0	R	NAV_TIMER	NAV timer (unit: 1us) The timer is set by other STA and will auto countdown to zero. The STA who set the NAV timer is called the NAV holder. When NAV timer is nonzero, MAC will not send any packet.	0

**CH\_TIME\_CFG** (offset:0x110C, default: 0x0000\_001E)

Bits	Type	Name	Description	Initial value
31:5	R		Reserved	0
4	R/W	EIFS_AS_CH_BUSY	Count EIFS as channel busy 0: disable 1: enable	1
3	R/W	NAV_AS_CH_BUSY	Count NAV as channel busy 0: disable 1: enable	1
2	R/W	RX_AS_CH_BUSY	Count RX busy as channel busy 0: disable 1: enable	1
1	R/W	TX_AS_CH_BUSY	Count TX busy as channel busy 0: disable 1: enable	1
0	R/W	CH_STA_TIMER_EN	Channel statistic timer enable 0: disable 1: enable	0

**PBF\_LIFE\_TIMER** (offset:0x1110, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R	PBF_LIFE_TIMER	TX/RX MPDU timestamp timer (free run) Unit: 1us	0

**BCN\_TIME\_CFG** (offset:0x1114, default: 0x000000640)

Bits	Type	Name	Description	Initial value
31:24	R/W	TSF_INS_COMP	TSF insertion compensation value (unit: 1us) When inserting TSF, add this value with local TSF timer as the TX timestamp.	0
23:21	R		Reserved	0
20	R/W	BCN_TX_EN	BEACON frame TX enable When enabled, MAC sends BEACON frame at TBTT interrupt. 0: disable 1: enable	0
19	R/W	TBTT_TIMER_EN	TBTT timer enable When enabled, TBTT interrupt will be issued periodically with period specified in (BCN_INTVAL). 0: disable 1: enable	0
18:17	R/W	TSF_SYNC_MODE	Local 64-bit TSF timer synchronization mode 00: disable 01: (STA infra-structure mode) Upon the reception of BEACON frame from associated BSS, local TSF is always updated with remote TSF. 10: (STA ad-hoc mode) Upon the reception of BEACON frame from associated BSS, local TSF is updated with remote TSF only if the remote TSF is greater than local TSF. 11: (AP mode) SYNC with nobody	0
16	R/W	TSF_TIMER_EN	Local 64-bit TSF timer enable When enabled, TSF timer will re-start from zero.	0

			0: disable 1: enable	
15:0	R/W	BCN_INTVAL	BEACON interval (unit: 64us) This value specified the interval between Maximum beacon interval is about 4sec.	1600

**TBTT\_SYNC\_CFG (offset:0x1118, default: 0x0042\_2010)**

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:20	R/W	BCN_CWMIN	Beacon transmission CWMIN after TBTT interrupt (unit: slot)	4
19:16	R/W	BCN_AIFSN	Beacon transmission AIFSN after TBTT interrupt (unit: slot)	2
15:8	R/W	BCN_EXP_WIN	Beacon expecting window duration (unit: 64us) The window starts from TBTT interrupt. The phase of "TBTT interrupt train" will NOT be adjusted by the beacon arrived within the window.	32
7:0	R/W	TBTT_ADJUST	IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us.  In IBSS mode (Ad hoc), if consecutive TX beacon failures (or consecutive success) happened, TBTT timer will adjust its phase to meet the external Ad hoc TBTT time.	16

**TSF\_TIMER\_DW0 (offset:0x111C, default: 0x0000\_0000)**

Bits	Type	Name	Description	Initial value
31:0	R	TSF_TIMER_DW0	Local TSF timer LSB 32 bits (unit: 1us)	0

**TSF\_TIMER\_DW1 (offset:0x1120, default: 0x0000\_0000)**

Bits	Type	Name	Description	Initial value
31:0	R	TSF_TIMER_DW1	Local TSF timer MSB 32 bits (unit: 1us)	0

**TBTT\_TIMER (offset:0x1124, default: 0x0000\_0000)**

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16:0	R	TBTT_TIMER	TBTT Timer (unit: 32us) The time remains till next TBTT.  When TBTT_TIMER_EN is enabled, the timer will down count from BCN_INTVAL to zero.  When TBTT_TIMER_EN is disabled, the timer will stay in zero.	0

**INT\_TIMER\_CFG (offset:0x1128, default: 0x0000\_0320)**

Bits	Type	Name	Description	Initial value
31:16	R/W	GP_TIMER	Period of general purpose interrupt timer (Unit: 64us)	0
15:0	R/W	PRE_TBTT_TIMER	Pre-TBTT interrupt time (unit: 64us) The value specified the interrupt timing before TBTT interrupt.	0

**INT\_TIMER\_EN (offset:0x112C, default: 0x0000\_0000)**

Bits	Type	Name	Description	Initial value
31:2	R		Reserved	0
1	R/W	GP_TIMER_EN	Periodic general purpose interrupt timer enable 0: disable 1: enable	0
0	R/W	PRE_TBTT_INT_EN	Pre-TBTT interrupt enable 0: disable 1: enable	0

**CH\_IDLE\_STA (offset:0x1130, default: 0x0000\_0000)**

Bits	Type	Name	Description	Initial value
31:0	RC	CH_IDLE_TIME	Channel idle time (unit: 1us)	0

In application, the channel busy time can be derived by the equation:

$$\text{CH_BUSY\_TIME} = \text{host polling period} - \text{CH_IDLE\_TIME}$$

**CH\_BUSY\_STA (offset:0x1134, default: 0x0000\_0000)**

Bits	Type	Name	Description	Initial value
31:0	RC	CH_BUSY_TIME	Channel busy time (unit: 1us)	0

**EXT\_CH\_BUSY\_STA** (offset:0x1138, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	RC	EXT_CH_BUSY_TIME	Extension Channel busy time (unit: 1us)	0

**BBP\_IPI\_TIMER** (offset:0x113C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	BBP_IPI_KICK	Write 1: Kick-off the measurement of BBP IPI Read 1: BBP IPI enabled, 0: BBP IPI disabled	0
15:0	R/W	BBP_IPI_TIMER	Measurement period of BBP IPI (unit: 1.024ms)	0

**ED\_CCA\_TIMER** (offset:0x1140, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	RC	ED_CCA_TIME	Energy detection CCA busy time (unit: 1us)	0

### 3.21.3.2.3 MAC Power save configuration registers (offset:0x1200)

**MAC\_STATUS\_REG** (offset:0x1200, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:2	R		Reserved	0
1	R	RX_STATUS	RX status 0: Idle 1: Busy	0
0	R	TX_STATUS	TX status 0: Idle 1: Busy	0

**PWR\_PIN\_CFG** (offset:0x1204, default: 0x0000\_000A)

Bits	Type	Name	Description	Initial value
31:4	R		Reserved	0
3	R/W	IO_ADDA_PD	AD/DA power down	1
2	R/W	IO_PLL_PD	PLL power down	0
1	R/W	IO_RA_PE	RA_PE	1
0	R/W	IO_RF_PE	RF_PE	0

**AUTO\_WAKEUP\_CFG** (offset:0x1208, default: 0x0000\_0014)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15	R/W	AUTO_WAKEUP_EN	Auto wakeup interrupt enable Auto wakeup interrupt will be issued after #(SLEEP_TBTT_NUM) TBTTs' at WAKEUP_LEAD_TIME before the target TBTT. 0: disable 1: enable Note: Please make sure TBTT_TIMER_EN is enabled.	0
14:8	R/W	SLEEP_TBTT_NUM	Number of sleeping TBTT	0
7:0	R/W	WAKEUP_LEAD_TIME	Auto wakeup lead time (unit: 1TU=1024us)	20

**AUX\_CLK\_EN** (offset:0x120C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:1	R		Reserved	0
0	R/W	AUX_CLK_EN	Enable slow clock for powersave period 0: disable, 1:enable	0

**MIMO\_PWSRV\_CFG** (offset:0x1210, default: 0x0000\_0004)

Bits	Type	Name	Description	Initial value
31:6	R		Reserved	0
5	R/W	MMPS_RF2_POL	MIMO power save RF2 standby signal polarity 0: high active, 1: low active	0
4	R/W	MMPS_RF1_POL	MIMO power save RF1 standby signal polarity 0: high active, 1: low active	0
3	R/W	MMPS_RF_EN	MIMO power save RF part enable 0: disable, 1: enable	0
2:1	R/W	MMPS_BBP_RX_ANT	MIMO power save RX antenna default number 0: 1R 1: 2R 2: 3R 3: reserved	2
0	R/W	MMPS_BBP_EN	MIMO power save BBP enable 0: disable, 1: enable	0

**3.21.3.2.4 MAC TX configuration registers (offset: 0x1300)**
**EDCA\_AC0\_CFG (BE) (offset: 0x1300, default: 0x0007\_3200)**

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC0_CWMAX	AC0 CWMAX (unit: power of 2)	7
15:12	R/W	AC0_CWMIN	AC0 CWMIN (unit: power of 2)	3
11:8	R/W	AC0_AIFSN	AC0 AIFSN (unit: # of slot time)	2
7:0	R/W	AC0_TXOP	AC0 TXOP limit (unit: 32us)	0

**EDCA\_AC1\_CFG (BK) (offset: 0x1304, default: 0x0007\_3200)**

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC1_CWMAX	AC1 CWMAX (unit: power of 2)	7
15:12	R/W	AC1_CWMIN	AC1 CWMIN (unit: power of 2)	3
11:8	R/W	AC1_AIFSN	AC1 AIFSN (unit: # of slot time)	2
7:0	R/W	AC1_TXOP	AC1 TXOP limit (unit: 32us)	0

**EDCA\_AC2\_CFG (VI) (offset: 0x1308, default: 0x0007\_3200)**

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC2_CWMAX	AC2 CWMAX (unit: power of 2)	7
15:12	R/W	AC2_CWMIN	AC2 CWMIN (unit: power of 2)	3
11:8	R/W	AC2_AIFSN	AC2 AIFSN (unit: # of slot time)	2
7:0	R/W	AC2_TXOP	AC2 TXOP limit (unit: 32us)	0

**EDCA\_AC3\_CFG (VO) (offset: 0x130C, default: 0x0007\_3200)**

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC3_CWMAX	AC3 CWMAX (unit: power of 2)	7
15:12	R/W	AC3_CWMIN	AC3 CWMIN (unit: power of 2)	3
11:8	R/W	AC3_AIFSN	AC3 AIFSN (unit: # of slot time)	2
7:0	R/W	AC3_TXOP	AC3 TXOP limit (unit: 32us)	0

**EDCA\_TID\_AC\_MAP (offset: 0x1310, default: 0000\_FA14)**

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:14	R/W	TID7_AC_MAP	AC value as TID=7	3
13:12	R/W	TID6_AC_MAP	AC value as TID=6	3
11:10	R/W	TID5_AC_MAP	AC value as TID=5	2
9:8	R/W	TID4_AC_MAP	AC value as TID=4	2
7:6	R/W	TID3_AC_MAP	AC value as TID=3	0
5:4	R/W	TID2_AC_MAP	AC value as TID=2	1
3:2	R/W	TID1_AC_MAP	AC value as TID=1	1
1:0	R/W	TID0_AC_MAP	AC value as TID=0	0

Note: default according 802.11e Table 20.23—User priority to Access Category mappings

**TX\_PWR\_CFG\_0 (offset: 0x1314, default: 0x6666\_6666)**

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_OFDM_12	TX power for OFDM 12M/18M	0x66
23:16	R/W	TX_PWR_OFDM_6	TX power for OFDM 6M/9M	0x66
15:8	R/W	TX_PWR_CCK_5	TX power for CCK5.5M/11M	0x66
7:0	R/W	TX_PWR_CCK_1	TX power for CCK1M/2M	0x66

**TX\_PWR\_CFG\_0\_EXT (offset: 0x1390, default: 0x0606\_0606)**

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_OFDM_12	TX power for OFDM 12M/18M (extension)	0x06
23:16	R/W	TX_PWR_OFDM_6	TX power for OFDM 6M/9M (extension)	0x06
15:8	R/W	TX_PWR_CCK_5	TX power for CCK5.5M/11M (extension)	0x06
7:0	R/W	TX_PWR_CCK_1	TX power for CCK1M/2M (extension)	0x06

**TX\_PWR\_CFG\_1** (offset: 0x1318, default: 0x6666\_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_2	TX power for HT MCS=2,3	0x66
23:16	R/W	TX_PWR_MCS_0	TX power for HT MCS=0,1	0x66
15:8	R/W	TX_PWR_OFDM_48	TX power for OFDM 48M	0x66
7:0	R/W	TX_PWR_OFDM_24	TX power for OFDM 24M/36M	0x66

**TX\_PWR\_CFG\_1\_EXT** (offset: 0x1394, default: 0x0606\_0606)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_2	TX power for HT MCS=2,3 (extension)	0x06
23:16	R/W	TX_PWR_MCS_0	TX power for HT MCS=0,1 (extension)	0x06
15:8	R/W	TX_PWR_OFDM_48	TX power for OFDM 48M (extension)	0x06
7:0	R/W	TX_PWR_OFDM_24	TX power for OFDM 24M/36M (extension)	0x06

**TX\_PWR\_CFG\_2** (offset: 0x131C, default: 0x6666\_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_10	TX power for HT MCS=10,11	0x66
23:16	R/W	TX_PWR_MCS_8	TX power for HT MCS=8,9	0x66
15:8	R/W	TX_PWR_MCS_6	TX power for HT MCS=6	0x66
7:0	R/W	TX_PWR_MCS_4	TX power for HT MCS=4,5	0x66

**TX\_PWR\_CFG\_2\_EXT** (offset: 0x1398, default: 0x0606\_0606)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_MCS_10	TX power for HT MCS=10,11 (extension)	0x06
23:16	R/W	TX_PWR_MCS_8	TX power for HT MCS=8,9 (extension)	0x06
15:8	R/W	TX_PWR_MCS_6	TX power for HT MCS=6,7 (extension)	0x06
7:0	R/W	TX_PWR_MCS_4	TX power for HT MCS=4,5 (extension)	0x06

**TX\_PWR\_CFG\_3** (offset: 0x1320, default: 0x6666\_6666)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_STBC_2	TX power for STBC MCS=2, 3	0x66
23:16	R/W	TX_PWR_STBC_0	TX power for STBC MCS=0, 1	0x66
15:8	R/W	TX_PWR_MCS_14	TX power for HT MCS=14	0x66
7:0	R/W	TX_PWR_MCS_12	TX power for HT MCS=12,13	0x66

**TX\_PWR\_CFG\_3\_EXT** (offset: 0x139C, default: 0x0606\_0606)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_PWR_STBC_2	TX power for STBC MCS=2, 3 (extension)	0x06
23:16	R/W	TX_PWR_STBC_0	TX power for STBC MCS=0, 1 (extension)	0x06
15:8	R/W	TX_PWR_MCS_14	TX power for HT MCS=14 (extension)	0x06
7:0	R/W	TX_PWR_MCS_12	TX power for HT MCS=12,13 (extension)	0x06

**TX\_PWR\_CFG\_4** (offset: 0x1324, default: 0x0000\_6666)

Bits	Type	Name	Description	Initial value
31:16	R	Reserved		0
15:8	R/W	TX_PWR_STBC_6	TX power for STBC MCS=6	0x66
7:0	R/W	TX_PWR_STBC_4	TX power for STBC MCS=4, 5	0x66

**TX\_PWR\_CFG\_4\_EXT** (offset: 0x13A0, default: 0x0000\_0606)

Bits	Type	Name	Description	Initial value
31:16	R	Reserved		0
15:8	R/W	TX_PWR_STBC_6	TX power for STBC MCS=6 (extension)	0x06
7:0	R/W	TX_PWR_STBC_4	TX power for STBC MCS=4, 5 (extension)	0x06

**TX\_PWR\_CFG\_5** (offset: 0x1384, default: 0x0666\_0666)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	0
27:16	R/W	TX_PWR_MCS_18	TX power for HT MCS=18, 19	0x666
15:12	R		Reserved	0
11:0	R/W	TX_PWR_MCS_16	TX power for HT MCS=16, 17	0x666

**TX\_PWR\_CFG\_6** (offset: 0x1388, default: 0x0666\_0666)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	0
27:16	R/W	TX_PWR_MCS_22	TX power for HT MCS=22	0x666
15:12	R		Reserved	0
11:0	R/W	TX_PWR_MCS_20	TX power for HT MCS=21, 20	0x666

TX\_PWR\_CFG\_7 (offset: 0x13D4, default: 0x0666\_0666)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	0
27:16	R/W	TX_PWR_MCS_7	TX power for HT MCS=7	0x666
15:12	R		Reserved	0
11:0	R/W	TX_PWR_OFDM_54	TX power for OFDM 54	0x666

TX\_PWR\_CFG\_8 (offset: 0x13D8, default: 0x0666\_0666)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	0
27:16	R/W	TX_PWR_MCS_23	TX power for HT MCS=23	0x666
15:12	R		Reserved	0
11:0	R/W	TX_PWR_MCS_15	TX power for HT MCS=15	0x666

TX\_PWR\_CFG\_8 (offset: 0x13DC, default: 0x0666\_0666)

Bits	Type	Name	Description	Initial value
31:12	R		Reserved	0
11:0	R/W	TX_PWR_STBC_7	TX power for STBC MCS=7	0x666

TX\_PIN\_CFG (offset: 0x1328, default: 0x3305\_0F0F)

Bits	Type	Name	Description	Initial value
31	R/W	LNA_PE_G2_POL	LNA_PE_G2 polarity	0
30	R/W	LNA_PE_A2_POL	LNA_PE_A2 polarity	0
29	R/W	LNA_PE_G2_EN	LNA_PE_G2 enable	1
28	R/W	LNA_PE_A2_EN	LNA_PE_A2 enable	1
27	R/W	PA_PE_G2_POL	PA_PE_G2 polarity	0
26	R/W	PA_PE_A2_POL	PA_PE_A2 polarity	0
25	R/W	PA_PE_G2_EN	PA_PE_G2 enable	1
24	R/W	PA_PE_A2_EN	PA_PE_A2 enable	1
23:20	R	Reserved		0
19	R/W	TRSW_POL	TRSW_EN polarity	0
18	R/W	TRSW_EN	TRSW_EN enable	1
17	R/W	RFTR_POL	RF_TR polarity	0
16	R/W	RFTR_EN	RF_TR enable	1
15	R/W	LNA_PE_G1_POL	LNA_PE_G1 polarity	0
14	R/W	LNA_PE_A1_POL	LNA_PE_A1 polarity	0
13	R/W	LNA_PE_G0_POL	LNA_PE_G0 polarity	0
12	R/W	LNA_PE_A0_POL	LNA_PE_A0 polarity	0
11	R/W	LNA_PE_G1_EN	LNA_PE_G1 enable	1
10	R/W	LNA_PE_A1_EN	LNA_PE_A1 enable	1
9	R/W	LNA_PE_G0_EN	LNA_PE_G0 enable	1
8	R/W	LNA_PE_A0_EN	LNA_PE_A0 enable	1
7	R/W	PA_PE_G1_POL	PA_PE_G1 polarity	0
6	R/W	PA_PE_A1_POL	PA_PE_A1 polarity	0
5	R/W	PA_PE_G0_POL	PA_PE_G0 polarity	0
4	R/W	PA_PE_A0_POL	PA_PE_A0 polarity	0
3	R/W	PA_PE_G1_EN	PA_PE_G1 enable	1
2	R/W	PA_PE_A1_EN	PA_PE_A1 enable	1
1	R/W	PA_PE_G0_EN	PA_PE_G0 enable	1
0	R/W	PA_PE_A0_EN	PA_PE_A0 enable	1

TX\_BAND\_CFG (offset: 0x132C, default: 0x0000\_0004)

Bits	Type	Name	Description	Initial value
------	------	------	-------------	---------------

31:3	R	Reserved		0
2	R/W	5G_BAND_SEL_N	5G band selection PIN (complement of 5G_BAND_SEL_P)	1
1	R/W	5G_BAND_SEL_P	5G band selection PIN	0
0	R/W	TX_BAND_SEL	0: use lower 40Mhz band in 20Mhz TX 1: use upper 40Mhz band in 20Mhz TX	0

Note1: TX\_BAND\_SEL is effective only when TX/RX bandwidth control register R4 of BBP is set to 40Mhz.

#### TX\_SW\_CFG0 (offset: 0x1330, default: 0x0004\_080C)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_RFTR_EN	Delay of RF_TR assertion	0x0
23:16	R/W	DLY_TRSW_EN	Delay of TR_SW assertion	0x4
15:8	R/W	DLY_PAPE_EN	Delay of PA_PE assertion	0x8
7:0	R/W	DLY_TXPE_EN	Delay of TX_PE assertion	0xC

Note1: The timing unit is 0.25us.

Note2: SIFS\_TIME should compensate with DLY\_TXPE\_EN.

#### TX\_SW\_CFG1 (offset: 0x1334, default: 0x000C\_0808)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:16	R/W	DLY_RFTR_DIS	Delay of RF_TR de-assertion	0xC
15:8	R/W	DLY_TRSW_DIS	Delay of TR_SW de-assertion	0x8
7:0	R/W	DLY_PAPE_DIS	Delay of PA_PE de-assertion	0x8

Note1: The timing unit is 0.25us.

Note2: The delay is started from TX\_END event of BBP.

Note3: TX\_PE is de-asserted automatically as last data byte passed to BBP.

#### TX\_SW\_CFG2 (offset: 0x1338, default: 0x000C\_0408)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_LNA_EN	Delay of LNA* assertion	0x0
23:16	R/W	DLY_LNA_DIS	Delay of LNA* de-assertion	0xC
15:8	R/W	DLY_DAC_EN	Delay of DAC_PE assertion	0x4
7:0	R/W	DLY_DAC_DIS	Delay of DAC_PE de-assertion	0x8

Note1: The timing unit is 0.25us.

Note 2: LNA\* includes LNA\_A0, LNA\_A1, LNA\_G0, LNA\_G1.

#### TXOP\_THRES\_CFG (offset: 0x133C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_Rem_Thres	Remaining TXOP threshold, unit: 32us As the remaining TXOP is less than the threshold, the TXOP is passed silently.	0
23:16	R/W	CF_End_Thres	CF-END threshold, unit: 32us As the remaining TXOP is greater than the threshold, the CF-END will be send to release the remaining TXOP reserved by long NAV. Set 0xFF to disable CF-END transmission.	0
15:8	R/W	RDG_In_Thres	RX RDG threshold, unit: 32us As the remaining TXOP (specified in the duration field of the RX frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used.	0
7:0	R/W	RDG_Out_Thres	TX RDG threshold, unit: 32us As the remaining TXOP is greater than or equal to the threshold, RDG in the TX frame may be set to one.	0

#### TXOP\_CTRL\_CFG (offset: 0x1340, default: 0x0000\_243F)

Bits	Type	Name	Description	Initial value
31:21	R		Reserved	0
20	R/W	ED_CCA_EN	Energy detection CCA enable	0

			When ED_CCA_EN is enabled, the activity in overlapping neighbor channel will defer MAC transmission. 0: disable, 1: enable	
19:16	R/W	EXT_CW_MIN	Cwmin for extension channel backoff When EXT_CCA_EN is enabled, 40Mhz transmission will be suppressed to 20Mhz if the extension CCA is busy or extension channel backoff is not finished. Default: Cwmin=0, disable.	0
15:8	R/W	EXT_CCA_DLY	Extension CCA signal delay time (unit: usec) Create delayed version of extension CCA signal reference time for extension channel IFS. Default: (ofdm SIFS) + (long slot time) = 16+20 = 36 (us)	36
7	R/W	EXT_CCA_EN	Extension CCA reference enable When transmit in 40Mhz mode, defer until extension CCA is also clear. 0: disable 1: enable	0
6	R/W	LSIG_TXOP_EN	L-SIG TXOP protection enable Extension of mix mode L-SIG protection range to following ACK/CTS.	0
5:0	R/W	TXOP_TRUN_EN	TXOP truncation enable Bit5: reserved Bit4: truncation for MIMO power save RTS/CTS Bit3: truncation for user TXOP mode Bit2: truncation for TX rate group change Bit1: truncation for AC change Bit0: TXOP timeout truncation 0: disable 1: enable	0x3F

**TX\_RTS\_CFG (offset: 0x1344, default: 0x00FF\_FF07)**

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
24	R/W	RTS_FBK_EN	RTS rate fallback enable	0
23:8	R/W	RTS_THRES	RTS threshold (unit: byte)  MPDU or AMPDU with length greater than RTS threshold will be protected with RTS/CTS exchange at the beginning of the TXOP.	65535
7:0	R/W	RTS_RTY_LIMIT	Auto RTS retry limit	7

**TX\_TIMEOUT\_CFG (offset: 0x1348, default: 0x010F\_0A90)**

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	ACKTO_END_TXOP	Truncate TXOP once ACK is failed to return 0: disable, 1: enable	1
23:16	R/W	TXOP_TIMEOUT	TXOP timeout value for TXOP truncation (Unit: us)  Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	15
15:8	R/W	RX_ACK_TIMEOUT	RX ACK/CTS timeout value for TX procedure (Unit: us)  Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	10
7:4	R/W	MPDU_LIFE_TIME	TX MPDU expiration time Expiration time = $2^{(9+MPDU\_LIFE\_TIME)}$ us Default value is $2^{(9+9)} \approx 256$ ms	9
3:0	R/W		Reserved	0

**TX\_RTY\_CFG (offset: 0x134C, default: 0x6BB8\_0407)**

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30	R/W	TX_AUTOFB_EN	TX retry PHY rate auto fallback enable 0: disable 1: enable	1
29	R/W	AGG_RTY_MODE	Aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	1
28	R/W	NAG_RTY_MODE	Non-aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	0
27:16	R/W	LONG_RTY_THRES	Long retry threshold MPDU with length over this threshold is applied with long retry limit.	3000
15:8	R/W	LONG_RTY_LIMIT	Long retry limit	4
7:0	R/W	SHORT_RTY_LIMIT	Short retry limit	7

TX\_LINK\_CFG (offset: 0x1350, default: 0x007f\_0020)

Bits	Type	Name	Description	Initial value
31:24	R	REMOTE_MFS	Remote MCS feedback sequence number	*
23:16	R	REMOTE_MFB	Remote MCS feedback	0x7F
15:13	R		Reserved	0
12	R/W	TX_CFACK_EN	Piggyback CF-ACK enable 0: disable 1: enable	0
11	R/W	TX_RDG_EN	RDG TX enable 0: disable 1: enable	0
10	R/W	TX_MRQ_EN	MCS request TX enable 0: disable 1: enable	0
9	R/W	REMOTE_UMFS_EN	Remote un-solicit MFB enable 0: do not apply remote un-solicit MFB (MFS=7) 1: apply un-solicit MFB	0
8	R/W	TX_MFB_EN	TX apply remote MFB 0: disable 1: enable	0
7:0	R/W	REMOTE_MFB_LITETIME	Remote MFB life time Unit: 32us	32

HT\_FBK\_CFG0 (offset: 0x1354, default: 0x6543\_2100)

Bits	Type	Name	Description	Initial value
31:28	R/W	HT_MCS7_FBK	Auto fall back MCS as HT MCS =7	6
27:24	R/W	HT_MCS6_FBK	Auto fall back MCS as HT MCS =6	5
23:20	R/W	HT_MCS5_FBK	Auto fall back MCS as HT MCS =5	4
19:16	R/W	HT_MCS4_FBK	Auto fall back MCS as HT MCS =4	3
15:12	R/W	HT_MCS3_FBK	Auto fall back MCS as HT MCS =3	2
11:8	R/W	HT_MCS2_FBK	Auto fall back MCS as HT MCS =2	1
7:4	R/W	HT_MCS1_FBK	Auto fall back MCS as HT MCS =1	0
3:0	R/W	HT_MCS0_FBK	Auto fall back MCS as HT MCS =0	0

HT\_FBK\_CFG1 (offset: 0x1358, default: 0xEDCB\_A988)

Bits	Type	Name	Description	Initial value
31:28	R/W	HT_MCS15_FBK	Auto fall back MCS as HT MCS =15	14
27:24	R/W	HT_MCS14_FBK	Auto fall back MCS as HT MCS =14	13
23:20	R/W	HT_MCS13_FBK	Auto fall back MCS as HT MCS =13	12
19:16	R/W	HT_MCS12_FBK	Auto fall back MCS as HT MCS =12	11
15:12	R/W	HT_MCS11_FBK	Auto fall back MCS as HT MCS =11	10
11:8	R/W	HT_MCS10_FBK	Auto fall back MCS as HT MCS =10	9
7:4	R/W	HT_MCS9_FBK	Auto fall back MCS as HT MCS =9	8
3:0	R/W	HT_MCS8_FBK	Auto fall back MCS as HT MCS =8	8

Note1. The MCS is a fallback stopping state, as the fallback MCS is the same as current MCS.

Note2. HT TX PHY rates will not fallback to legacy PHY rates.

#### LG\_FBK\_CFG0 (offset: 0x135C, default: 0xEDCB\_A988)

Bits	Type	Name	Description	Initial value
31:28	R/W	OFDM7_FBK	Auto fall back MCS as previous TX rate is OFDM 54Mbps.	14
27:24	R/W	OFDM6_FBK	Auto fall back MCS as previous TX rate is OFDM 48Mbps.	13
23:20	R/W	OFDM5_FBK	Auto fall back MCS as previous TX rate is OFDM 36Mbps.	12
19:16	R/W	OFDM4_FBK	Auto fall back MCS as previous TX rate is OFDM 24Mbps.	11
15:12	R/W	OFDM3_FBK	Auto fall back MCS as previous TX rate is OFDM 18Mbps.	10
11:8	R/W	OFDM2_FBK	Auto fall back MCS as previous TX rate is OFDM 12Mbps.	9
7:4	R/W	OFDM1_FBK	Auto fall back MCS as previous TX rate is OFDM 9Mbps.	8
3:0	R/W	OFDM0_FBK	Auto fall back MCS as previous TX rate is OFDM 6Mbps.	8

#### LG\_FBK\_CFG1 (offset: 0x1360, default: 0x0000\_2100)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:12	R/W	CCK3_FBK	Auto fall back MCS as previous TX rate is CCK 11Mbps.	2
11:8	R/W	CCK2_FBK	Auto fall back MCS as previous TX rate is CCK 5.5Mbps.	1
7:4	R/W	CCK1_FBK	Auto fall back MCS as previous TX rate is CCK 2Mbps.	0
3:0	R/W	CCK0_FBK	Auto fall back MCS as previous TX rate is CCK 1Mbps.	0

Note1. Bit3 of each legacy fallback rate is selection of OFDM/CCK. 0=CCK, 1=OFDM.

#### TX\_FBK\_CFG\_3S\_0 (offset: 0x13C4, default: 0x1211\_100F)

Bits	Type	Name	Description	Initial value
31:29	R		Reserved	0
28:24	R/W	HT_MCS19_FBK	Auto fall back MCS as HT MCS =19	0x12
23:21	R		Reserved	0
20:16	R/W	HT_MCS18_FBK	Auto fall back MCS as HT MCS =18	0x11
15:13	R		Reserved	0
12:8	R/W	HT_MCS17_FBK	Auto fall back MCS as HT MCS =17	0x10
7:5	R		Reserved	0
4:0	R/W	HT_MCS16_FBK	Auto fall back MCS as HT MCS =16	0x0F

#### TX\_FBK\_CFG\_3S\_1 (offset: 0x13C8, default: 0x1615\_1413)

Bits	Type	Name	Description	Initial value
31:29	R		Reserved	0
28:24	R/W	HT_MCS23_FBK	Auto fall back MCS as HT MCS =23	0x16
23:21	R		Reserved	0
20:16	R/W	HT_MCS22_FBK	Auto fall back MCS as HT MCS =22	0x15
15:13	R		Reserved	0
12:8	R/W	HT_MCS21_FBK	Auto fall back MCS as HT MCS =21	0x14
7:5	R		Reserved	0
4:0	R/W	HT_MCS20_FBK	Auto fall back MCS as HT MCS =20	0x13

#### CCK\_PROT\_CFG (offset: 0x1364, default: 0x0010\_0003)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	CCK_RTSTH_EN	RTS threshold enable on CCK TX 0: disable                    1: enable	0
25:20	R/W	CCK_TXOP_ALLOW	CCK TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX	1

			Bit20: allow CCK TX	
19:18	R/W	CCK_PROT_NAV	TXOP protection type for CCK TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	CCK_PROT_CTRL	Protection control frame type for CCK TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	CCK_PROT_RATE	Protection control frame rate for CCK TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

**OFDM\_PROT\_CFG (offset: 0x1368, default: 0x0020\_0003)**

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	OFDM_RTSTH_EN	RTS threshold enable on OFDM TX 0: disable 1: enable	0
25:20	R/W	OFDM_PROT_TXOP	OFDM TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	2
19:18	R/W	OFDM_PROT_NAV	TXOP protection type for OFDM TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	OFDM_PROT_CTRL	Protection control frame type for OFDM TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	OFDM_PROT_RATE	Protection control frame rate for OFDM TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

**MM20\_PROT\_CFG (offset: 0x136C, default: 0x0040\_4004)**

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	MM20_RTSTH_EN	RTS threshold enable on MM20 TX 0: disable 1: enable	0
25:20	R/W	MM20_PROT_TXOP	MM20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX	4

			Bit20: allow CCK TX	
19:18	R/W	MM20_PROT_NAV	TXOP protection type for MM20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM20_PROT_CTRL	Protection control frame type for MM20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM20_PROT_RATE	Protection control frame rate for MM20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

MM40\_PROT\_CFG (offset: 0x1370, default: 0x0080\_4084)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	MM40_RTSTH_EN	RTS threshold enable on MM40 TX 0: disable 1: enable	0
25:20	R/W	MM40_PROT_TXOP	MM40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	8
19:18	R/W	MM40_PROT_NAV	TXOP protection type for MM40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM40_PROT_CTRL	Protection control frame type for MM40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM40_PROT_RATE	Protection control frame rate for MM40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x4084

GF20\_PROT\_CFG (offset: 0x1374, default: 0x0100\_4004)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	GF20_RTSTH_EN	RTS threshold enable on GF20 TX 0: disable 1: enable	0
25:20	R/W	GF20_PROT_TXOP	GF20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX	16

			Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	
19:18	R/W	GF20_PROT_NAV	TXOP protection type for GF20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF20_PROT_CTRL	Protection control frame type for GF20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF20_PROT_RATE	Protection control frame rate for GF20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

GF40\_PROT\_CFG (offset: 0x1378, default: 0x0200\_4084)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	GF40_RTSTH_EN	RTS threshold enable on GF40 TX 0: disable 1: enable	0
25:20	R/W	GF40_PROT_TXOP	GF40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	16
19:18	R/W	GF40_PROT_NAV	TXOP protection type for GF40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF40_PROT_CTRL	Protection control frame type for GF40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF40_PROT_RATE	Protection control frame rate for GF40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x4084

EXP\_CTS\_TIME (offset: 0x137C, default: 0x0038\_013A)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:16	R/W	EXP_OFDM_CTS_TIME	Expected time for OFDM CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps CTS	56
15	R		Reserved	0
14:0	R/W	EXP_CCK_CTS_TIME	Expected time for CCK CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps CTS	314

EXP\_ACK\_TIME (offset: 0x1380, default: 0x0024\_00CA)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:16	R/W	EXP_OFDM_ACK_TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps ACK preamble	36

15	R		Reserved	0
14:0	R/W	EXP_CCK_ACK_TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps ACK preamble	202

**TX\_Txbf\_CFG\_0** (offset: 0x138C, default: 0x8004\_FC21)

Bits	Type	Name	Description	Initial value
31:16	R/W	ETXBF_FBK_RATE	Explicit TxBF feedback rate	0x8004
15	R/W	ETXBF_FBK_EN	Explicit TxBF feedback enable 0: disable, 1: enable	0x1
14	R/W	ETXBF_FBK_SEQ_EN	Explicit TxBF feedback frame sequence number counting enable 0: disable, 1: enable	0x1
13:12	R/W	ETXBF_FBK_COEF	Explicit TxBF feedback coefficient for non-compressed form 0: 4bit 1: 2bit 2: 6bit 3: 8bit	0x3
11:10	R/W	ETXBF_FBK_CODE	Explicit TxBF feedback codebook for compressed form 0: 1 bit psi, 3 bit phi 1: 2 bit psi, 4 bit phi 2: 3 bit psi, 5 bit phi 3: 4 bit psi, 6 bit phi	0x3
9:8	R/W	ETXBF_FBK_NG	Explicit TxBF feedback number of group 0: 1 subcarrier in each group 1: 2 subcarrier in each group 2: 4 subcarrier in each group 3: reserved	0x0
7	R/W	CSD_BYPASS	BBP CSD bypass	0x0
6	R/W	ETXBF_FORCE	Force Explicit TxBF enable 0: according to TXWI setting 1: force ETXBF_EN bit in TXWI to 1	0x0
5	R/W	ETXBF_ENABLE	Explicit TxBF enable 0: disable, 1: enable	0x1
4:2	R/W	AUTO_Txbf_EN	Enable TxBF on auto-responding frames like ACK/BA/CTS	0x0
1	R/W	ITXBF_FORCE	Force implicit TxBF enable 0: according to TXWI setting 1: force ITXBF_EN bit in TXWI to 1	0x0
0	R/W	ITXBF_EN	Implicit TxBF enable 0: disable, 1: enable	0x1

**TX\_Txbf\_CFG\_1** (offset: 0x13A4, default: 0xFE23\_727F)

Bits	Type	Name	Description	Initial value
31:27	R/W	ETXBF_FBK_TIMEOUT	Explicit TxBF feedback timeout value (unit: slot time)	0x1F
26	R/W	ETXBF_FBK_TIMEOUT_EN	Explicit TxBF feedback timeout enable 0: disable, 1: enable	0x1
25	R/W	ETXBF_NDP_WAIT_EN	Explicit TxBF feedback wait for NDP 0: disable, 1: enable	0x1
24	R/W	ETXBF_BKOFF_EN	Explicit TxBF feedback backoff before transmission 0: disable, 1: enable	0x0
23:20	R/W	ETXBF_AIFSN	Explicit TxBF feedback backoff AIFS	0x2
19:16	R/W	ETXBF_CWMIN	Explicit TxBF feedback backoff CWMIN	0x3
15:12	R/W	ETXBF_RTY_LIMIT	Explicit TxBF feedback retry limit	0x7
11:8	R/W	ETXBF_ACK_TIMEOUT	Explicit TxBF feedback ACK timeout window (unit: slot time)	0x2
7	R		Reserved	0
6:4	R/W	TXBF_VALID_TYPE	Implicit TxBF profile update trigger frame types Bit6: data frame Bit5: control frame Bit4: management frame	0x7
3:0	R/W	TXBF_VALID_RATE	Implicit TxBF profile update trigger frame rates Bit3: HT-Greenfield	0xF

			Bit2: HT-Mixmode Bit1: OFDM Bit0: CCK	
--	--	--	---	--

**TX\_TXBFCFG\_2** (offset: 0x13A8, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_TSF_DELTA	The explicit TxBF feedback is applied only when the value of (local TSF timer) - (TSF timestamp of the feedback frame) is greater than or equal to ETXBF_TSF_DELTA.	0x0

**TX\_TXBFCFG\_3** (offset: 0x13AC, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0x0
15:0	R/W	ETXBF_TIMEOUT	Explicit TxBF profile timeout value (unit: usec)	0x0

**TX\_ETXBF\_MAN\_0** (offset: 0x13B0, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_0	Explicit TxBF manual write data bit31:bit0	0x0

**TX\_ETXBF\_MAN\_1** (offset: 0x13B4, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_1	Explicit TxBF manual write data bit63:bit32	0x0

**TX\_ETXBF\_MAN\_2** (offset: 0x13B8, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_2	Explicit TxBF manual write data bit95:bit64	0x0

**TX\_ETXBF\_MAN\_3** (offset: 0x13BC, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_3	Explicit TxBF manual write data bit127:bit96	0x0

**TX\_ETXBF\_MAN\_4** (offset: 0x13C0, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0x0
26	R/W	ETXBF_MAN_EN	Explicit TxBF manual write enable	0x0
25	R/W	ETXBF_MAN_KICK	Explicit TxBF manual write kick/busy Write- 1 to kick explicit TxBF manual write Read- 0: idle, 1: busy	0x0
24	R/W	ETXBF_MAN_TAG	Explicit TxBF manual write tag bit	0x0
23	R/W	ETXBF_MAN_COMP	Explicit TxBF manual write compress bit	0x0
22:16	R/W	ETXBF_MAN_SUBC	Explicit TxBF manual write sub-carrier bit6:bit0	0x0
15:0	R/W	ETXBF_MAN_DATA_4	Explicit TxBF manual write data bit143:bit128	0x0

**TX\_AC\_RTY\_LIMIT** (offset: 0x13CC, default: 0x0707\_0707)

Bits	Type	Name	Description	Initial value
31:24	R/W	AC3_TX_RTY_LIMIT	AC3 TX retry limit	0x07
23:16	R/W	AC2_TX_RTY_LIMIT	AC2 TX retry limit	0x07
15:8	R/W	AC1_TX_RTY_LIMIT	AC1 TX retry limit	0x07
7:0	R/W	AC0_TX_RTY_LIMIT	AC0 TX retry limit	0x07

**TX\_AC\_FBK\_SPEED** (offset: 0x13D0, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:28	R/W	AC3_FBK_SPEED	AC3 TX fallback speed 0: fallback speed x0 1: fallback speed x1/2 2: fallback speed x1/4 3: fallback speed x1/8 4: fallback speed x0 5: fallback speed x2 6: fallback speed x4 7: fallback speed x8	0x0
27	R		Reserved	0
26:24	R/W	AC2_FBK_SPEED	AC2 TX fallback speed 0: fallback speed x0 1: fallback speed x1/2	0x0

			2: fallback speed x1/4 3: fallback speed x1/8 4: fallback speed x0 5: fallback speed x2 6: fallback speed x4 7: fallback speed x8	
23	R		Reserved	0
22:20	R/W	AC1_FBK_SPEED	AC1 TX fallback speed 0: fallback speed x0 1: fallback speed x1/2 2: fallback speed x1/4 3: fallback speed x1/8 4: fallback speed x0 5: fallback speed x2 6: fallback speed x4 7: fallback speed x8	0x0
19	R		Reserved	0
18:16	R/W	AC0_FBK_SPEED	AC0 TX fallback speed 0: fallback speed x0 1: fallback speed x1/2 2: fallback speed x1/4 3: fallback speed x1/8 4: fallback speed x0 5: fallback speed x2 6: fallback speed x4 7: fallback speed x8	0x0
15:2	R		Reserved	0
1	R/W	AC_TX_FBK_SPEED_EN	Per AC TX fallback speed enable 0: disable, 1: enable	0
0	R/W	AC_TX_RTY_LIMIT_EN	Per AC TX retry limit enable 0: disable, 1: enable	0

### 3.21.3.2.5 MAC RX configuration registers (offset: 0x1400)

RX\_FILTR\_CFG (offset: 0x1400, default: 0x0001\_5F9F)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	DROP_CTRL_RSV	Drop reserve control subtype	1
15	R/W	DROP_BAR	Drop BAR	0
14	R/W	DROP_BA	Drop BA	1
13	R/W	DROP_PSPOLL	Drop PS-Poll	0
12	R/W	DROP_RTS	Drop RTS	1
11	R/W	DROP_CTS	Drop CTS	1
10	R/W	DROP_ACK	Drop ACK	1
9	R/W	DROP_CFEND	Drop CF-END	1
8	R/W	DROP_CFACK	Drop CF-END + CF-ACK	1
7	R/W	DROP_DUPL	Drop duplicated frame	1
6	R/W	DROP_BC	Drop broadcast frame	0
5	R/W	DROP_MC	Drop multicast frame	0
4	R/W	DROP_VER_ERR	Drop 802.11 version error frame	1
3	R/W	DROP_NOT_MYBSS	Drop frame that is not my BSSID	1
2	R/W	DROP_UC_NOME	Drop not to me unicast frame	1
1	R/W	DROP_PHY_ERR	Drop physical error frame	1
0	R/W	DROP_CRC_ERR	Drop CRC error frame	1

Note: 1: enable, 0: disable.

AUTO\_RSP\_CFG (offset: 0x1404, default: 0x0000\_0003)

Bits	Type	Name	Description	Initial value
31:8	R		Reserved	0

7	R/W	CTRL_PWR_BIT	Power bit value in control frame	0
6	R/W	BAC_ACK_POLICY	BA frame -> BAC -> Ack policy bit value	0
5	R/W	CTRL_WRAP_EN	ACK/CTS Control Wrapper frame auto-responding enable 0: disable 1: enable	0
4	R/W	CCK_SHORT_EN	CCK short preamble auto response enable 0: disable 1: enable	0
3	R/W	CTS_40M_REF	In duplicate legacy CTS response mode, refer to extension CCA to decide duplicate or not. 0: disable 1: enable	0
2	R/W	CTS_40M_MODE	Duplicate legacy CTS response mode 0: disable 1: enable	0
1	R/W	BAC_ACKPOLICY_EN	BAC ACK policy bit enable 0: disable; don't care this bit 1: enable; no BA auto responding upon reception of BAR with no ACK policy	1
0	R/W	AUTO_RSP_EN	Auto responder enable	1

**LEGACY\_BASIC\_RATE** (offset: 0x1408, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31: 12	R/W		Reserved	0
11: 0	R/W	LEGACY_BASIC_RATE	Legacy basic rate bit mask Bit0: 1 Mbps is basic rate Bit1: 2 Mbps is basic rate Bit2: 5.5 Mbps is basic rate Bit3: 11 Mbps is basic rate Bit4: 6 Mbps is basic rate Bit5: 9 Mbps is basic rate Bit6: 12 Mbps is basic rate Bit7: 18 Mbps is basic rate Bit8: 24 Mbps is basic rate Bit9: 36 Mbps is basic rate Bit10: 48 Mbps is basic rate Bit11: 54 Mbps is basic rate 0: disable 1: enable	0

**HT\_BASIC\_RATE** (offset: 0x140C, default: 0x8200\_8000)

Bits	Type	Name	Description	Initial value
31: 0	R/W	Reserved		0

**HT\_CTRL\_CFG** (offset: 0x1410, default: 0x0000\_0100)

Bits	Type	Name	Description	Initial value
31: 9	R		Reserved	0
8: 0	R/W	HT_CTRL_THRES	Remaining TXOP threshold for HT control frame auto responding (unit: us)	256

**SIFS\_COST\_CFG** (offset: 0x1414, default: 0x0000\_100A)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	
15:8	R/W	OFDM_SIFS_COST	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_COST	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

**Note:** The OFDM\_SIFS\_COST and CCK\_SIFS\_COST are used only for duration field calculation. It will not affect the responding timing.

**RX\_PARSER\_CFG** (offset: 0x1418, default: 0x0FFF\_0000)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	

27:16	R/W	LSIG_LEN_THRES	When the length in L-SIG is longer than this threshold, the L-SIG TXOP will not be applied as NAV channel reservation.	4095
15:02	R		Reserved	
1	R/W	RX_LSIG_TXOP_EN	Respect LSIG-TXOP as channel reservation 0: disable 1: enable	0
0	R/W	NAV_ALL_EN	Set NAV for all received frames 0: disable (unicast to me frame will not set the NAV) 1: enable	0

### 3.21.3.2.6 MAC Security Configuration Registers (offset:0x1500)

TX\_SEC\_CNT0 (offset:0x1500, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_SEC_ERR_CNT	TX SEC packet error count	0
15:0	RC	TX_SEC_CPL_CNT	TX SEC packet complete count	0

RX\_SEC\_CNT0 (offset:0x1504, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16			Reserved	0
15:0	RC	RX_SEC_CPL_CNT	RX SEC packet complete count	0

CCMP\_FC\_MUTE (offset:0x1508, default: 0xC78F\_C78f)

Bits	Type	Name	Description	Initial value
31:16	R/W	HT_CCMP_FC_MUTE	HT rate CCMP FC mute	0xc78f
15:0	R/W	LG_CCMP_FC_MUTE	Legacy rate CCMP FC mute	0xc78f

### 3.21.3.2.7 MAC HCCA/PSMP CSR (offset:0x1600)

TXOP\_HLDR\_ADDR0 (offset:0x1600, default :0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP HOL 3	TXOP holder MAC address byte3	0
23:16	R/W	TXOP HOL 2	TXOP holder MAC address byte2	0
15:8	R/W	TXOP HOL 1	TXOP holder MAC address byte1	0
7:0	R/W	TXOP HOL 0	TXOP holder MAC address byte0	0

TXOP\_HLDR\_ADDR1 (offset:0x1604, default :0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	TXOP HOL 5	TXOP holder MAC address byte5	0
7:0	R/W	TXOP HOL 4	TXOP holder MAC address byte4	0

**Note:** Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

TXOP\_HLDR\_ET (offset:0x1608, default :0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	AMPDU_ACC_EN	Accumulate AMPDU enable 0: disable, 1: enable	0
23:19	R/W	TX_DMA_TIMEOUT	When AMPDU_ACC_EN is enabled: Wait at most (TX_DMA_TIMEOUT * 32) usec for the MPDU for aggregation	0
18	R/W	TX_FBK_THRES_EN	Transmission MCS fallback threshold enable 0: disable, 1: enable	0
17:16	R/W	TX_FBK_THRES	When TX_FBK_THRES_EN is enabled, fallback when 0: less than 25% in AMPDU are success. 1: less than 50% in AMPDU are success. 2: less than 75% in AMPDU are success. 3: less than 100% in AMPDU are success.	0
15:5	R		Reserved	0
4	R/W	PAPE_MAP	When PAPE_MAP1S_EN is enabled:	0

			0: only turn on PAPE0 for 1S transmission 1: only turn on PAPE1 for 1S transmission	
3	R/W	PAPE_MAP1S_EN	Turn on only on PAPE in 1S transmission 0: disable, 1: enable	0
2	R/W	TX_BCN_HIPRI_DIS	Disable high priority beacon transmission 1: disable, 0: enable	0
1	R/W	TX40M_BLK_EN	Block 40Mhz transmission as extension CCA is busy 0: disable, 1: enable	0
0	R/W	PER_RX_RST_EN	Baseband RX_PE per RX reset enable 0: disable, 1: enable	0

**QOS\_CFPOLL\_RA\_DW0** (offset:0x160C, default :0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:24	R	CFPOLL_A1_BYTE3	Byte3 of A1 of received QoS Data (+) CF-Poll frame	X
23:16	R	CFPOLL_A1_BYTE2	Byte2 of A1 of received QoS Data (+) CF-Poll frame	X
15:8	R	CFPOLL_A1_BYTE1	Byte1 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE0	Byte0 of A1 of received QoS Data (+) CF-Poll frame	X

**QOS\_CFPOLL\_A1\_DW1** (offset:0x1610, default :0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
16	R	CFPOLL_A1_TOME	1: QoS CF-Poll to me 0: QoS CF-Poll not to me	X
15:8	R	CFPOLL_A1_BYTE5	Byte5 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE4	Byte4 of A1 of received QoS Data (+) CF-Poll frame	X

**QOS\_CFPOLL\_QC** (offset:0x1614, default :0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
15:8	R	CFPOLL_QC_BYTE1	Byte1 of QC of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_QC_BYTE0	Byte0 of QC of received QoS Data (+) CF-Poll frame	X

**Note:** CFPOLL\_RA\_DW0, CFPOLL\_RA\_DW1, and CFPOLL\_QC are updated after the reception of QoS Data (+) CF-Poll frame and RX QoS CF-Poll interrupt (RX\_QOS\_CFPOLL\_INT) is launched then.

### 3.21.3.2.8 MAC Statistic Counters (offset:0x1700)

**RX\_STA\_CNT0** (offset:0x1700, default: 0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:16	RC	PHY_ERRCNT	RX PHY error frame count	0
15:0	RC	CRC_ERRCNT	RX CRC error frame count	0

**Note1:** RX PHY error means PSDU length is shorter than indicated by PLCP.

**Note2:** RX PHY error is also treated as CRC error.

**RX\_STA\_CNT1** (offset:0x1704, default: 0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:16	RC	PLPC_ERRCNT	RX PLCP error count	0
15:0	RC	CCA_ERRCNT	CCA false alarm count	0

**Note1:** CCA false alarm means there is no PLCP after CCA indication.

**Note2:** RX PLCP error means there is no PSDU after PLCP indication.

**RX\_STA\_CNT2** (offset:0x1708, default: 0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_OVFL_CNT	RX FIFO overflow frame count	0
15:0	RC	RX_DUPL_CNT	RX duplicated filtered frame count	0

**Note:** MAC will NOT auto respond ACK/BA to the frame originator when frame is lost due to RXFIFO overflow.

However, MAC will respond when frame is duplicated filtered.

**TX\_STA\_CNT0** (offset:0x170C, default: 0xFFFF\_FFFF)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_BCN_CNT	TX beacon count	0
15:0	RC	TX_FAIL_CNT	Failed TX count	0

**TX\_STA\_CNT1** (offset:0x1710, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_RTY_CNT	TX retransmission count	0
15:0	RC	TX_SUCC_CNT	Successful TX count	0

**TX\_STA\_CNT2** (offset:0x1714, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_UDFL_CNT	TX underflow count	0
15:0	RC	TX_ZERO_CNT	TX zero length frame count	0

**TX\_STAT\_FIFO** (offset:0x1718, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R	TXQ_RATE	TX success rate	*
15:8	R	TXQ_WCID	TX WCID	*
7	R	TXQ_ACKREQ	TX acknowledge required 0: not required      1: required	*
6	R	TXQ_AGG	TX aggregate 0: non-aggregated      1: aggregated	*
5	R	TXQ_OK	TX success 0: failed      1: success	*
4:1	R	TXQ_PID	TX Packet ID (Latched from TXWI)	*
0	RC	TXQ_VLD	TX status queue valid 0: queue empty      1: valid	0

**Note:** TX status FIFO size = 16.

**TX\_NAG\_AGG\_CNT** (offset:0x171C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_CNT	Aggregate TX count	0
15:0	RC	TX_NAG_CNT	Non-aggregate TX count	0

**TX\_AGG\_CNT0** (offset:0x1720, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_2_CNT	Aggregate Size = 2 MPDU count	0
15:0	RC	TX_AGG_1_CNT	Aggregate Size = 1 MPDU count	0

**TX\_AGG\_CNT1** (offset:0x1724, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_4_CNT	Aggregate Size = 4 MPDU count	0
15:0	RC	TX_AGG_3_CNT	Aggregate Size = 3 MPDU count	0

**TX\_AGG\_CNT2** (offset:0x1728, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_6_CNT	Aggregate Size = 6 MPDU count	0
15:0	RC	TX_AGG_5_CNT	Aggregate Size = 5 MPDU count	0

**TX\_AGG\_CNT3** (offset:0x172C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_8_CNT	Aggregate Size = 8 MPDU count	0
15:0	RC	TX_AGG_7_CNT	Aggregate Size = 7 MPDU count	0

**TX\_AGG\_CNT4** (offset:0x1730, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_10_CNT	Aggregate Size = 10 MPDU count	0
15:0	RC	TX_AGG_9_CNT	Aggregate Size = 9 MPDU count	0

**TX\_AGG\_CNT5** (offset:0x1734, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_12_CNT	Aggregate Size = 12 MPDU count	0
15:0	RC	TX_AGG_11_CNT	Aggregate Size = 11 MPDU count	0

**TX\_AGG\_CNT6** (offset:0x1738, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_14_CNT	Aggregate Size = 14 MPDU count	0
15:0	RC	TX_AGG_13_CNT	Aggregate Size = 13 MPDU count	0

TX\_AGG\_CNT7 (offset:0x173C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_16_CNT	Aggregate Size = 16 MPDU count	0
15:0	RC	TX_AGG_15_CNT	Aggregate Size = 15 MPDU count	0

MPDU\_DENSITY\_CNT (offset:0x1740, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_ZERO_DEL_CNT	RX zero length delimiter count	0
15:0	RC	TX_ZERO_DEL_CNT	TX zero length delimiter count	0

RTS\_TX\_CNT (offset:0x1744, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RTS_TX_FAIL_CNT	RTS TX fail count	0
15:0	RC	RTS_TX_OK_CNT	RTS TX OK count	0

CTS\_TX\_CNT (offset:0x1748, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	RC	CTSTS_TX_CNT	CTS-to-self TX count	0

TX\_AGG\_CNT8 (offset:0x174C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_18_CNT	Aggregate Size = 18 MPDU count	0
15:0	RC	TX_AGG_17_CNT	Aggregate Size = 17 MPDU count	0

TX\_AGG\_CNT9 (offset:0x1750, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_20_CNT	Aggregate Size = 20 MPDU count	0
15:0	RC	TX_AGG_19_CNT	Aggregate Size = 19 MPDU count	0

TX\_AGG\_CNT10 (offset:0x1754, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_22_CNT	Aggregate Size = 22 MPDU count	0
15:0	RC	TX_AGG_21_CNT	Aggregate Size = 21 MPDU count	0

TX\_AGG\_CNT11 (offset:0x1758, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_24_CNT	Aggregate Size = 24 MPDU count	0
15:0	RC	TX_AGG_23_CNT	Aggregate Size = 23 MPDU count	0

TX\_AGG\_CNT12 (offset:0x175C, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_26_CNT	Aggregate Size = 26 MPDU count	0
15:0	RC	TX_AGG_25_CNT	Aggregate Size = 25 MPDU count	0

TX\_AGG\_CNT13 (offset:0x1760, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_28_CNT	Aggregate Size = 28 MPDU count	0
15:0	RC	TX_AGG_27_CNT	Aggregate Size = 27 MPDU count	0

TX\_AGG\_CNT14 (offset:0x1764, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_30_CNT	Aggregate Size = 30 MPDU count	0
15:0	RC	TX_AGG_29_CNT	Aggregate Size = 29 MPDU count	0

TX\_AGG\_CNT15 (offset:0x1768, default: 0x0000\_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_32_CNT	Aggregate Size = 32 MPDU count	0
15:0	RC	TX_AGG_31_CNT	Aggregate Size = 31 MPDU count	0

WCID\_TX\_CNT0 (offset:0x176C, default: 0x0000\_0000)

DSRT3662\_V1.0\_101309

Form No. : QS-073-F02

Rev. : 1

Kept by : DCC

Ret. Time : 5 Years

-200-

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_A	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_A	0
WCID_TX_CNT1 (offset:0x1770, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_B	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_B	0
WCID_TX_CNT2 (offset:0x1774, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_C	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_C	0
WCID_TX_CNT3 (offset:0x1778, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_D	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_D	0
WCID_TX_CNT4 (offset:0x177C, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_E	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_E	0
WCID_TX_CNT5 (offset:0x1780, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_F	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_F	0
WCID_TX_CNT6 (offset:0x1784, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_G	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_G	0
WCID_TX_CNT7 (offset:0x1788, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16	RC	WCID_TX_RTY_CNT0	TX retry count for WCID_H	0
15:0	RC	WCID_TX_OK_CNT0	Successful TX count for WCID_H	0
WCID_MAPING_0 (offset:0x178C, default: 0xFFFF_FFFF)				
Bits	Type	Name	Description	Initial value
7:0	R/W	WCID_D	The WCID number maps to WCID_D	0xFF
7:0	R/W	WCID_C	The WCID number maps to WCID_C	0xFF
7:0	R/W	WCID_B	The WCID number maps to WCID_B	0xFF
7:0	R/W	WCID_A	The WCID number maps to WCID_A	0xFF
WCID_MAPING_1 (offset:0x1790, default: 0xFFFF_FFFF)				
Bits	Type	Name	Description	Initial value
7:0	R/W	WCID_H	The WCID number maps to WCID_H	0xFF
7:0	R/W	WCID_G	The WCID number maps to WCID_G	0xFF
7:0	R/W	WCID_F	The WCID number maps to WCID_F	0xFF
7:0	R/W	WCID_E	The WCID number maps to WCID_E	0xFF
TX_REPORT_CNT (offset:0x1794, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:16			Reserved	0
15:0	RC	TX_REPORT_CNT	Successful TX count for frames which TXWI.REPORT bit =1.	0
TX_STAT_FIFO_EXT (offset:0x1798, default: 0x0000_0000)				
Bits	Type	Name	Description	Initial value
31:8			Reserved	0
7:0	R	TXQ_RTY_CNT	Per frame TX retry count (read before reading 0x1718)	0

**3.21.3.3 MAC search table (base: 1018.0000, offset: 0x1800)**

RX WCID search entry format (8 bytes)

Offset	Type	Name	Description	Initial value
0x00	R/W	WC_MAC_ADDR0	Client MAC address byte0	0x00
0x01	R/W	WC_MAC_ADDR1	Client MAC address byte1	0x00
0x02	R/W	WC_MAC_ADDR2	Client MAC address byte2	0x00
0x03	R/W	WC_MAC_ADDR3	Client MAC address byte3	0x00
0x04	R/W	WC_MAC_ADDR4	Client MAC address byte4	0x00
0x05	R/W	WC_MAC_ADDR5	Client MAC address byte5	0x00
0x06	R/W	BA_SESS_MASK0	BA session mask (lower) Bit0 for TID0 Bit7 for TID7	0x00
0x07	R/W	BA_SESS_MASK1	BA session mask (upper) Bit8 for TID8 Bit15 for TID15	0x00

RX WCID search table (offset:0x1800)

Offset	Type	Name	Description	Initial value
0x1800	R/W	WC_ENTRY_0	WC MAC address with WCID=0	0
0x1808	R/W	WC_ENTRY_1	WC MAC address with WCID=1	0
....	R/W	....	WC MAC address with WCID=2~253	0
0x1FF0	R/W	WC_ENTRY_254	WC MAC address with WCID=254	0
0x1FF8	R/W	WC_ENTRY_255	Reserved (shall not be used)	0

**Note1:** WCID=Wireless Client ID
**3.22 Security table/CIS/Beacon/NULL frame (base: 1018.0000, offset: 0x4000)**
**3.22.1 Security Key Format (8DW)**

Offset	Type	Name	Description	Initial value
0x00	R/W	SECKEY_DW0	Security key byte3~0	*
0x04	R/W	SECKEY_DW1	Security key byte7~4	*
0x08	R/W	SECKEY_DW2	Security key byte11~8	*
0x0C	R/W	SECKEY_DW3	Security key byte15~12	*
0x10	R/W	TXMIC_DW0	TX MIC key byte3~0	*
0x14	R/W	TXMIC_DW1	TX MIC key byte7~4	*
0x18	R/W	RXMIC_DW0	RX MIC key byte3~0	*
0x1C	R/W	RXMIC_DW1	RX MIC key byte7~4	*

## Note:

1. FOR WEP40, CKIP40, ONLY BYTE4~0 OF SECURITY KEY ARE VALID.
2. For WEP104, CKIP104, only byte12~0 of security key are valid.
3. For TKIP, AES, all the bytes of security key are valid.
4. TX/RX MIC key is used only for TKIP MIC calculation.
5. 128 byte space of TX/RX MIC key are used together for WAPI MIC key.

Offset	Type	Name	Description	Initial value
0x00	R/W	SECKEY_DW0	Security key byte3~0	*
0x04	R/W	SECKEY_DW1	Security key byte7~4	*
0x08	R/W	SECKEY_DW2	Security key byte11~8	*
0x0C	R/W	SECKEY_DW3	Security key byte15~12	*
0x10	R/W	TXMIC_DW0	TX MIC key byte3~0	*
0x14	R/W	TXMIC_DW1	TX MIC key byte7~4	*
0x18	R/W	RXMIC_DW0	RX MIC key byte3~0	*
0x1C	R/W	RXMIC_DW1	RX MIC key byte7~4	*

## Note:

1. FOR WEP40, CKIP40, ONLY BYTE4~0 OF SECURITY KEY ARE VALID.
2. For WEP104, CKIP104, only byte12~0 of security key are valid.
3. For TKIP, AES, all the bytes of security key are valid.
4. TX/RX MIC key is used only for TKIP MIC calculation.
5. 128 byte space of TX/RX MIC key are used together for WAPI MIC key.

### 3.22.2 IV/EIV format (2 DW)

When TXINFO.WIV=0, hardware will auto lookup IV/EIV/WAPI\_PN from this table and update IV/EIV/WAPI\_PN after encryption is finished.

Offset	Type	Name	Description	Initial value
0x00	R/W	IV_FIELED	IV field	*
0x04	R/W	EIV_FIELED	EIV field	*

Offset	Type	Name	Description	Initial value
0x00	R/W	WAPI_PN_MSB	WAPI PN byte11-byte8	*
0x04	R/W	WAPI_PN_MSB	WAPI PN byte15-byte12	*

**Note1:** The key index and extension IV bit shall be initialized by software. The MSB octet of IV will not be modified by hardware.

**Note2:** IV/EIV packet number (PN) counter modes:

- a. For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.
- b. For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7f) is generated by hardware.
- c. For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.
- d. For non-WAPI mode, PN = PN + 1 after each encryption.
- e. For WAPI mode, PN={WAPI\_PN\_MSB\_1[31:0], WAPI\_PN\_MSB\_0[31:0], EIV[31:0], IV[31:0]}.
- f. For WAPI mode, PN=PN+2 when WAPI\_MC\_BC=0 in WCID attribute.
- g. For WAPI mode, PN=PN+1 when WAPI\_MC\_BC=1 in WCID attribute.

**Note3:** Software may initialize the PN counter to any value.

### 3.22.3 WCID attribute entry format (1DW)

Offset	Type	Name	Description	Initial value
31:24	R/W	WAPI_KEYID_BYTE	WAPI KeyID byte 0-1: WAPI Key ID 2-255: reserved	*
23:16	R/W	WAPI_RSV_BYTE	WAPI reserved byte (set to 0)	*
15	R/W	WAPI_MCBC	WAPI broadcast/multicast packet number (PN) increment 0: unicast, PN = PN + 2; 1: multicast/broadcast, PN = PN + 1;	*
14:12	R/W		Reserved	*
11	R/W	BSS_IDX_MBS	Use together with BSS_IDX(bit6:bit4),	*

			(BSS_IDX_MSB *8 + BSS_IDX) = BSS Index of the WCID	
10	R/W	RX_PKEY_MODE_MSB	Use together with RX_PKEY_MODE(bit3:bit1), (RX_PKEY_MODE_MSB *8 + RX_PKEY_MODE) = 0~7: as listed in RX_PKEY_MODE 8: WAPI 9-15: Reserved	*
9:7	R/W	RXWI_UDF	RXWI user define field This field is tagged in the RXWI.UDF fields for the WCID.	*
6:4	R/W	BSS_IDX	Multiple-BSS index for the WCID	*
3:1	R/W	RX_PKEY_MODE	Pair-wise key security mode 0: No security 1: WEP40 2: WEP104 3: TKIP 4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128	*
0	R/W	RX_PKEY_EN	Key table selection 0: shared key table 1: pair-wise key table	*

### 3.22.4 Share key mode entry format (1DW)

Bits	Type	Name	Description	Initial value
31:28	R/W	SKEY_MODE_7+	Shared key7+(8x) mode, x=0~3	*
27:24	R/W	SKEY_MODE_6+	Shared key6+(8x) mode, x=0~3	*
23:20	R/W	SKEY_MODE_5+	Shared key5+(8x) mode, x=0~3	*
19:16	R/W	SKEY_MODE_4+	Shared key4+(8x) mode, x=0~3	*
15:12	R/W	SKEY_MODE_3+	Shared key3+(8x) mode, x=0~3	*
11:8	R/W	SKEY_MODE_2+	Shared key2+(8x) mode, x=0~3	*
7:4	R/W	SKEY_MODE_1+	Shared key1+(8x) mode, x=0~3	*
3:0	R/W	SKEY_MODE_0+	Shared key0+(8x) mode, x=0~3	*

Key mode definition:

0: No security	1: WEP40	2: WEP104	3: TKIP
4: AES-CCMP	5: CKIP40	6: CKIP104	7: CKIP128
8: WAPI	9~15: Reserved		

Bits	Type	Name	Description	Initial value
31:28	R/W	SKEY_MODE_7+	Shared key7+(8x) mode, x=0~3	*
27:24	R/W	SKEY_MODE_6+	Shared key6+(8x) mode, x=0~3	*
23:20	R/W	SKEY_MODE_5+	Shared key5+(8x) mode, x=0~3	*
19:16	R/W	SKEY_MODE_4+	Shared key4+(8x) mode, x=0~3	*
15:12	R/W	SKEY_MODE_3+	Shared key3+(8x) mode, x=0~3	*
11:8	R/W	SKEY_MODE_2+	Shared key2+(8x) mode, x=0~3	*
7:4	R/W	SKEY_MODE_1+	Shared key1+(8x) mode, x=0~3	*
3:0	R/W	SKEY_MODE_0+	Shared key0+(8x) mode, x=0~3	*

Key mode definition:

0: No security	1: WEP40	2: WEP104	3: TKIP
4: AES-CCMP	5: CKIP40	6: CKIP104	7: CKIP128
8: WAPI	9~15: Reserved		

### 3.22.5 Security Table

#### 3.22.5.1 Pair-wise key table (offset:0x4000)

Offset	Type	Name	Description	Initial value
0x4000	R/W	PKEY_0	Pair-wise key for WCID0	*
0x4020	R/W	PKEY_1	Pair-wise key for WCID1	*
....	R/W	....	Pair-wise key for WCID2~253	*
0x5FC0	R/W	PKEY_254	Pair-wise key for WCID254	*
0x5FE0	R/W	PKEY_255	Pair-wise key for WCID255 (not used)	*

### 3.22.5.2 IV/EIV table (offset:0x6000)

Offset	Type	Name	Description	Initial value
0x6000	R/W	IVEIV_0	IV/EIV for WCID0	*
0x6008	R/W	IVEIV_1	IV/EIV for WCID1	*
....	R/W	....	IV/EIV for WCID2~253	*
0x67F0	R/W	IVEIV_254	IV/EIV for WCID254	*
0x67F8	R/W	IVEIV_255	IV/EIV for WCID255 (not used)	*

### 3.22.5.3 WCID attribute table (offset:0x6800)

Offset	Type	Name	Description	Initial value
0x6800	R/W	WCID_ATTR_0	WCID Attribute for WCID0	*
0x6804	R/W	WCID_ATTR_1	WCID Attribute for WCID1	*
....	R/W	....	WCID Attribute for WCID2~253	*
0x6BF8	R/W	WCID_ATTR_254	WCID Attribute for WCID254	*
0x6BFC	R/W	WCID_ATTR_255	WCID Attribute for WCID255	*

### 3.22.5.4 Shared Key Table (offset:0x6C00)

Offset	Type	Name	Description	Initial value
0x6C00	R/W	SKEY_0	Shared key for BSS_IDX=0, KEY_IDX=0	*
0x6C20	R/W	SKEY_1	Shared key for BSS_IDX=0, KEY_IDX=1	*
0x6C40	R/W	SKEY_2	Shared key for BSS_IDX=0, KEY_IDX=2	*
0x6C60	R/W	SKEY_3	Shared key for BSS_IDX=0, KEY_IDX=3	*
0x6C80	R/W	SKEY_4	Shared key for BSS_IDX=1, KEY_IDX=0	*
0x6CA0	R/W	SKEY_5	Shared key for BSS_IDX=1, KEY_IDX=1	*
0x6CC0	R/W	SKEY_6	Shared key for BSS_IDX=1, KEY_IDX=2	*
0x6CE0	R/W	SKEY_7	Shared key for BSS_IDX=1, KEY_IDX=3	*
0x6D00	R/W	SKEY_8	Shared key for BSS_IDX=2, KEY_IDX=0	*
0x6D20	R/W	SKEY_9	Shared key for BSS_IDX=2, KEY_IDX=1	*
0x6D40	R/W	SKEY_10	Shared key for BSS_IDX=2, KEY_IDX=2	*
0x6D60	R/W	SKEY_11	Shared key for BSS_IDX=2, KEY_IDX=3	*
0x6D80	R/W	SKEY_12	Shared key for BSS_IDX=3, KEY_IDX=0	*
0x6DA0	R/W	SKEY_13	Shared key for BSS_IDX=3, KEY_IDX=1	*
0x6DC0	R/W	SKEY_14	Shared key for BSS_IDX=3, KEY_IDX=2	*
0x6DE0	R/W	SKEY_15	Shared key for BSS_IDX=3, KEY_IDX=3	*
0x6E00	R/W	SKEY_16	Shared key for BSS_IDX=4, KEY_IDX=0	*
0x6E20	R/W	SKEY_17	Shared key for BSS_IDX=4, KEY_IDX=1	*
0x6E40	R/W	SKEY_18	Shared key for BSS_IDX=4, KEY_IDX=2	*
0x6E60	R/W	SKEY_19	Shared key for BSS_IDX=4, KEY_IDX=3	*
0x6E80	R/W	SKEY_20	Shared key for BSS_IDX=5, KEY_IDX=0	*
0x6EA0	R/W	SKEY_21	Shared key for BSS_IDX=5, KEY_IDX=1	*
0x6EC0	R/W	SKEY_22	Shared key for BSS_IDX=5, KEY_IDX=2	*
0x6EE0	R/W	SKEY_23	Shared key for BSS_IDX=5, KEY_IDX=3	*
0x6F00	R/W	SKEY_24	Shared key for BSS_IDX=6, KEY_IDX=0	*
0x6F20	R/W	SKEY_25	Shared key for BSS_IDX=6, KEY_IDX=1	*
0x6F40	R/W	SKEY_26	Shared key for BSS_IDX=6, KEY_IDX=2	*
0x6F60	R/W	SKEY_27	Shared key for BSS_IDX=6, KEY_IDX=3	*
0x6F80	R/W	SKEY_28	Shared key for BSS_IDX=7, KEY_IDX=0	*
0x6FA0	R/W	SKEY_29	Shared key for BSS_IDX=7, KEY_IDX=1	*
0x6FC0	R/W	SKEY_30	Shared key for BSS_IDX=7, KEY_IDX=2	*
0x6FE0	R/W	SKEY_31	Shared key for BSS_IDX=7, KEY_IDX=3	*

**3.22.5.5 Shared Key Mode (offset:0x7000)**

Offset	Type	Name	Description	Initial value
0x7000	R/W	SKEY_MODE_0_7	Shared mode for SKEY0-SKEY7	*
0x7004	R/W	SKEY_MODE_8_15	Shared mode for SKEY8-SKEY15	*
0x7008	R/W	SKEY_MODE_16_23	Shared mode for SKEY16-SKEY23	*
0x700C	R/W	SKEY_MODE_24_31	Shared mode for SKEY24-SKEY31	*

**3.22.5.6 Spared Memory Space Mode (offset:0x7010~0x73EC)**
**3.22.5.7 Shared Key Mode Extension (for BSS\_IDX=8~15) (offset:0x73F0)**

Offset	Type	Name	Description	Initial value
0x73F0	R/W	SKEY_MODE_32_39	Shared mode for SKEY32-SKEY39	*
0x73F4	R/W	SKEY_MODE_40_47	Shared mode for SKEY40-SKEY47	*
0x73F8	R/W	SKEY_MODE_48_55	Shared mode for SKEY48-SKEY55	*
0x73FC	R/W	SKEY_MODE_56_63	Shared mode for SKEY56-SKEY63	*

**3.22.5.8 Shared Key Table Extension (for BSS\_IDX=8~15) (offset:0x7400)**

Offset	Type	Name	Description	Initial value
0x7400	R/W	SKEY_32	Shared key for BSS_IDX=8, KEY_IDX=0	*
0x7420	R/W	SKEY_33	Shared key for BSS_IDX=8, KEY_IDX=1	*
0x7440	R/W	SKEY_34	Shared key for BSS_IDX=8, KEY_IDX=2	*
0x7460	R/W	SKEY_35	Shared key for BSS_IDX=8, KEY_IDX=3	*
0x7480	R/W	SKEY_36	Shared key for BSS_IDX=9, KEY_IDX=0	*
0x74A0	R/W	SKEY_37	Shared key for BSS_IDX=9, KEY_IDX=1	*
0x74C0	R/W	SKEY_38	Shared key for BSS_IDX=9, KEY_IDX=2	*
0x74E0	R/W	SKEY_39	Shared key for BSS_IDX=9, KEY_IDX=3	*
0x7500	R/W	SKEY_40	Shared key for BSS_IDX=10, KEY_IDX=0	*
0x7520	R/W	SKEY_41	Shared key for BSS_IDX=10, KEY_IDX=1	*
0x7540	R/W	SKEY_42	Shared key for BSS_IDX=10, KEY_IDX=2	*
0x7560	R/W	SKEY_43	Shared key for BSS_IDX=10, KEY_IDX=3	*
0x7580	R/W	SKEY_44	Shared key for BSS_IDX=11, KEY_IDX=0	*
0x75A0	R/W	SKEY_45	Shared key for BSS_IDX=11, KEY_IDX=1	*
0x75C0	R/W	SKEY_46	Shared key for BSS_IDX=11, KEY_IDX=2	*
0x75E0	R/W	SKEY_47	Shared key for BSS_IDX=11, KEY_IDX=3	*
0x7600	R/W	SKEY_48	Shared key for BSS_IDX=12, KEY_IDX=0	*
0x7620	R/W	SKEY_49	Shared key for BSS_IDX=12, KEY_IDX=1	*
0x7640	R/W	SKEY_50	Shared key for BSS_IDX=12, KEY_IDX=2	*
0x7660	R/W	SKEY_51	Shared key for BSS_IDX=12, KEY_IDX=3	*
0x7680	R/W	SKEY_52	Shared key for BSS_IDX=13, KEY_IDX=0	*
0x76A0	R/W	SKEY_53	Shared key for BSS_IDX=13, KEY_IDX=1	*
0x76C0	R/W	SKEY_54	Shared key for BSS_IDX=13, KEY_IDX=2	*
0x76E0	R/W	SKEY_55	Shared key for BSS_IDX=13, KEY_IDX=3	*
0x7700	R/W	SKEY_56	Shared key for BSS_IDX=14, KEY_IDX=0	*
0x7720	R/W	SKEY_57	Shared key for BSS_IDX=14, KEY_IDX=1	*
0x7740	R/W	SKEY_58	Shared key for BSS_IDX=14, KEY_IDX=2	*
0x7760	R/W	SKEY_59	Shared key for BSS_IDX=14, KEY_IDX=3	*
0x7780	R/W	SKEY_60	Shared key for BSS_IDX=15, KEY_IDX=0	*
0x77A0	R/W	SKEY_61	Shared key for BSS_IDX=15, KEY_IDX=1	*
0x77C0	R/W	SKEY_62	Shared key for BSS_IDX=15, KEY_IDX=2	*
0x77E0	R/W	SKEY_63	Shared key for BSS_IDX=15, KEY_IDX=3	*

### 3.22.5.9 WAPI PN table (extension of IV/EIV table) (offset:0x7800)

Offset	Type	Name	Description	Initial value
0x7800	R/W	WAPI_PN_MSB_0	Extension byte11-byte8 of WAPI PN for WCID0	*
0x7804	R/W	WAPI_PN_MSB_0	Extension byte15-byte12 of WAPI PN for WCID0	*
0x7808	R/W	WAPI_PN_MSB_1	Extension byte11-byte8 of WAPI PN for WCID1	*
0x780C	R/W	WAPI_PN_MSB_1	Extension byte15-byte12 of WAPI PN for WCID1	*
....	R/W	....	Extension byte11-byte8 of WAPI PN for WCID2~254	*
....	R/W	....	Extension byte15-byte12 of WAPI PN for WCID2~254	*
0x7FF8	R/W	WAPI_PN_MSB_255	Extension byte11-byte8 of WAPI PN for WCID255	*
0x7FFC	R/W	WAPI_PN_MSB_255	Extension byte15-byte12 of WAPI PN for WCID255	*

Note: Do not set WIV bit to 1 when WAPI mode is turned on.

## 3.23 Descriptor and Wireless information

### 3.23.1 TX frame information

To transmit a frame, the driver needs to prepare the TX frame information for hardware. The TX frame information contains the transmission control, the header, and the payload. The transmission control information (the “**TXWI**”) is used by the MAC and BBP and is applied for the associated TX frame when transmission. The header and payload is the content of an 802.11 packet.

The TX information could be scattered in several segments. The TX descriptor (the “**TXD**”) specifies the location and length of the TX frame information segment. TX frame information could be linked by use of several TXD. These TXD are arranged in a TXD ring in serial. Below diagram illustrates the linking between TXD and TX frame information.

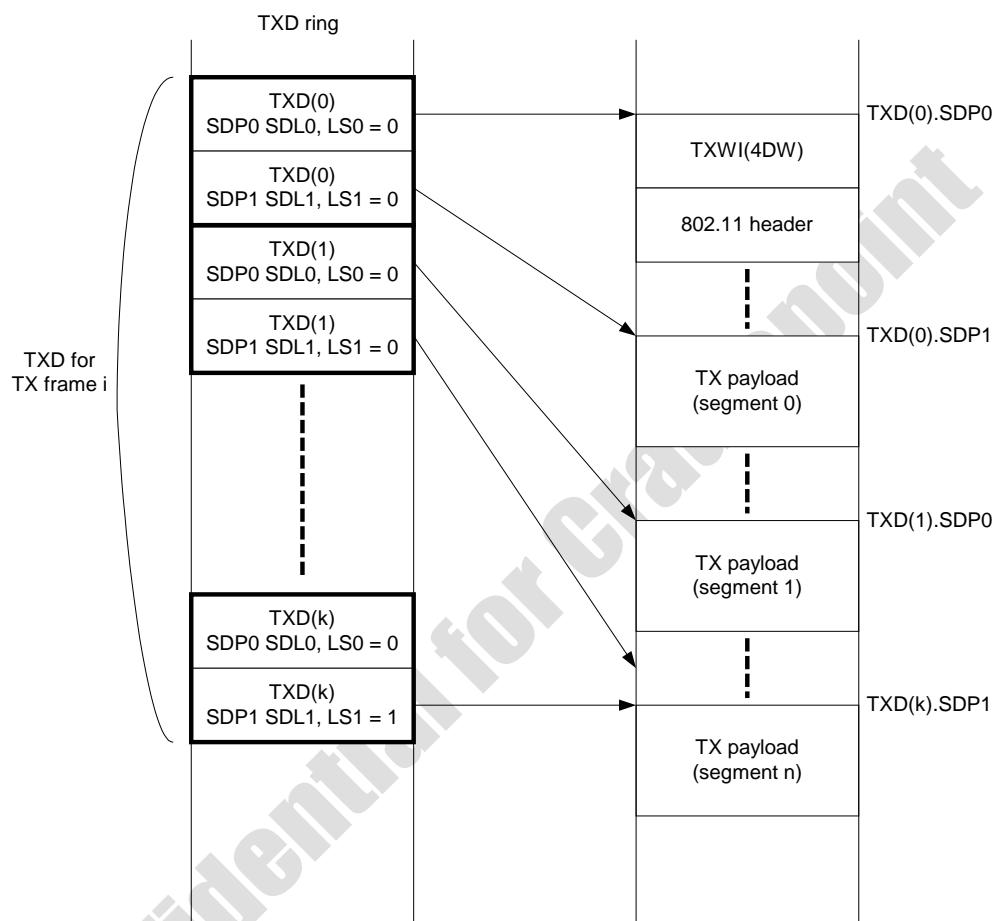


Fig. 3-23-1 TX frame information

### 3.23.1.1 TX descriptor format

bit 31

bit 0



Fig. 3-23-2 TX descriptor format

- ◆ **SDP0:** Segment Data Pointer 0.
- ◆ **SDL0:** Segment Data Length for the data pointed by SDP0.
- ◆ **SDP1:** Segment Data Pointer 1.
- ◆ **SDL1:** Segment Data Length for the data pointed by SDP1.
- ◆ **LS0:** data pointed by SDP0 is the last segment
- ◆ **LS1:** data pointed by SDP1 is the last segment
- ◆ **DDONE:** DMA Done. DMA has transferred the segments pointed by this TX descriptor
- ◆ **Burst:** force DMA to access next TX frame from the same queue.
- ◆ **QSEL:** the ID of the on-chip queue that the TX frame is moved into. 0: MGMT queue, 1: HCCA queue, 2: EDCA queue, 3: unused.
- ◆ **WIV:** 1: driver prepared all 16-byte TXWI. 0: driver prepared only the first 8-byte TXWI.

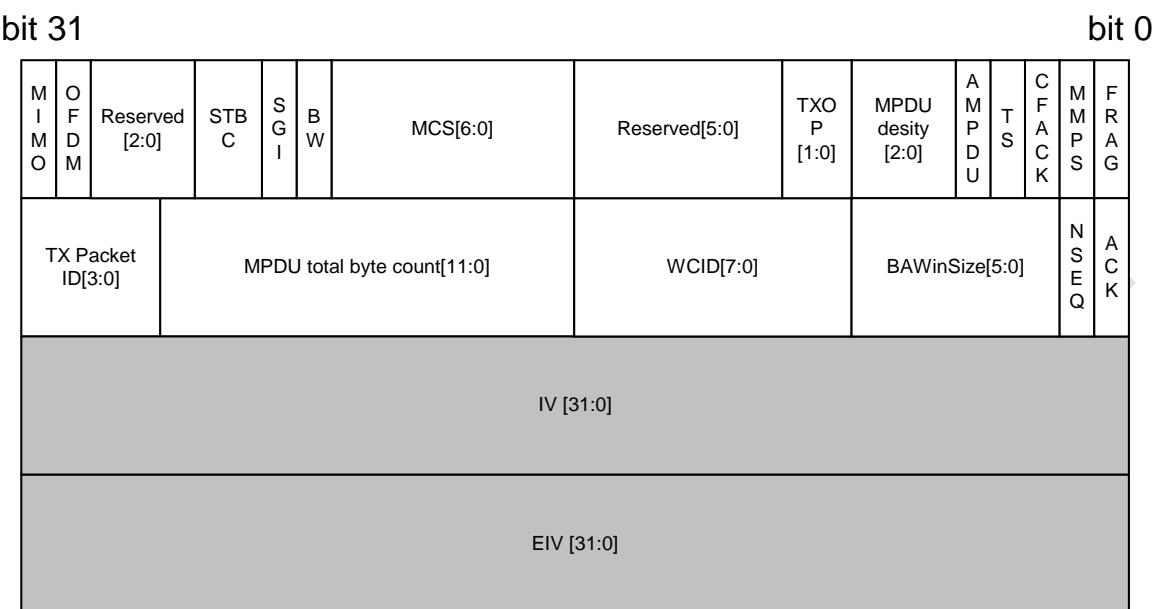
**3.23.1.2 TXWI format**


Fig. 3-23-3 TXWI format

- **FRAG:** 1: to inform TKIP engine this is a fragment, so that TKIP MIC is appended by driver at the last fragment; hardware TKIP engine only need to insert IV/EIV and ICV.
- **MMPS:** 1: the remote peer is in dynamic MIMO-PS mode
- **CFACK:** 1: if an ACK is required to the same peer as this outgoing DATA frame, then MAC TX will send a single DATA+CFACK frame instead of separate ACK and DATA frames. 0: no piggyback ACK allowed for the RA of this frame.
- **TS:** 1: This is a BEACON or ProbeResponse frame and MAC needs to auto insert 8-byte timestamp after 802.11 WLAN header.
- **AMPDU:** this frame is eligible for AMPDU. MAC TX will aggregate subsequent outgoing frames having <same RA, same TID, AMPDU=1> whenever TXOP allows. Even there's only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC will still package it as AMPDU with implicit BAR. This adds only 4-byte AMPDU delimiter overhead into the outgoing frame and imply the response frame is a BA instead of ACK. NOTE: driver should set AMPDU=1 only after a BA session is successfully negotiated, because Block ACK is the only way to acknowledge in AMPDU case.
- **MPDU density:** 1/4usec ~ 16usec per-peer parameter used in outgoing A-MPDU. (This field complies with the "minimum MDPU Starting Spacing" of the A-MPDU parameter field of draft 1.08).
  - 000- no restriction
  - 001- 1/4 μsec
  - 010- 1/2 μsec
  - 011- 1 μsec
  - 100- 2 μsec
  - 101- 4 μsec
  - 110- 8 μsec
  - 111- 16 μsec
- **TXOP:** TX back off mode. 0: HT TXOP rule; 1: PIFS TX; 2: SIFS (only when previous frame exchange is successful); 3: Back off.
- **NDPS:** Number of stream in NDP, 0: 1s, 1: 2s, 2: 3s, 3: 4s
- **NDPBW:** NDP bandwidth, 0: 20MHz, 1: 40MHz
- **TXBFK:** Disable TX auto fallback for this frame, 1: disable, 0: follow the register setting
- **TXRPT:** TX report tag. Set to 1: TX\_REPROT\_CNT increase by one. Set to 0: do nothing.
- **"MCS/BW/ShortGI/PHY mode":** TX data rate & MIMO parameters for this outgoing frame to be filled

into BBP

- **ITXB<sub>F</sub>**: Implicit TxBF enable
- **SOUND**: Sounding packet enable
- **ETXB<sub>F</sub>**: Explicit TxBF enable
- **ACK**: this bit informs MAC to wait for ACK or not after transmission of the frame. Event though QOD DATA frame has ACK policy in its QOS CONTROL field, MAC TX solely depends on this ACK bit to decide waiting of ACK or not.
- **NSEQ**: 1: to use the special h/w SEQ number register in MAC block.
- **BA window size**: tell MAC the maximum number of to-be-BAed frames is allowed of the RA (RA's BA re-ordering buffer size)
- **WCID (Wireless Client Index)** : lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. TX rate, TX power, pair-wise KEY, IV, EIV,). This index has consistent meaning in both driver and hardware.
- **MSDU total byte count**: total length of this frame.
- **Packet ID**: as a cookie specified by driver and will be latched into the TX result register stack. Driver use this field to identify special frame's TX result.
- **IV**: used by encryption engine.
- **EIV**: used by encryption engine.

### 3.23.2 RX descriptor ring

The RX descriptor (the “**RXD**”) specifies the location to place the payload of the received frame (the RX payload) and the associated receiving information (the “**RXWI**”). One RXD serves for one receiving frame. Only SDP0 and SDL0 are useful in the RXD. The RXD is arranged in the RXD ring in serial. The hardware links the RXWI and RX payload in serial and place it to the location specified in SDP0. See below diagram.

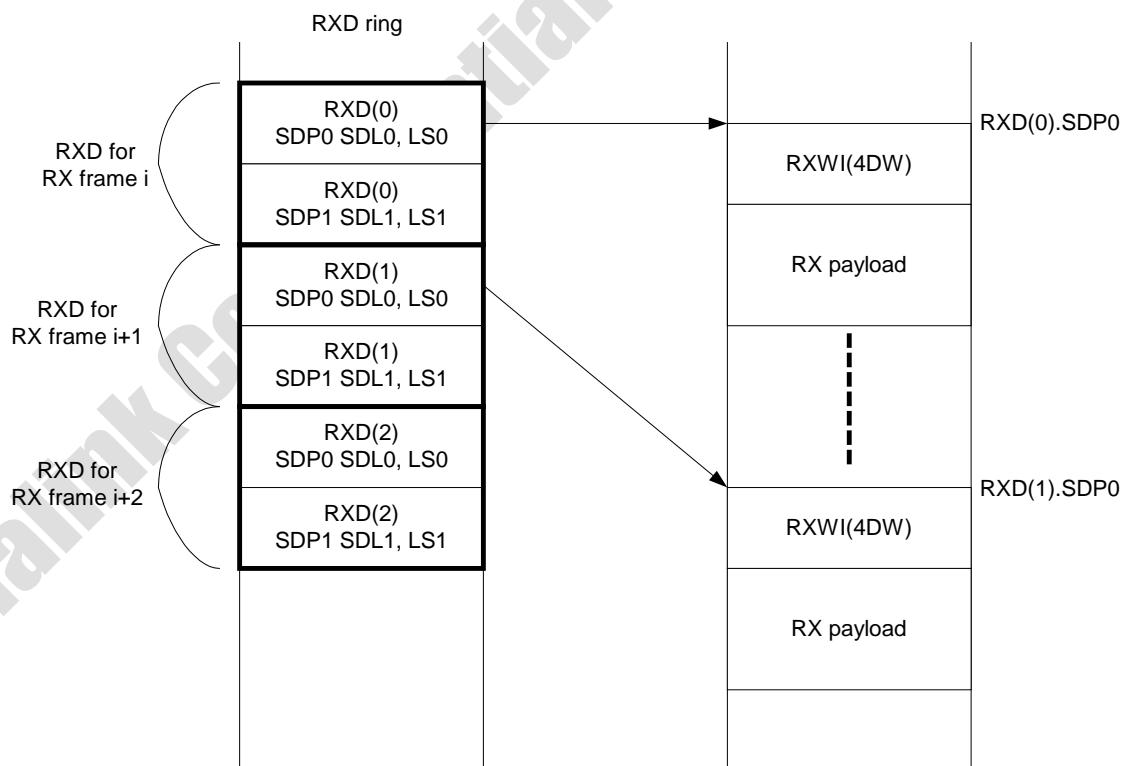


Fig. 3-23-4 RX descriptor ring

### 3.23.2.1 RX descriptor format

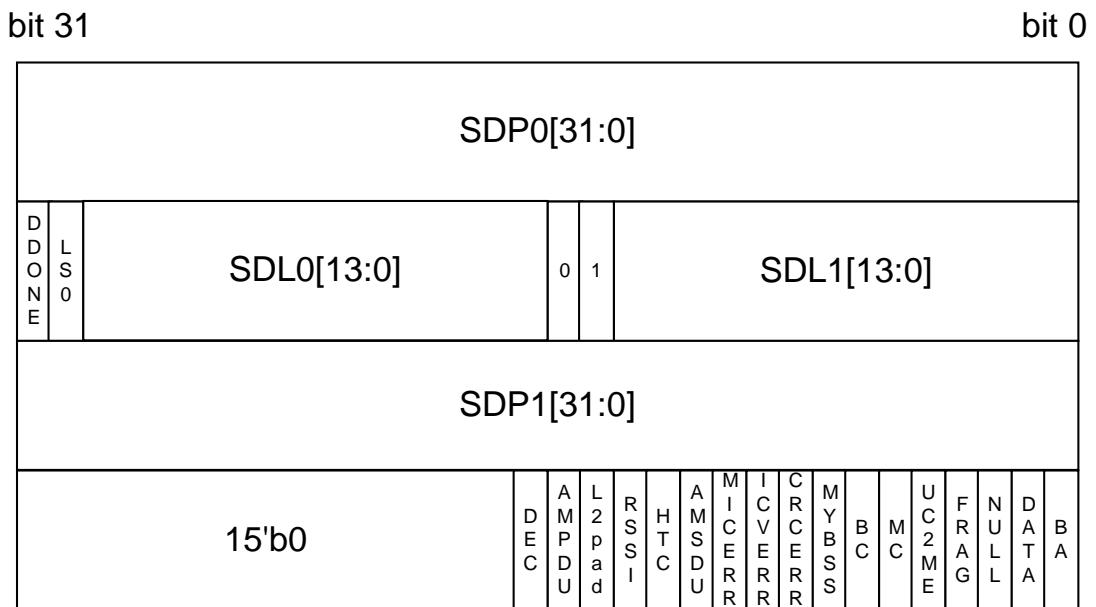


Fig. 3-23-5 RX descriptor format

Following fields are driver-specified.

- ◆ **SDP0:** Segment Data Pointer 0.
- ◆ **SDL0:** Segment Data Length for the data pointed by SDP0.
- ◆ **SDP1:** Segment Data Pointer 1.
- ◆ **SDL1:** Segment Data Length for the data pointed by SDP1.
- ◆ **DDONE:** DMA Done. DMA has moved the RX frame to the specified location. Set by hardware and cleared by driver.

Following fields are filled by hardware.

- ◆ **BA:** the received frame is part of BA session, need to do re-ordering
- ◆ **DATA:** 1: the received frame is DATA type
- ◆ **NULL:** 1: the received frame has sub-type NULL/QOS-NUL
- ◆ **FRAG:** 1: the receive frame is a fragment
- ◆ **UC2ME:** 1: the received frame ADDR1 = my MAC address
- ◆ **MC:** 1: the received frame ADDR1 = multicast
- ◆ **BC:** 1: the received frame ADDR1 = ff:ff:ff:ff:ff:ff
- ◆ **MyBSS:** 1: the received frame BSSID is one of my BSS (as an AP, max 4 BSSID supported)
- ◆ **CRC error:** 1: the received frame is CRC error
- ◆ **ICV error:** 1: the received frame is ICV error
- ◆ **MIC error:** 1: the received frame is MIC error (RX CNRL register should support individual pass-up error frame to driver in order to implement MIC error detection feature)
- ◆ **AMSDU:** the received frame is in A-MSDU sub frame format which is <802.3 + MSDU + padding>
- ◆ **HTC:** 1: this received frame came with HTC field, 0: no HTC field
- ◆ **RSSI:** 1: RSSI information available in RSSI0, RSSI1, RSSI2 fields
- ◆ **L2Pad:** 1: the L2 header is recognizable and been 2-byte-padded to ensure payload to align at 4-byte boundary. 0: L2 header not extra padded
- ◆ **AMPDU:** 1: this is an AMPDU segregated frame
- ◆ **DEC:** 1: this is a decrypted frame

### 3.23.2.2 RXWI format

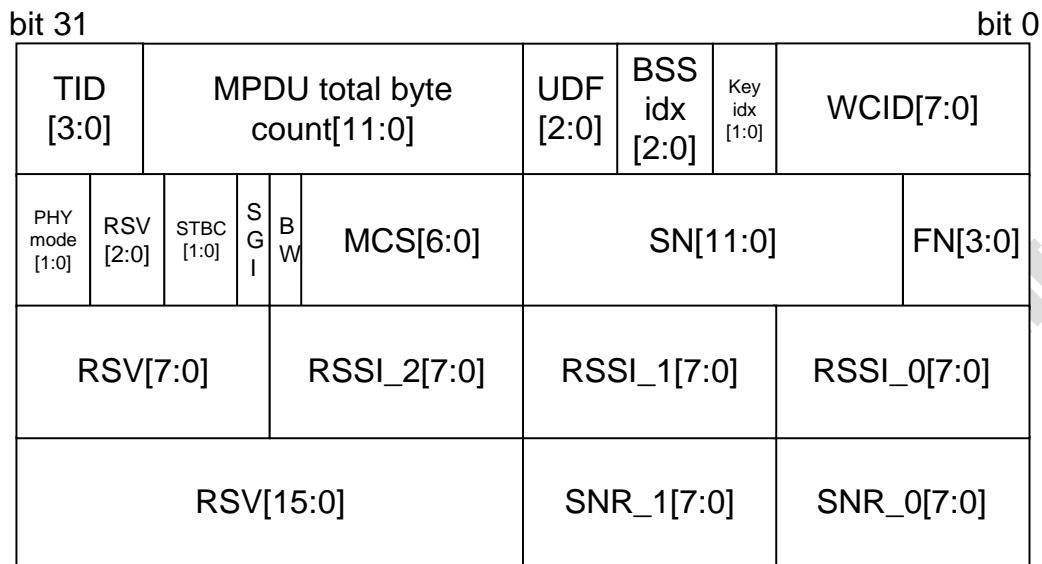


Fig. 3-23-6 RXWI format

- **WCID:** index of ADDR2 in the pair wise KEY table. This value uniquely identifies the TA. WCID=255 means not found.
- **KEY Index:** 0~3 extracted from IV field. For driver reference only, no particular usage so far.
- **BSSID index:** 0~7 for BSSID0~7. Extract from 802.11 header (the last three bits of BSSID field).
- **UDF:** User Defined Field.
- **MPDU total byte count:** the entire MPDU length.
- **TID:** extracted from 8002.11 QOS control field.
- **FN:** fragment number of the received MPDU. Extract from 802.11 header.
- **SN:** sequence number of the received MPDU. Used for BA re-ordering especially that AMSDU are auto segregated by hardware and lost the 802.11 header.
- **"MCS/BW/SGI/PHYmode":** RX data rate & related MIMO parameters of this frame got from PLCP header. See next section for the detail.
- **ITXBF:** Implicit TxBF enable
- **SOUND:** Sounding packet enable
- **ETXBF:** Explicit TxBF enable
- **RSSI0, RSSI1, RSSI2:** BBP reported RSSI information of the received frame.
- **SNR0, SNR1, SNR1:** BBP reported SNR information of the received frame.
- **FREQ\_OFFSET:** BBP reported Frequency offset of the received frame
- **RSSI\_ANTO:** BBP reported RSSI on antenna 0 of the received frame
- **BFSNR\_0, BFSNR\_1, BFSNR\_2:** BBP reported TxBF SNR of the received frame

### 3.23.3 Brief PHY rate format and definition

A 16-bit brief PHY rate is used in MAC hardware.

It is the same PHY rate field described in TXWI and RXWI.

Bit	Name	Description
15:14	PHY MODE	Preamble mode 0: Legacy CCK, 1: Legacy OFDM, 2: HT mix mode, 3: HT green field
13:11	-	Reserved
10:9	-	Reserved

8	SGI	Short Guard Interval, only support for HT mode 0: 800ns, 1: 400ns
7	BW	Bandwidth Support both legacy and HT modes 40Mhz in legacy mode means duplicate legacy 0: 20Mhz, 1: 40Mhz
6:0	MCS	Modulation Coding Scheme

Table. Brief PHY rate format

MODE = Legacy CCK	
MCS = 0	Long Preamble CCK 1Mbps
MCS = 1	Long Preamble CCK 2Mbps
MCS = 2	Long Preamble CCK 5.5Mbps
MCS = 3	Long Preamble CCK 11Mbps
MCS = 8	Short Preamble CCK 1Mbps * illegal rate
MCS = 9	Short Preamble CCK 2Mbps
MCS = 10	Short Preamble 5.5Mbps
MCS = 11	Short Preamble 11Mbps
Other MCS codes are reserved in legacy CCK mode.	
BW and SGI are reserved in legacy CCK mode.	
MODE = Legacy OFDM	
MCS = 0	6Mbps
MCS = 1	9Mbps
MCS = 2	12Mbps
MCS = 3	18Mbps
MCS = 4	24Mbps
MCS = 5	36Mbps
MCS = 6	48Mbps
MCS = 7	54Mbps
Other MCS code in legacy CCK mode are reserved	
When BW = 1, duplicate legacy OFDM is sent.	
SGI is reserved in legacy OFDM mode.	
MODE = HT mix mode / HT green field	
MCS = 0 (1S)	(BW=0, SGI=0) 6.5Mbps
MCS = 1	(BW=0, SGI=0) 13Mbps
MCS = 2	(BW=0, SGI=0) 19.5Mbps
MCS = 3	(BW=0, SGI=0) 26Mbps
MCS = 4	(BW=0, SGI=0) 39Mbps
MCS = 5	(BW=0, SGI=0) 52Mbps
MCS = 6	(BW=0, SGI=0) 58.5Mbps
MCS = 7	(BW=0, SGI=0) 65Mbps
MCS = 8 (2S)	(BW=0, SGI=0) 13Mbps
MCS = 9	(BW=0, SGI=0) 26Mbps
MCS = 10	(BW=0, SGI=0) 39Mbps
MCS = 11	(BW=0, SGI=0) 52Mbps
MCS = 12	(BW=0, SGI=0) 78Mbps
MCS = 13	(BW=0, SGI=0) 104Mbps
MCS = 14	(BW=0, SGI=0) 117Mbps
MCS = 15	(BW=0, SGI=0) 130Mbps
MCS = 32	(BW=1, SGI=0) HT duplicate 6Mbps

When BW=1, PHY\_RATE = PHY\_RATE \* 2

When SGI=1, PHY\_RATE = PHY\_RATE \* 10/9

The effects of BW and SGI are accumulative.

When MCS=0~7(1S), SGI option is supported. BW option is supported.

When MCS=8~15(2S), SGI option is supported. BW option is supported.

When MCS=32, only SGI option is supported. BW option is not supported. (BW =1)

Other MCS code in HT mode are reserved

Ralink confidential for cradlepoint

Draft

### **3.23.4 Driver implementation note**

#### **3.23.4.1 Instruction of down load 8051 firmware**

1. Select on-chip program memory
  - i. SYS\_CTRL.HST\_PM\_SEL (0x0400.bit[16]) = 1
2. Write firmware into program memory space, which starts at 0x2000.
3. Close on-chip program memory:
  - i. SYS\_CTRL.HST\_PM\_SEL (0x0400.bit[16]) = 0
4. 8051 starts.

#### **3.23.4.2 Instruction of initialize DMA**

1. Set base addresses and total number of descriptors:
  - i. TX\_BASE\_PTR0~TX\_BASE\_PTR5
  - ii. RX\_BASE\_PTR
  - iii. TX\_MAX\_CNT0~TX\_MAX\_CNT5
  - iv. RX\_MAX\_CNT
2. Set WMM parameters:
  - i. WMM\_AIFSN\_CFG
  - ii. WMM\_CWMIN\_CFG
  - iii. WMM\_CWMAX\_CFG
  - iv. WMM\_TXOP0\_CFG and WMM\_TXOP1\_CFG
3. Set DMA global configuration except TX\_DMA\_EN and RX\_DMA\_EN bits:
  - i. WPDMA\_GLO\_CFG
4. Set interrupt configuration:
  - i. DELAY\_INT\_CFG
5. Enable DMA interrupt:
  - i. INT\_MASK
6. Enable DMA:
  - i. WPDMA\_GLO\_CFG.TX\_DMA\_EN = 1, WPDMA\_GLO\_CFG.RX\_DMA\_EN = 1

#### **3.23.4.3 Instruction of clock control**

##### **3.23.4.3.1 Clock turn-off sequence**

1. Switch 80MHz main clock to PLL clock:
  - i. Set SYS\_CTRL.CLKSELECT = 1.
2. Turn clock off:
  - i. Set SYS\_CTRL.MAC\_CLK\_EN = 0.
  - ii. Set SYS\_CTRL.DMA\_CLK\_EN = 0.
3. Turn off PLL:
  - i. Set PWR\_PIN\_CFG.IO\_PLL\_PD = 1.

##### **3.23.4.3.2 Clock turn-on sequence**

1. Turn on PLL:
  - i. Set PWR\_PIN\_CFG.IO\_PLL\_PD = 0.
2. Waiting at least \$bbp\_pll\_ready for PLL clock stable.
3. Turn on clock:
  - i. Set SYS\_CTRL.MAC\_CLK\_EN = 1.
  - ii. Set SYS\_CTRL.DMA\_CLK\_EN = 1.

### **3.23.4.4 Instruction of TX/RX control**

#### **3.23.4.4.1 Freeze TX and RX sequence**

1. Disable DMA TX:
  - i. Set WPDMA\_GLO\_CFG..TX\_DMA\_EN = 0.
2. Polling until DMA TX becomes idle and PBF TX queue becomes empty:
  - i. Polling WPDMA\_GLO\_CFG. TX\_DMA\_BUSY = 0.
  - ii. Polling TXRXQ\_STA.TX0Q\_STA = 2, TXRXQ\_STA.TX1Q\_STA = 2, polling TXRXQ\_STA.TX2Q\_STA = 2.
  - iii. If the polling period > \$dma\_tx\_polling\_timeout, abort power saving procedure.
3. Disable MAC TX and RX:
  - i. Set MAC\_SYS\_CTRL.MAC\_RX\_EN = 0, MAC\_SYS\_CTRL.MAC\_TX\_EN = 0.
4. Polling until MAC TX and RX is disabled:
  - i. Polling MAC\_STATUS\_REG. TX\_STATUS = 0,  
MAC\_STATUS\_REG. RX\_STATUS = 0
  - ii. If the polling period > \$mac\_polling\_timeout, abort power saving procedure.
5. Disable DMA RX:
  - i. Set WPDMA\_GLO\_CFG..RX\_DMA\_EN = 0.
6. Polling until both DMA RX becomes idle and PBF RX queue becomes empty:
  - i. Polling WPDMA\_GLO\_CFG. RX\_DMA\_BUSY = 0.
  - ii. Polling TXRXQ\_STA.RX0Q\_STA = 0x22.
  - iii. If the polling period > \$dma\_rx\_polling\_timeout, abort power saving procedure.

#### **3.23.4.4.2 Recover TX and RX sequence**

1. Enable DMA TX and RX:
  - i. Set WPDMA\_GLO\_CFG..RX\_DMA\_EN = 1.
  - ii. Set WPDMA\_GLO\_CFG..TX\_DMA\_EN = 1.
2. Enable MAC TX and RX:
  - i. Set MAC\_SYS\_CTRL.MAC\_RX\_EN = 1.
  - ii. Set MAC\_SYS\_CTRL.MAC\_TX\_EN = 1.

### **3.23.4.5 Instruction of RF power on/off sequence**

1. Power down RF components sequence
  - i. Power down RF component
2. Set PWR\_PIN\_CFG.IO\_ADDA\_PD = 1.
3. Set PWR\_PIN\_CFG.IO\_RF\_PE = 0.
4. Set TX\_PIN\_CFG.TRSW\_EN = 0.
5. Set TX\_PIN\_CFG.RFTR\_EN = 0.
6. Set TX\_PIN\_CFG.LNA\_PE\*EN = 0.
7. Set TX\_PIN\_CFG.PA\_PE\*EN = 0.
8. Enable RF components sequence
  - i. Recover the registers in previous sequence.
  - ii. Wait \$rf\_pll\_ready for RF PLL becomes stable.

**3.23.4.6 Power saving procedure**

1. Freeze TX and RX
2. Power down LED and RF components
3. Clock turn-off

**3.23.4.7 Power recovery procedure**

1. Clock turn-on
2. Enable LED and RF components
3. Recover TX and RX

**3.23.4.8 Parameters**

1. \$rf\_pll\_ready = TBD.
2. \$bbp\_pll\_ready = 500 us.
3. \$dma\_rx\_polling\_timeout = TBD.
4. \$dma\_tx\_polling\_timeout = TBD.
5. \$mac\_polling\_timeout = TBD.

Ralink confidential for cradlepoint

Draft

### 3.24 PCI/PCI Express Controller

#### 3.24.1 Features

- PCI controller
  - Supports both Host mode and Device mode.
  - Supports burst transfer to maximize memory bandwidth
  - Support maximum up to two external PCI devices
  - Fully supports PCI 2.2 compliant.
  - Zero wait state PCI data transfer. Up to 133byte/sec at 33Mhz and 266Mbyte/sec at 66Mhz
  - Support target retry, disconnect and target abort
  - Automatic transfer restart on target retry and disconnect
  - Supports all PCI specific configuration registers
- PCI Express controller
  - Supports both RC(PCI-PCI bridge) and Endpoint mode
  - Support PCIe Gen1 X1 lane
  - Support maximum one external PCI Express endpoint when RC mode

#### 3.24.2 Block Diagram

##### 3.24.2.1 Host bridge with both PCI and PCIe Slot

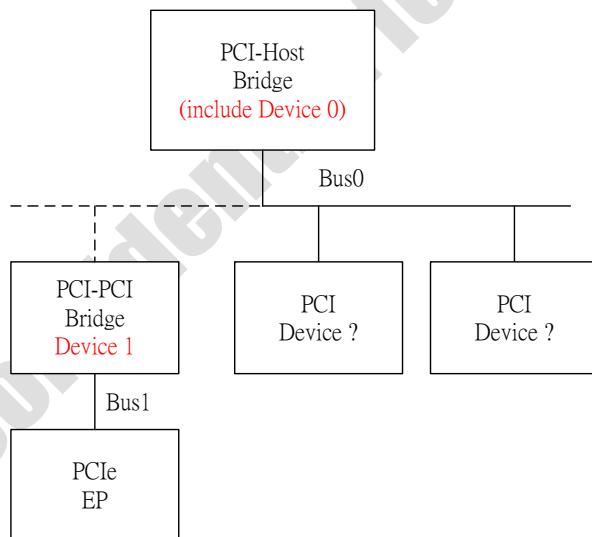


Fig. 3-24-1 PCI/PCIe Host Topology

For example, as shown in the following figure, RT3662 works as a standalone AP (Access Point).

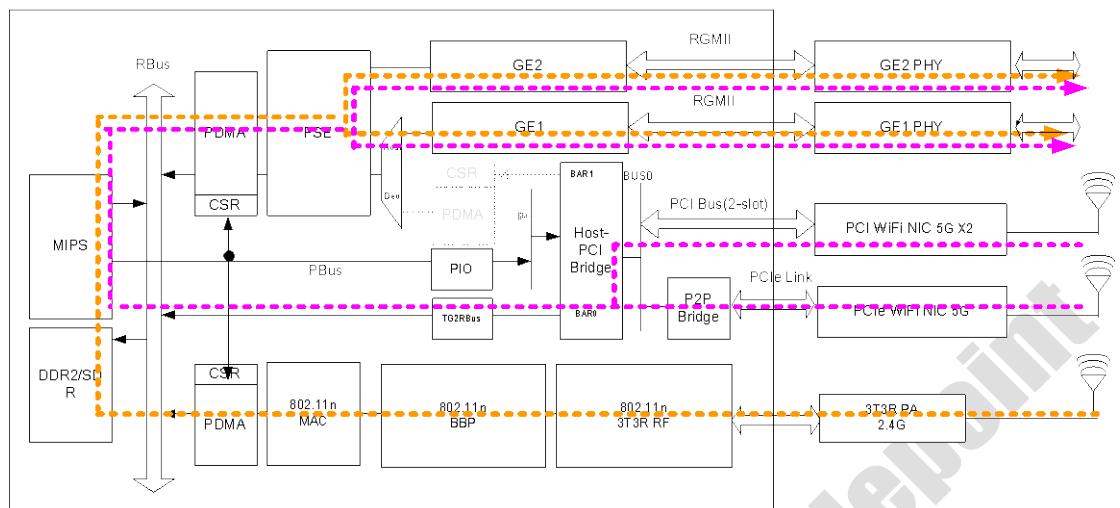
**AP Mode (as a stand alone SoC)**


Fig. 3-24-2 PCI/PCIe AP mode

**3.24.2.2 PCI/PCIe controller behaves as a PCI/PCIe Device**

For example, as shown in the following figure, RT3662 works as an intelligent NIC to offload the external 3<sup>rd</sup> party SoC by performing wireless and Ethernet packet format conversion functions.

Note 1: In this configuration, RGMII(port1), PCI, PCIe interface are exclusive. That means you can select one of them as the iNIC host interface.

Note 2: A dedicated PDMA can be seen by the 3<sup>rd</sup> party SOC when RT3662 works as an intelligent NIC when select the PCI or PCIe as the interface. The operation of this PDMA is exactly the same as the one described in Frame Engine section. The first PDMA register PDMA\_GLO\_CFG can be accessed by PCI BAR1 in PCI address space.

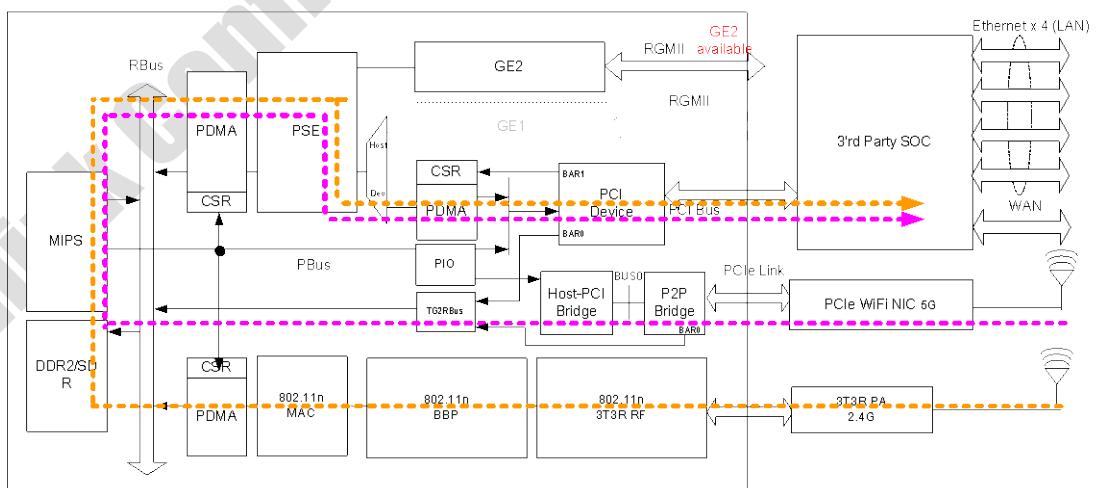
**PCI INic Mode with PCIe Host**


Fig. 3-24-3 PCI controller behaves as a PCI device

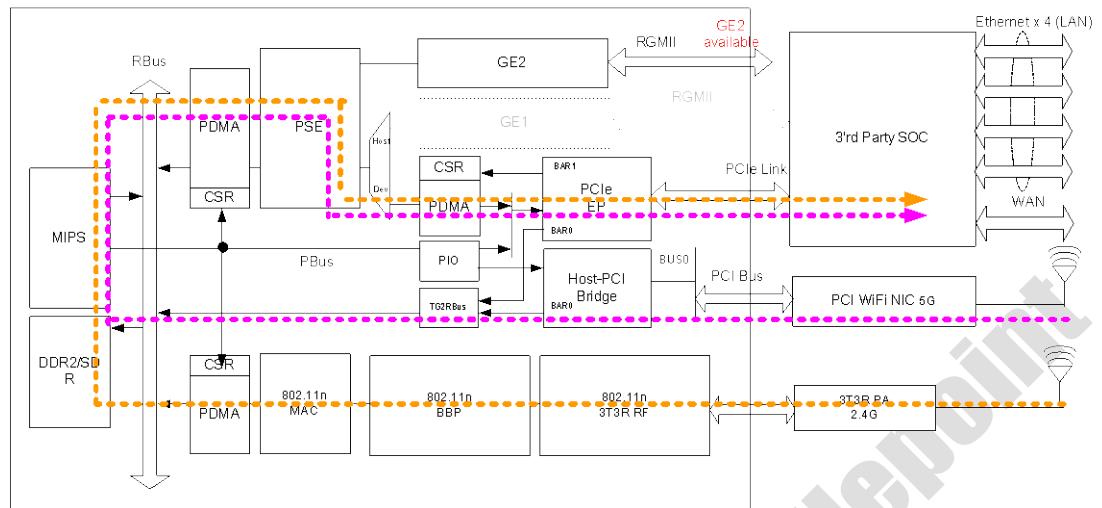
**PCIe INic Mode with PCI Host**


Fig. 3-24-4 PCIe controller behaves as a PCIe endpoint

	PCI Device only	PCI Host only	PCIe RC only	PCIe EP only	PCI-Device PCIe-RC	PCI-host PCIe-EP	PCI-PCIe Host comb	PCI-PCIe Both disable
pci_host_mode	1'b0	1'b1	Don't care	Don't care	1'b0	1'b0	1'b1	Don't care
pcie_rc_mode	1'b1	Don't care	1'b1	1'b0	1'b1	1'b1	1'b1	Don't care
pci_srst	1'b0	1'b0	1'b1	1'b1	1'b0	1'b0	1'b0	1'b1
pcie_srst	1'b1	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1
pci_share_mode	3'b000	X2:3'b011 X1:3'b010	Don't care	Don't care	3'b000	X2:3'b011 X1:3'b010	X2:3'b011 X1:3'b010	Don't care
pci_clk_en	1'b1	1'b1	1'b0	1'b0	1'b1	1'b1	1'b1	1'b0
pcie_clk_en	1'b0	1'b0	1'b1	1'b1	1'b1	1'b1	1'b1	1'b0

PCI/PCIe scenery and relative control register setting

### 3.24.2.3 Block Diagram

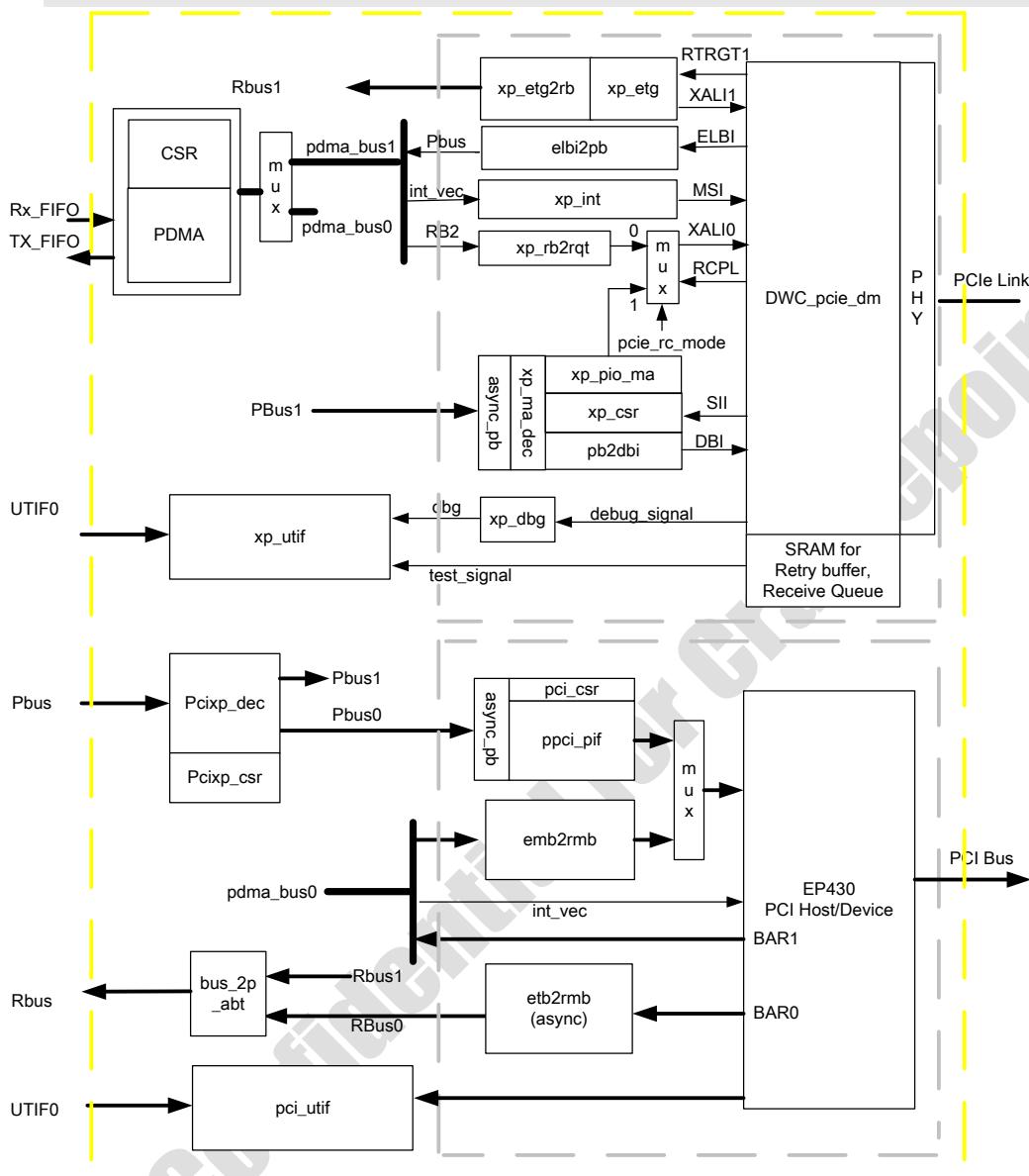


Fig. 3-24-5 PCI/PCIe host/device controller block diagram

### 3.24.3 PCI/PCIe master access in Host mode

For PCI/PCIe Memory space access, there are two approach, one is the fixed mapping from 32'h2000\_0000 to 32'h2FFF\_FFFF(256MByte) address space, the other one is PCI memory space programmable mapping which is supports via membase register + memwin offset

For PCI I/O space access, the PCI controller supports programmable mapping via iobase register + iowin offset.

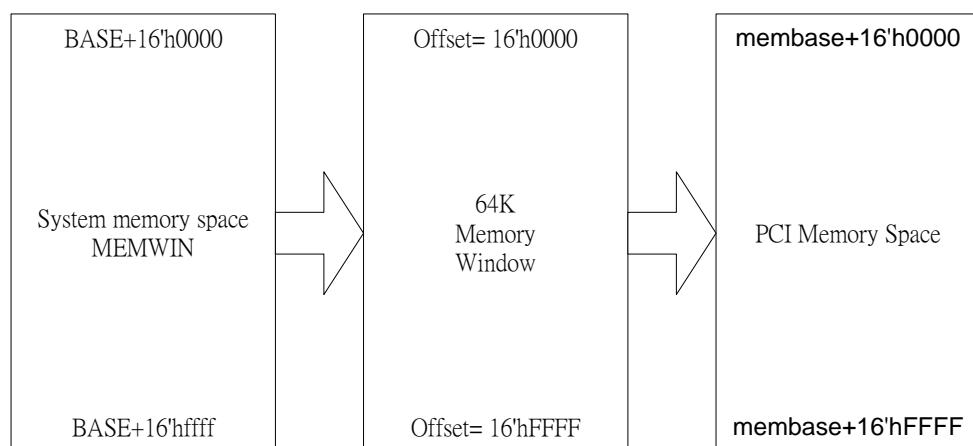


Fig. 3-24-6 PCIe memory space programmable mapping

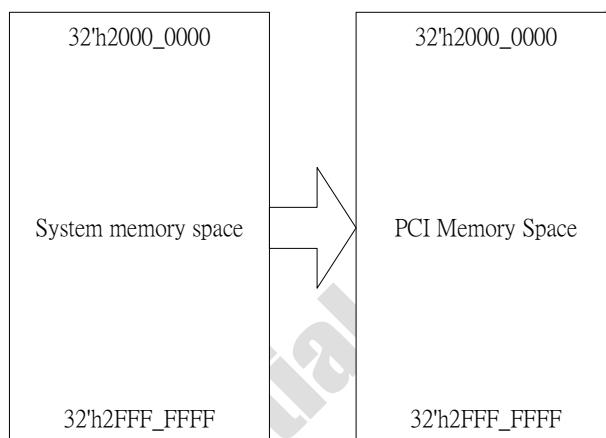


Fig. 3-24-7 PCI memory space fixed mapping

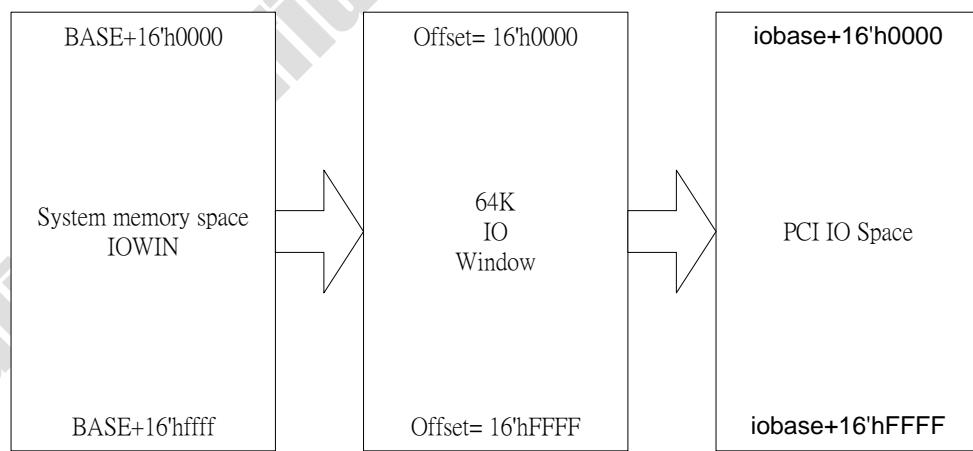


Fig. 3-24-8 PCI I/O space programmable mapping

### 3.24.3.1 PCI/PCIe Controller Host mode initialization example

- Step #1: Set ENABLE bit in ARBCTL(offset=0x80) register to enable PCI arbiter  
 Step #2: Set PCI\_HOST\_MODE bit in SYSCFG change to Host mode.  
 Step #3: Set the PCIRST bit in PCICFG register to assert reset the PCI device card, then reset the PCIRST bit to de-assert the reset output  
 Step #4: PCI driver performs PCI scan to detect PCI devices and device initialization.

### 3.24.3.2 PCI Device mode initialization example

- Step #1: Clear ENABLE bit in ARBCTL(offset=0x80)register to disable PCI arbiter.  
 Step #2: Reset PCI\_HOST\_MODE bit in SYSCFG to configure RT3662 as device mode.  
 Step #3: PCI host (3rd party SoC) scans PCI devices and setups BAR1 of RT3662  
 Step #4: 3rd Party SOC Set PDMA related registers by PCI master writes to BAR1 space. Then enable PDMA data transmit via PCI bus.

## 3.24.4 Host-PCI Bridge Register Description (base: 0x1014.0000)

PCICFG : PCI Configuration and Status Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:19	R	-	Reserved	12'b0
19:16	R/W	P2P_BR_DEVNUM	Device number setting of Virtual PCI-PCI bridge.	4'h1
15:3	R	-	Reserved	14'b0
2	R/W	-	Reserved	1'b0
1	R/W	PCIRST	PCI reset control: Writing to this bit with '1' will assert the PCIRSTn pin, writing to this bit with '0' will de-assert the PCIRSTn pin. This bit is set to '1' at chip reset, and output drive enable when in PCI Host mode (Available when PCI and/or PCIe Controller in Host mode)	1'b1
0	-	-	Reserved	1'b0

PCIINT : PCI Interrupt after enable mask(offset: 0x08)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	11'b0
20	RO	PCIINT2	PCIe interrupt input in Host mode This bit indicates the PCIe interrupt from PCIe slot	1'b0
19	RO	PCIINT1	PCI interrupt input in Host mode This bit indicates the PCI interrupt 1 occur	1'b0
18	RO	PCIINT0	PCI interrupt input in Host mode This bit indicates the PCI interrupt 0 occur	1'b0
17:15	-	-	Reserved	3'b0
14	RO	PIODONE	PIO master transfer complete	1'b0
13	RO	DETPERR	Detect Parity Error	1'b0
12	RO	SIGSERR	Signaled System Error	1'b0
11	RO	RCVMABRT	Receive Master Abort	1'b0
10	RO	RCVTABRT	Receive Target Abort	1'b0
9	RO	SIGTABRT	Signaled Target Abort	1'b0
8	RO	MASDPERR	Master Data Parity Error This bit is set if the PCI core received a data parity error	1'b0
7:0	-	-	Reserved	8'b0

PCIENA : PCI Interrupt Enable (offset: 0x0C)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	12'b0
20	R/W	PCIINT2	PCIe interrupt input in RC mode	1'b0

			1: Enable PCIe interrupt 0: Disable PCIe interrupt	
19	R/W	PCIINT1	PCI interrupt B input in Host mode 1: Enable PCI interrupt 1 0: Disable PCI interrupt 1	1'b0
18	R/W	PCIINT0	PCI interrupt A input in Host mode 1: Enable PCI interrupt 0 0: Disable PCI interrupt 0	1'b0
17:15	-	-	Reserved	3'b0
14	R/W	PIODONE	PIO master transfer complete interrupt 1:Enable 0:Disable	1'b0
13	R/W	DETPERR	Detect Parity Error interrupt 1:Enable 0:Disable	1'b0
12	R/W	SIGSERR	Signaled System Error interrupt 1:Enable 0:Disable	1'b0
11	R/W	RCVMABRT	Receive Master Abort interrupt 1:Enable 0:Disable	1'b0
10	R/W	RCVTABRT	Receive Target Abort interrupt 1:Enable 0:Disable	1'b0
9	R/W	SIGTABRT	Signaled Target Abort interrupt 1:Enable 0:Disable	1'b0
8	R/W	MASDPERR	Master Data Parity Error interrupt 1:Enable 0:Disable	1'b0
7:0	-	-	Reserved	8'b0

CFGADDR : CONFIG\_ADDR register (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	4'b0
27:24	R/W	EXTREGNUM	Extent Register Number, only avail for PCIe	4'b0
23:16	R/W	BUSNUM	Bus Number	8'b0
15:11	R/W	DEVICENUM	Device Number	5'b0
10:8	R/W	FUNNUM	Function Number	3'b0
7:2	R/W	REGNUM	Register Number	6'b0
1:0			Reserved	2'b0

CFGDATA : CONFIG\_DATA Register (offset: 0x024)

Bits	Type	Name	Description	Initial value
31:0	R/W	CFGDATA	CONFIG_DATA Register Write to or read from this register will generates a Configuration Cycle in Host mode.	Unknow

MEMBASE Base Address for Memory Space Window (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:16	R/W	MEMBASE	Base Address for Memory Space window This register specifies the base address for master PIO accesses to external PCI memory space. When a firmware accesses any of the MEMWIN registers, the PCI Controller will bus master a single transfer in memory mode to the address specified at window address (0 - 1F hex) plus MEMBASE.	16'b0

			Note: This register is only used when the PCI core is functioning as a master.	
15:0	-	-	Reserved	16'b0

**IOBASE** : Base Address for IO Space Window (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:16	R/W	IOBASE	Base Address for IO Space window This register specifies the base address for master PIO accesses to external PCI I/O space. When an firmware accesses any of the IOWIN registers, the PCI Controller will bus master a single transfer in I/O mode to the address specified at window address (0 - 1F hex) plus IOBASE. Note: This register is only used when the PCI core is functioning as a master.	16'b0
15:0	-	-	Reserved	16'b0

**ARBCTL** : PCI Arbiter Control (offset: 0x80)

Bits	Type	Name	Description	Initial value
31:7	-	-	Reserved	25'b0
6:4	R/W	PRIORVD	0: Requestor 0 (PCI Host)has highest priority than others 1: Requestor 1 (PCI Device on Slot0)has highest priority than others 2: Requestor 2 (PCI Device on Slot 1) has highest priority than others 3: Default priorities are used 4: Default priorities are used 5: Default priorities are used 6: Default priorities are used 7: Default priorities are used	3'b111
3:2	R/W	ARBMODE	0: Arbitration scheme is Butterfly 1: Arbitration scheme is Fixed Priority 2: Arbitration scheme is Rotating (Round Robin) Priority 3: Reserved	2'b10
1	-	-	Reserved	1'b0
0	R/W	ENABLE	Enable Arbiter	1'b0

This register is only available when the PCI control is set in host mode

**MEMWINx** : PCI Memory Space Access Window (offset: 0x00010000-0x0001ffff)

Bits	Type	Name	Description	Initial value
31:0	R/W	MEMWIN	PCI Memory Space Access Window Writing to this register will initiate a bus master write access to an external PCI device's memory space; reading this register will initiate a bus master read access to an external PCI device's memory space. The address accessed is specified as requested address ('0' if MEMWIN00 is accessed, '4' if MEMWIN04 is accessed, etc.) plus MEMBASE.	32'b0

**IOWINx** : PCI IO Space Access Window (offset: 0x00020000-0x0002ffff)

Bits	Type	Name	Description	Initial value
31:0	R/W	IOWIN	PCI IO Space Access Window Writing to this register will initiate a bus master write access to an external PCI device's IO space; reading this register will initiate a bus master read access to an external PCI device's IO space. The address accessed is specified as requested address ('0' if IOWIN00 is accessed, '4' if IOWIN04 is accessed, etc.) plus IOBASE.	32'b0

		Note: This register is only used when the PCI core is functioning as a master.	
--	--	--	--

Note: The description of the PDMA that is controlled by the external host when RT3662 works as PCI/PCIe intelligent NIC is not shown here. Please refer to the register description of PDMA of Frame Engine (see next chapter) for details.

### 3.24.5 PCI Host/Dev Control Register Description (base: 0x1014.1000)

BAROSETUP : Setup for BAR0 (offset: 0x10)

Bits	Type	Name	Description	Initial value																																				
31:16	R/W	BAROMSK	Setup for Base Address Register BAR0 When the mask bit is '1', the corresponding address bit will be masked as a hit as if no address comparison has been made. When the mask bit is '0', the corresponding address bit will be used for address comparison to determine an address hit. Each base address register can be mapped from 64KB to 2GB. The mask bit will be ignored when the corresponding enable bit is '0'. <table border="1"> <tr><td>BAROMSK[31:16]</td><td>Space</td></tr> <tr><td>Others</td><td>Not support</td></tr> <tr><td>0111111111111111</td><td>2G</td></tr> <tr><td>0011111111111111</td><td>1G</td></tr> <tr><td>0001111111111111</td><td>512M</td></tr> <tr><td>0000111111111111</td><td>256M</td></tr> <tr><td>0000011111111111</td><td>128M</td></tr> <tr><td>0000001111111111</td><td>64M</td></tr> <tr><td>0000000111111111</td><td>32M</td></tr> <tr><td>0000000011111111</td><td>16M</td></tr> <tr><td>0000000001111111</td><td>8M</td></tr> <tr><td>0000000000111111</td><td>4M</td></tr> <tr><td>0000000000011111</td><td>2M</td></tr> <tr><td>0000000000001111</td><td>1M</td></tr> <tr><td>0000000000000111</td><td>512K</td></tr> <tr><td>0000000000000011</td><td>256K</td></tr> <tr><td>0000000000000001</td><td>128K</td></tr> <tr><td>0000000000000000</td><td>64K</td></tr> </table>	BAROMSK[31:16]	Space	Others	Not support	0111111111111111	2G	0011111111111111	1G	0001111111111111	512M	0000111111111111	256M	0000011111111111	128M	0000001111111111	64M	0000000111111111	32M	0000000011111111	16M	0000000001111111	8M	0000000000111111	4M	0000000000011111	2M	0000000000001111	1M	0000000000000111	512K	0000000000000011	256K	0000000000000001	128K	0000000000000000	64K	16'b0
BAROMSK[31:16]	Space																																							
Others	Not support																																							
0111111111111111	2G																																							
0011111111111111	1G																																							
0001111111111111	512M																																							
0000111111111111	256M																																							
0000011111111111	128M																																							
0000001111111111	64M																																							
0000000111111111	32M																																							
0000000011111111	16M																																							
0000000001111111	8M																																							
0000000000111111	4M																																							
0000000000011111	2M																																							
0000000000001111	1M																																							
0000000000000111	512K																																							
0000000000000011	256K																																							
0000000000000001	128K																																							
0000000000000000	64K																																							
15:1	-	-	Reserved	15'b0																																				
0	R/W	BAROENB	Enable 1'b1: the BAR0 register will be created and the mask bit will be decoded. 1'b0: the BAR0 register will not be created and the mask bit will be ignored .	1'b0																																				

IMBASEBAR0 : Internal Memory Base address for BAR0 Space (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:16	R/W	IMBASEBAR0	Internal Memory Base address for BAR0 This register is used when RT3662 behaves as a PCI Host. The actually internal memory address being accessed by an external PCI host can be obtained from the following formula: RT3662 address begin accessed = (PCI Address – BAR0) +	16'b0

			IMBASEBARO.  When write to this register, the related bit will take effect when the corresponding bit in BAROMSK bit is '1' and BAROENB is '1'.	
15:0	-	-	Reserved	16'b0

PCI\_ID : PCI-Host Bridge - Vendor and Device ID (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:16	R/W	DEVID	Device ID	16'h0801
15:0	R/W	VENID	Vendor ID	16'h1814

PCI\_CLASS : PCI Class Code and Revision ID (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:8	R/W	CCODE	Class Code	16'h0d80
7:0	R/W	REVID	Revision ID	16'h0001

PCI\_SUBID : PCI Sub Vendor and Device ID (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:16	R/W	SUBSYSID	Sub System ID	16'h3883
15:0	R/W	SUBVENID	Sub Vendor ID	16'h1814

This register is valid when PCI\_HOST\_MODE = 0;

### 3.24.6 PCIe RC/EP Control Register Description (base: 0x1014.2000)

PCIE\_BAROSETUP : Setup for BAR0 of PCIe Controller (offset: 0x10)

Bits	Type	Name	Description	Initial value																																				
31:16	R/W	BAROMSK	<p>Setup for Base Address Register BAR0 When the mask bit is '1', the corresponding address bit will be masked as a hit as if no address comparison has been made. When the mask bit is '0', the corresponding address bit will be used for address comparison to determine an address hit. Each base address register can be mapped from 64KB to 2GB. The mask bit will be ignored when the corresponding enable bit is '0'.</p> <table border="1"> <tr><td>BAROMSK[31:16]</td><td>Space</td></tr> <tr><td>Others</td><td>Not support</td></tr> <tr><td>0111111111111111</td><td>2G</td></tr> <tr><td>0011111111111111</td><td>1G</td></tr> <tr><td>0001111111111111</td><td>512M</td></tr> <tr><td>0000111111111111</td><td>256M</td></tr> <tr><td>0000011111111111</td><td>128M</td></tr> <tr><td>0000001111111111</td><td>64M</td></tr> <tr><td>0000000111111111</td><td>32M</td></tr> <tr><td>0000000011111111</td><td>16M</td></tr> <tr><td>0000000001111111</td><td>8M</td></tr> <tr><td>0000000000111111</td><td>4M</td></tr> <tr><td>0000000000011111</td><td>2M</td></tr> <tr><td>0000000000001111</td><td>1M</td></tr> <tr><td>0000000000000111</td><td>512K</td></tr> <tr><td>0000000000000011</td><td>256K</td></tr> <tr><td>0000000000000001</td><td>128K</td></tr> <tr><td>0000000000000000</td><td>64K</td></tr> </table> <p>*Please set this value before the CfgWr to BAR0, else the CFGWr to BAR0 will get unknown result.</p>	BAROMSK[31:16]	Space	Others	Not support	0111111111111111	2G	0011111111111111	1G	0001111111111111	512M	0000111111111111	256M	0000011111111111	128M	0000001111111111	64M	0000000111111111	32M	0000000011111111	16M	0000000001111111	8M	0000000000111111	4M	0000000000011111	2M	0000000000001111	1M	0000000000000111	512K	0000000000000011	256K	0000000000000001	128K	0000000000000000	64K	16'h00ff
BAROMSK[31:16]	Space																																							
Others	Not support																																							
0111111111111111	2G																																							
0011111111111111	1G																																							
0001111111111111	512M																																							
0000111111111111	256M																																							
0000011111111111	128M																																							
0000001111111111	64M																																							
0000000111111111	32M																																							
0000000011111111	16M																																							
0000000001111111	8M																																							
0000000000111111	4M																																							
0000000000011111	2M																																							
0000000000001111	1M																																							
0000000000000111	512K																																							
0000000000000011	256K																																							
0000000000000001	128K																																							
0000000000000000	64K																																							

15:1	-	-	Reserved	15'b0
0	R/W	BAROENB	Enable 1'b1: the BAR0 register will be created and the mask bit will be decoded. 1'b0: the BAR0 register will not be created and the mask bit will be ignored .	1'b0

PCIE\_IMBASEBAR0 : Internal Memory Base address for BAR0 Space of PCIe Controller (offset: 0x18)

Bits	Type	Name	Description	Initial value
31:16	R/W	IMBASEBAR0	Internal Memory Base address for BAR0 This register is used when RT3662 behaves as a PCI Express RC.  The actually internal memory address being accessed by an external PCI host can be obtained from the following formula: RT3662 address begin accessed = (PCI Address – BAR0) + IMBASEBAR0.	16'b0
15:0	-	-	When write to this register, the related bit will take effect when the corresponding bit in BAROMSK bit is '1' and BAROENB is '1' .	16'b0
15:0	-	-	Reserved	16'b0

PCIE\_ID : Vendor and Device ID of PCIe Controller (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:16	R/W	DEVID	Device ID	16'h0801
15:0	R/W	VENID	Vendor ID	16'h1814

PCIE\_CLASS : Class Code and Revision ID of PCIe Controller(offset: 0x34)

Bits	Type	Name	Description	Initial value
31:8	R/W	CCODE	Class Code	16'h0d80
7:0	R/W	REVID	Revision ID	16'h0001

PCIE\_SUBID : Sub Vendor and Device ID of PCIe Controller (offset: 0x38)

Bits	Type	Name	Description	Initial value
31:16	R/W	SUBSYSID	Sub System ID	16'h3883
15:0	R/W	SUBVENID	Sub Vendor ID	16'h1814

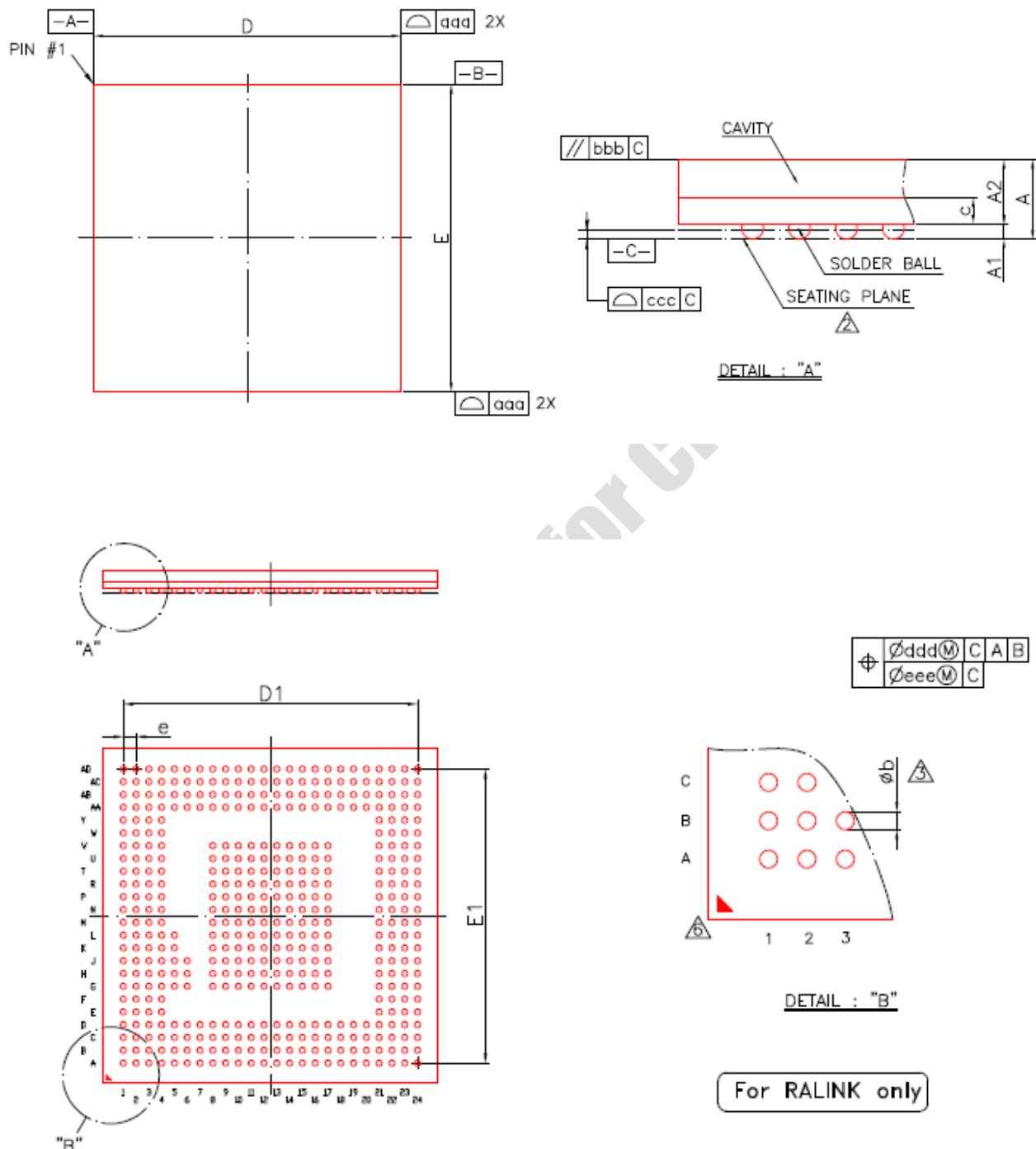
This register is valid when PCIE\_RC\_MODE = 0;

PCIE\_STATUS : PCIe Status Register (offset: 0x0050)

Bits	Type	Name	Description	Initial value
31:1	R	-	Reserved	31'b0
0	R	PCIE_LINK_UP_ST	PCIe LTSSM Link up indicator This bit will reflect the PCIe link up status User can use this bit to see if any device plug in to the slot	1'b0

## 4 Package Physical Dimension

### 4.1 TFBGA 17x17



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	16.90	17.00	17.10	0.665	0.669	0.673
E	16.90	17.00	17.10	0.665	0.669	0.673
D1	---	14.95	---	---	0.589	---
E1	---	14.95	---	---	0.589	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.15			0.006		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	24/24			24/24		

**NOTE :**

1. CONTROLLING DIMENSION : MILLIMETER.
- △ PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- △ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MO-207
- △ THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ccc

Ralink®

-231-

Draft

## 5 Revision History

Date	Revision	Author	Description
2009/10/13	1.0	Leon Chung	Initial Release

Ralink confidential for cradlepoint

*This product is not designed for use in medical, life support applications. Do not use this product in these types of equipments or applications .This document is subject to change without notice and Ralink assumes no responsibility for any inaccuracies that may be contained in this document. Ralink reserves the right to make change in the products to improve function, performance, reliability, and to attempt to supply the best product possible.*

Draft