Diamond Standard 106Micro Controller

Very Small, Very Low Power Basic 32-bit CPU

Product Brief

FEATURES

- Small, low power 32-bit RISC controller core
- Cache-less processor with memory protection unit
- 5-stage pipeline
- Dhrystone 2.1: 1.22 DMIPS/MHz
- 24/16-bit ISA with modeless switching
- Iterative 32x32 multiplier
- Separate instruction and data memory interfaces
- Integrated interrupt controller with 15 interrupts at 2 priority levels
- Integrated timer
- On-chip debugging hardware
- Embedded trace support
- Comprehensive software development environment
- AHB-lite and AXI bridges

BENEFITS

- Easy migration from 8– and 16-bit microcontrollers
- Lower total system cost due to smaller size, higher performance and better code density
- Deterministic real-time operation through optional single-cycle local instruction and data SRAMs
- Achieve high frequency: 900 MHz in 45gs process
- Multiplier provides arithmetic and DSP performance
- No memory contention between instructions and data
- Fast and flexible interrupt handling
- Drop into existing AMBA™-based SOCs

Ideal for Migrating Up from 8– or 16-bit Controllers

The Diamond Standard 106Micro controller lets you move up to a 32-bit controller, with all of the benefits of C-language programmability, without the usual area and power penalties.

Tensilica's Smallest Standard Controller

The Diamond Standard 106Micro CPU is a cache-less 32-bit controller ideal for designers looking for a basic 32-bit controller, particularly for those migrating up from an 8– or 16-bit controller. Designed for applications with requirements for minimal size and low power, the Diamond Standard 106Micro controller enables SOC architects to quickly integrate this efficient CPU in their designs.

Although the Diamond 106Micro is extremely small, it employs a 5-stage pipeline so it can achieve 650 MHz in 65gp process and up to 900 MHz in 45gs process technology. By modelessly switching between 24– and 16-bit narrow instructions, it achieves much higher code density than other 32/16-bit architectures.

The local, tightly-coupled instruction and data memory on the Diamond Standard 106Micro can be used to store performance-sensitive code and data, for example, to achieve high performance on interrupt handlers. The Diamond 106Micro has an iterative, multi-cycle (non-pipelined) 32x32 multiplier that enhances performance on arithmetic and DSP code. The processor uses a non-windowed 16-entry register file to keep area low.

The Diamond Standard 106Micro has a rich interrupt architecture with the integrated interrupt controller providing 15 interrupts, and an integrated timer. This simplifies system design since no external hardware needs to be added for these functions.

Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs.

The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16-and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance. The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions (the instructions that constitute the application program) and the average number of bits per instruction.

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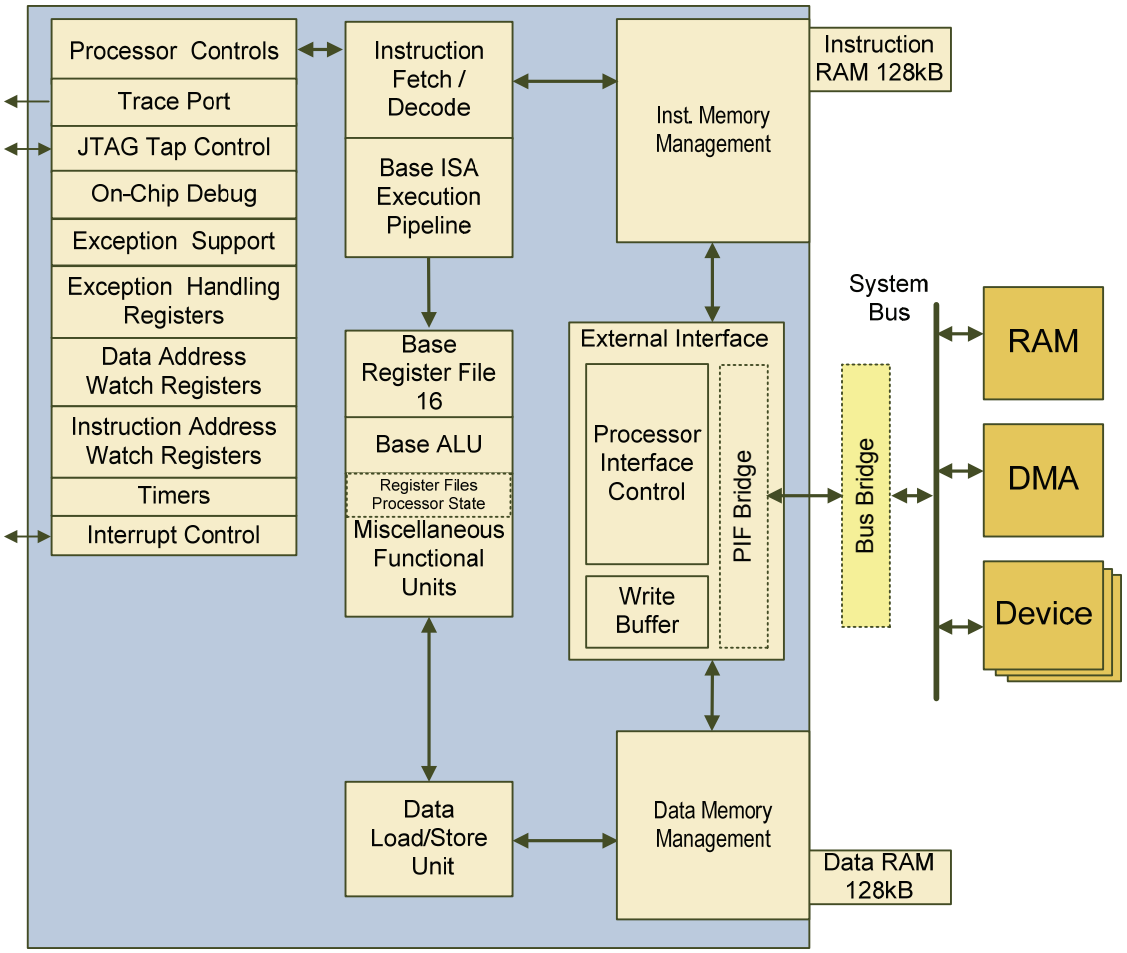

The Diamond Standard 106Micro

Instruction Set Architecture (Continued)

The use of 24- and 16-bit instruction words and compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors' small code size. The 24-/16-bit Diamond processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16- bit ISA-based RISC cores.

Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.

Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™ – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development .

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code execution performance and reduce code size. Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, source code editor, debugger, performance-modeling tool, the Xenergy™ energy estimation tool, the cache performance explorer, and a number of graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP, as well as SystemC models of the Diamond processors. For fast-functional simulation, Tensilica offers TurboXim for a 40-80x faster simulation than the ISS. See Tensilica's Software Developer's Toolkit product brief for more information.

Specifications

	65gp		65lp		45gs		40lp	
Flows:	**High-Speed**	**Low-Power**	**High-Speed**	**Low-Power**	**High-Speed**	**Low-Power**	**High-Speed**	**Low-Power**
Post-route cell area (mm^2)	0.113	0.0715	0.114	0.0667	0.0743	0.0447	0.0737	0.0456
Speed (MHz) post Prime Time	657	58	405	57	907	57	542	57
Post-Route Power (mW/MHz)	0.035	0.022	0.042	0.027	0.019	0.013	0.025	0.017

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