Pin Description

Name	Type	Direction	Description
`user_clk`	DIGITAL	IN	Clock synchronizes the operations of the memory. All inputs are sampled on rising edge of clock.
`user_rst`	DIGITAL	IN	This is the reset pin, which is active low. Reset is applied when this pin is low, and deasserted when the pin is high.
`wb_rst_i`	DIGITAL	IN	Wishbone reset input, active low. Reset is asserted when this pin is low , and released when pin is high.
`wb_clk_i`	DIGITAL	IN	Wishbone clock input. All bus signals are sampled on the rising edge of this clock.
`wbs_adr_i[31:0]`	DIGITAL	IN	This is the wishbone address input pin. When the value on this pin is `32'h3000_0004`, the read or write operation starts; otherwise, no action is taken.
`wbs_dat_i[31:0]`	DIGITAL	IN	This is the data input bus. Data is written into the memory location specified by the address

Name	Type	Direction	Description
			bits of this register during a write cycle
wbs_ack_o	DIGITAL	OUT	Output acknowledge signal. Asserted high by the slave to indicate the completion of a Wishbone bus cycle (read or write).
wbs_cyc_i	DIGITAL	IN	Input cycle signal. Asserted high by the master to indicate that a valid bus cycle (read or write) is in progress.
wbs_stb_i	DIGITAL	IN	Input strobe signal..Asserted high by the master to indicate a valid data transfer request (read or write) to the slave.
wbs_we_i	DIGITAL	IN	Input write-enable signal.When pin is low it performs a write operation. When the pin is high it performs a read operation.
wbs_sel_i[3:0]	DIGITAL	IN	These are input pins. To perform a read or write operation, SEL must be 4'b0010
wbs_dat_o[31:0]	DIGITAL	OUT	During a read operation (wbs_we_i = 0), this pin carries data from memory.

Name	Type	Direction	Description
ScanInCC	DIGITAL	IN	Scan enable input pin. When asserted high, the scan chain is activated, allowing serial test data to be shifted through for scan-based testing. When deasserted low, the scan chain is disabled, and the module operates normally in its functional mode.
ScanInDL	DIGITAL	IN	This pin is the input to the data scan chain for the user-clock-specified design. When the scan mode is enabled via the scan enable signal, serial test data is shifted into the module through this pin for scan-based testing.
ScanInDR	DIGITAL	IN	This pin is the input to the data scan chain for the Wishbone-clock-based design. When scan mode is enabled via the scan enable signal, serial test data is shifted into the module through this pin for scan-based testing. During normal functional operation, this pin remains inactive.
TM	DIGITAL	IN	When TM (Testmode)is high, memory is in testmode and normal

Name	Type	Direction	Description
			memory operation is disabled. Inputs are tied to outputs through scan chain logic.
ScanOutCC	DIGITAL	OUT	output of scan chain of data input pins.
Iref	ANALOG	IN	100 µA DC current reference input; provide a quiet, low-noise source to bias internal analog circuits.
VSS	ANALOG	IN	0 V analog ground reference.
Vcc_read	ANALOG	IN	0.3 V read rail.
Vcomp	ANALOG	IN	0.6 V comparator/reference bias input.
Bias_comp2	ANALOG	IN	0.6 V comparator bias input.
Vcc_wl_read	ANALOG	IN	0.7 V wordline read rail.
Vcc_wl_set	ANALOG	IN	1.8 V wordline set rail.
VDDA	ANALOG	IN	1.8 V analog supply.
VDDC	ANALOG	IN	1.8 V analog core digital supply.
Vbias	ANALOG	IN	1.8 V analog bias input.
Vcc_wl_reset	ANALOG	IN	2.6 V wordline reset rail.
Vcc_set	ANALOG	IN	3.3 V array “set” rail.
Vcc_reset	ANALOG	IN	3.3 V array “reset”

Name	Type	Direction	Description
`Vcc_L`	ANALOG	IN	5 V for level shifter.
`Vcc_Body`	ANALOG	IN	5 V body-bias supply.