CMOS NAND GATE CHARACTERSTICS

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Lab Slot: L15+L16

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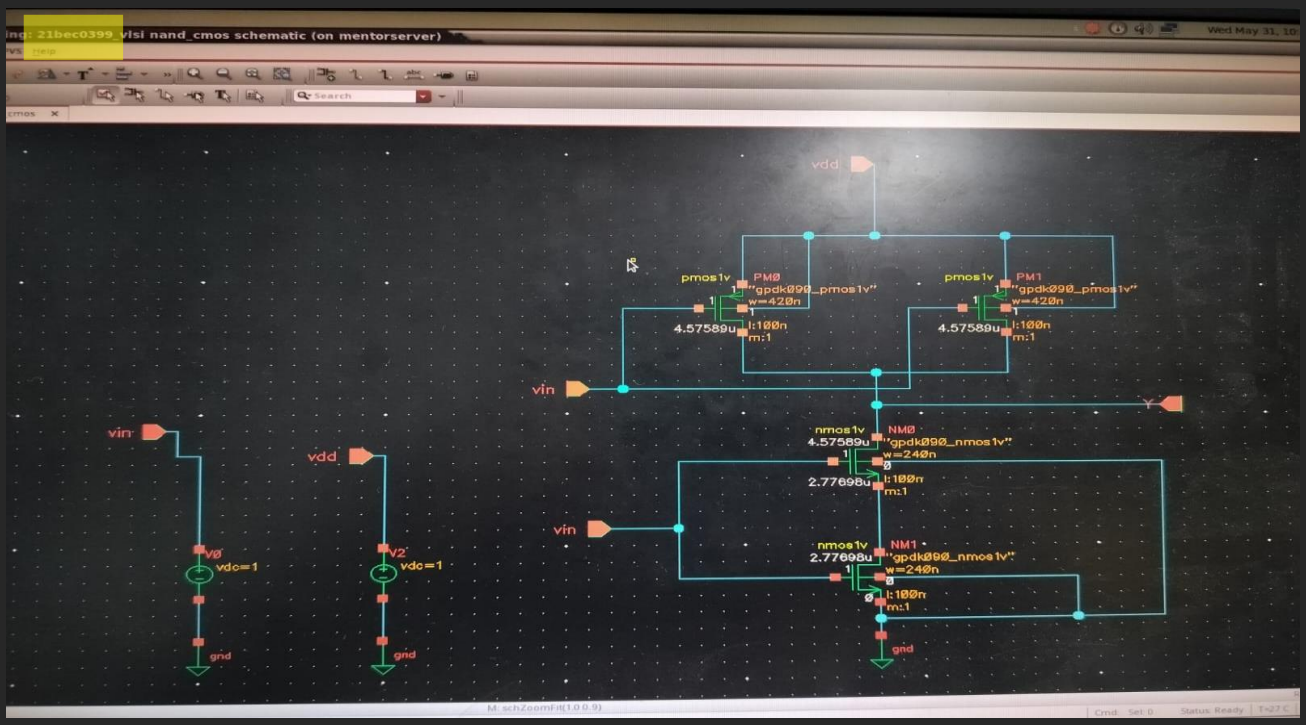
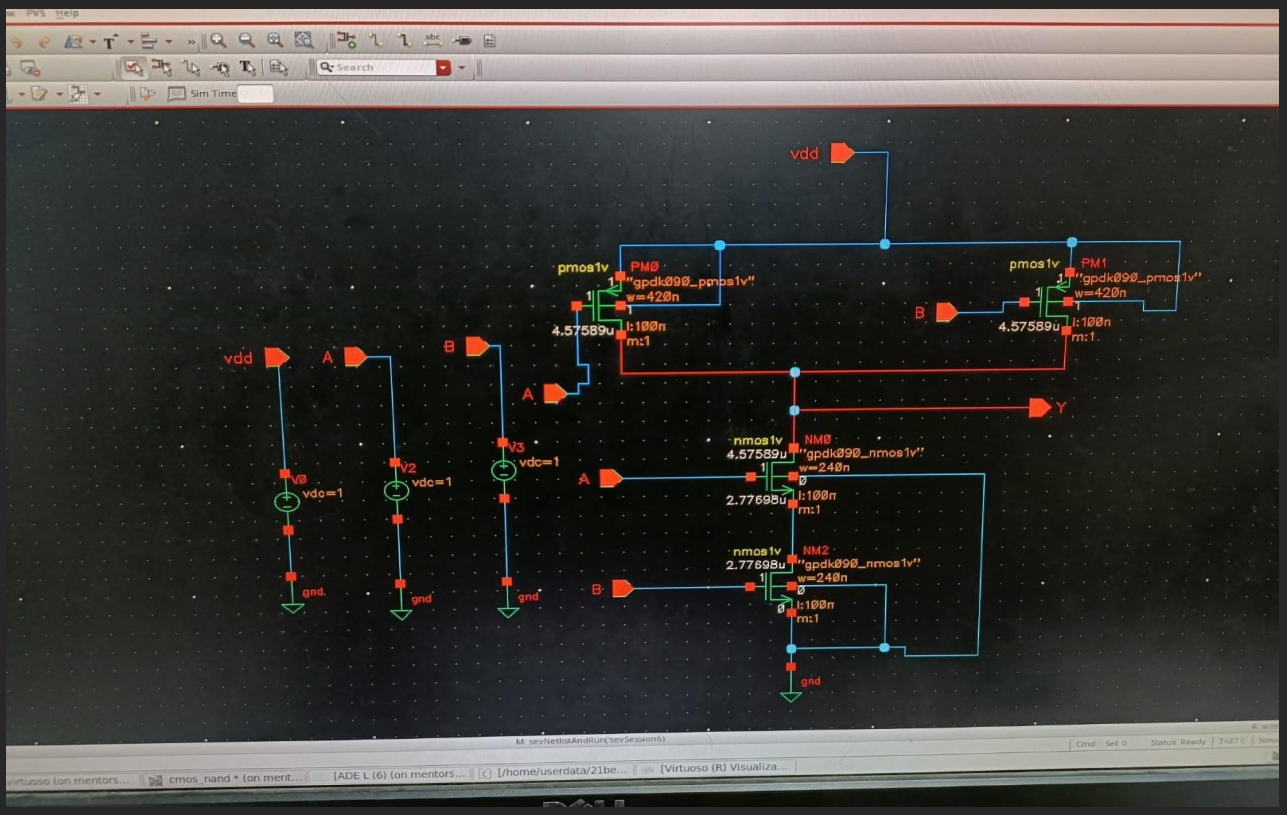
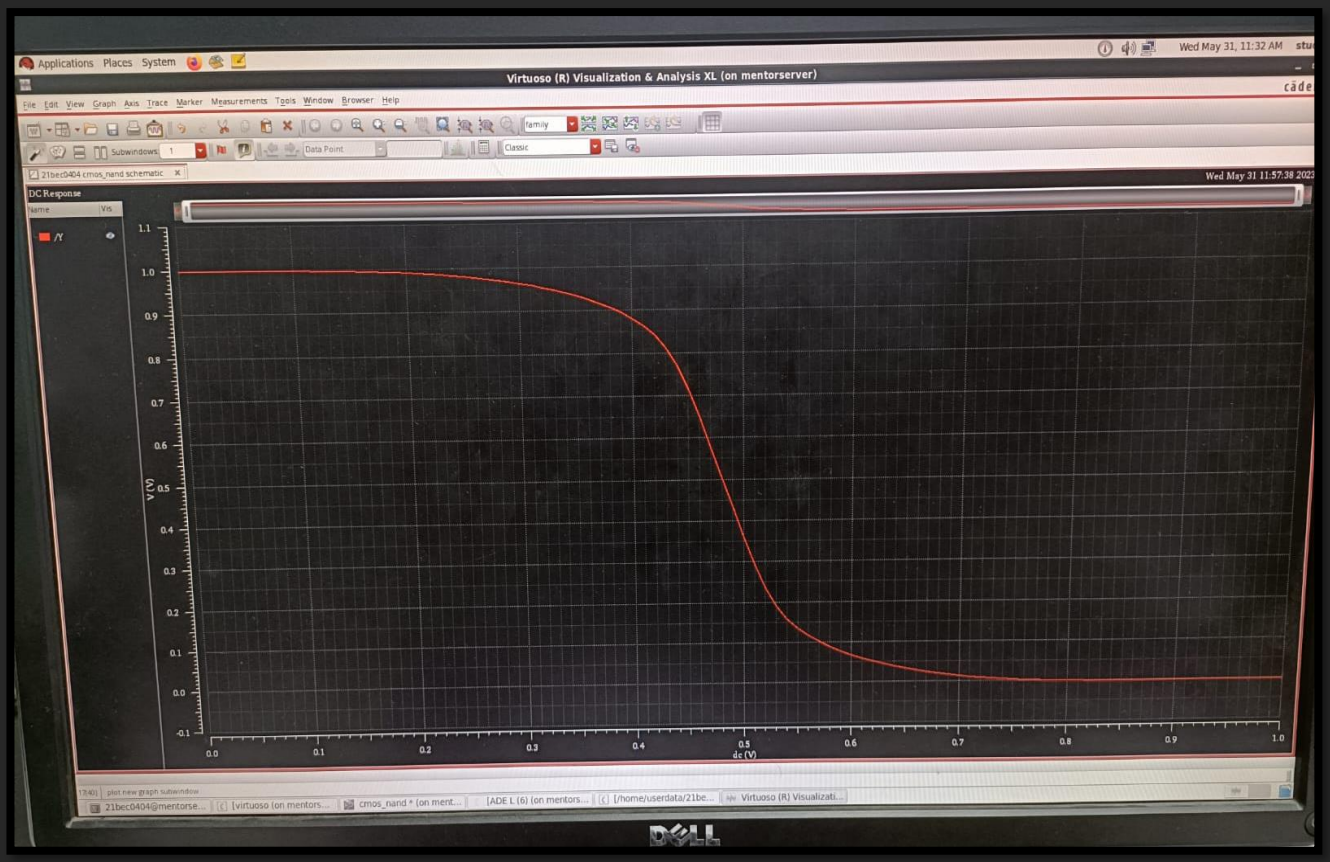
1. NAND CMOS CIRCUIT



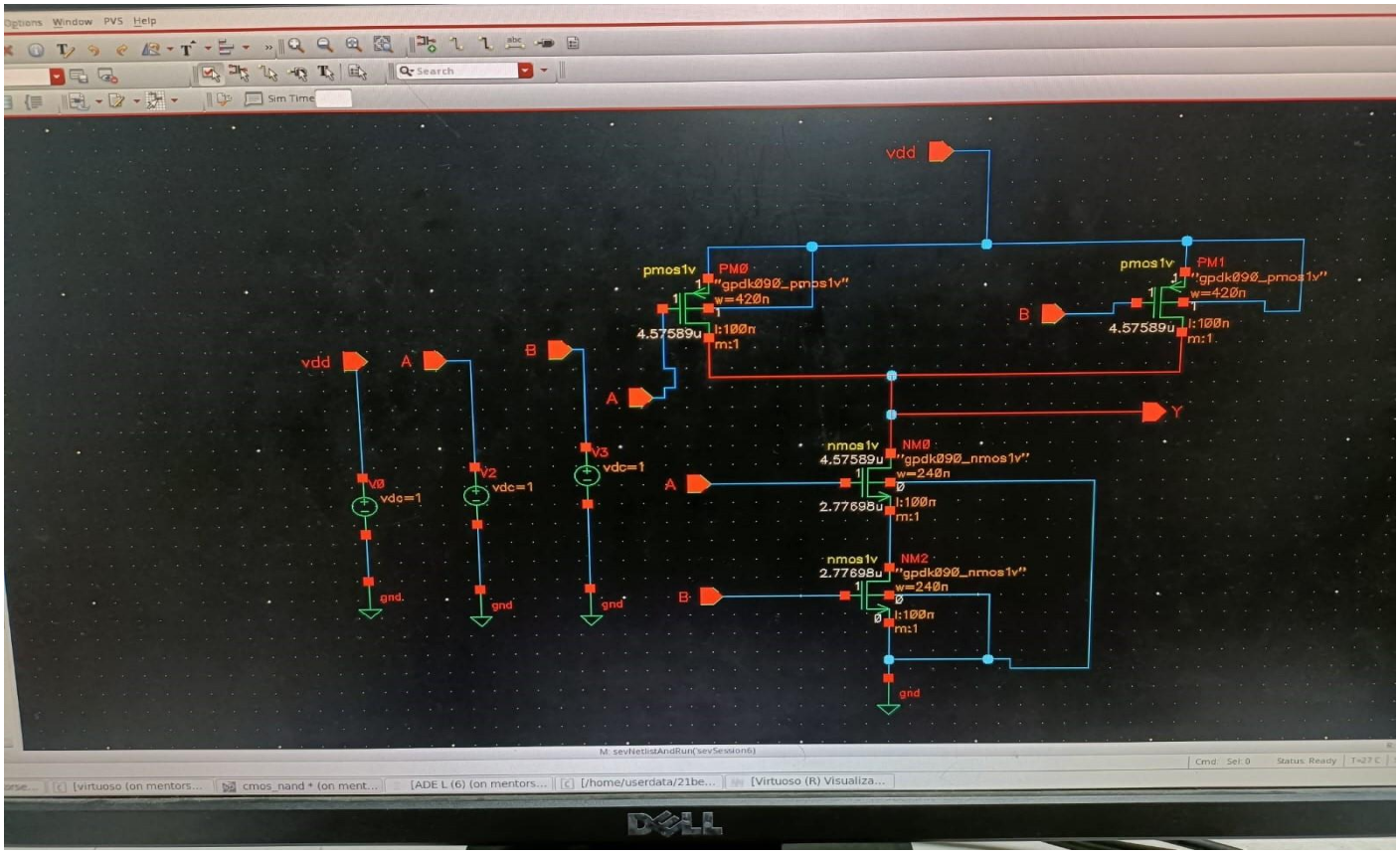
1. **CASE 1:** A=B= 0->1

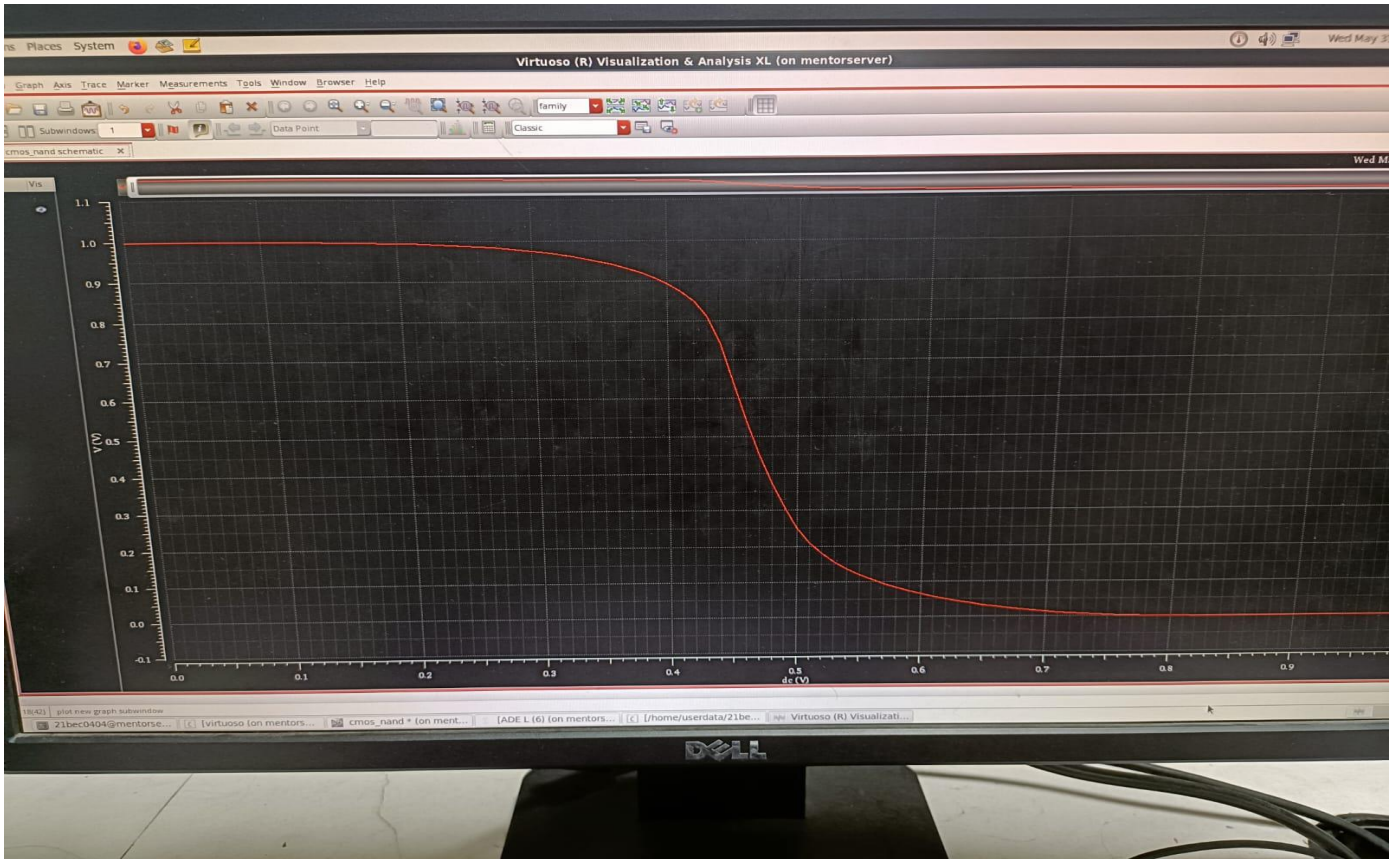
2. CASE 2 - When A=1 and B is on X-axis



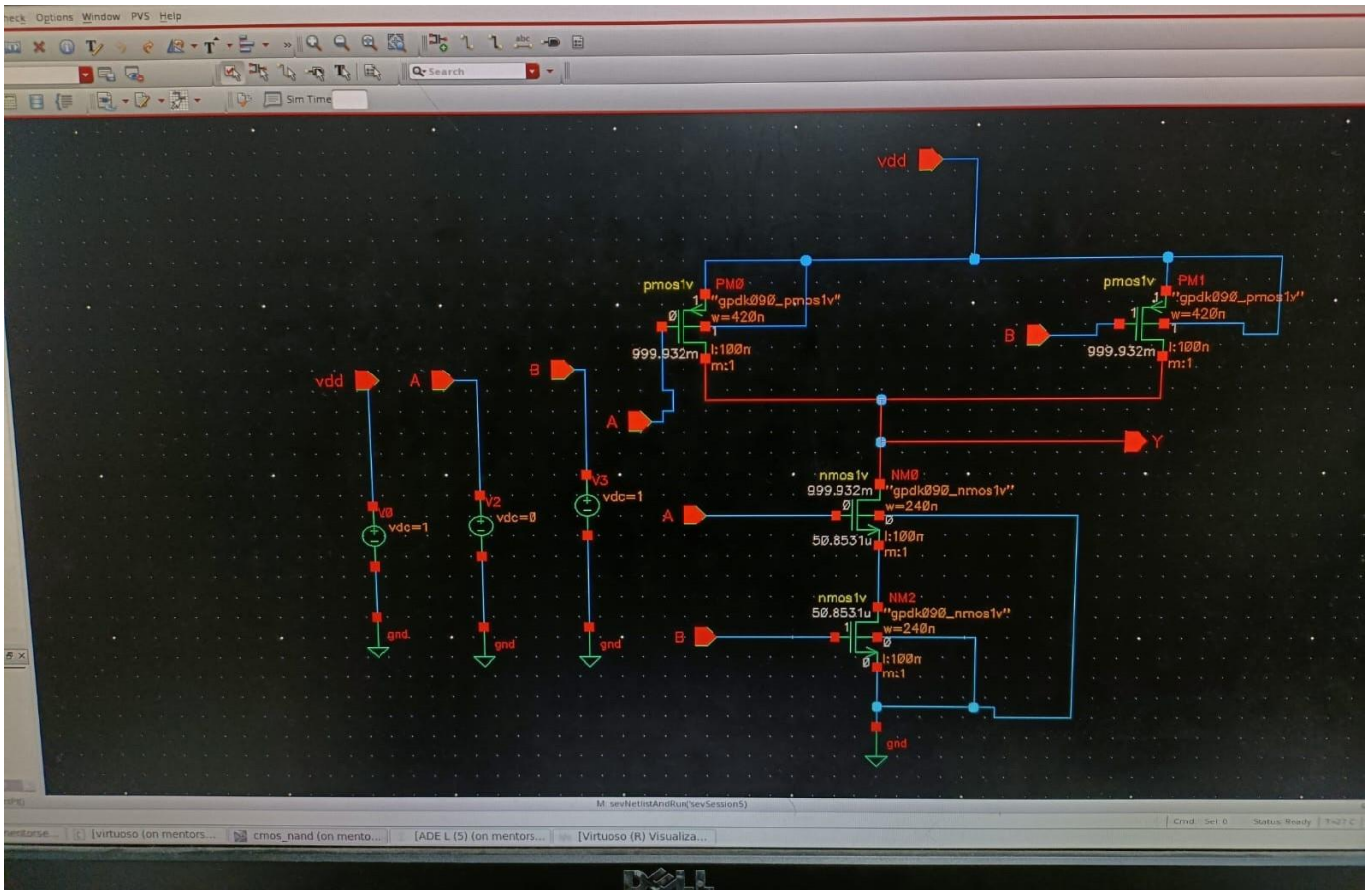


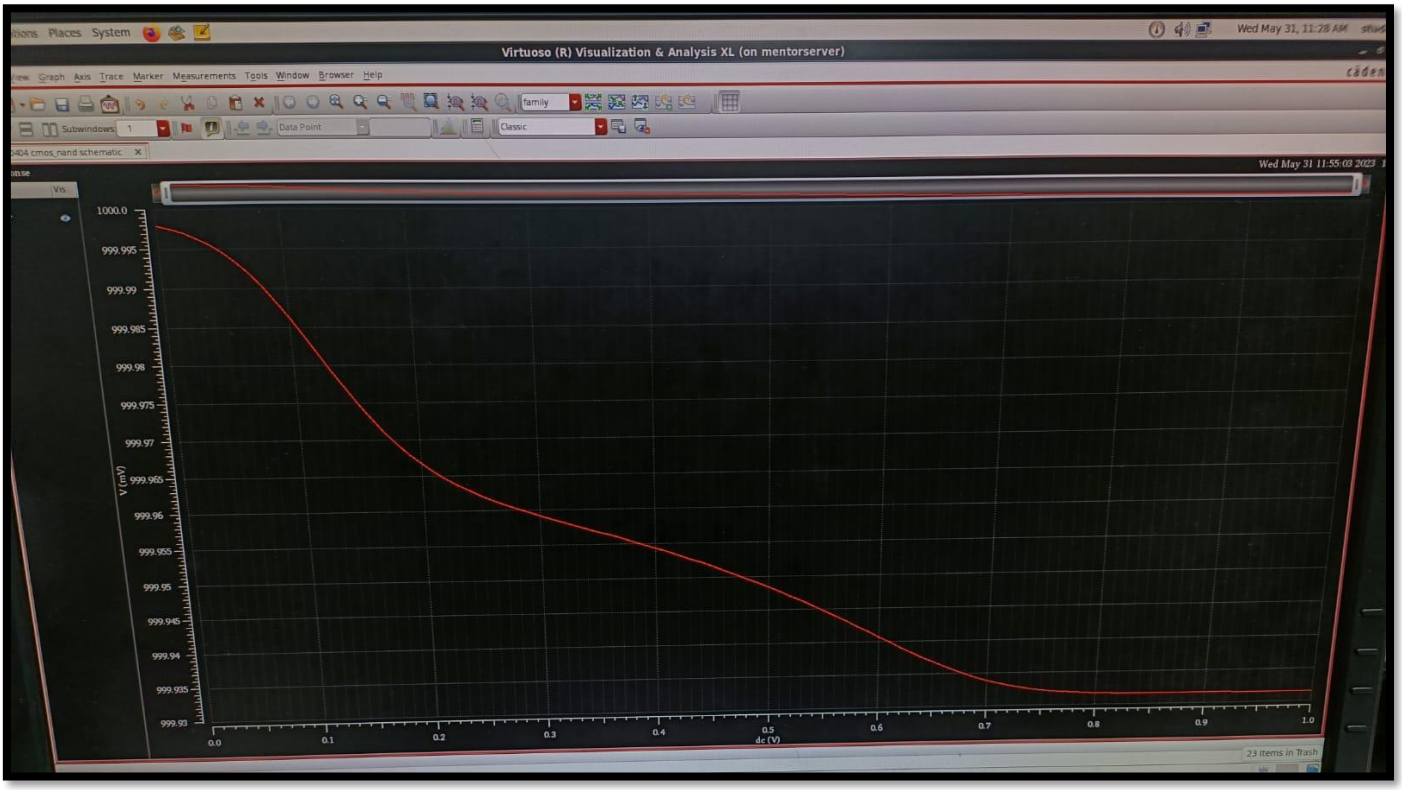
Case 3: When B=1 and A is on X-axis



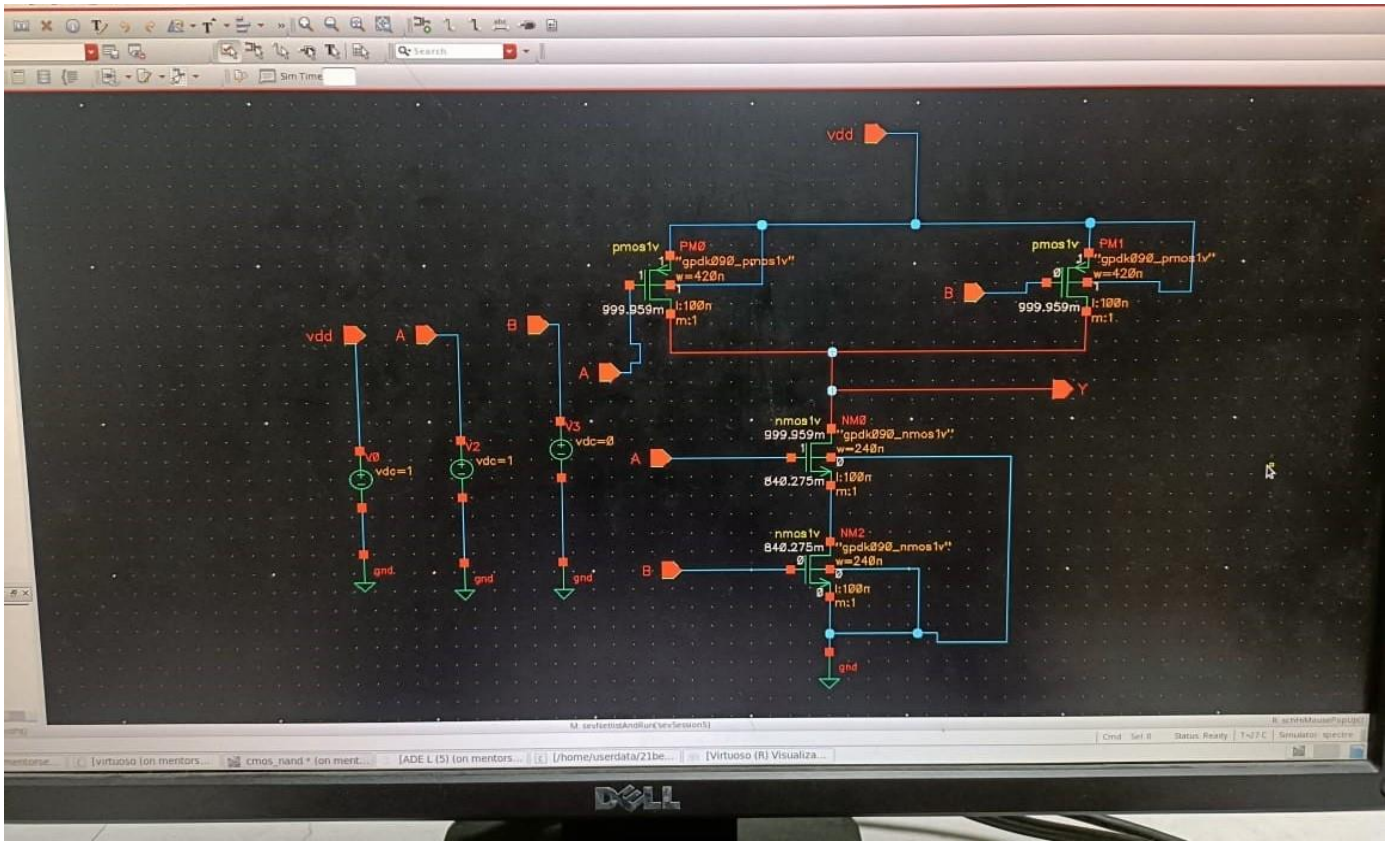


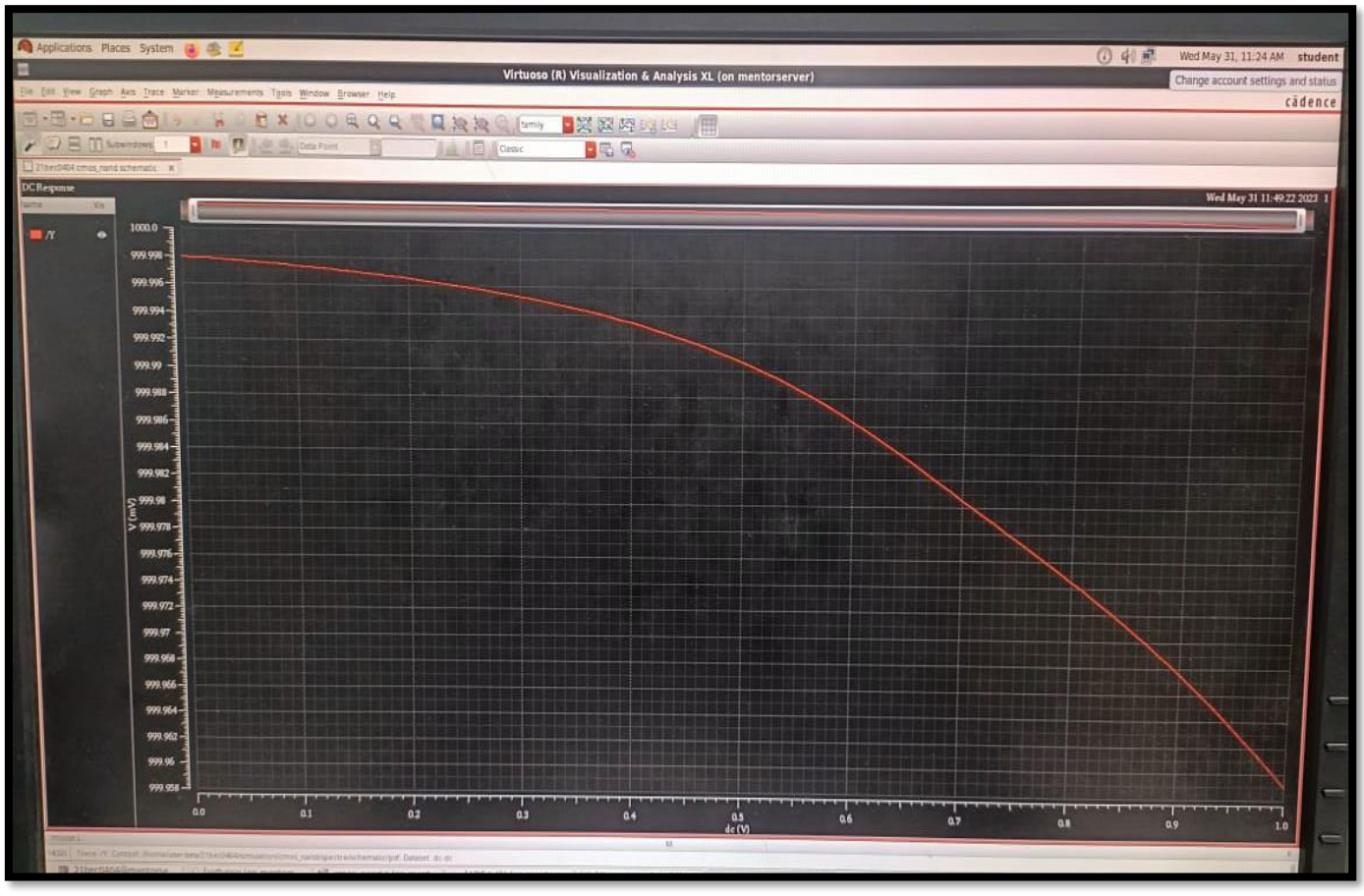
Case 4: When A=0 and B on X-axis



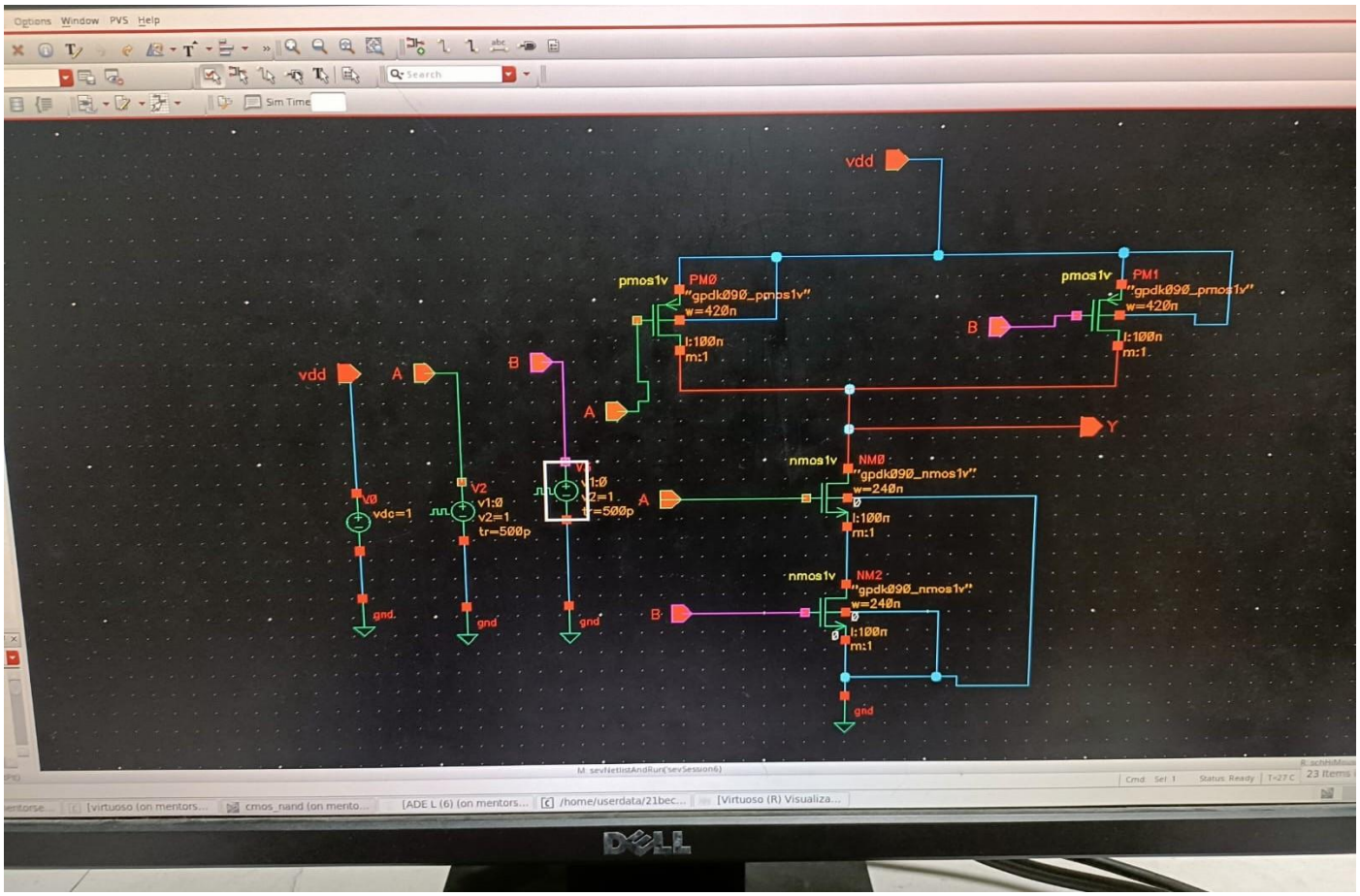


Case 5: When B=0 and A on X-axis





3 **Transient Analysis:**



Inference: When either A or B is 1, the graph is similar to the CMOS Inverter DC Analysisgraph but shifted towards the origin. For A=B=0->1, it shows the same characteristics as CMOS Inverter DC Analysis graph but is away from the origin as due to different sizing ratio in CMOS inverter (3.5:1) and CMOS Nand Gate (3.5:2). When either A or B is 0, and the other is sweeped from 0 to 1, the output is approximately equal to 1 or VDD.