Verification Plan:

- Designed the functionality of an asynchronous FIFO across various clock domains.
- Handling of metastability and synchronization between the write and read clock domains.
- Verified the proper reset and initialization of the FIFO and its internal signals.
- Performed write and read operations with different burst sizes and idle cycles, as per the design specifications.
- The write operation is performed successfully ensuring that FIFO accepts the data whenever the write signal is enabled, and the data is stored.
- The read operation is performed successfully ensuring that FIFO sends valid data whenever the read signal is enabled, and the data is retrieved.
- FIFO full condition is verified by ensuring data is written into FIFO till maximum depth is reached.
- FIFO empty condition is verified by making sure that the data read is done from the FIFO until it becomes empty.
- With a simple conventional testbench we have checked the very basic functionality of the design.

Contribution:

Kumar Durga Manohar Karna - Gone through the design specifications and have implemented the synchronization read to write module and top module.

Mohammeed Abbas Shaik – Have gone through the design specifications and have done the synchronization, synchronization write to read module, synchronizer module.

Nivedita Boyina– Have gone through the design specifications and tested the design.

Nikhitha Vadnala– Have gone through the design specifications, calculated the FIFO depth calculations, FIFO memory module.