

Future Hardware Directions of Quantum Annealing

Qubits Europe 2018
D-Wave Users Conference
Munich

Mark W Johnson
D-Wave Systems Inc.

April 11, 2018

Overview

- ▶ Where are we today?
 - ▶ annealing options
 - ▶ reverse annealing
 - ▶ quantum materials simulation
- ▶ Where are we going?
 - ▶ next generation processor - improved connectivity
 - ▶ lower noise

Overview

► Where are we today?

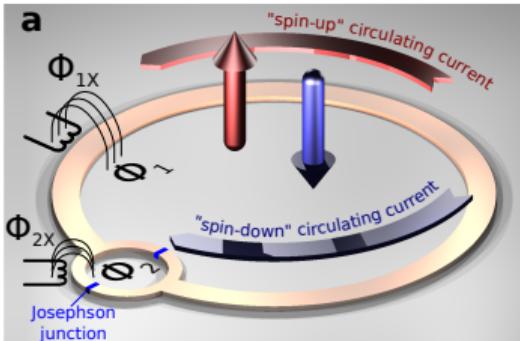
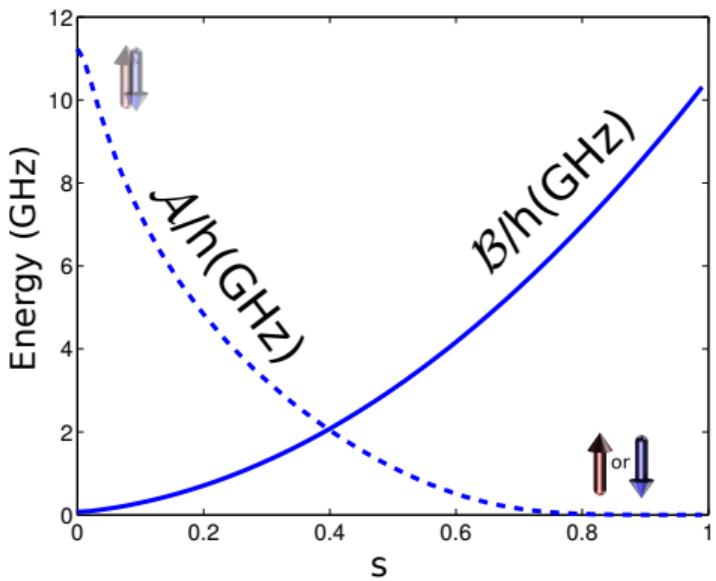
- ▶ annealing options
- ▶ reverse annealing
- ▶ quantum materials simulation

► Where are we going?

- ▶ next generation processor - improved connectivity
- ▶ lower noise

The goal of quantum annealing (QA): model the Hamiltonian

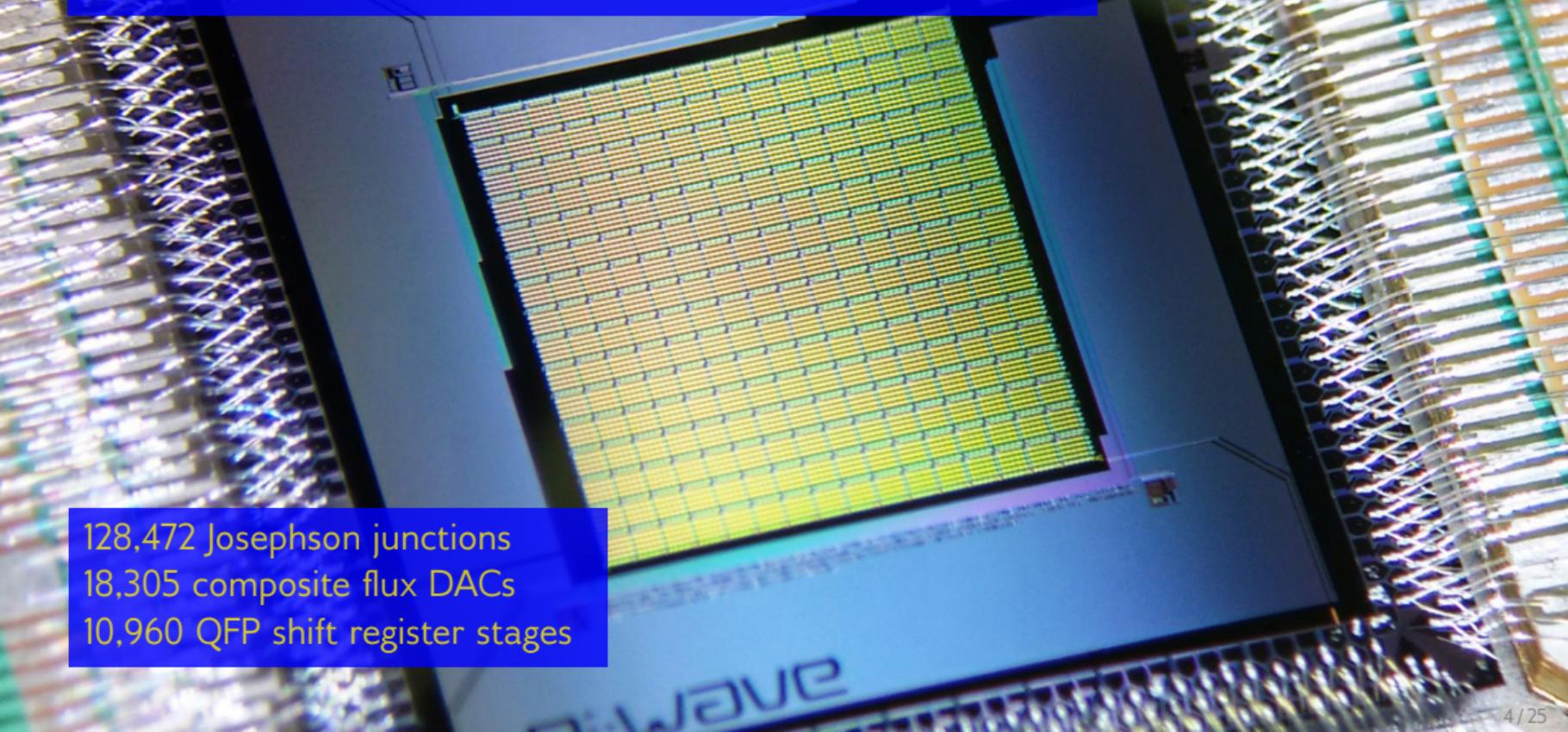
$$\mathcal{H}_S(s) = -\frac{1}{2} \mathcal{A}(s) \sum_i \sigma_{x,i} + \mathcal{B}(s) \left[- \sum_i h_i \sigma_{z,i} + \sum_{i < j} J_{ij} \sigma_{z,i} \sigma_{z,j} \right]$$



- ▶ T. Kadowaki and H. Nishimori, PRE, **58**(5), pp. 5355-5363, (1998)
- ▶ E. Farhi, *et al.*, Science **292**, 472 (2001)
- ▶ W. Kaminsky, S. Lloyd, T. Orlando, [arXiv:quant-ph/0403090](https://arxiv.org/abs/quant-ph/0403090), “Scalable Superconducting Architecture for Adiabatic Quantum Computation”

D-Wave 2000Q quantum annealing processor

Quantum processing unit = QPU



128,472 Josephson junctions
18,305 composite flux DACs
10,960 QFP shift register stages

2000 qubits: Chimera architecture at C16 scale

	D-Wave Two	D-Wave 2X	2000Q
Qubits (max)	512	1,152	2,048
Couplers	1472	3360	6016
Target Qubit Yield	95%+	95%+	97%+
Qubit degree	Chimera, degree = 6		

New features: Supporting more control over annealing:

- ▶ **Anneal Offsets**

Give user per-qubit control over transverse field

- ▶ **Anneal Pause**

Specify start and duration of global pause in anneal

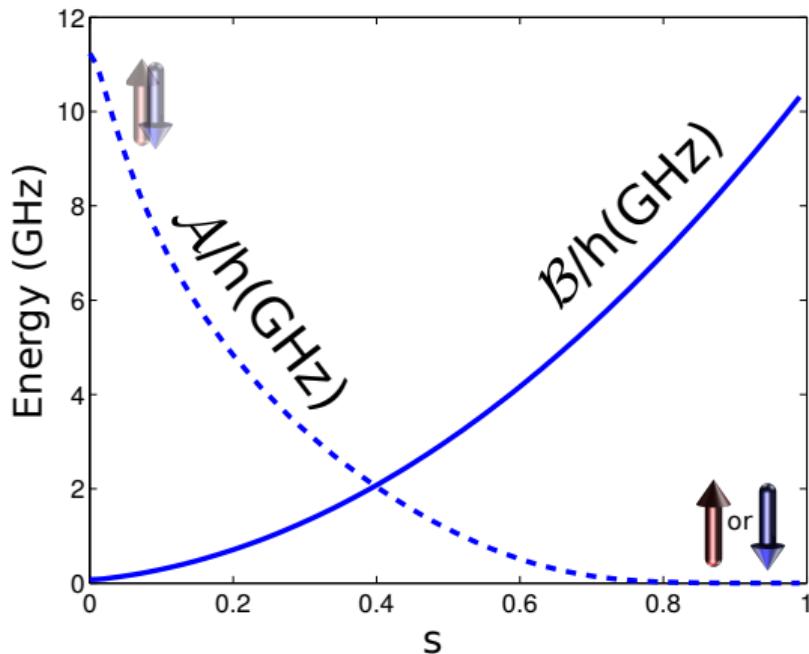
- ▶ **Anneal Quench**

Specify when to abruptly quench transverse field

- ▶ **Reverse Anneal:** a new quantum algorithm

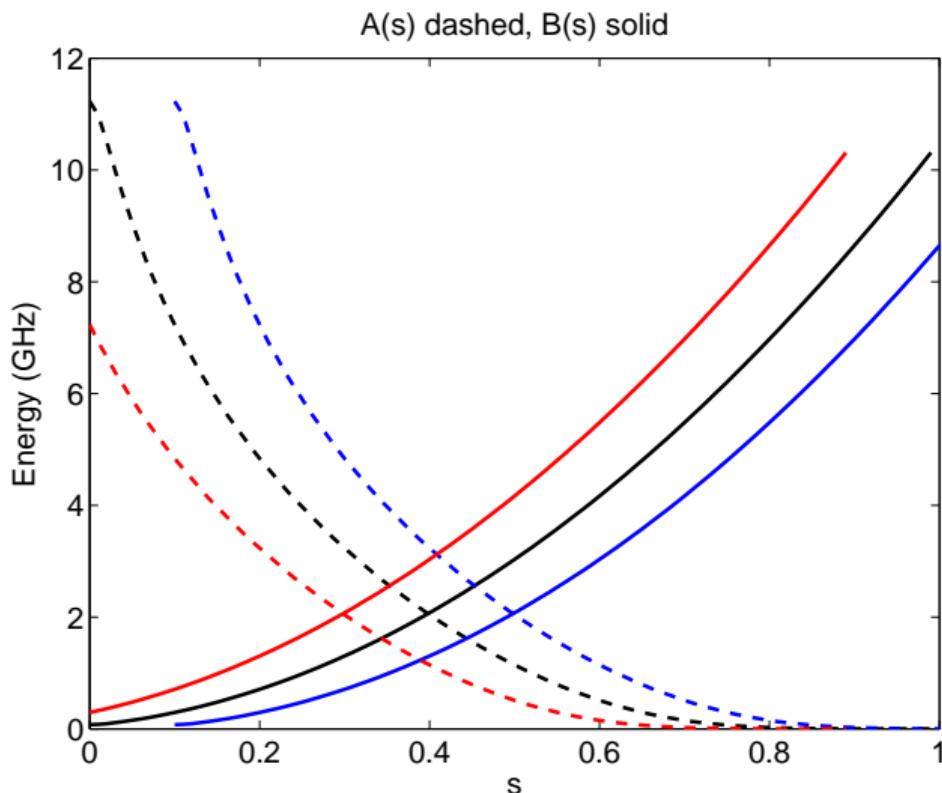
Standard annealing trajectory

$$\mathcal{H}_S(s) = -\frac{\mathcal{A}(s)}{2} \sum_i \sigma_{x,i} + \frac{\mathcal{B}(s)}{2} \left[-\sum_i h_i \sigma_{z,i} + \sum_{i < j} J_{ij} \sigma_{z,i} \sigma_{z,j} \right]$$



- ▶ ratio $\frac{\mathcal{A}(s)}{\mathcal{B}(s)}$ a fixed function of s for given qubit design
- ▶ trajectory: choose $s(t)$ linear
- ▶ \Rightarrow quadratic growth in $B(s)$

Modifications to the QA path: What is possible?

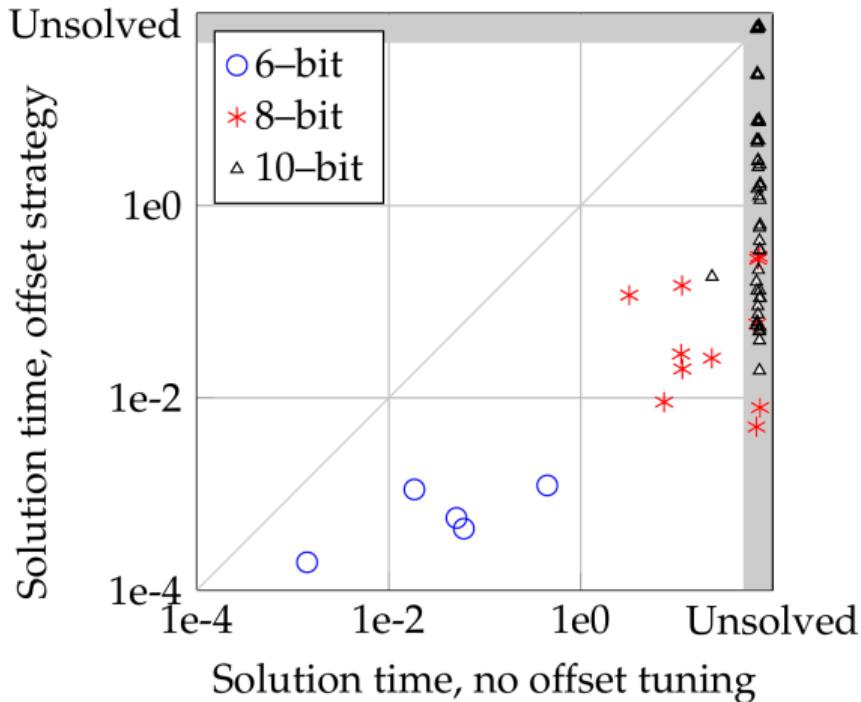


- ▶ Added control:
a *per qubit* offset
- ▶ *advance or delay* individual
qubit schedule

Application: Factoring

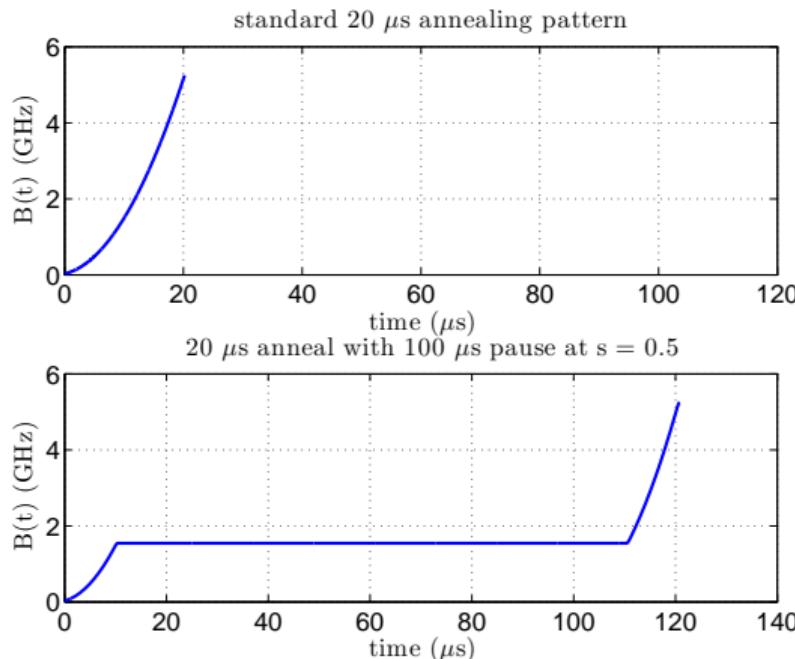
Percentage of solved instances

product size (bits)	standard anneal	delay long chains
6	100%	100%
8	55%	100%
10	2%	98%



"Boosting integer factorization performance via quantum annealing offsets", E. Andriyash, et al., 2016
see "D-Wave White Papers" at <http://www.dwavesys.com/resources/publications>

Modifications to the QA path: What is possible?

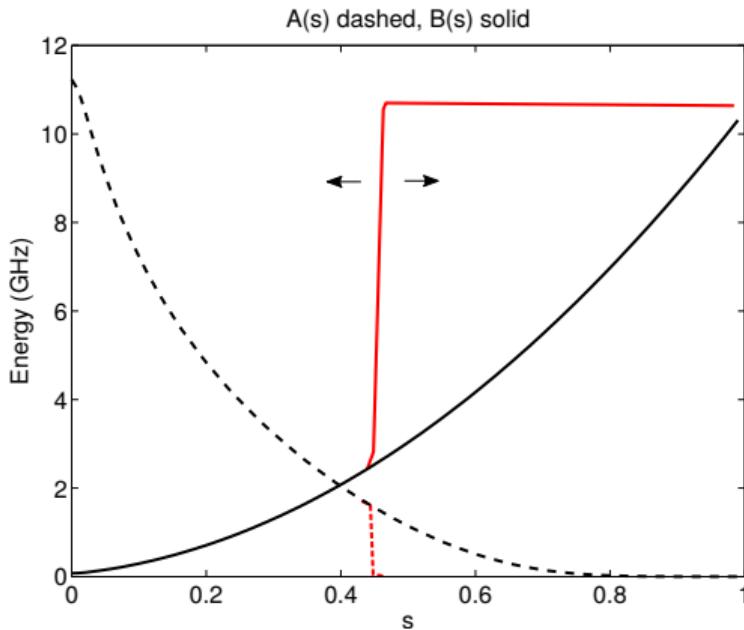


Manipulate global schedule:
pause mid-anneal

Why? What good does this do?

- ▶ Useful for study of instances with perturbative crossings
- ▶ identify regions during anneal where dynamics occur
- ▶ probe of global *freeze-out, localization*

Modifications to the QA path: What is possible?

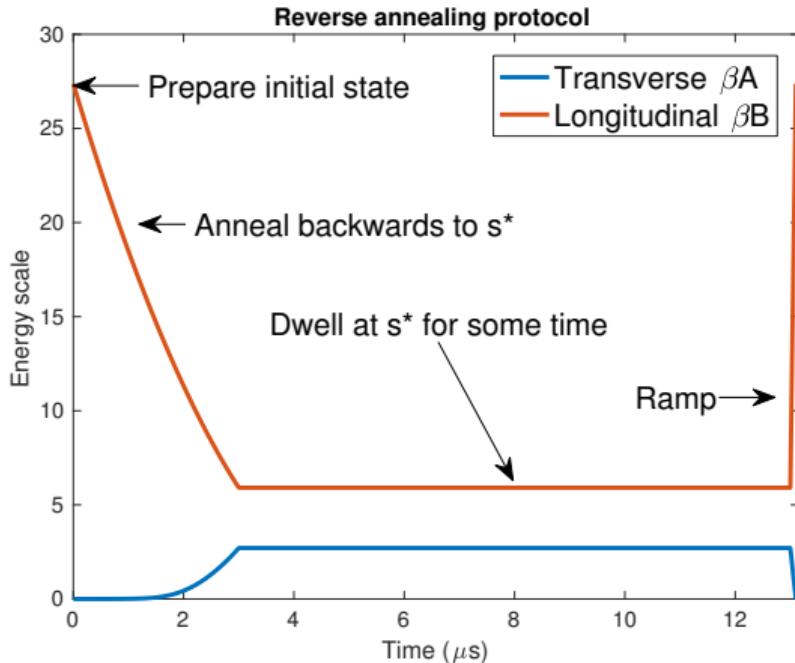


QUENCH! abruptly terminate the anneal

What good does this do?

- ▶ can sample distribution at point earlier in the anneal
- ▶ useful for Quantum Boltzman Sampling
- ▶ enabling capability for machine learning

Reverse anneal enables hybrid algorithms



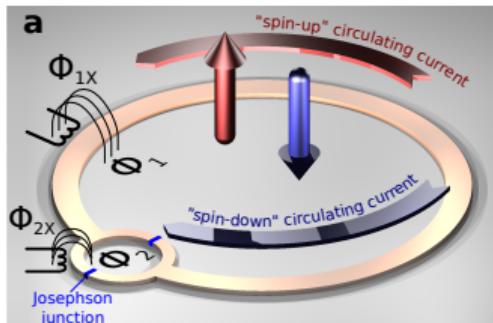
A new **Quantum Machine Instruction (QMI)**

1. Initialize *given classical state*
2. *Increase transverse field to specified value s^**
3. *wait for dwell time*
4. *anneal forward to complete*

Tunable *local* search

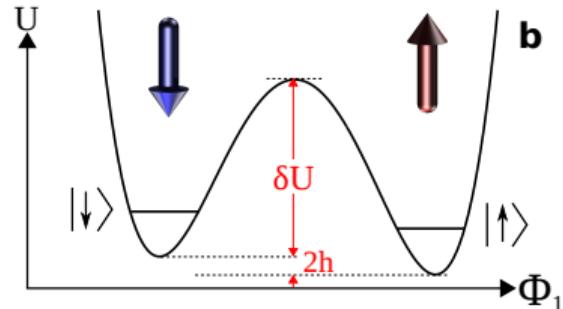
- N. Chancellor “Modernizing quantum annealing using local searches”, New J. Phys. **19**, 023024 (2017)
- “Reverse Quantum Annealing for Local Refinement of Solutions”,
D-Wave Whitepaper, www.dwavesys.com/resources/publications

Quantum simulation: flux qubit can behave like a quantum Ising spin

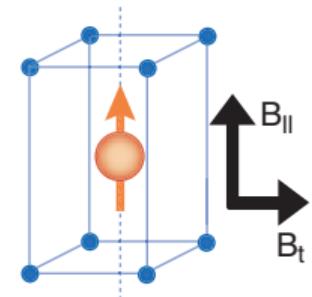


$$\mathcal{H}_q = -\frac{1}{2} [\epsilon_q \sigma_z + \Delta_q \sigma_x]$$

$$\text{where } \epsilon_q = 2 |I_q^p| \Phi_q^x$$



$$\begin{aligned} \mathcal{H}_{QS} &= -g\mu_B [B_{||}\sigma_z + B_t\sigma_x] \\ &= -h_i\sigma_z - \frac{1}{2}\Delta\sigma_x \end{aligned}$$

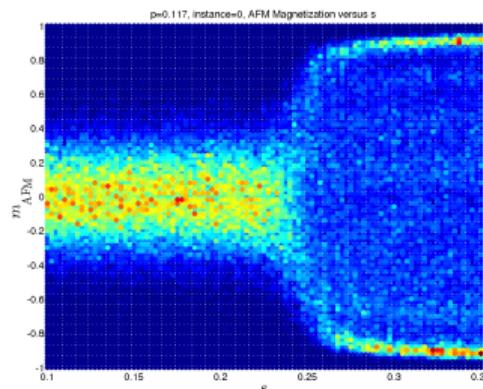
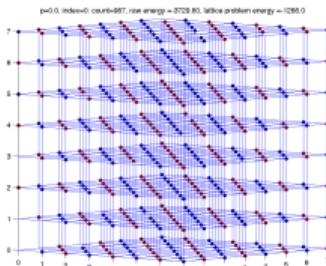


Parameter	QUBIT	Quantum Ising Spin
bias energy	$\epsilon_q/2$	$g\mu_B B_{ }$ or h
tunneling energy	$\Delta_q/2$	$g\mu_B B_t$
magnetic moment	$ I_q^p $	$g\mu_B$

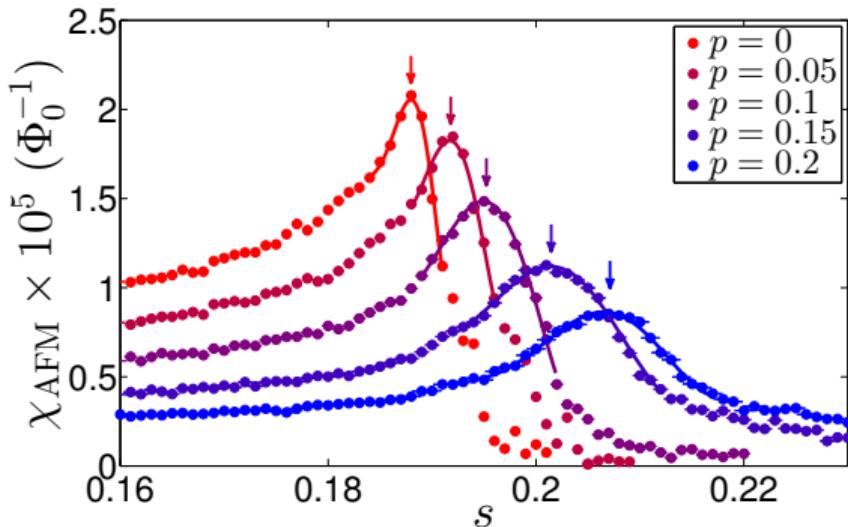
Binary information encoded in flux basis: $|0\rangle \rightarrow |\downarrow\rangle$ and $|1\rangle \rightarrow |\uparrow\rangle$

Quantum simulation of transverse field cubic Ising lattice (R. Harris)

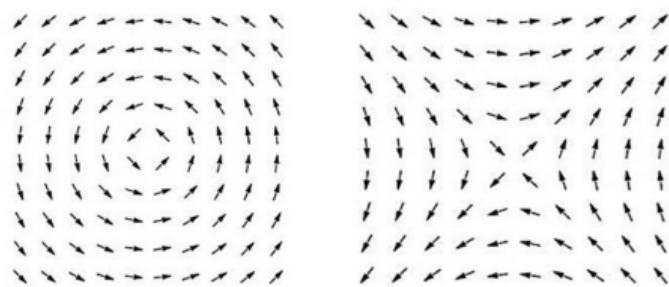
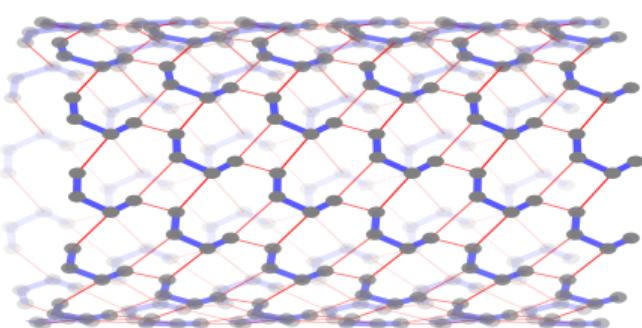
$$\mathcal{H}_{3D}(s) = -\frac{\Gamma(s)}{2} \sum_i \sigma_i^x + \mathcal{J}(s) \sum_{\langle i,j \rangle} J_{ij} \sigma_i^z \sigma_j^z$$



- ▶ 3D transverse Ising models embedded in D-Wave QA processor
- ▶ Quantitative agreement with locations of phase transitions:
vs. disorder (doping p) & transverse field Γ

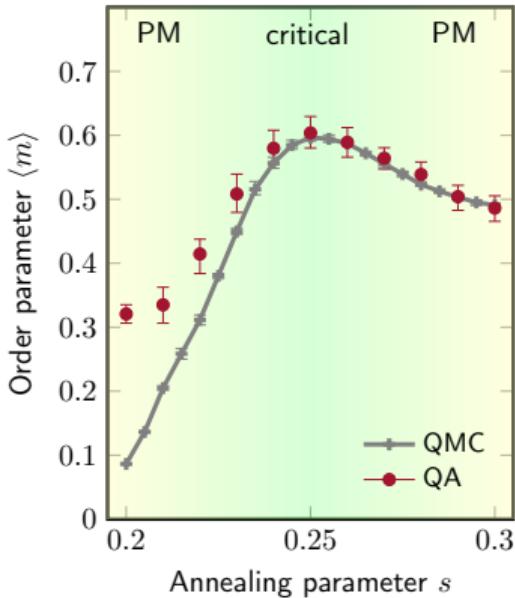
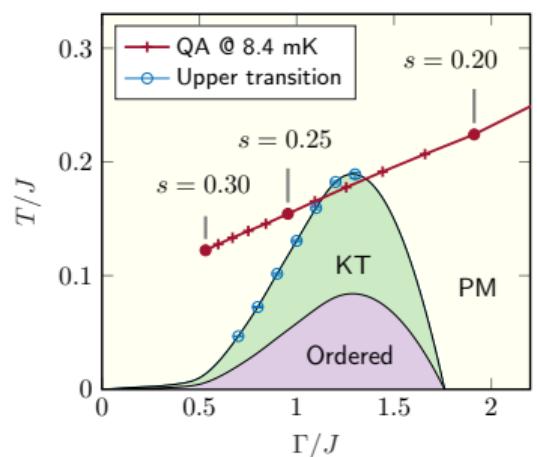
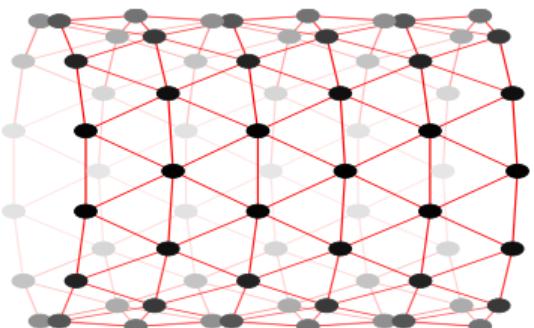


Quantum simulation of topological phase transition (A King)



vortex

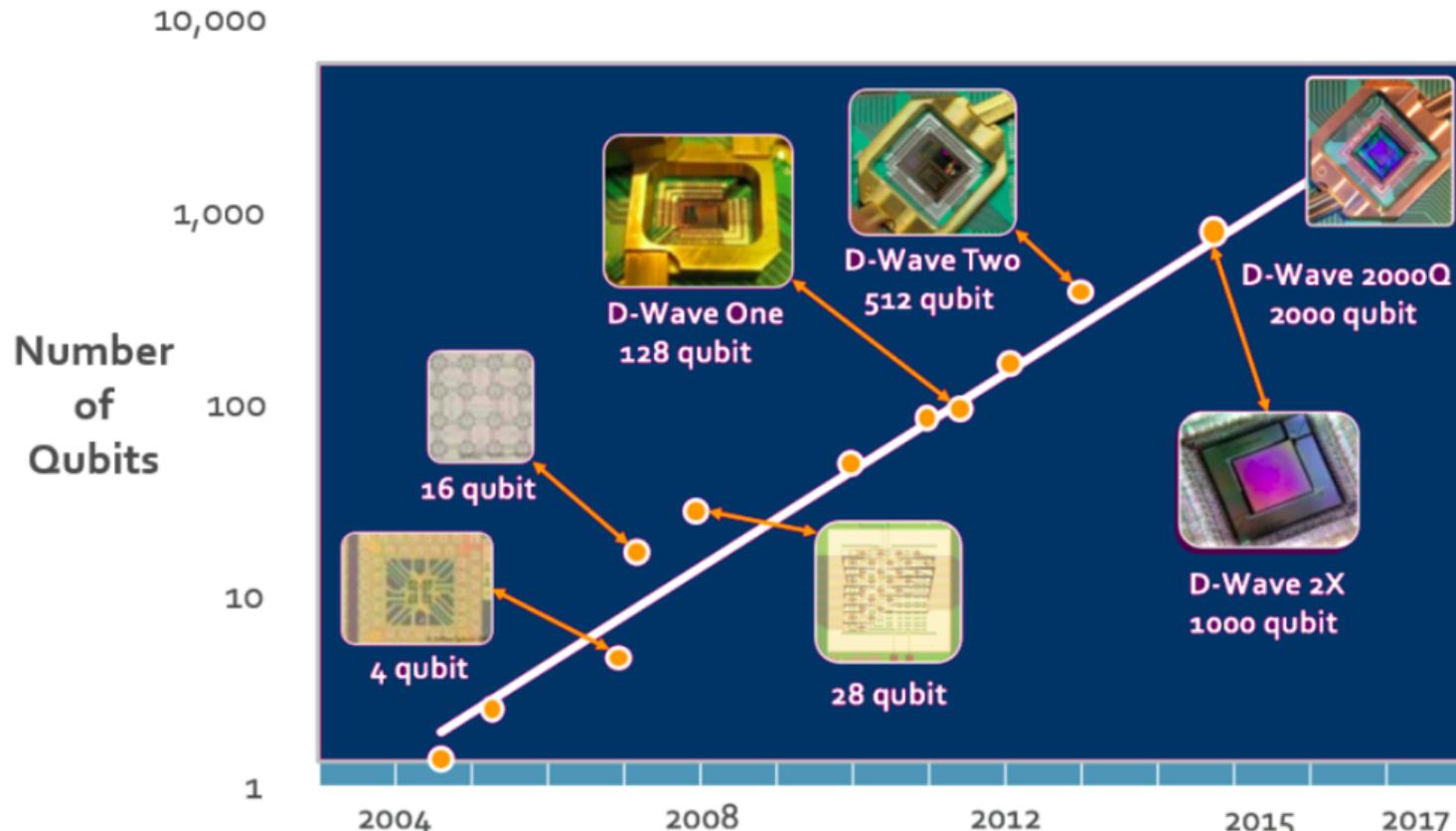
anti-vortex



Overview

- ▶ Where are we today?
 - ▶ annealing options
 - ▶ reverse annealing
 - ▶ quantum materials simulation
- ▶ Where are we going?
 - ▶ next generation processor - improved connectivity
 - ▶ lower noise

Progression of processor scale over time

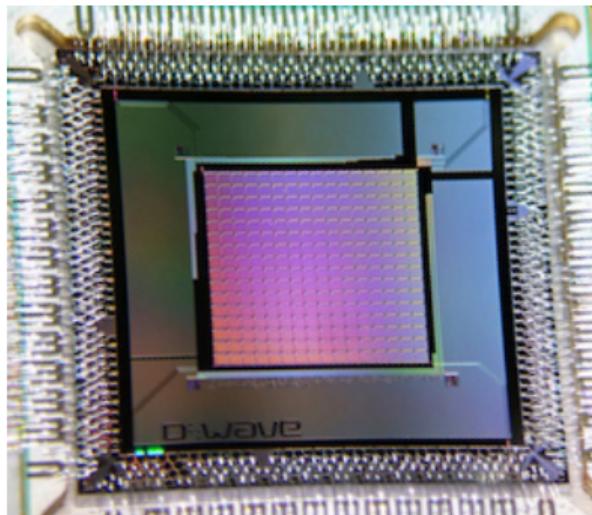


Important processor characteristics

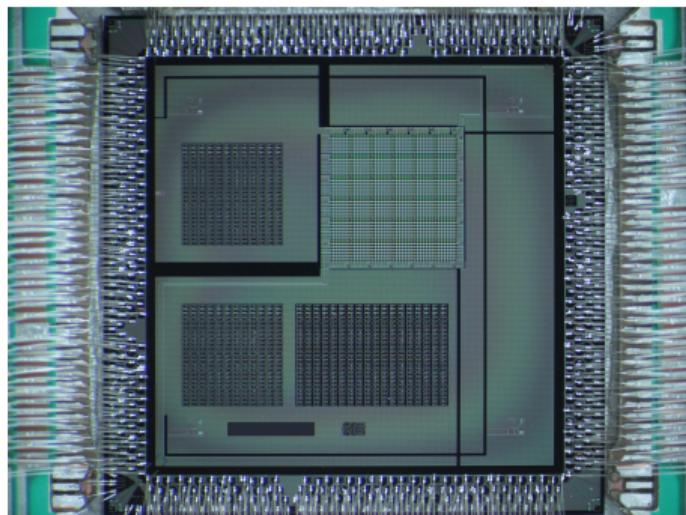
- ▶ number of qubits
How large of a problem can be posed?
- ▶ connectivity
How feasible is it to solve my problem?
- ▶ noise
How precisely can a problem be posed?
How well will QA perform?

Next generation architecture significantly enhances connectivity

Chimera C16 - DW 2000Q



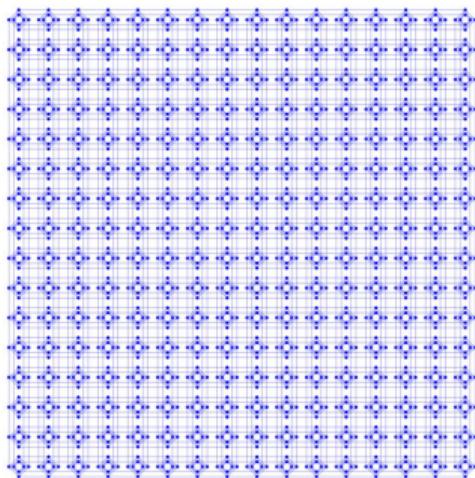
Pegasus P6 - 680 Qubit Prototype



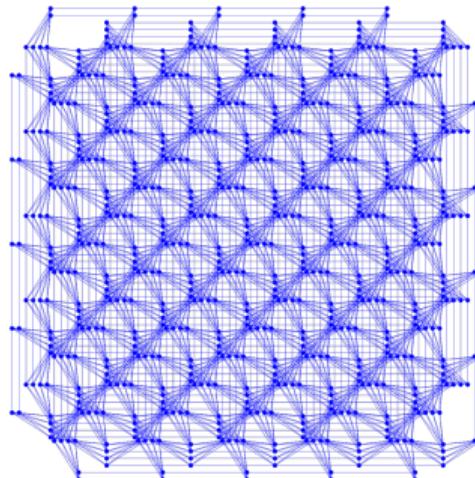
- ▶ most significant architecture change since first processor D-Wave One
- ▶ enabled by major technology changes in fabrication stack
- ▶ have demonstrated P6 prototype

Pegasus architecture significantly enhances connectivity

Chimera C16 - DW 2000Q

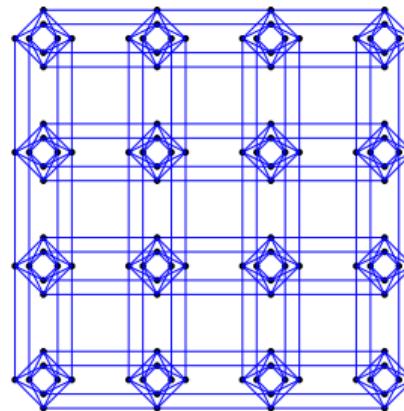
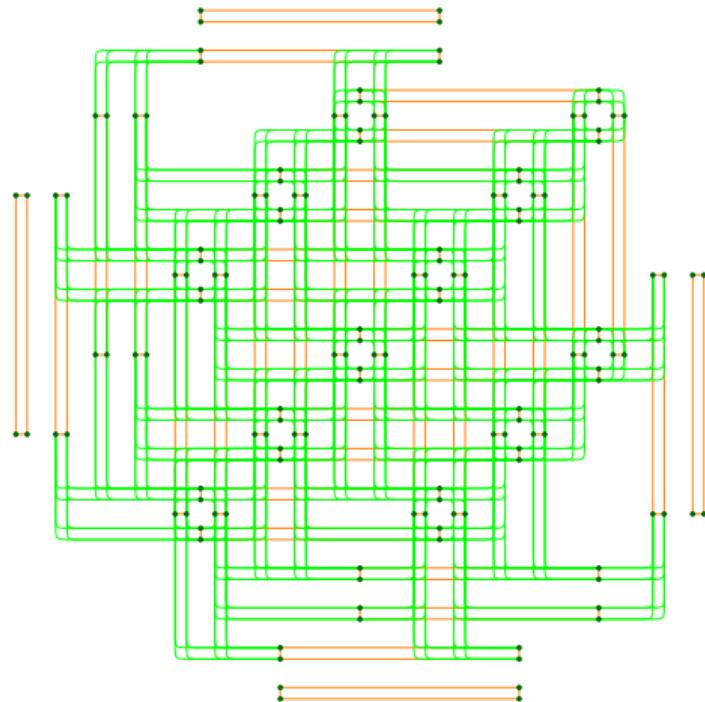


Pegasus P6 - 680 Qubit Prototype



Device Count	C16	P6	P12	P16
Qubits	2048	680	3080	5640
Couplers	6000	4784	21764	40484
max degree	6	15	15	15

A closer look at Pegasus



Chimera - C4

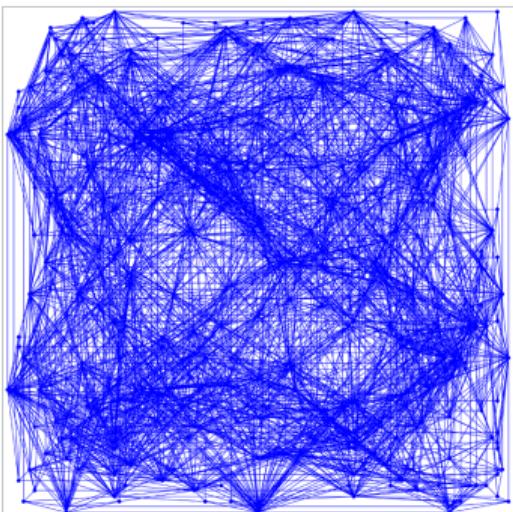
Basic Graph Embedding Statistics

	C16	P6	P16
Complete Graph	64 (17)	60 (7)	180 (17)
Complete Bipartite	64x64 (16)	52x52 (5)	172x172 (15)
Cubic Lattice	8x8x8 (4)	5x5x12 (2)	15x15x12 (2)
Factoring Circuit	16-bit (16)	10-bit (5)	30-bit (15)
Grid with Diagonals	16x16 (6)	15x15 (6)	45x45 (6)

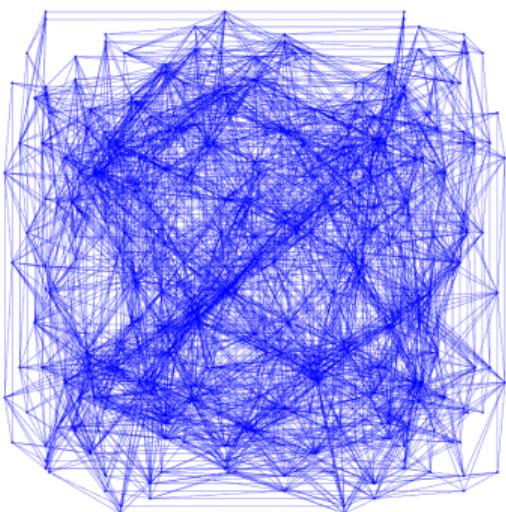
(max chain length in blue)

Compare embedding of graphs with similar average degree

Chimera C16 - DW 2000Q



Pegasus P6 - 680 Qubit Prototype



Logical Qubits	366
Average chain length	5.6
Average degree	24

318
2.1
25

Noise and coherence are important for quantum annealing

Lower intrinsic device noise will allow:

- ▶ more precise control of h , J , Γ
- ▶ more multiqubit tunneling
- ▶ faster calibration

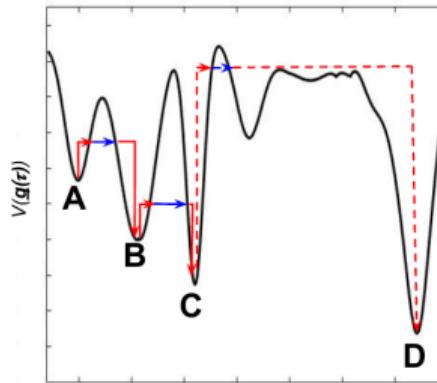
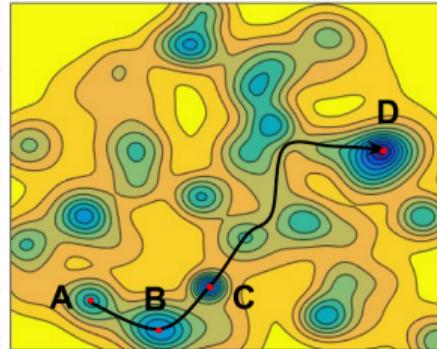
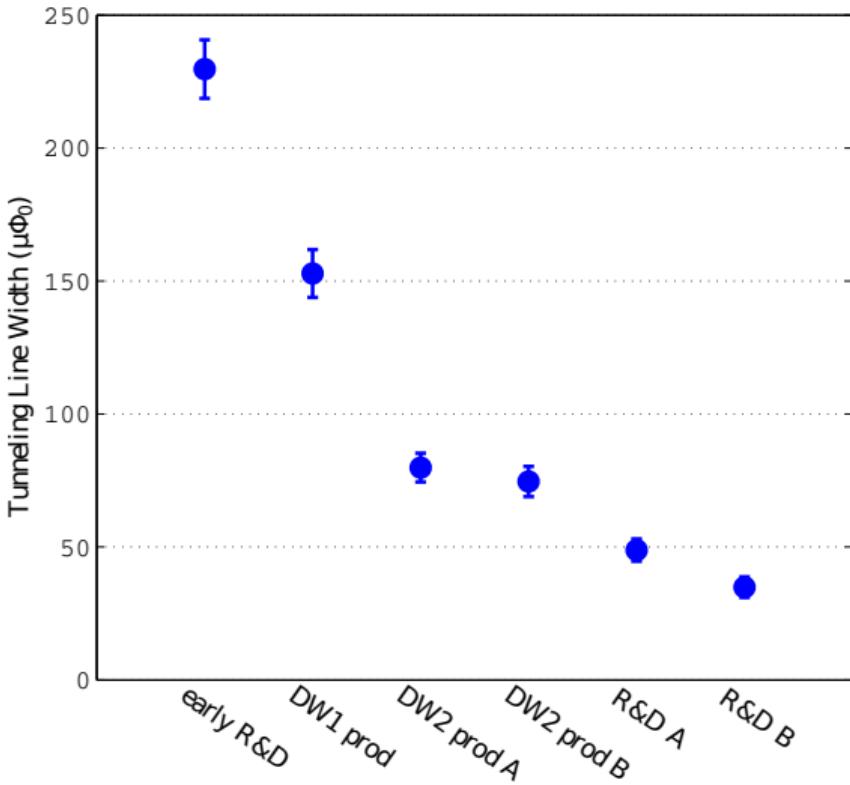


figure from Denchev, et al., PRX 6 031015 (2016), "What is the Computational Value of Finite-Range Tunneling?"

Continuing research on lower noise materials

Examining alternatives

- ▶ conductor material & processing
- ▶ dielectric material & processing



Summary

- ▶ D-Wave 2000Q processor
- ▶ Pegasus architecture significantly increases connectivity
- ▶ continued progress on noise & coherence