Zero (Z) gaines and the state of thought of something like and (EPR), meaning (Z) one Many arithmetic and logic instructions affect the zero flag. For example, deef instruction can be used to decrement a variable in RAM, and if the result is zero, Z bit is set, otherwise cleared. Note that all the instructions do not affect the Z flag. For example, decfsz can decrement a RAM location, but do not affect the Z flag. Similarly, incfsz increments a RAM variable and test for zero, but do not affect the Z flag. Further, there are many other instructions that do not affect any of the status bits. And a region with give while, ellipsies or transmitted

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These bits are used along with the SLEEP mode of PIC. During the SLEEP mode, the microcontroller can save a lot of power. After coming out of this mode, the CPU can check these two status bits to determine which kind of event is responsible to bring it out of the SLEEP mode. RPO

This is the register bank select bit. RPO is used to calculate the effective address in direct addressing mode. To select register bank 0, this bit is cleared, and if set, it selects bank 1. RPO is discussed further in Section 9.5.2. To set this bit, the PIC instruction "bsf STATUS, 05" may be used. Similarly, "bef STATUS, 05" will clear the RPO bit.

FSR (FILE SELECTION REGISTER) [INDIRECT DATA MEMORY ADDRESS POINTER]

FSR is the pointer used for indirect memory addressing in the whole register file. It must be noted that, in PIC, every instruction that can be used for direct addressing may also be used in a different way for indirect addressing. The only difference in indirect addressing mode is that one has to write the address byte in FSR and then use INDF in the instruction. Thus, FSR points to the desired memory location.

INDF (INDirect through FSR)

INDF stands for Indirect through FSR. This is not a physical register. Addressing INDF register will cause indirect addressing. Thus, the meaning of INDF can be thought as (FSR) or indirect through FSR, where the brackets indicate indirect addressing. Any instruction using INDF register actually accesses the register pointed by the FSR. For example, in case of array handling, it is required to have indirect addressing. The array address register can be incremented/decremented to point the required location in array. FSR is one such address register. Due to INDF, it is possible to indirectly address a RAM location. For example, to clear the RAM location 20H, the program would be as follows:

> movlw 0x20H : Initialize pointer to RAM movwf FSR : Clear INDF register cirf INDF