COVER

Schematics Index:

REVISION HISTORY

Rev	Description	Date	Drawn	Checked	Approved
A20_HOMLET_STD_V1_00		2013-03-18	YT		
A20_HOMLET_STD_V1_01		2013-05-28	YT		
A20_HOMLET_STD_V1_20		2013-07-10	YT		
A20_HOMLET_STD_V1_30		2014-05-27			

AllWinner Technology Co.,Ltd

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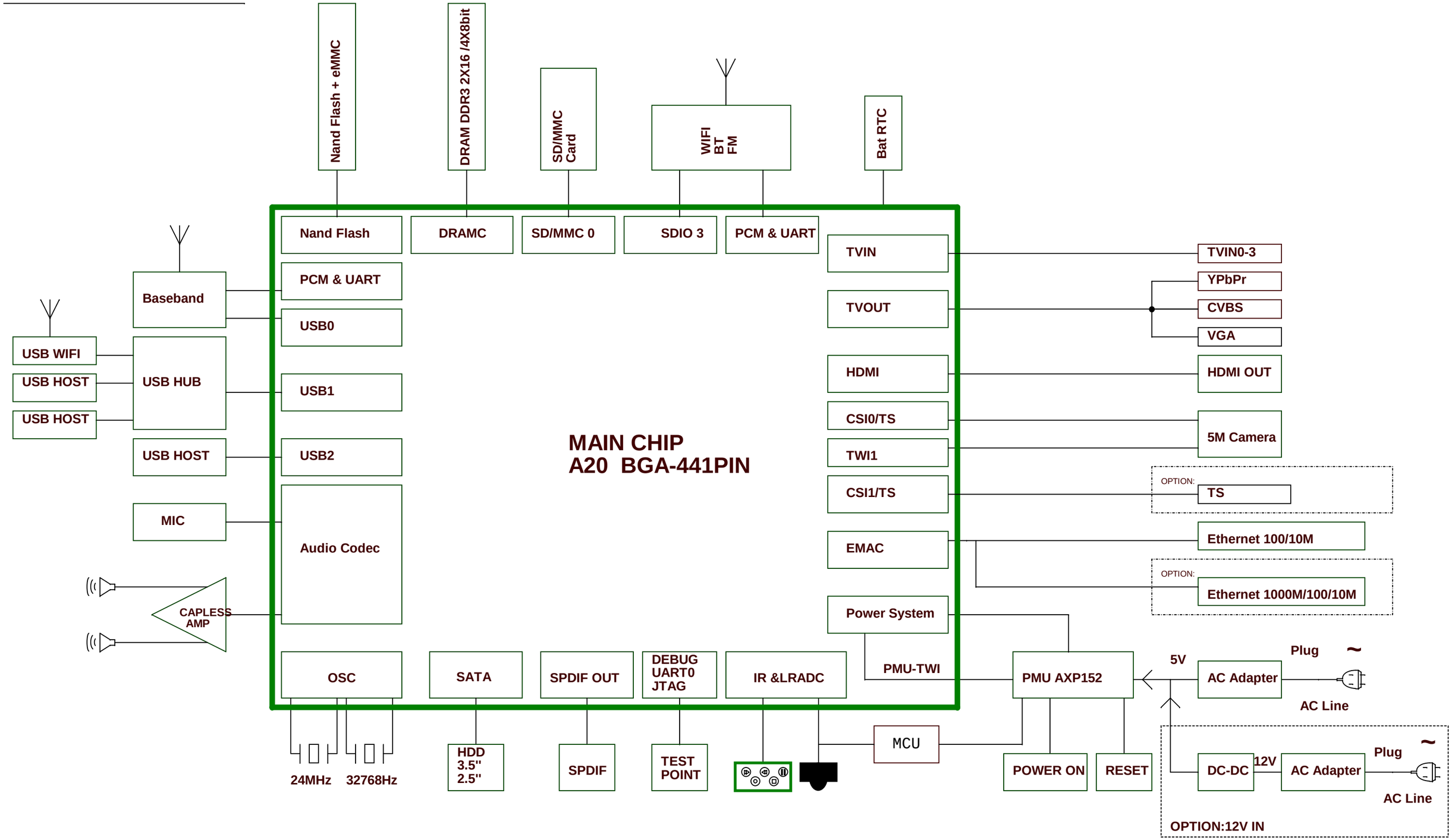
BLOCK



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GPIO ASSIGNMENT

Pin Group	Pin Name	Define	Function
PA(18)	PA0	ERXD3	EMAC/GMAC
	PA1	ERXD2	
	PA2	ERXD1	
	PA3	ERXD0	
	PA4	ETXD3	
	PA5	ETXD2	
	PA6	ETXD1	
	PA7	ETXD0	
	PA8	ERXCK	
	PA9	ERXERR	
	PA10	ERXDV	
	PA11	EMDC	
	PA12	EMDIO	
	PA13	ETXEN	
	PA14	ETXCK	
	PA15	ECRS	
	PA16	ECOL	
	PA17	ETXERR	
PB(24)	PB0	TWI0_SCK	PMU
	PB1	TWI0_SDA	
	PB2	PWM0	
	PB3	GPIO_OUT	MUTE
	PB4	IR0_RX	IR-A20
	PB5	GPIO_OUT	BT-REST
	PB6	I2S_BCLK	BT-PCM-CLK
	PB7	I2S_LRCK	BT-PCM-SYNC
	PB8	I2S_DO0	BT-PCM-OUT
	PB9	GPIO	
	PB10	GPIO	
	PB11	GPIO	
	PB12	GPIO	
	PB13	GPIO	
	PB14	JTAG_MS0	JTAG
	PB15	JTAG_CK0	
	PB16	JTAG_DO0	
	PB17	JTAG_DI0	
	PB18	TWI1_SCK	TWI1
	PB19	TWI1_SDA	
	PB20	TWI2_SCK	
	PB21	TWI2_SDA	
	PB22	UART0_TX	UART(DBUG)
	PB23	UART0_RX	

Pin Group	Pin Name	Define	Function
PC(25)	PC0	NWE# /Nor	NAND
	PC1	NALE /Nor	
	PC2	NCLE /Nor	
	PC3	NCE1	
	PC4	NCE0	
	PC5	NRE#	
	PC6	NRB0	
	PC7	NRB1	
	PC8	NDQ0	
	PC9	NDQ1	
	PC10	NDQ2	
	PC11	NDQ3	
	PC12	NDQ4	
	PC13	NDQ5	
	PC14	NDQ6	
	PC15	NDQ7	
	PC16	NWP	
	PC17	NCE2	
	PC18	NCE3	
	PC19	SPI2_CS	
	PC20	SPI2_SCLK	
	PC21	SPI2_MOSI	
	PC22	GPIO_OUT	
	PC23		Nor
	PC24	NDQS	NDQS
PD(28)	PD0	WIFI-SHDN	WIFI
	PD1		
	PD2	USB0-DRV	USB
	PD3	USB0-IDDET	
	PD4	SD0-DET#	Card DET
	PD5	RECOVERY	RECOVERY Key
	PD6	VGA-DET	VGA DET
	PD7	YPBPR-DET	YPbPr
	PD8	AV-5V-EN	AV-5V-EN
	PD9	AP-WORK-DET#	MCU
	PD10	AP-OFF-INT#	
	PD11	CSI0-STBY-EN	CSI
	PD12	CSI0-PWR-EN	
	PD13	CSI0-RESET#	
	PD14	HDD-PWR-EN	HDD-PWR-EN
	PD15	EMAC-PWR-EN	EMAC-PWR-EN
	PD16	STATUS-LED	LED
	PD17	PWR-LED	

Pin Group	Pin Name	Define	Function
PD(28)	PD18	LCD0_D18	
	PD19	LCD0_D19	HDMI-RX-DET
	PD20	LCD0_D20	HDMI-RXINT
	PD21	LCD0_D21	HDMI-RST#
	PD22	LCD0_D22	HDMI-PWR-EN
	PD23	LCD0_D23	HUB-PWR-EN
	PD24	LCD0_CLK	
	PD25	LCD0_DE	
	PD26	LCD0_HSYNC	
	PD27	LCD0_VSYNC	
PE(12)	PE0	CSI0_PCLK	CSI0
	PE1	CSI0_MCLK	
	PE2	CSI0_HSYNC	
	PE3	CSI0_VSYNC	
	PE4	CSI0_D0	
	PE5	CSI0_D1	
	PE6	CSI0_D2	
	PE7	CSI0_D3	
	PE8	CSI0_D4	
	PE9	CSI0_D5	
	PE10	CSI0_D6	
	PE11	CSI0_D7	
PF(6)	PF0	SDC0_D1	SDC0
	PF1	SDC0_D0	
	PF2	SDC0_CLK	
	PF3	SDC0_CMD	
	PF4	SDC0_D3	
	PF5	SDC0_D2	
PG(12)	PG0	CSI1_PCLK	TS1
	PG1	CSI1_MLCK	
	PG2	CSI1_HSYNC	
	PG3	CSI1_VSYNC	
	PG4	CSI1_D0	
	PG5	CSI1_D1	
	PG6	CSI1_D2	
	PG7	CSI1_D3	
	PG8	CSI1_D4	
	PG9	CSI1_D5	
	PG10	CSI1_D6	
	PG11	CSI1_D7	

Pin Group	Pin Name	Define	Function
PH(28)	PH0	GPIO	
	PH1	GPIO	
	PH2	GPIO	
	PH3	GPIO	
	PH4	GPIO	
	PH5	GPIO	
	PH6	GPIO	
	PH7	GPIO	
	PH8	GPIO	
	PH9	GPIO	
	PH10	GPIO	
	PH11	GPIO	
	PH12	GPIO	
	PH13	GPIO	
	PH14	GPIO	
	PH15	GPIO	
	PH16	GPIO	
	PH17	GPIO	
	PH18	GPIO	
	PH19	GPIO	
	PH20	GPIO	
	PH21	GPIO	
	PH22	GPIO	
	PH23	GPIO	
	PH24	GPIO	
	PH25	GPIO	
	PH26	GPIO	
	PH27	GPIO	
PI(22)	PI0	BB-WAKE-HOST	BB
	PI1	BB-PWRON	
	PI2	BB-RST-N	
	PI3	BB-VBAT-EN	
	PI4	SDC3_CMD	WIFI SDIO
	PI5	SDC3_CLK	
	PI6	SDC3_D0	
	PI7	SDC3_D1	
	PI8	SDC3_D2	
	PI9	SDC3_D3	
	PI10	SPI0_CS0	
	PI11	GPIO	
	PI12	SPI0_MOSI	CLK-32K
	PI13	HCEC	HDMI OUT
	PI14	WIFI-HOST-WAKE	WIFI

Pin Group	Pin Name	Define	Function
PI(22)	PI15	BT-HOST-WAKE	BT
	PI16	UART2_RTS	BT UART
	PI17	UART2_CTS	
	PI18	UART2_TX	
	PI19	UART2_RX	
	PI20	GPIO_OUT	BT-WAKE
	PI21		

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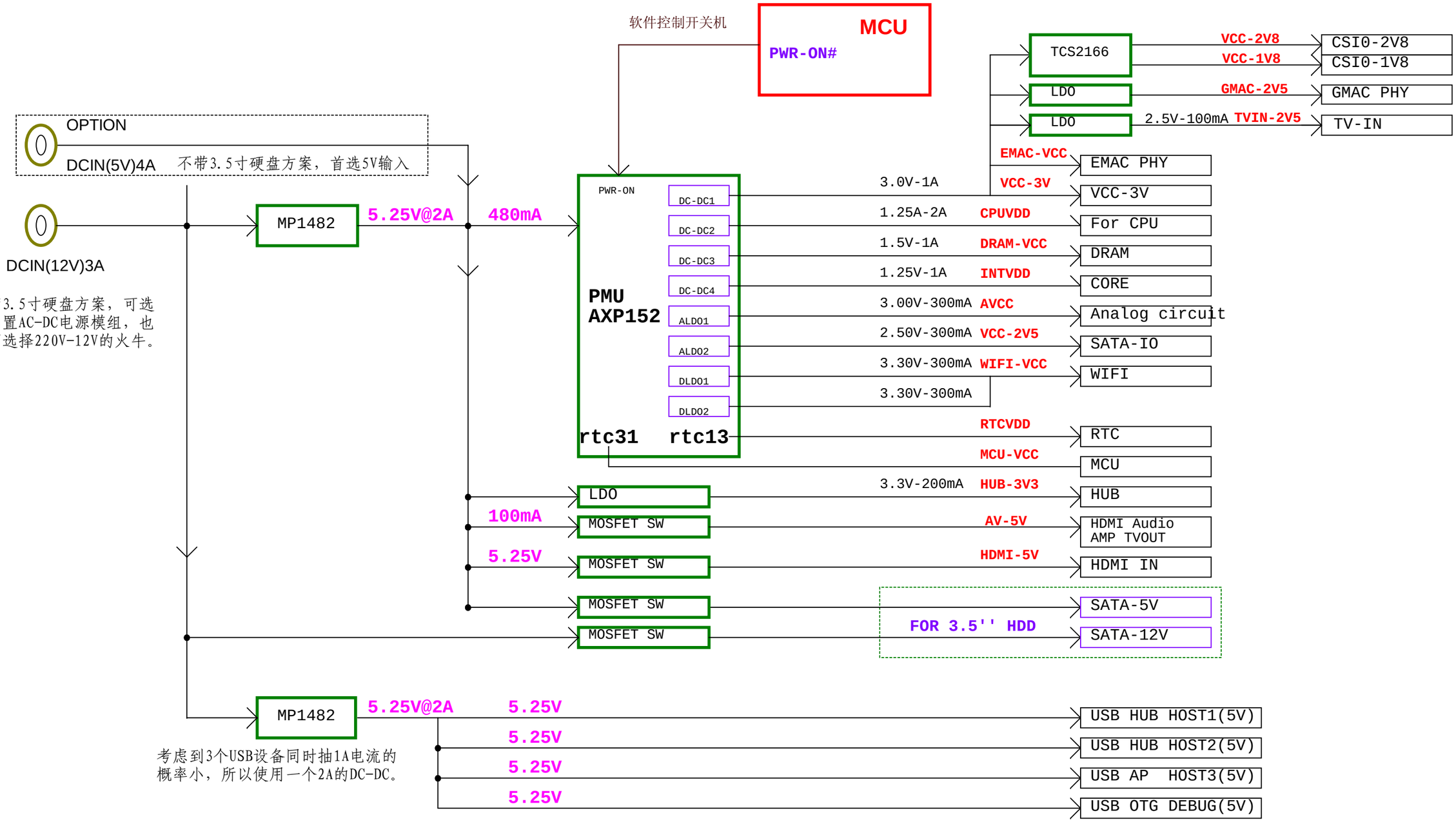
POWER TREE



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CPU1

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DRAM

NAND

TS0/CSI0

TS1/CSI1

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U6-2

FBGA441-A20_42

TS流接口

TS连接示意图
串口数据: CLK/ERR/SYNC/DVLD/D0
并口数据: CLK/ERR/SYNC/DVLD/D0-D7

OPTION:
如果不考虑摄像头，或者TS口，可以
将CSI部分或TS部分删除，并接地!

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CPU2

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MISC

19,20	ERXD3	D5	RXD3/SPI1_CS0/UART2_RTS/PA0
19,20	ERXD2	E5	RXD2/SPI1_CLK/UART2_CTS/PA1
19,20	ERXD1	D6	RXD1/SPI1_MOSI/UART2_TX/PA2
19,20	ERXD0	E6	RXD0/SPI1_MISO/UART2_RX/PA3
19,20	ETXD3	D7	TXD3/SPI1_CS1/PA4
19,20	ETXD2	E7	TXD2/SPI3_CS0/PA5
19,20	ETXD1	D8	TXD1/SPI3_CLK/PA6
19,20	ETXD0	E8	TXD0/SPI3_MOSI/PA7
19,20	ERXCK	D9	RXCK/SPI3_MISO/PA8
19	ERXERR	E9	ERXERR/SPI3_CS1/I2S1_MCLK/PA9
19,20	ERXDV	D10	ERXDV/GRXCTL/UART1_TX/PA10
19,20	EMDC	E10	MDC/UART1_RX/PA11
19,20	EMDIO	D11	MDIO/UART6_TX/UART1_RTS/PA12
19,20	ETXEN	E11	ETXEN/GTXCTL/UART6_RX/UART1_CTS/PA13
19	ETXCK	D12	ETXCK/UART7_TX/UART1_DTR/I2S1_BCLK/PA14
19,20	ECRS	E12	ECRS/GTXCK/UART7_RX/UART1_DSR/I2S1_LRCK/PA15
19,20	ECOL	D13	ECOL/GCLKIN/CAN_TX/UART1_DCD/I2S1_DO/PA16
19,20	ETXERR	C13	ETXERR/CAN_RX/UART1_RING/I2S1_DI/PA17

TWI

9,10	PMU-SCK	A15	TWI0_SCK/PB0
9,10	PMU-SDA	B15	TWI0_SDA/PB1
9,13,19	TWI1-SCK	A8	TWI1_SCK/PB18
9,13,19	TWI1-SDA	B8	TWI1_SDA/PB19
		C8	TWI2_SCK/PB20
		C7	TWI2_SDA/PB21
21	BB-WAKE-HOST	A20	TWI3_SCK/PI0
21	BB-PWRON	B20	TWI3_SDA/PI1
21	BB-RST-N	A19	TWI4_SCK/PI2
21	BB-VBAT-EN	B19	PWM1/TWI4_SDA/PI3

SPI

		C17	SPI0_CS0/UART5_TX/EINT22/PI10
		D17	SPI0_CLK/UART5_RX/EINT23/PI11
16	CLK-32K	C16	SPI0_MOSI/UART6_TX/CLK_OUT_A/EINT24/PI12
15	HCEC	D16	SPI0_MISO/UART6_RX/CLK_OUT_B/EINT25/PI13

PS2

16	WIFI-HOST-WAKE	C15	PS2_SCK1/TCLKIN0/EINT26/SPI0_CS1/PI14
16	BT-HOST-WAKE	D15	PS2_SDA1/TCLKIN1/EINT27/SPI1_CS1/PI15

UART

14	UART0-TX	A7	UART0_TX/IR1_TX/PB22
14	UART0-RX	B7	UART0_RX/IR1_RX/PB23

IR

17	MUTE	B14	IR0_TX/SPDIF_MCLK/STANBYWFI/PB3
14	IR-AP	A13	IR0_RX/PB4

SYS Ctrl

14	JTAG-MS	A10	JTAG_MS0/SPI2_CS0/PB14
14	JTAG-CK	B10	JTAG_CK0/SPI2_CLK/PB15
14	JTAG-DO	A9	JTAG_DO0/SPI2_MOSI/PB16
14	JTAG-DI	B9	JTAG_DI0/SPI2_MISO/PB17
14	UBOOT	W8	UBOOT_SEL
14	JTAG-SEL	T10	JTAG_SEL
10	NMI#	F5	NMI#
9,10,18	RESET#	C14	RESET#
		T9	VDDQE
		H16	TEST

CLK SRC

9	CLK32K-IN	F1	X32KI
9	CLK32K-OUT	F2	X32KO
9	OSC24MI	N23	X24MI
9	OSC24MO	N22	X24MO

	T15	PLLTEST
	T16	PLLDV
	R15	PLLVREG
PLLVP	P16	VCC-PLL
RTCVDD	K8	VDD-RTC
	P15	PLLGND

GND

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CARD0

	SDC0_D1/JTAG_MS1/PF0	M20	SD0-D1	14
	SDC0_D0/JTAG_DI1/PF1	M19	SD0-D0	14
	SDC0_CLK/UART0_TX/PF2	L20	SD0-CLK	14
	SDC0_CMD/JTAG_DO1/PF3	L19	SD0-CMD	14
	SDC0_D3/UART0_RX/PF4	K20	SD0-D3	14
	SDC0_D2/JTAG_CK1/PF5	K19	SD0-D2	14

CARD3

	SDC3_CMD/PI4	A18	SD3-CMD	16
	SDC3_CLK/PI5	B18	SD3-CLK	16
	SDC3_D0/PI6	A17	SD3-D0	16
	SDC3_D1/PI7	B17	SD3-D1	16
	SDC3_D2/PI8	A16	SD3-D2	16
	SDC3_D3/PI9	B16	SD3-D3	16

EINT

EINT28/SPI1_CS0/UART2_RTS/PI16	E17	AP-BT-RTS	16	13	TXP-SATA
EINT29/SPI1_CLK/UART2_CTS/PI17	E16	AP-BT-CTS	16	13	TXN-SATA
EINT30/SPI1_MOSI/UART2_TX/PI18	E15	AP-BT-TXD	16	13	RXP-SATA
EINT31/SPI1_MISO/UART2_RX/PI19	D14	AP-BT-RXD	16	13	RXN-SATA
				13	REXT-SATA

AUDIO INT

I2S_MCLK/AC97_MCLK/PB5	B13	BT-REST	16	
I2S_BCLK/AC97_BCLK/PB6	A12	BT-PCM-CLK	16	
I2S_LRCK/AC97_SYNC/PB7	B12	BT-PCM-SYNC	16	
I2S_DO0/AC97_DO/PB8	A11	BT-PCM-OUT	16	15
I2S_DO1/PB9	C12			15
I2S_DO2/PB10	C11			15
I2S_DO3/PB11	C10			15
I2S_DI/AC97_DI/SPDIF_DI/PB12	C9	BT-PCM-IN	16	15
SPI2_CS1/SPDIF_DO/PB13	B11	SPDIF-DO	17	15

AUDIO CODEC

PHOUTN	AC23			
PHOUTP	AC22			
FMINL	Y20			
FMINR	Y21			
VMIC	AA21	VMIC	17	
MICIN1	AC20	MICIN1	17	
MICIN2	AC21			
LINEINL	AB20			
LINEINR	AB21			
HPOUTR	W19	HPR	17	
HPCOM	AA19			
HPCOMFB	AA20			
VCC-HP	AB19	HPVCCIN		
HPBP	AC19	HPBP	9	
HPOUTL	Y19	HPL	17	16 BT-WAKE
HPGND	V19	GND		
AVCC	T19	AVCC		
VRP	W21	VRP	9	
VRA2	V20	VRA2	9	
VRA1	W20	VRA1	9	9,14 LRADC0
AGND	U19	A-GND	9,17	

USB

DM0	N20	DM0	12,21	
DP0	N21	DP0	12,21	
DM1	P20	DM1	12	
DP1	P21	DP1	12	
DM2	R20	DM2	12	
DP2	R21	DP2	12	

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TV

TVIN0	AC18	TVIN0	
TVIN1	AB18	TVIN1	
TVIN2	AA17	TVIN2	
TVIN3	Y17	TVIN3	
VRP-TVIN	AA16	VRP_TVIN	
VRN-TVIN	Y16	VRN_TVIN	
TV-OUT0	AC16	TVOUT0	
TV-OUT1	AB16	TVOUT1	
TV-OUT2	AC17	TVOUT2	
TV-OUT3	AB17	TVOUT3	

SATA

TXP-SATA	T20	TXP_SATA	
TXN-SATA	T21	TXM_SATA	
RXP-SATA	U21	RXP_SATA	
RXN-SATA	U20	RXM_SATA	
REXT-SATA	V21	REXT_SATA	
	R19	CLKP_SATA	
	P19	CLKM_SATA	

HDMI

HTX0P	V23	TX0P_HDMI	
HTX0N	V22	TX0N_HDMI	
HTX1P	U23	TX1P_HDMI	
HTX1N	U22	TX1N_HDMI	
HTX2P	T23	TX2P_HDMI	
HTX2N	T22	TX2N_HDMI	
HTXCP	W23	TXCP_HDMI	
HTXCN	W22	TXCN_HDMI	
	T14	VREG1_HDMI	
HSCL	R23	SCL_HDMI	
HSDA	R22	SDA_HDMI	
HHPD	P22	HPD_HDMI	
	P23	CEC_HDMI	

PWM

A14	PWM0/PB2	

E14	HSCL/UART7_TX/PS2_SCK0/PI20	
E13	HSDA/UART7_RX/PS2_SDA0/PI21	

ADC

AB23	LRADC0	
AB22	LRADC1	

TP

Y22	X1_TP	
AA22	X2_TP	
Y23	Y1_TP	
AA23	Y2_TP	

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LCD0

LCD0_D0/LVDS0_VP0/PD0	AB15	WIFI-SHDN	16
LCD0_D1/LVDS0_VN0/PD1	AC15		
LCD0_D2/LVDS0_VP1/PD2	AB14	USB0-DRV	10
LCD0_D3/LVDS0_VN1/PD3	AC14	USB0-IDDET	12
LCD0_D4/LVDS0_VP2/PD4	AB13	SD0-DET#	14
LCD0_D5/LVDS0_VN2/PD5	AC13	RECOVERY	14
LCD0_D6/LVDS0_VPC/PD6	AB12	VGA-DET	15
LCD0_D7/LVDS0_VNC/PD7	AC12	YPBPR-DET	15
LCD0_D8/LVDS0_VP3/PD8	AB11	AV-5V-EN	15
LCD0_D9/LVDS0_VN3/PD9	AC11	AP-WORK-DET#	18
LCD0_D10/LVDS1_VP0/PD10	Y15	AP-OFF-INT#	18
LCD0_D11/LVDS1_VN0/PD11	AA15	CSI0-STBY-EN	13
LCD0_D12/LVDS1_VP1/PD12	Y14	CSI0-PWR-EN	13
LCD0_D13/LVDS1_VN1/PD13	AA14	CSI0-RESET#	13
LCD0_D14/LVDS1_VP2/PD14	Y13	HDD-PWR-EN	13
LCD0_D15/LVDS1_VN2/PD15	AA13	EMAC-PWR-EN	20
LCD0_D16/LVDS1_VPC/PD16	Y12	STATUS-LED	18
LCD0_D17/LVDS1_VNC/PD17	AA12	PWR-LED	18
LCD0_D18/LVDS1_VP3/PD18	Y11		
LCD0_D19/LVDS1_VN3/PD19	AA11		
LCD0_D20/CSI1_MCLK/PD20	Y10		
LCD0_D21/SMC_VPPEN/PD21	AA10		
LCD0_D22/SMC_VPPPP/PD22	AB10		
LCD0_D23/SMC_DET/PD23	AC10	HUB-PWR-EN	10
LCD0_CLK/SMC_VCCEN/PD24	Y9		
LCD0_DE/SMC_RST/PD25	AA9		
LCD0_HSYNC/SMC_SLK/PD26	AB9	LCD0-HSYNC	15
LCD0_VSYNC/SMC_SDA/PD27	AC9	LCD0-VSYNC	15

LCD1

LCD1_D0/UART3_TX/EINT0/CSI1_D0/PH0	A6		
LCD1_D1/UART3_RX/EINT1/CSI1_D1/PH1	B6		
LCD1_D2/UART3_RTS/EINT2/CSI1_D2/PH2	C6		
LCD1_D3/UART3_CTS/EINT3/CSI1_D3/PH3	A5		
LCD1_D4/UART4_TX/EINT4/CSI1_D4/PH4	B5		
LCD1_D5/UART4_RX/EINT5/CSI1_D5/PH5	C5		
LCD1_D6/UART5_TX/MS_BS/EINT6/CSI1_D6/PH6	A4		
LCD1_D7/UART5_RX/MS_CLK/EINT7/CSI1_D7 /PH7	B4		
LCD1_D8/ERXD3/KP_IN0/MS_D0/EINT8/CSI1_D8/PH8	C4		
LCD1_D9/ERXD2/KP_IN1/MS_D1/EINT9/CSI1_D9/PH9	D4		
LCD1_D10/ERXD1/KP_IN2/MS_D2/EINT10/CSI1_D10/PH10	A3		
LCD1_D11/ERXD0/KP_IN3/MS_D3/EINT11/CSI1_D11/PH11	B3		
LCD1_D12/PS2_SCK1/EINT12/CSI1_D12/PH12	C3		
LCD1_D13/PS2_SDA1/SMC_RST/EINT13/CSI1_D13/PH13	A2		
LCD1_D14/ETXD3/KP_IN4/SMC_VPPEN/EINT14/CSI1_D14/PH14	B2		
LCD1_D15/ETXD2/KP_IN5/SMC_VPPPP/EINT15/CSI1_D15/PH15	A1		
LCD1_D16/ETXD1/KP_IN6/SMC_DET/EINT16/CSI1_D16/PH16	B1		
LCD1_D17/ETXD0/KP_IN7/SMC_VCCEN/EINT17/CSI1_D17/PH17	C1		
LCD1_D18/ERXCK/KP_OUT0/SMC_SLK/EINT18/CSI1_D18/PH18	C2		
LCD1_D19/ERXERR/KP_OUT1/SMC_SDA/EINT19/CSI1_D19/PH19	D1		
LCD1_D20/ERXDV/CAN_TX/EINT20/CSI1_D20/PH20	D2		
LCD1_D21/EMDC/CAN_RX/EINT21/CSI1_D21/PH21	D3		
LCD1_D22/EMDIO/KP_OUT2/SDC1_CMD/CSI1_D22/PH22	E1		
LCD1_D23/ETXEN/KP_OUT3/SDC1_CLK/CSI1_D23/PH23	E2		
LCD1_CLK/ETXCK/KP_OUT4/SDC1_D0/CSI1_PCLK/PH24	E3		
LCD1_DE/ECRS/KP_OUT5/SDC1_D1/CSI1_FIELD/PH25	E4		
LCD1_HSYNC/ECOL/KP_OUT6/SDC1_D2/CSI1_HSYNC/PH26	F3		
LCD1_VSYNC/ETXERR/KP_OUT7/SDC1_D3/CSI1_VSYNC/PH27	F4		

GND

DDR3-8BITX4

Please copy DRAM PCB template and follow PCB layout guide. The circuit is only for single-side PCB layout.

option

5,8 SDQ[31:0] SDQ[31:0]
5,8 SDQSB[3:0] SDQSB[3:0]
5,8 SDQS[3:0] SDQS[3:0]
5,8 SDQM[3:0] SDQM[3:0]
5,8 SA[15:0] SA[15:0]
5,8 SBA[2:0] SBA[2:0]
5,8 SCK-N
5,8 SCK
5,8 SCKE
5,8 SWE
5,8 SCAS
5,8 SRAS
5,8 SCS
5,8 SRST
5,8 SODT

DRAM-VCC
R2 2K-1% R0402
C1 104 C0402
5,8 CPU-REF
DREF
R3 2K-1% R0402
C2 104 C0402
GND

SCK R8 0R R0402 DSCK
C3 100R R0402
SCK-N R9 0R R0402 DSCK-N

U2

SA0	K3	A0	DQ0	B3	SDQ3
SA1	L7	A1	DQ1	C7	SDQ4
SA2	L3	A2	DQ2	C2	SDQ1
SA3	K2	A3	DQ3	C8	SDQ0
SA4	L8	A4	DQ4	E3	SDQ7
SA5	L2	A5	DQ5	E8	SDQ2
SA6	M8	A6	DQ6	D2	SDQ6
SA7	M2	A7	DQ7	E7	SDQ5
SA8	N8	A8			
SA9	M3	A9			
SA10	H7	A10/AP			
SA11	M7	A11			
SA12	K7	A12/BC#			
SA13	N3	A13			
SA14	N7	A14			
SA15	J7	A15			
SDQM0	B7	DM/TDQS	VDD1	A2	DRAM-VCC
	A7	NF/TDQS	VDD2	A9	
SDQS0	C3	DQS	VDD3	D7	
SDQSB0	D3	DQS	VDD4	G2	
SODT	G1	ODT	VDD5	G8	
SBA0	J2	BA0	VDD6	K1	
SBA1	K8	BA1	VDD7	K9	
SBA2	J3	BA2	VDD8	M1	
			VDD9	M9	
SCAS	G3	CAS	VDDQ1	B9	
SRAS	F3	RAS	VDDQ2	C1	
SCS	H2	CS	VDDQ3	E2	
DSCK	F7	CK	VDDQ4	E9	
DSCK-N	G7	CK			
SCKE	G9	CKE	VSS1	A1	
SWE	H3	WE	VSS2	A8	
SRST	N2	RESET	VSS3	B1	
DREF	E1	VREFDQ	VSS4	D8	
	J8	VREFCA	VSS5	F2	
	H8	ZQ	VSS6	F8	
			VSS7	J1	
R4 240-1% R0402	A3	NC1	VSS8	J9	
	F1	NC2	VSS9	L1	
	F9	NC3	VSS10	L9	
	H1	NC4	VSS11	N1	
	H9	NC5	VSS12	N9	
			VSSQ1	B2	
			VSSQ2	B8	
			VSSQ3	C9	
			VSSQ4	D1	
			VSSQ5	D9	

DDR3x8
GND

U3

SA0	K3	A0	DQ0	B3	SDQ15
SA1	L7	A1	DQ1	C7	SDQ11
SA2	L3	A2	DQ2	C2	SDQ8
SA3	K2	A3	DQ3	C8	SDQ9
SA4	L8	A4	DQ4	E3	SDQ13
SA5	L2	A5	DQ5	E8	SDQ14
SA6	M8	A6	DQ6	D2	SDQ10
SA7	M2	A7	DQ7	E7	SDQ12
SA8	N8	A8			
SA9	M3	A9			
SA10	H7	A10/AP			
SA11	M7	A11			
SA12	K7	A12/BC#			
SA13	N3	A13			
SA14	N7	A14			
SA15	J7	A15			
SDQM1	B7	DM/TDQS	VDD1	A2	DRAM-VCC
	A7	NF/TDQS	VDD2	A9	
SDQS1	C3	DQS	VDD3	D7	
SDQSB1	D3	DQS	VDD4	G2	
SODT	G1	ODT	VDD5	G8	
SBA0	J2	BA0	VDD6	K1	
SBA1	K8	BA1	VDD7	K9	
SBA2	J3	BA2	VDD8	M1	
			VDD9	M9	
SCAS	G3	CAS	VDDQ1	B9	
SRAS	F3	RAS	VDDQ2	C1	
SCS	H2	CS	VDDQ3	E2	
DSCK	F7	CK	VDDQ4	E9	
DSCK-N	G7	CK			
SCKE	G9	CKE	VSS1	A1	
SWE	H3	WE	VSS2	A8	
SRST	N2	RESET	VSS3	B1	
DREF	E1	VREFDQ	VSS4	D8	
	J8	VREFCA	VSS5	F2	
	H8	ZQ	VSS6	F8	
			VSS7	J1	
R5 240-1% R0402	A3	NC1	VSS8	J9	
	F1	NC2	VSS9	L1	
	F9	NC3	VSS10	L9	
	H1	NC4	VSS11	N1	
	H9	NC5	VSS12	N9	
			VSSQ1	B2	
			VSSQ2	B8	
			VSSQ3	C9	
			VSSQ4	D1	
			VSSQ5	D9	

DDR3x8
GND

U4

SA0	K3	A0	DQ0	B3	SDQ19
SA1	L7	A1	DQ1	C7	SDQ20
SA2	L3	A2	DQ2	C2	SDQ17
SA3	K2	A3	DQ3	C8	SDQ16
SA4	L8	A4	DQ4	E3	SDQ23
SA5	L2	A5	DQ5	E8	SDQ18
SA6	M8	A6	DQ6	D2	SDQ22
SA7	M2	A7	DQ7	E7	SDQ21
SA8	N8	A8			
SA9	M3	A9			
SA10	H7	A10/AP			
SA11	M7	A11			
SA12	K7	A12/BC#			
SA13	N3	A13			
SA14	N7	A14			
SA15	J7	A15			
SDQM2	B7	DM/TDQS	VDD1	A2	DRAM-VCC
	A7	NF/TDQS	VDD2	A9	
SDQS2	C3	DQS	VDD3	D7	
SDQSB2	D3	DQS	VDD4	G2	
SODT	G1	ODT	VDD5	G8	
SBA0	J2	BA0	VDD6	K1	
SBA1	K8	BA1	VDD7	K9	
SBA2	J3	BA2	VDD8	M1	
			VDD9	M9	
SCAS	G3	CAS	VDDQ1	B9	
SRAS	F3	RAS	VDDQ2	C1	
SCS	H2	CS	VDDQ3	E2	
DSCK	F7	CK	VDDQ4	E9	
DSCK-N	G7	CK			
SCKE	G9	CKE	VSS1	A1	
SWE	H3	WE	VSS2	A8	
SRST	N2	RESET	VSS3	B1	
DREF	E1	VREFDQ	VSS4	D8	
	J8	VREFCA	VSS5	F2	
	H8	ZQ	VSS6	F8	
			VSS7	J1	
R6 240-1% R0402	A3	NC1	VSS8	J9	
	F1	NC2	VSS9	L1	
	F9	NC3	VSS10	L9	
	H1	NC4	VSS11	N1	
	H9	NC5	VSS12	N9	
			VSSQ1	B2	
			VSSQ2	B8	
			VSSQ3	C9	
			VSSQ4	D1	
			VSSQ5	D9	

DDR3x8
GND

U5

SA0	K3	A0	DQ0	B3	SDQ31
SA1	L7	A1	DQ1	C7	SDQ27
SA2	L3	A2	DQ2	C2	SDQ24
SA3	K2	A3	DQ3	C8	SDQ25
SA4	L8	A4	DQ4	E3	SDQ29
SA5	L2	A5	DQ5	E8	SDQ30
SA6	M8	A6	DQ6	D2	SDQ26
SA7	M2	A7	DQ7	E7	SDQ28
SA8	N8	A8			
SA9	M3	A9			
SA10	H7	A10/AP			
SA11	M7	A11			
SA12	K7	A12/BC#			
SA13	N3	A13			
SA14	N7	A14			
SA15	J7	A15			
SDQM3	B7	DM/TDQS	VDD1	A2	DRAM-VCC
	A7	NF/TDQS	VDD2	A9	
SDQS3	C3	DQS	VDD3	D7	
SDQSB3	D3	DQS	VDD4	G2	
SODT	G1	ODT	VDD5	G8	
SBA0	J2	BA0	VDD6	K1	
SBA1	K8	BA1	VDD7	K9	
SBA2	J3	BA2	VDD8	M1	
			VDD9	M9	
SCAS	G3	CAS	VDDQ1	B9	
SRAS	F3	RAS	VDDQ2	C1	
SCS	H2	CS	VDDQ3	E2	
DSCK	F7	CK	VDDQ4	E9	
DSCK-N	G7	CK			
SCKE	G9	CKE	VSS1	A1	
SWE	H3	WE	VSS2	A8	
SRST	N2	RESET	VSS3	B1	
DREF	E1	VREFDQ	VSS4	D8	
	J8	VREFCA	VSS5	F2	
	H8	ZQ	VSS6	F8	
			VSS7	J1	
R7 240-1% R0402	A3	NC1	VSS8	J9	
	F1	NC2	VSS9	L1	
	F9	NC3	VSS10	L9	
	H1	NC4	VSS11	N1	
	H9	NC5	VSS12	N9	
			VSSQ1	B2	
			VSSQ2	B8	
			VSSQ3	C9	
			VSSQ4	D1	
			VSSQ5	D9	

DDR3x8
GND

DRAM-VCC
C4 1uF C0402
C5 104 C0402
C6 104 C0402
C7 104 C0402
GND

DRAM-VCC
C8 1uF C0402
C9 104 C0402
C10 104 C0402
C11 104 C0402
GND

DRAM-VCC
C12 1uF C0402
C13 104 C0402
C14 104 C0402
C15 104 C0402
GND

DRAM-VCC
C16 1uF C0402
C17 104 C0402
C18 104 C0402
C19 104 C0402
GND

DREF C25 104 C0402 GND
DREF C26 104 C0402 GND
DREF C27 104 C0402 GND
DREF C28 104 C0402 GND

AllWinner Technology Co.,Ltd		
Design Name: A20_HOMLET_STD		
Size: A3	Page Name: DDR3 8bit x 4pcs	Rev: 1.0
Date: Wednesday, June 04, 2014	Sheet 7 of 22	

DDR3-16BITX2

5,7 SDQ[31:0] — SDQ[31:0]
5,7 SDQSB[3:0] — SDQSB[3:0]
5,7 SDQS[3:0] — SDQS[3:0]
5,7 SDQM[3:0] — SDQM[3:0]
5,7 SA[15:0] — SA[15:0]
5,7 SBA[2:0] — SBA[2:0]
5,7 SCK-N
5,7 SCK
5,7 SCKE
5,7 SWE
5,7 SCAS
5,7 SRAS
5,7 SCS
5,7 SRST
5,7 SODT

DRAM-VCC
R2 2K-1% R0402
C1 104 C0402
5,7 CPU-REF — DREF
R3 2K-1% R0402
C2 104 C0402
GND

SCK — R8 0R R0402 — D-SCK
C3 100R R0402
SCK-N — R9 0R R0402 — D-SCK-N

U2

SA0	N3	A0	DQL0	E3	SDQ6
SA1	P7	A1	DQL1	F7	SDQ4
SA2	P3	A2	DQL2	F2	SDQ7
SA3	N2	A3	DQL3	F8	SDQ0
SA4	P8	A4	DQL4	H3	SDQ3
SA5	P2	A5	DQL5	H8	SDQ2
SA6	R8	A6	DQL6	G2	SDQ1
SA7	R2	A7	DQL7	H7	SDQ5
SA8	T8	A8	DQU0	D7	SDQ14
SA9	R3	A9	DQU1	C3	SDQ15
SA10	L7	A10	DQU2	C8	SDQ11
SA11	R7	A11	DQU3	C2	SDQ8
SA12	N7	A12	DQU4	A7	SDQ9
SA13	T3	A13	DQU5	A2	SDQ13
SA14	T7	A14	DQU6	B8	SDQ12
SA15	M7	A15	DQU7	A3	SDQ10
SBA0	M2	BA0	CK	J7	D-SCK
SBA1	N8	BA1	CK#	K7	D-SCK-N
SBA2	M3	BA2	DQSL	F3	SDQS0
			DQSL#	G3	SDQSB0
SWE	L3	WE	DQSU	C7	SDQS1
SRAS	J3	RAS#	DQSU#	B7	SDQSB1
SCAS	K3	CAS#	DML	E7	SDQM0
SCS	L2	CS#	DMU	D3	SDQM1
SCKE	K9	CKE		J1	
DREF	M8		NC#1	L1	
DREF	H1	VREFCA	NC#2	J9	
SODT	K1	VREFDQ	NC#3	L9	
		ODT	NC#4		
	A1			T2	SRST
DRAM-VCC	C1	VDDQ#1	RESET	L8	
	F1	VDDQ#2	ZQ		
	D2	VDDQ#3			
	H2	VDDQ#4			
	A8	VDDQ#5	VSSQ#1	B1	
	H9	VDDQ#6	VSSQ#2	D1	
	E9	VDDQ#7	VSSQ#3	G1	
	C9	VDDQ#8	VSSQ#4	E2	
	N1	VDDQ#9	VSSQ#5	D8	
	R1	VDD#1	VSSQ#6	E8	
	B2	VDD#2	VSSQ#7	B9	
	K2	VDD#3	VSSQ#8	F9	
	G7	VDD#4	VSSQ#9	G9	
	K8	VDD#5	VSS#1	E1	
	D9	VDD#6	VSS#2	M1	
	N9	VDD#7	VSS#3	P1	
	R9	VDD#8	VSS#4	T1	
		VDD#9	VSS#5	J2	
			VSS#6	B3	
			VSS#7	G8	
			VSS#8	J8	
			VSS#9	A9	
			VSS#10	M9	
			VSS#11	P9	
			VSS#12	T9	

R4 240-1% R0402
GND
DDR3-FBGA96
FBGA96C80P9X13

U3

SA0	N3	A0	DQL0	E3	SDQ19
SA1	P7	A1	DQL1	F7	SDQ20
SA2	P3	A2	DQL2	F2	SDQ17
SA3	N2	A3	DQL3	F8	SDQ16
SA4	P8	A4	DQL4	H3	SDQ23
SA5	P2	A5	DQL5	H8	SDQ21
SA6	R8	A6	DQL6	G2	SDQ22
SA7	R2	A7	DQL7	H7	SDQ18
SA8	T8	A8	DQU0	D7	SDQ30
SA9	R3	A9	DQU1	C3	SDQ29
SA10	L7	A10	DQU2	C8	SDQ28
SA11	R7	A11	DQU3	C2	SDQ24
SA12	N7	A12	DQU4	A7	SDQ25
SA13	T3	A13	DQU5	A2	SDQ31
SA14	T7	A14	DQU6	B8	SDQ27
SA15	M7	A15	DQU7	A3	SDQ26
SBA0	M2	BA0	CK	J7	D-SCK
SBA1	N8	BA1	CK#	K7	D-SCK-N
SBA2	M3	BA2	DQSL	F3	SDQS2
			DQSL#	G3	SDQSB2
SWE	L3	WE	DQSU	C7	SDQS3
SRAS	J3	RAS#	DQSU#	B7	SDQSB3
SCAS	K3	CAS#	DML	E7	SDQM2
SCS	L2	CS#	DMU	D3	SDQM3
SCKE	K9	CKE		J1	
DREF	M8		NC#1	L1	
DREF	H1	VREFCA	NC#2	J9	
SODT	K1	VREFDQ	NC#3	L9	
		ODT	NC#4		
	A1			T2	SRST
DRAM-VCC	C1	VDDQ#1	RESET	L8	
	F1	VDDQ#2	ZQ		
	D2	VDDQ#3			
	H2	VDDQ#4			
	A8	VDDQ#5	VSSQ#1	B1	
	H9	VDDQ#6	VSSQ#2	D1	
	E9	VDDQ#7	VSSQ#3	G1	
	C9	VDDQ#8	VSSQ#4	E2	
	N1	VDDQ#9	VSSQ#5	D8	
	R1	VDD#1	VSSQ#6	E8	
	B2	VDD#2	VSSQ#7	B9	
	K2	VDD#3	VSSQ#8	F9	
	G7	VDD#4	VSSQ#9	G9	
	K8	VDD#5	VSS#1	E1	
	D9	VDD#6	VSS#2	M1	
	N9	VDD#7	VSS#3	P1	
	R9	VDD#8	VSS#4	T1	
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			VSS#6	B3	
			VSS#7	G8	
			VSS#8	J8	
			VSS#9	A9	
			VSS#10	M9	
			VSS#11	P9	
			VSS#12	T9	

R5 240-1% R0402
GND
DDR3-FBGA96
FBGA96C80P9X13

DREF — C25 104 C0402 — GND
DRAM-VCC
C4 1uF C0402 C5 1uF C0402 C6 104 C0402 C7 104 C0402 C8 104 C0402
GND

DREF — C26 104 C0402 — GND
DRAM-VCC
C10 1uF C0402 C11 1uF C0402 C12 104 C0402 C13 104 C0402 C9 104 C0402
GND

AllWinner Technology Co.,Ltd
Design Name: A20_HOMLET_STD
Size: A3 | Page Name: DDR3 16bit x 2pcs | Rev: 1.0
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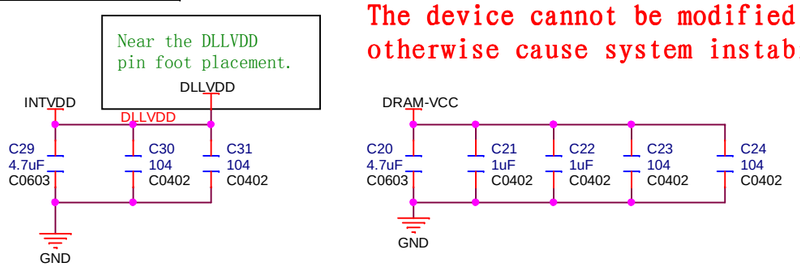
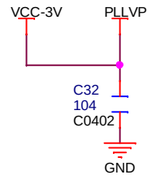
BESIDE CPU

The device cannot be modified or deleted, otherwise cause system instability!

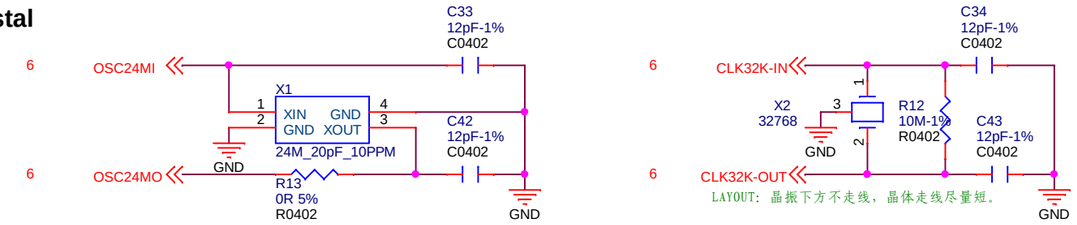
DRAM



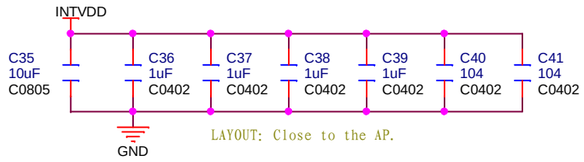
PLL



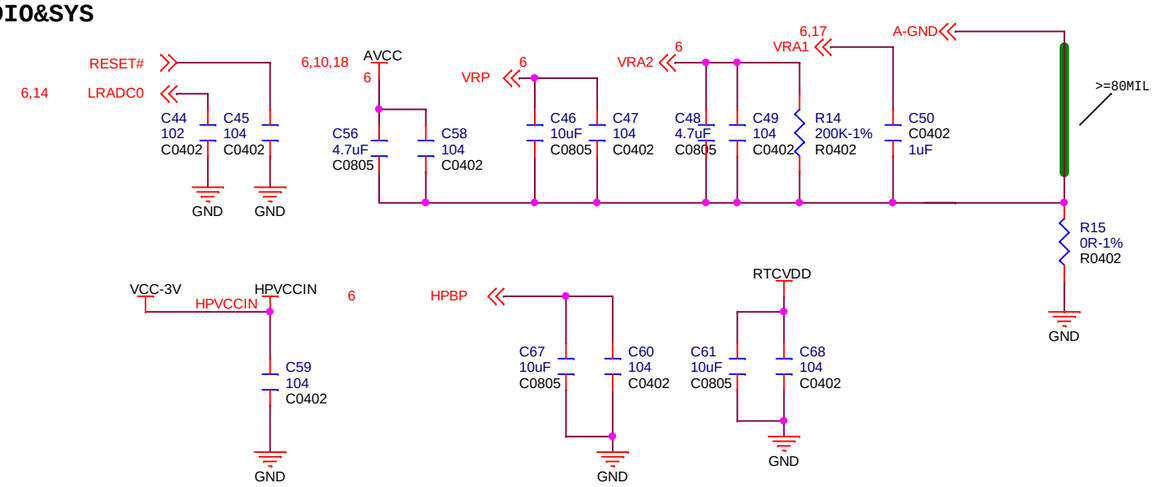
Crystal



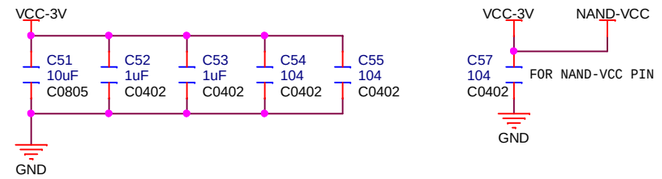
CORE

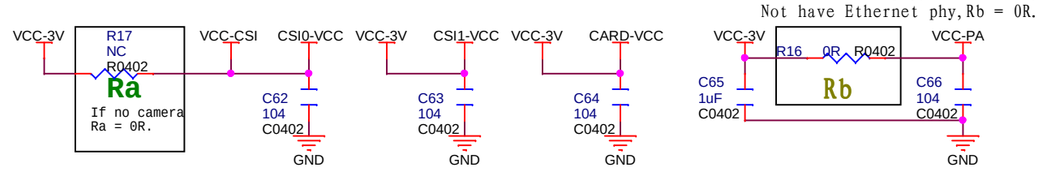


AUDIO&SYS

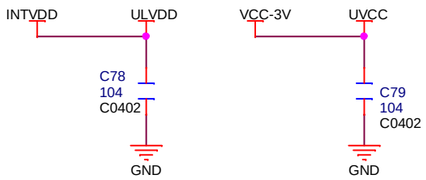


PIO-INTFACE

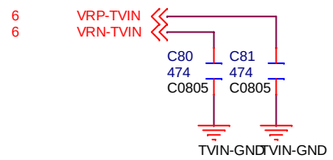




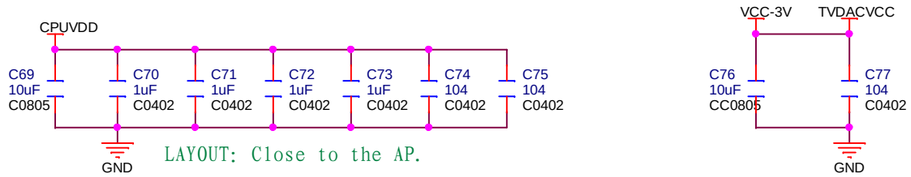
USB



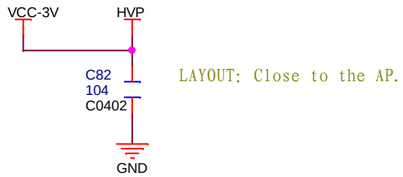
TVIN



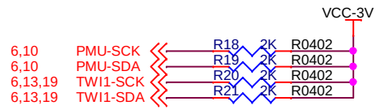
CPU&TV



HDMI



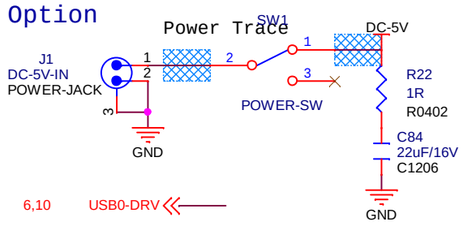
TWI-PULLUP

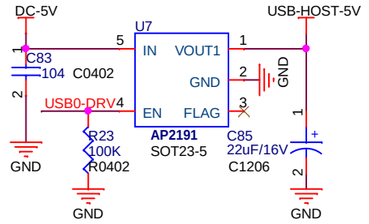


AllWinner Technology Co.,Ltd		
Design Name: A20_HOMLET_STD		
Size: A3	Page Name: BESIDE CPU	Rev: 1.0
Date: Wednesday, June 04, 2014	Sheet 9 of 22	

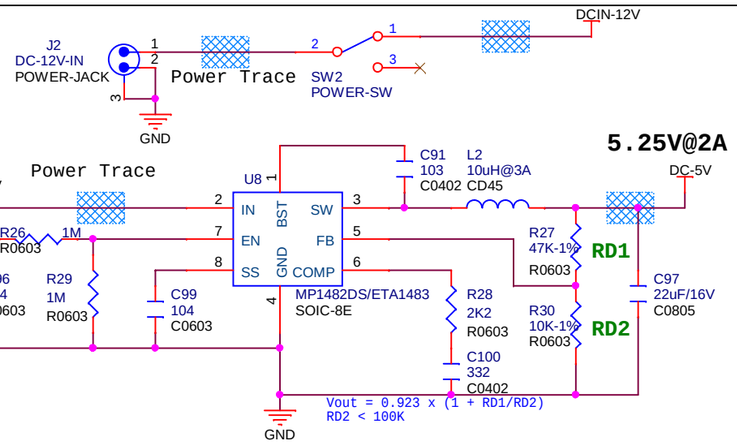
DC-IN-5V

Option





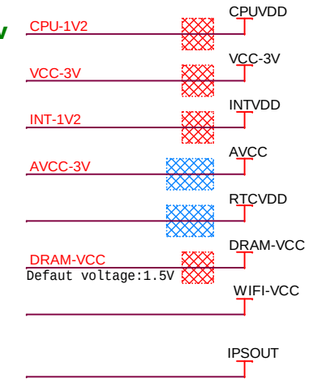
DC-IN-12V

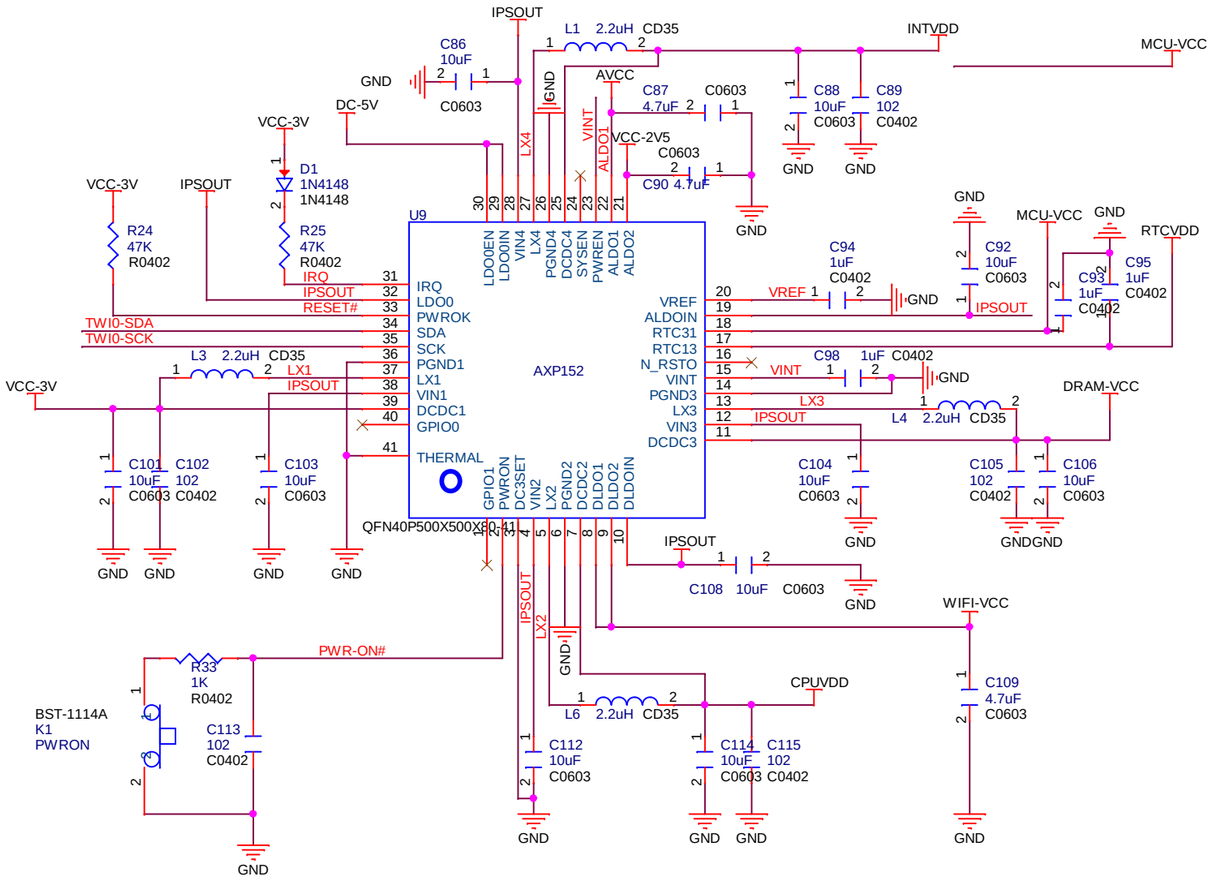


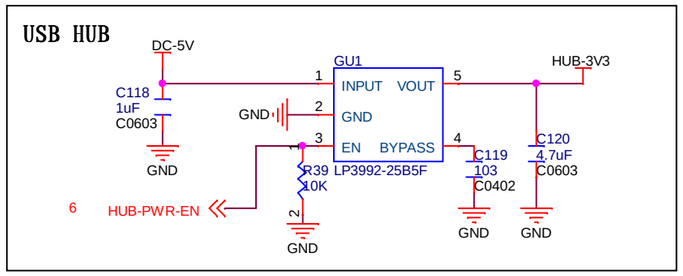
PMU-AXP152

LAYOUT注意：要求电源层做电源切割。
优先级：CPUVDD>DRAM-VCC>INTVDD>VCC-3V

按电源线规范走线，保证线宽。







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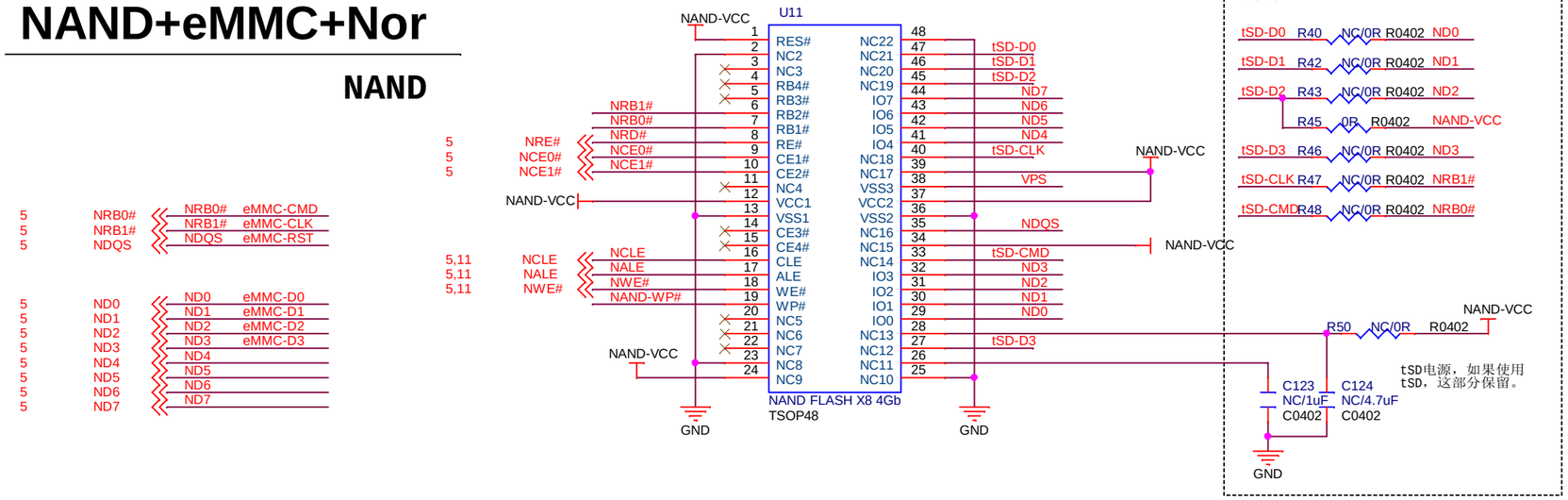
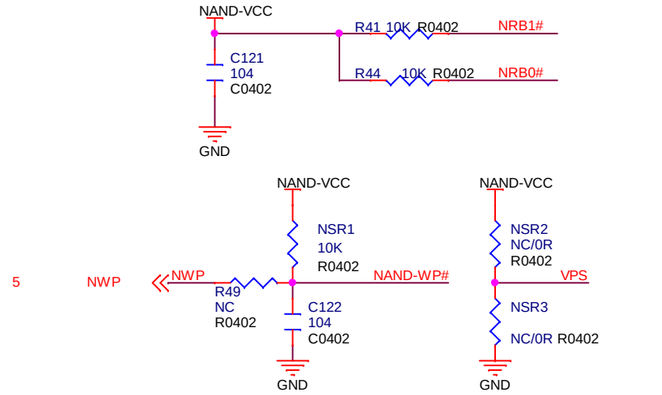
NAND+eMMC+Nor

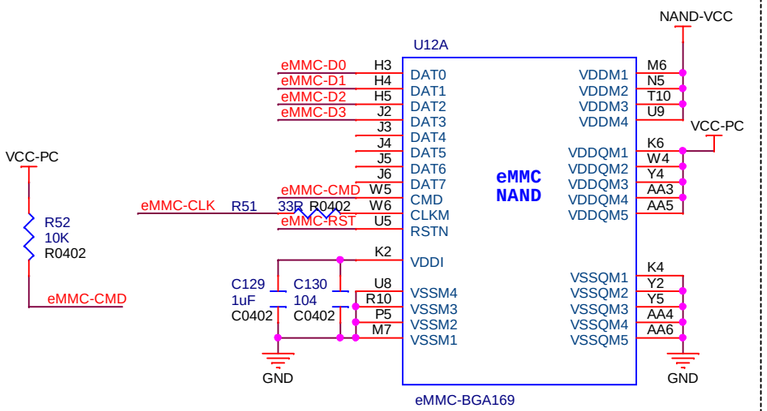
NAND



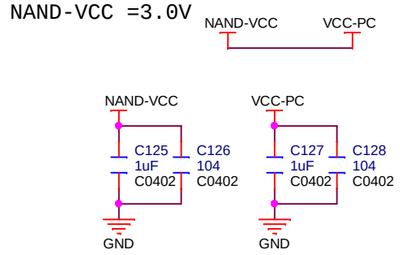


Please check datasheet when pasting NSR2 or NSR3

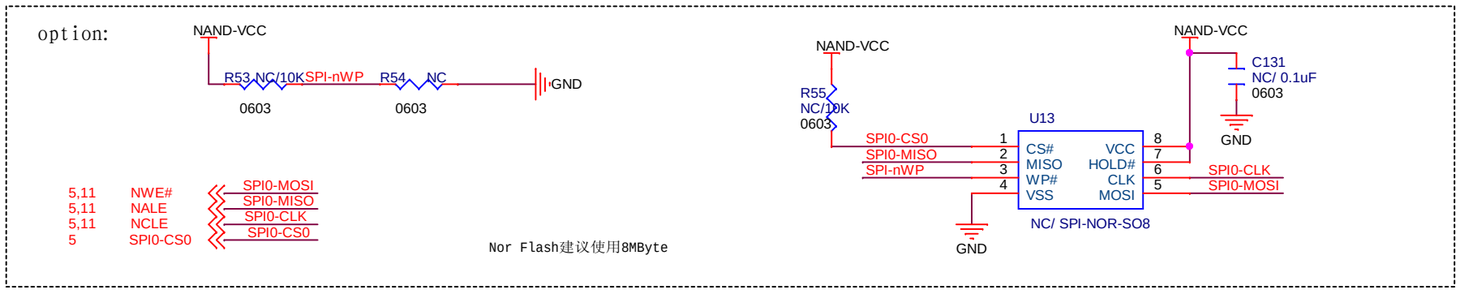
eMMC



Note layout :Put the eMMC in TSOP48, producing two choose one..



Nor



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Design Name	A20_HOMLET_STD
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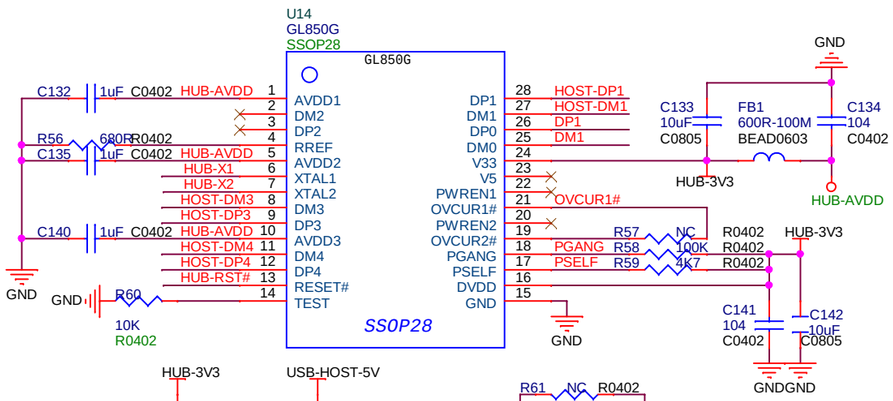
USB

USB HUB

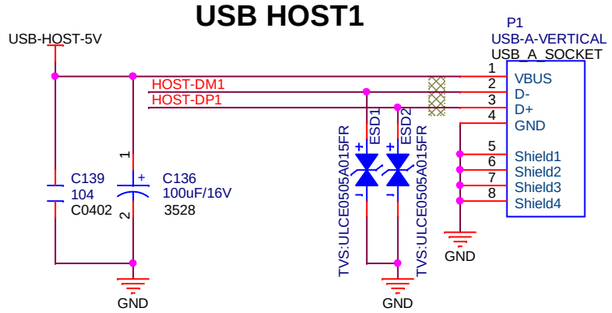
6 DM1
6 DP1
16 HOST-DM3
16 HOST-DP3
HOST-DM3
HOST-DP3

For wifi

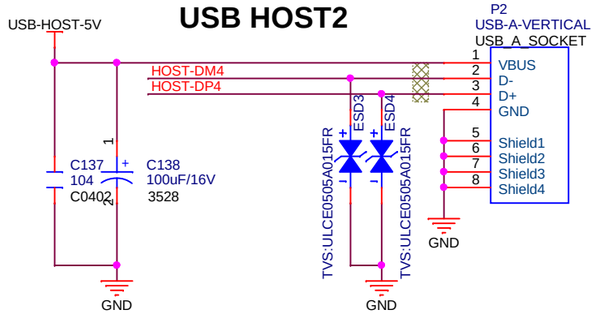
Differential pairs
Z0= 90 ohm +/-5 ohm



USB HOST1



USB HOST2

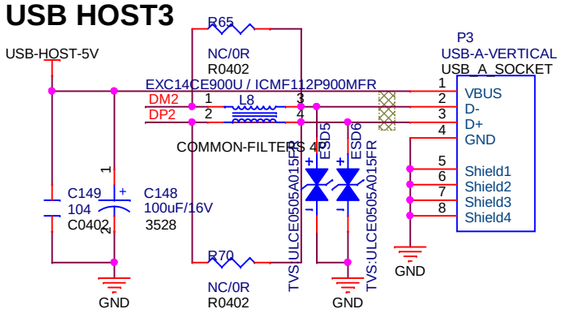


If the use of hard disk, the need to pay attention to the power load capacity.

USB HOST

6 DM2
6 DP2

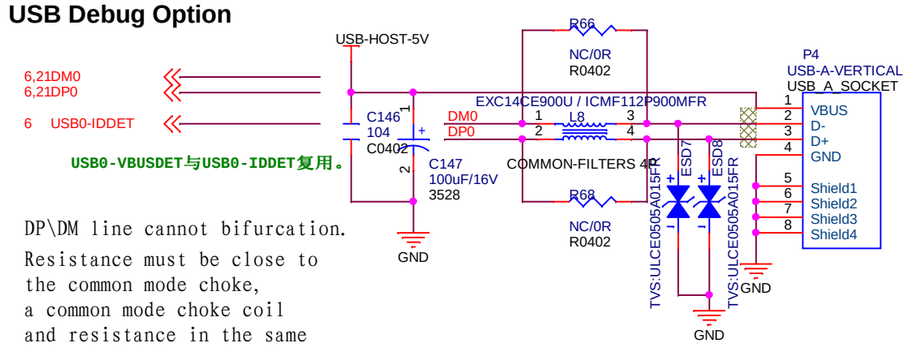
USB HOST3



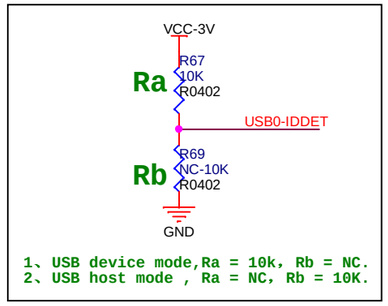
USB Debug Option

6,21DM0
6,21DP0
6 USB0-IDDET

USB0-VBUSDET与USB0-IDDET复用。



DP\DM line cannot bifurcation.
Resistance must be close to the common mode choke, a common mode choke coil and resistance in the same DP\DM network.



1、USB device mode,Ra = 10k, Rb = NC.
2、USB host mode , Ra = NC, Rb = 10K.

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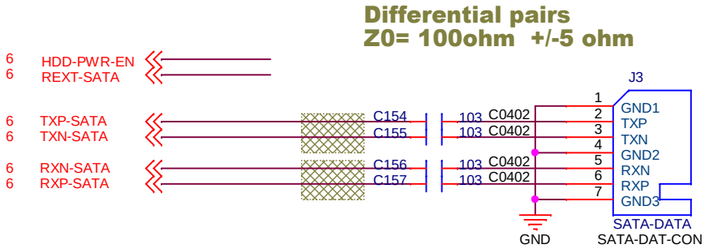
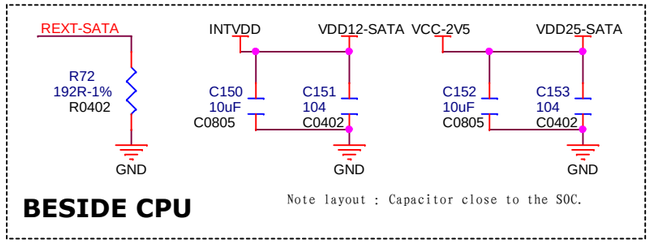
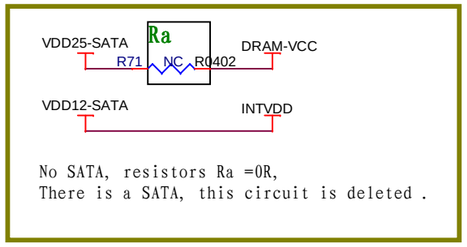
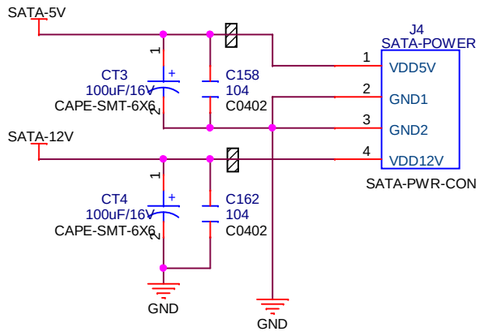
SATA-CSI

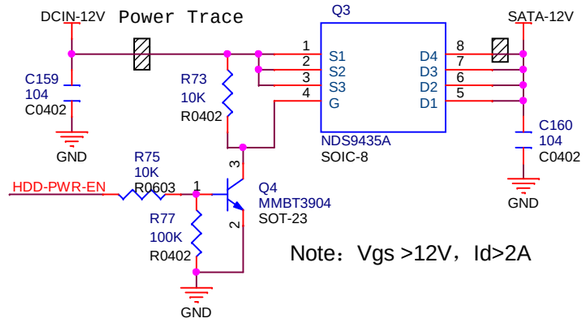
SATA

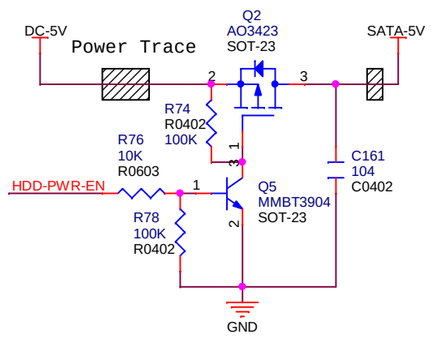






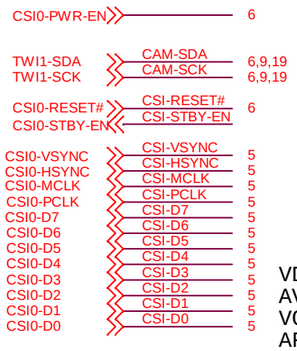




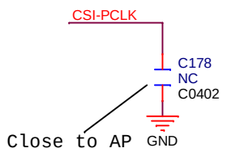


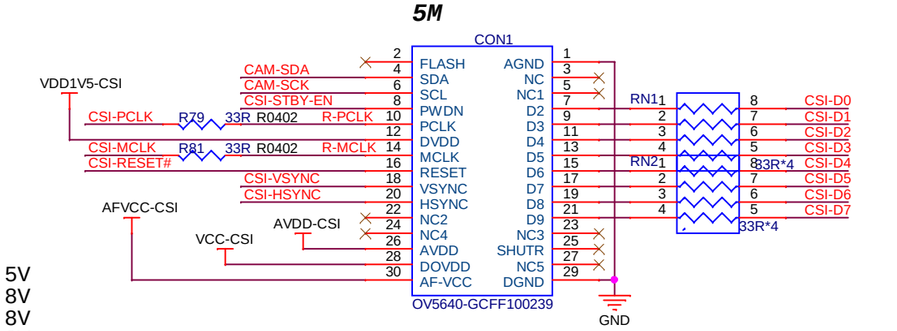
CSI

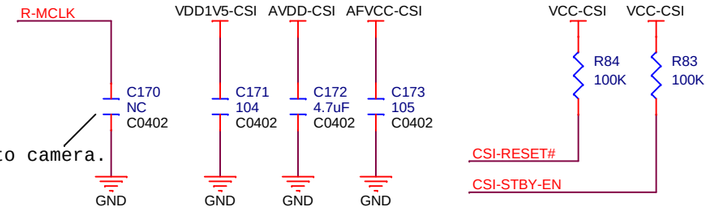
OPTION: (5M)
If the camera is not used, please remove the camera!

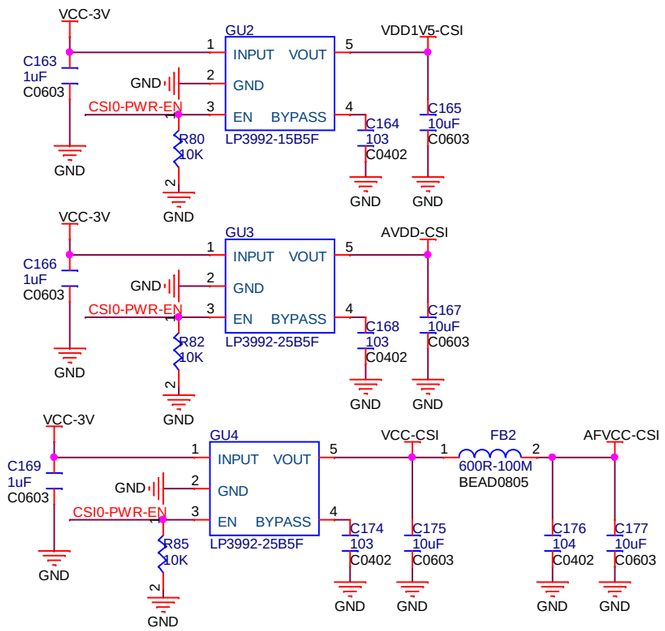


VDD1V5-CSI=1.5V
AVDD-CSI =2.8V
VCC-CSI =2.8V
AFVCC-CSI =2.8V







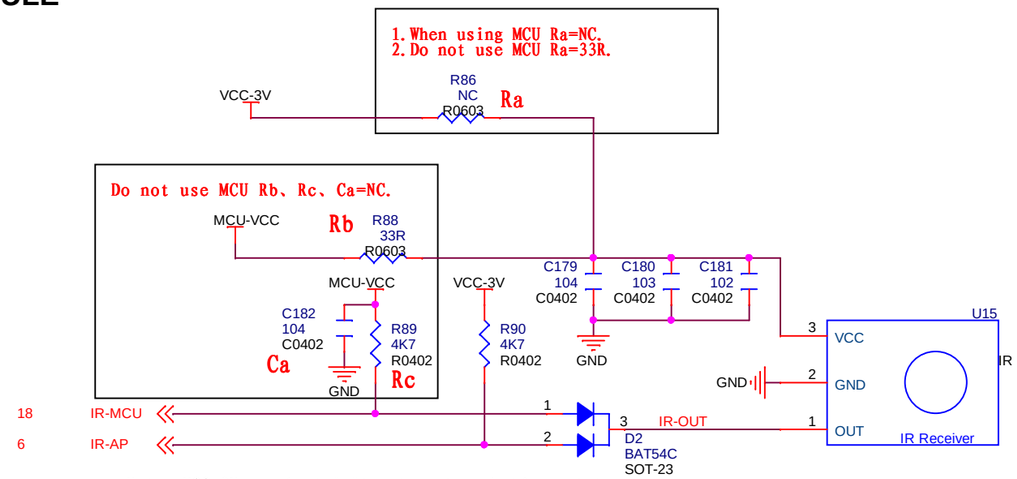


KEY-IR-JTAG-UART-SD

Debug

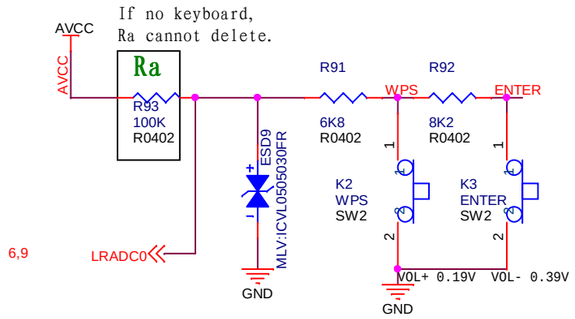
JTAG port : For debugging hardware, and cannot be deleted!
UART0 port: For the development of software, the output
to print information, and cannot be deleted!

IR MODULE

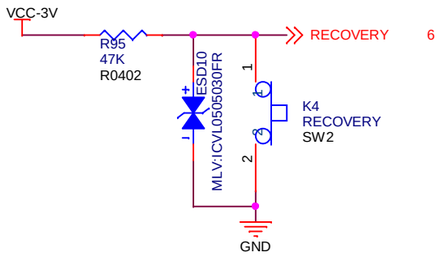


Note: VCC-3V no electricity at system shutdown state.
MCU-VCC has been in the insert adapter.

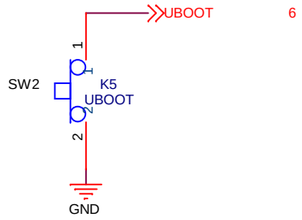
KEY



Recovery key必须保留。

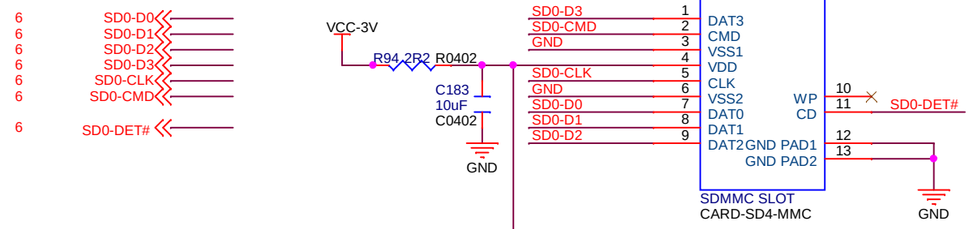


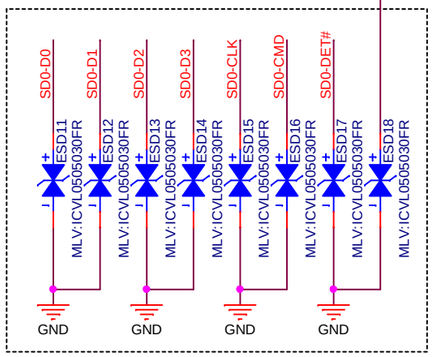
The Recovery key:
The key for the system upgrade.
必须保留。



The UBOOT key:
As the system of mandatory upgrade button.

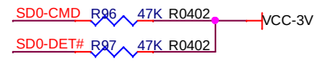
SD-CARD0





Supported card production and card start.

The pull-up resistor cannot be deleted.



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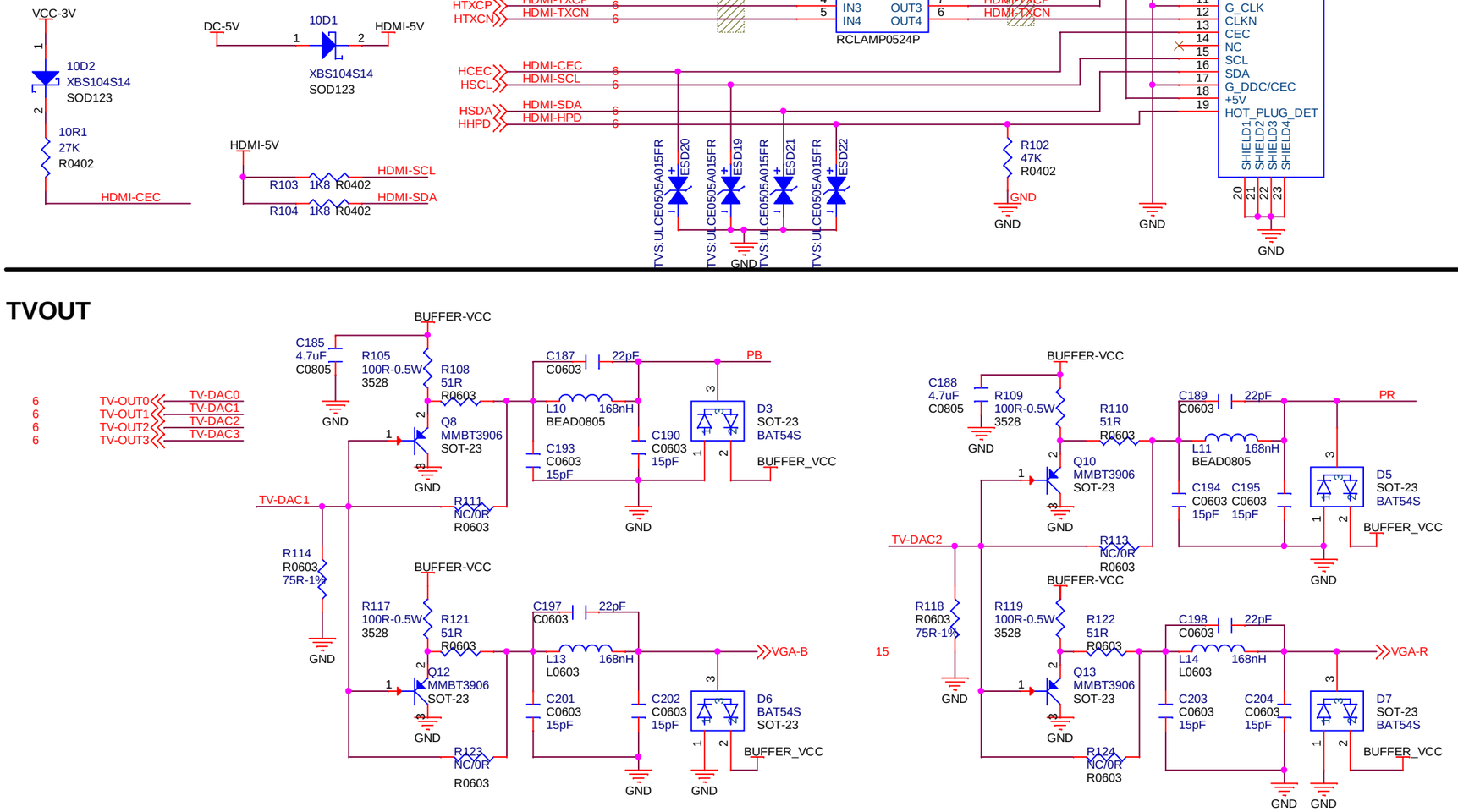
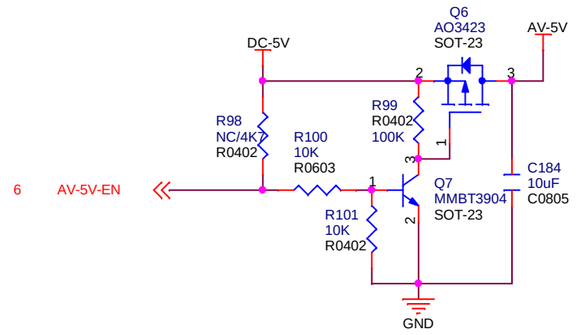
HDMI-TVOUT

HDMI

Differential pairs
Z0= 100 ohm +/-5 ohm

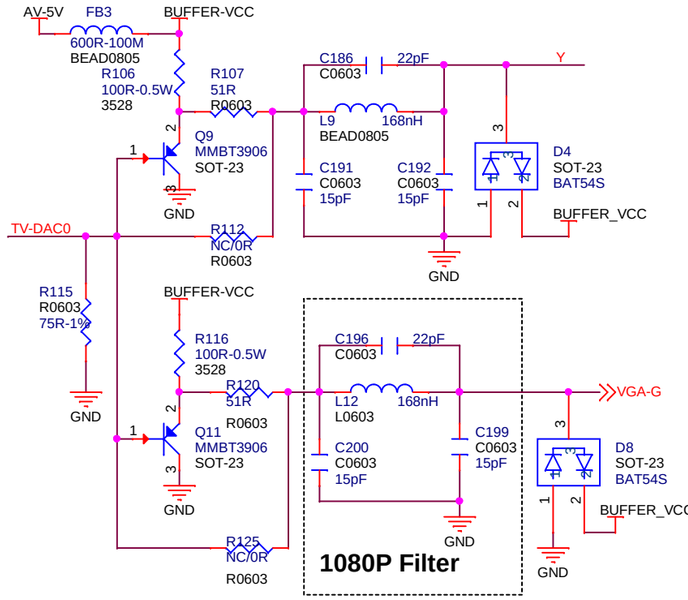


AV-5V

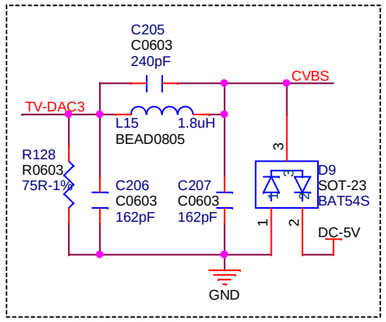


When the system is in standby, shut off the TV HDMI pour current.

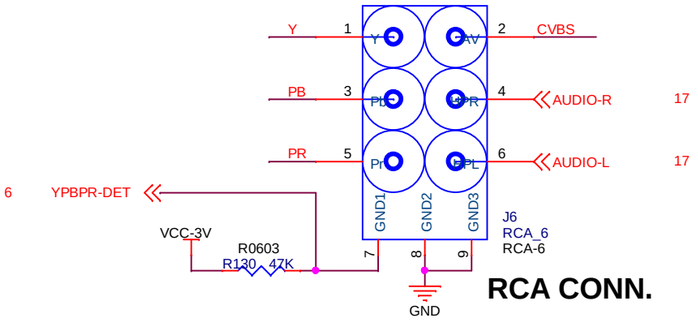
TVOUT



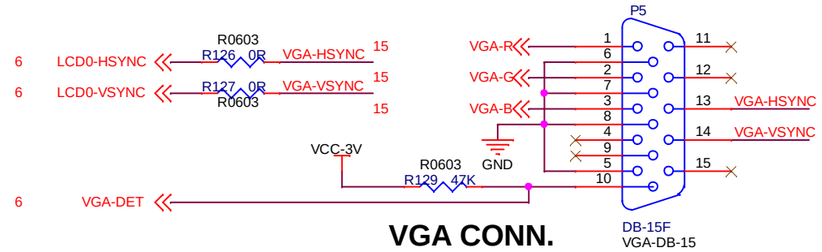
YPbPr and VGA need to share the main control TVDAC. It is best to choose one of two using (VGA and YPbPr cannot be simultaneously output),
if the two circuit is selected at the same time, need to add an buffer circuit, to prevent VGA and YPbPr inserted at the same time leads to poor quality images.



CVBS Filter



RCA CONN.



VGA CONN.

In order to realize the plug wire detection.GND1,GND2 and GND3 are separated.
When not inserted YPbPr line, the GND1 is a high level . When inserted into the YPbPr line, GND1 through the YPbPr line wire connected to the system of GND, YPBPR-DE is pulled low, so as to judge the plug wire. Detection of VGA-DET also is such.

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WIFI_BT

6 BT-PCM-OUT — BT-PCM-OUT
6 BT-PCM-IN — BT-PCM-IN
6 BT-PCM-SYNC — BT-PCM-SYNC
6 BT-PCM-CLK — BT-PCM-CLK

6 AP-BT-CTS — BT-UART-RTS
6 AP-BT-RTS — BT-UART-CTS
6 AP-BT-TXD — BT-UART-RXD
6 AP-BT-RXD — BT-UART-TXD

6 SD3-D0 — SDIO-D0
6 SD3-D1 — SDIO-D1
6 SD3-D2 — SDIO-D2
6 SD3-D3 — SDIO-D3
6 SD3-CMD — SDIO-CMD
6 SD3-CLK — SDIO-CLK

6 BT-REST — BT-REST

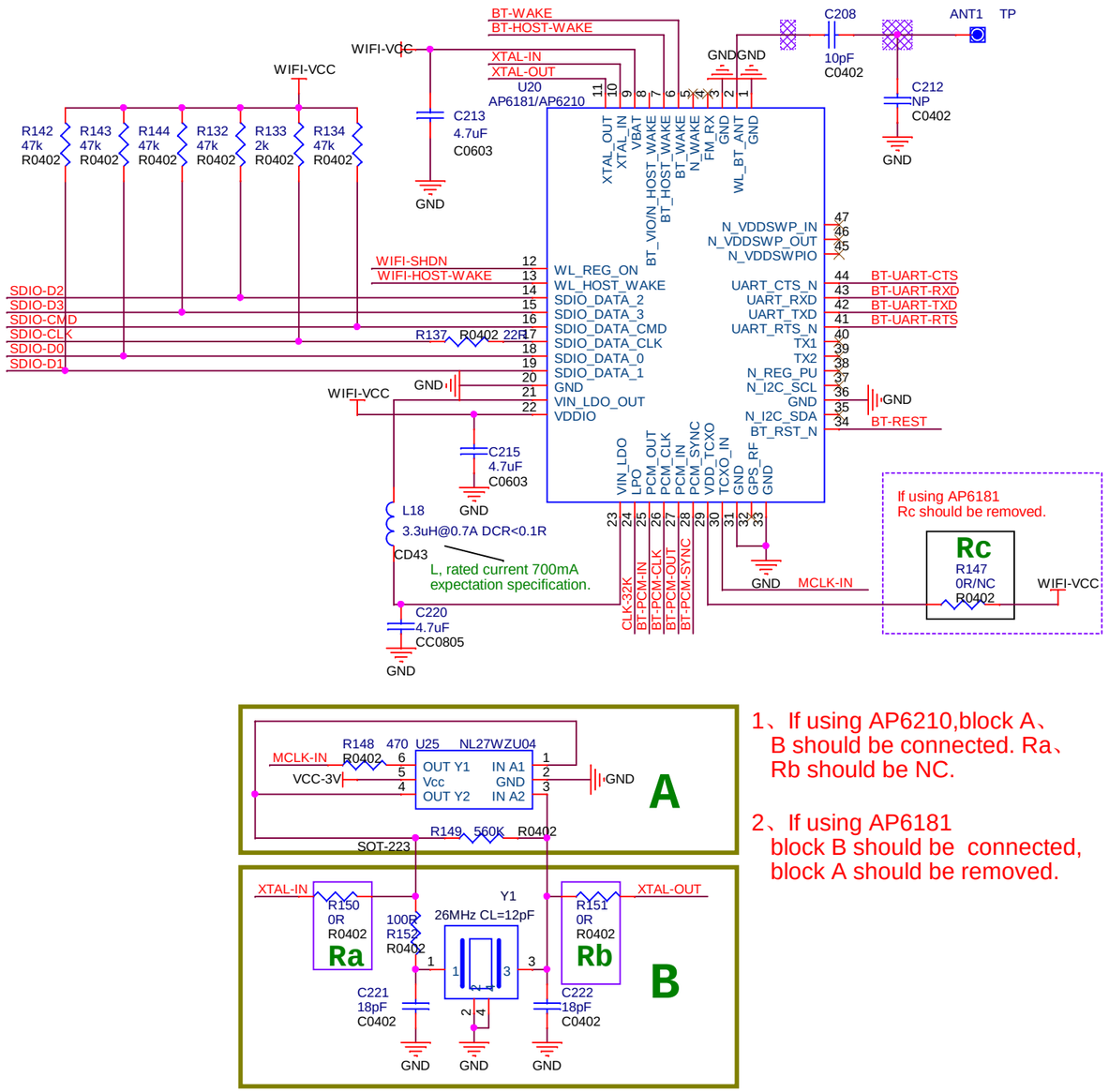
6 BT-WAKE — BT-WAKE
6 BT-HOST-WAKE — BT-HOST-WAKE

6 WIFI-SHDN — WIFI-SHDN
6 WIFI-HOST-WAKE — WIFI-HOST-WAKE

6 CLK-32K — CLK-32K

RF trace
50 Ohm

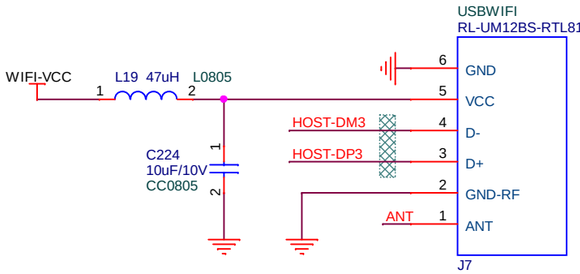
1.AP6181:BCM40181/2.4GHz WiFi only
2.AP6210:BCM40181 +20710/Combo(WLAN+BT4.0)
Support AP6181/AP6210

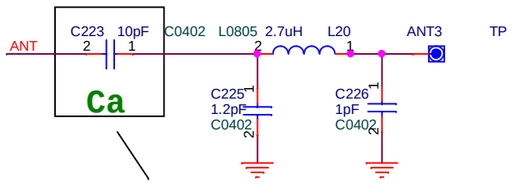


1、If using AP6210,block A、B should be connected. Ra、Rb should be NC.

2、If using AP6181 block B should be connected, block A should be removed.

USB-WIFI





The capacitor Ca is placed at a distance of less than 5mm module edge,or the capacitor Ca = 0R.

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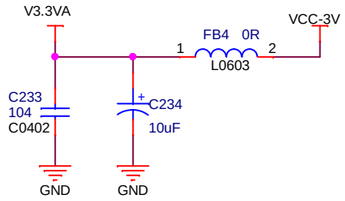
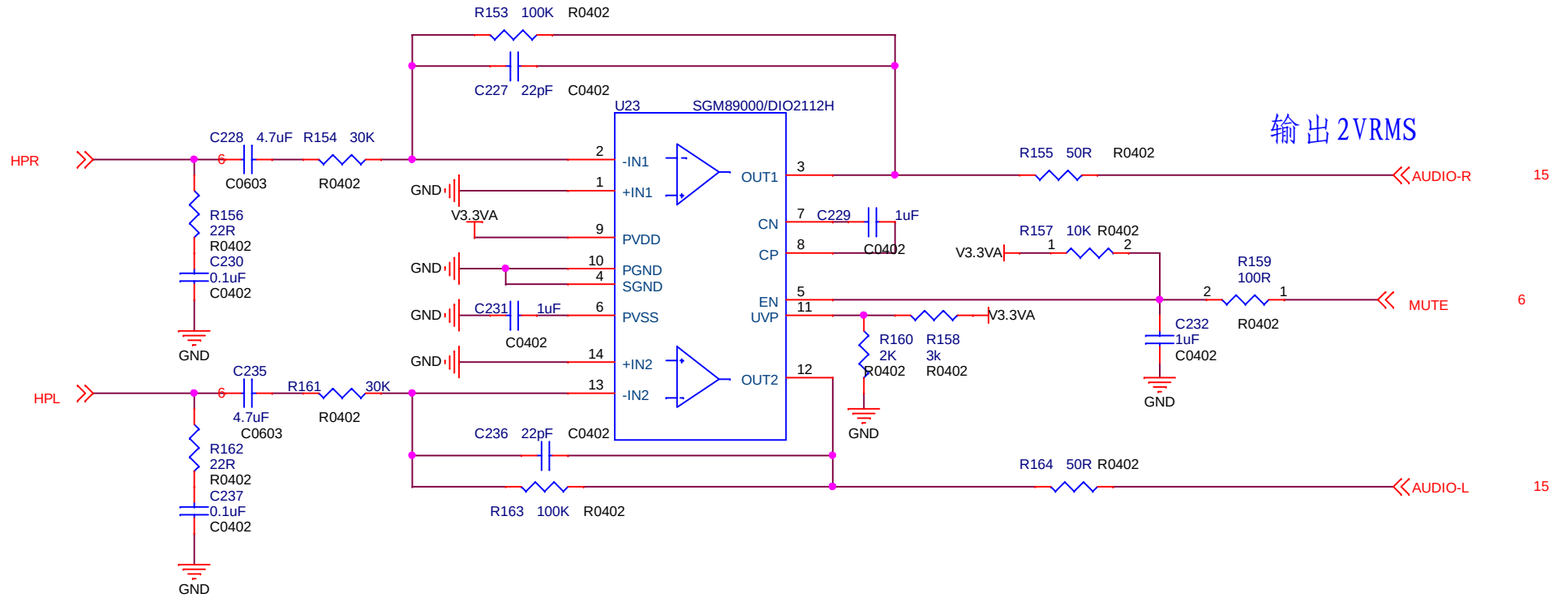
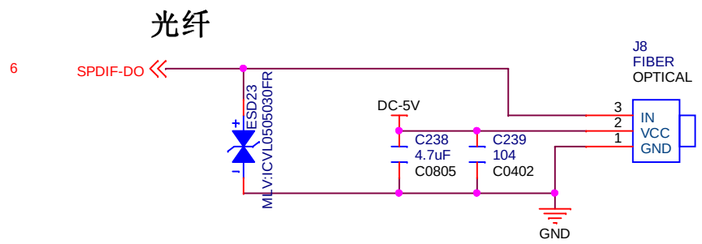
AUDIO

Analog Output

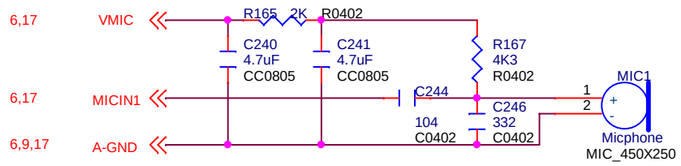


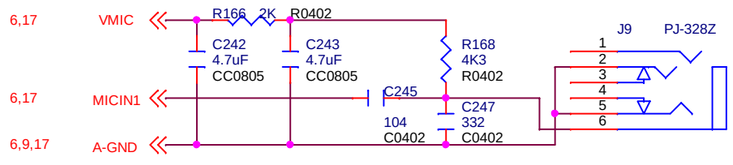


SPDIF



Microphone





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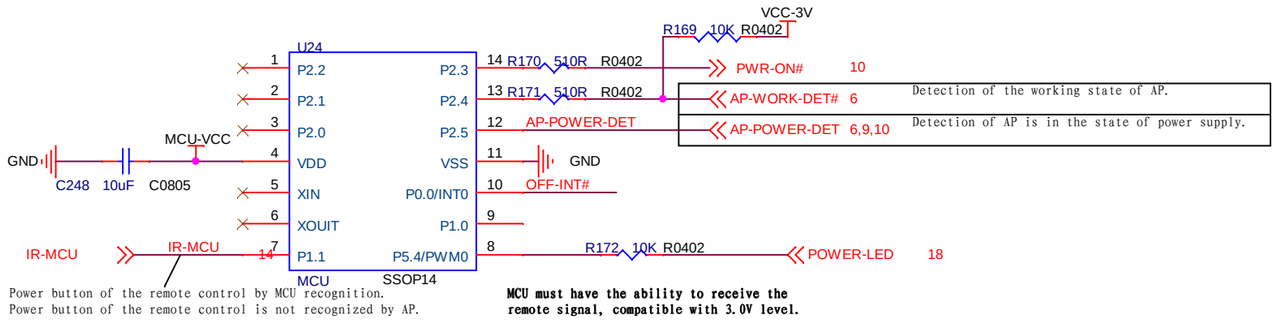
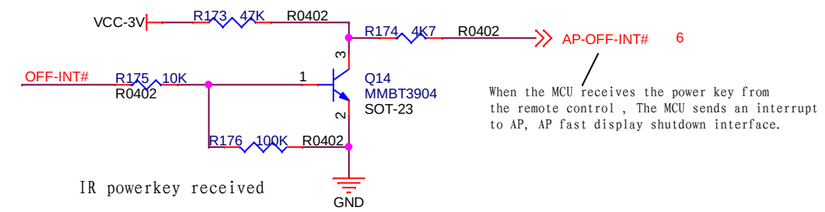
MCU-LED

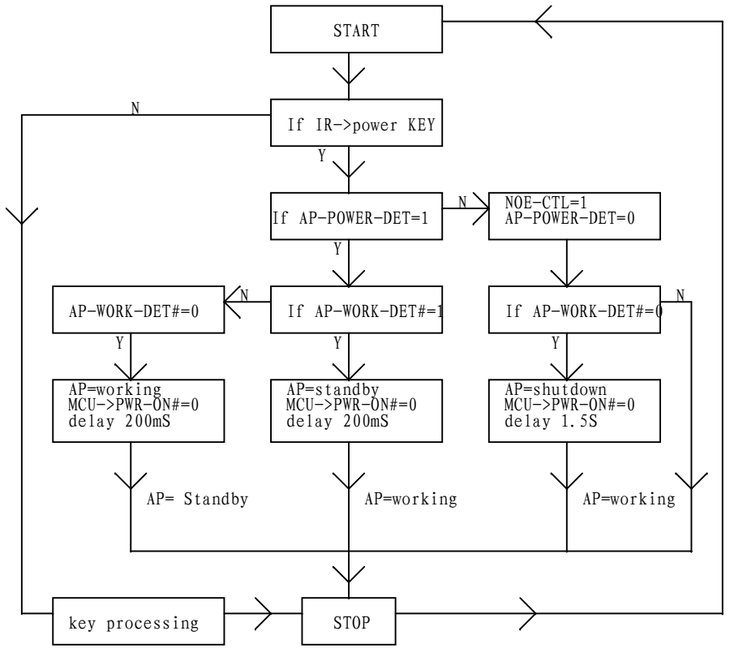
MCU

OPTION:
If we do not consider the power consumption, the MCU part can be removed!

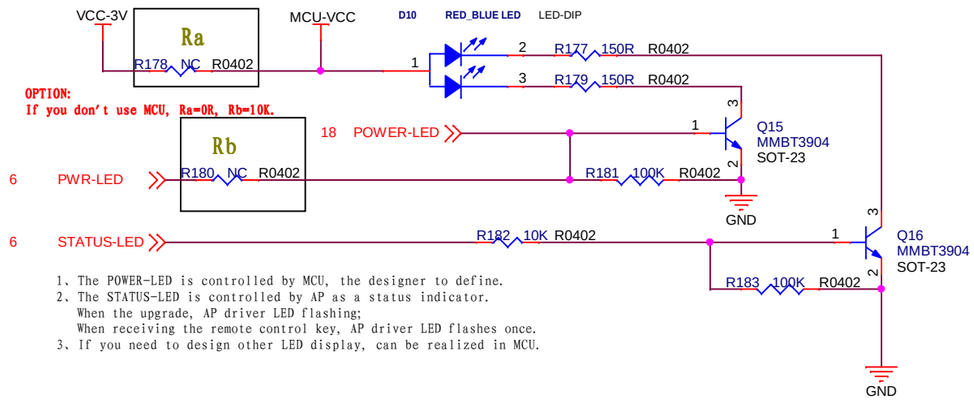




MCU programming:
Startup, shutdown, standby flow chart:



LED



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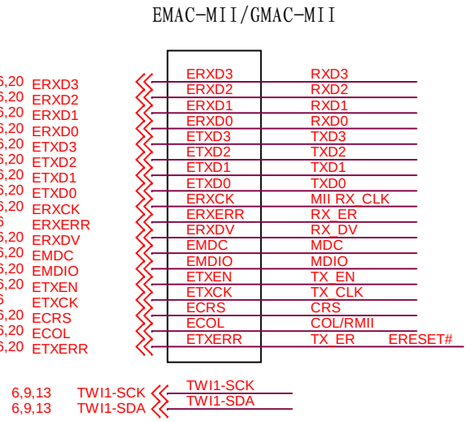
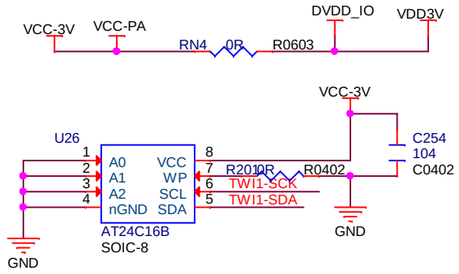
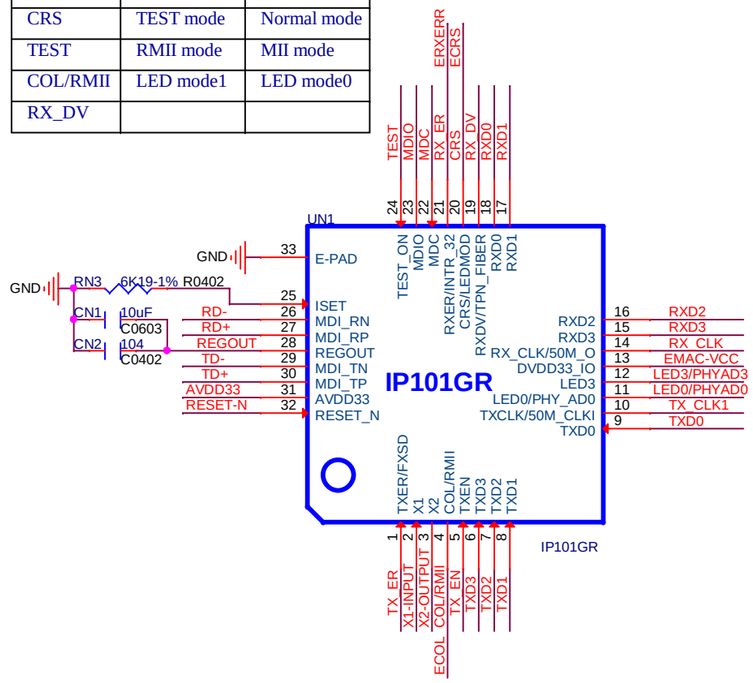
EMAC

10/100 MII Ethernet PHY

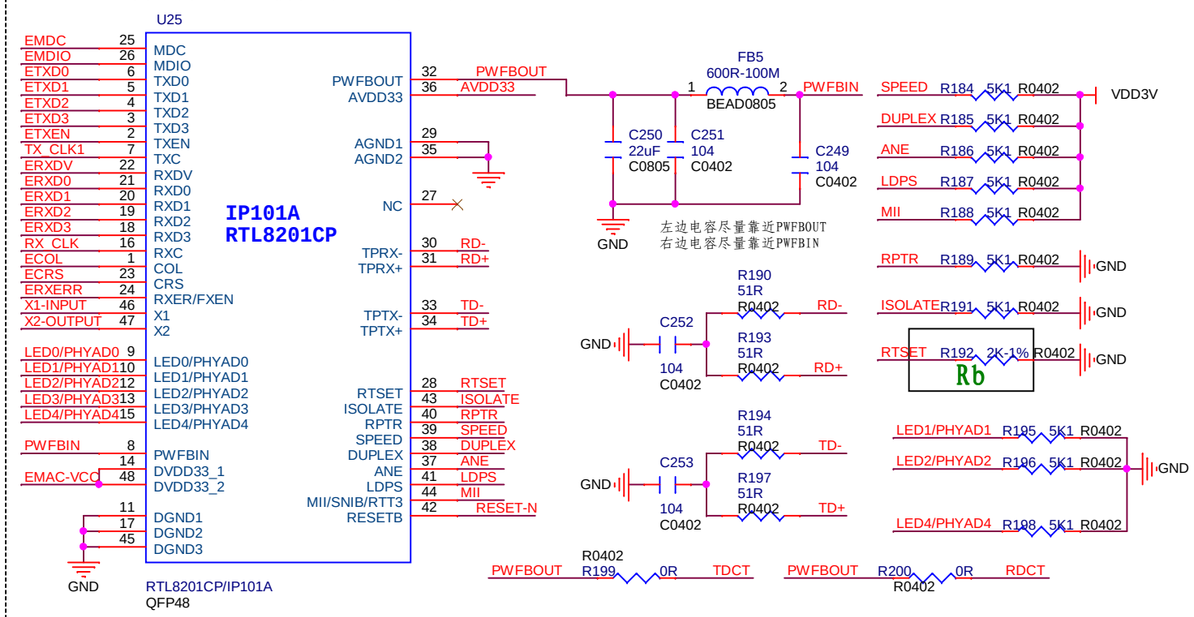


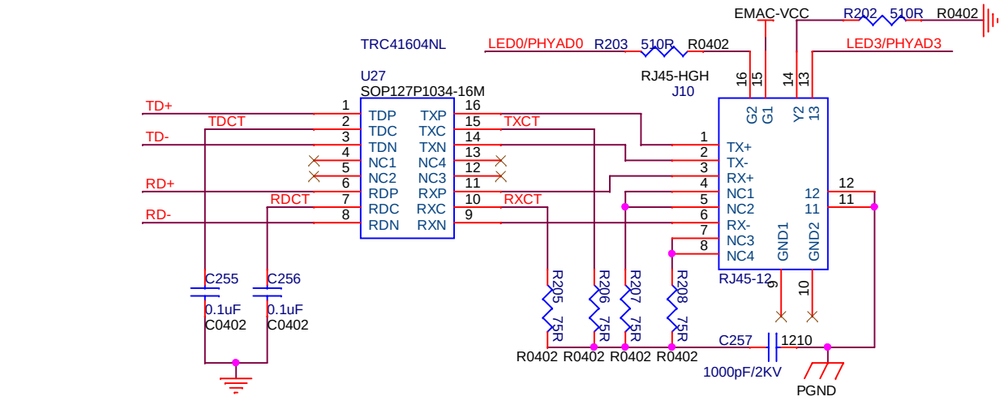


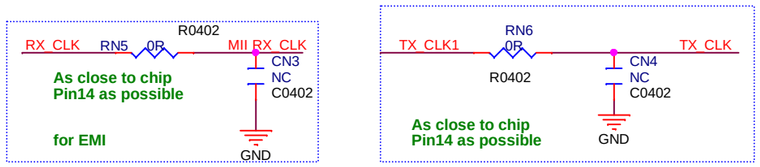
	Pull high	Pull down
CRS	TEST mode	Normal mode
TEST	RMII mode	MII mode
COL/RMII	LED mode1	LED mode0
RX_DV		

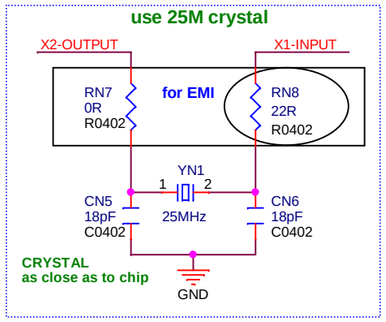


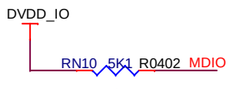
Use the GMAC-MII or EMAC-MII interface,
Please use the fast Ethernet PHY.

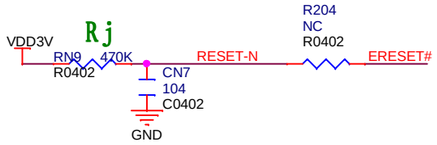


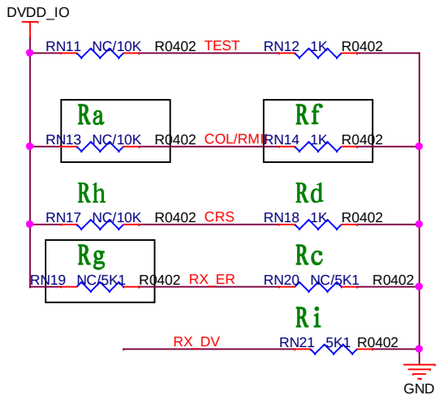


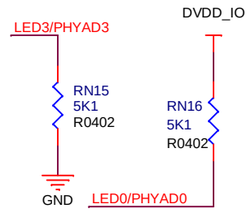


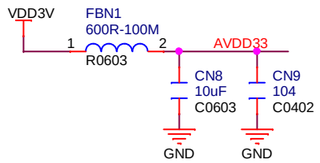


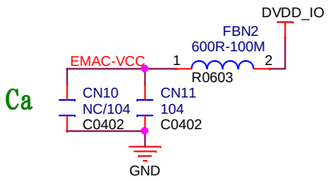












Ethernet Inteface

IP101GR:
1 the resistance Re=5k1;
2 the resistance Ra=NC;
3 the resistance Rf=1K;
4 the resistance Rc=NC;
5 the resistance Rg=NC;
6 the resistance Rd=1k;
7 the resistance Rh=NC;
8 the resistance Ri=5k1;
9 the resistance Rj=470k;
10 the resistance Ca=NC;

IP101A:
1 the resistance Ra=NC;
2 the resistance Rb=6.8K.
3 the resistance Re=2k;
4 the resistance Rf=NC;
5 the resistance Rc=5k1;
6 the resistance Rg=NC;
7 the resistance Rd=5k1;
8 the resistance Rh=NC;
9 the resistance Ri=NC;
10 the resistance Rj=5k1;
11 the resistance Ca=104;

RTL8201CP:
1 the resistance Ra=5k1;
2 the resistance Rb=2K-1%.
3 the resistance Re=2k;
4 the resistance Rf=NC;
5 the resistance Rc=5k1;
6 the resistance Rg=NC;
7 the resistance Rd=5k1;
8 the resistance Rh=NC;
9 the resistance Ri=NC;
10 the resistance Rj=5k1;
11 the resistance Ca=104;

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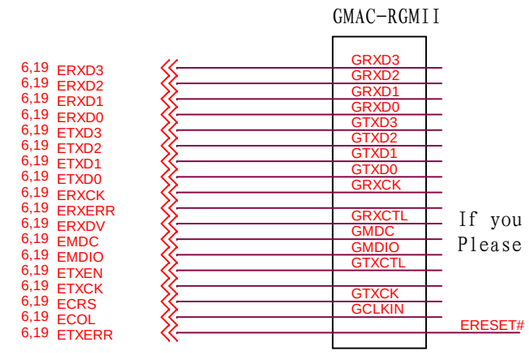
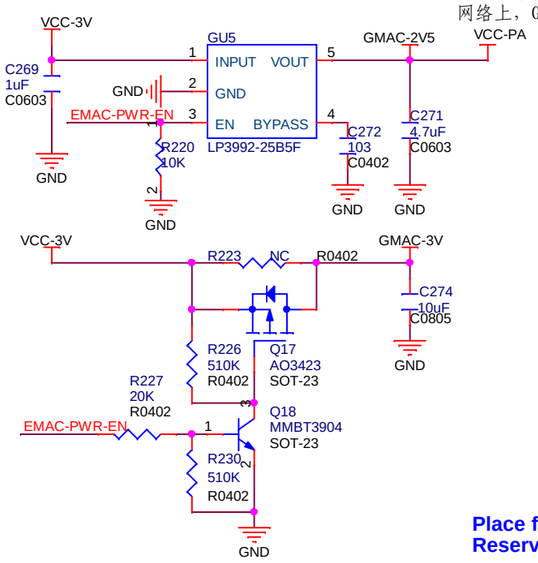
GMAC

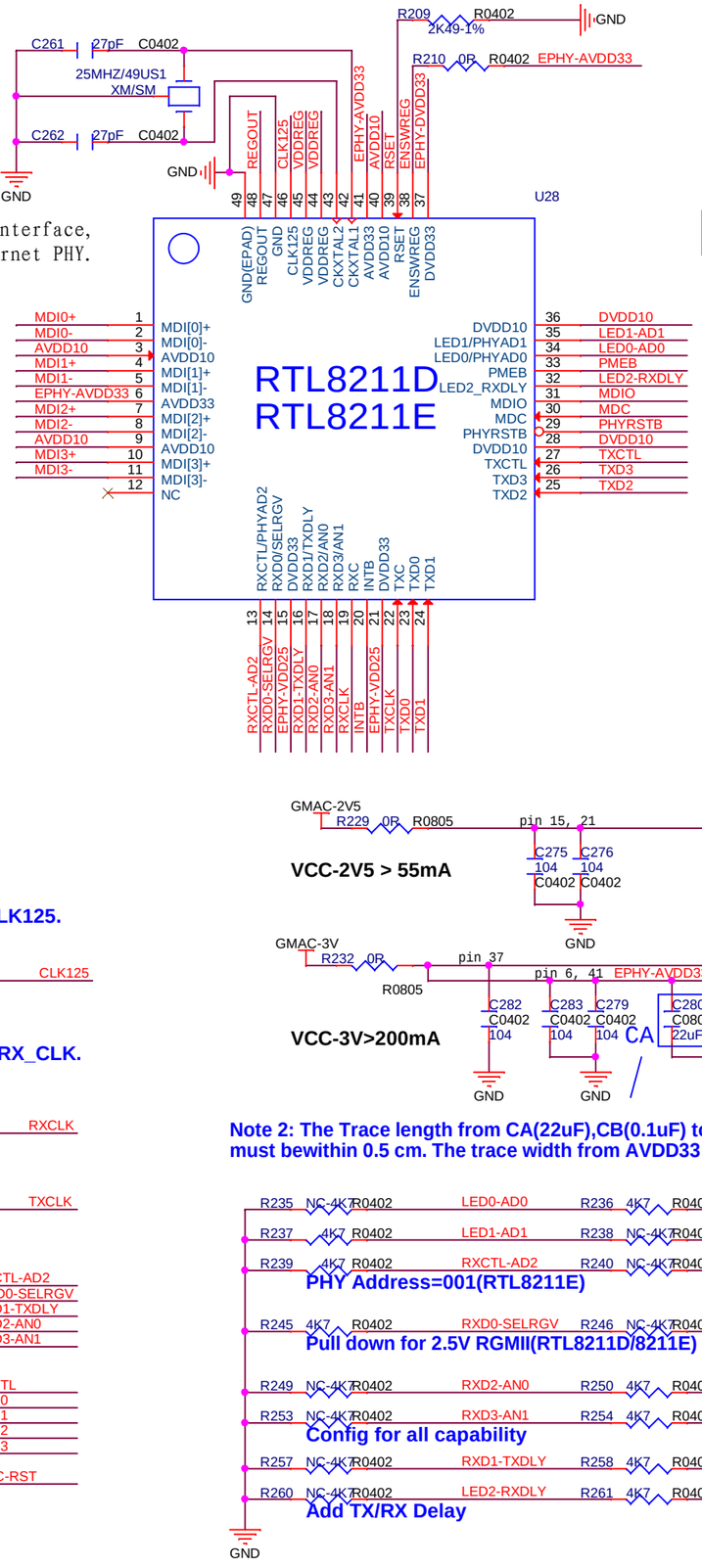
10/100/1000 RGMII Ethernet PHY



If you use the GMAC-RGMII interface,
Please use the Gigabit Ethernet PHY.

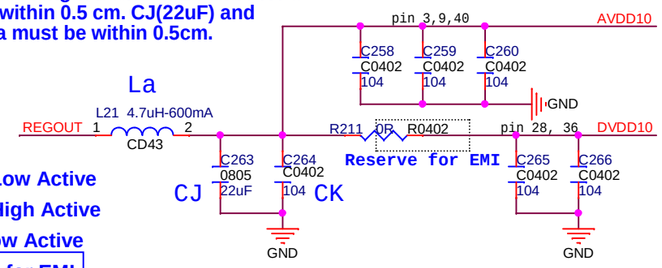


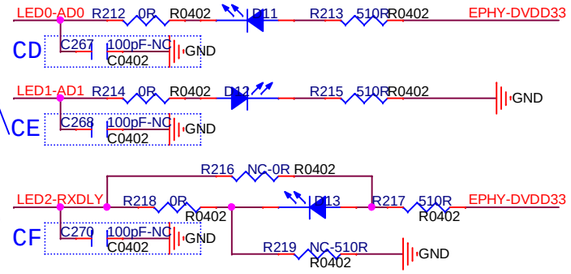
VCC-PA不能接到其它电源
网络上，GMAC供电为2.5V。

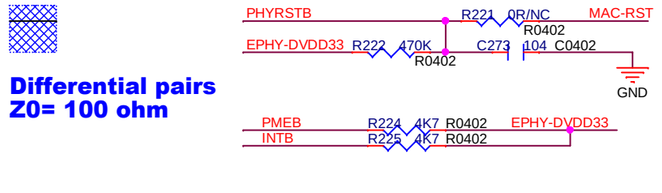


Note 1: The Trace length between La and PHY's Pin48 must be within 0.5 cm. CJ(22uF) and CK(0.1uF) to La must be within 0.5cm.

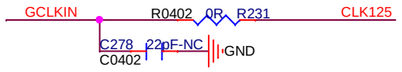
PHYAD0=1: LED0 Low Active
PHYAD1=0: LED1 High Active
RXDLY=1: LED2 Low Active
CD, CE, CF reserve for EMI.



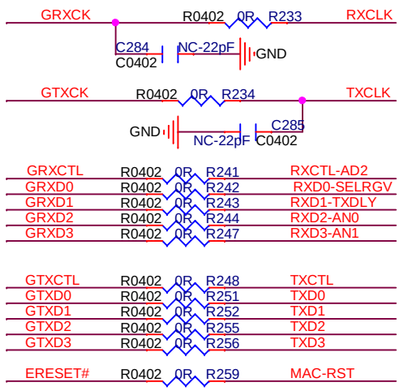




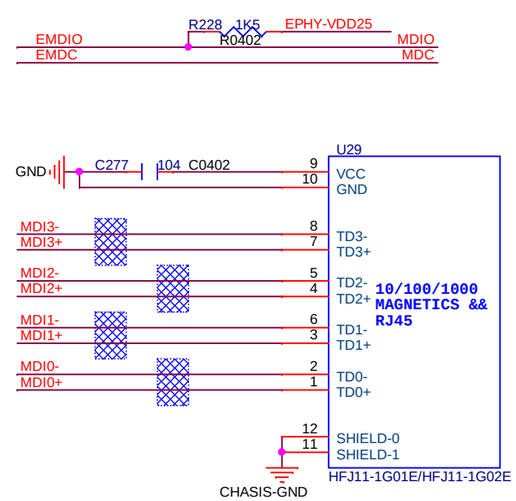
Place filter network close to CLK125. Reserved for EMI



Place filter network close to RX_CLK. Reserved for EMI



Note 2: The Trace length from CA(22uF),CB(0.1uF) to Pin 44,45(VDDREG) must bewithin 0.5 cm. The trace width from AVDD33 to Pin 44,45 should>40mils.



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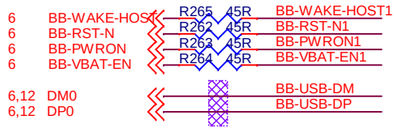
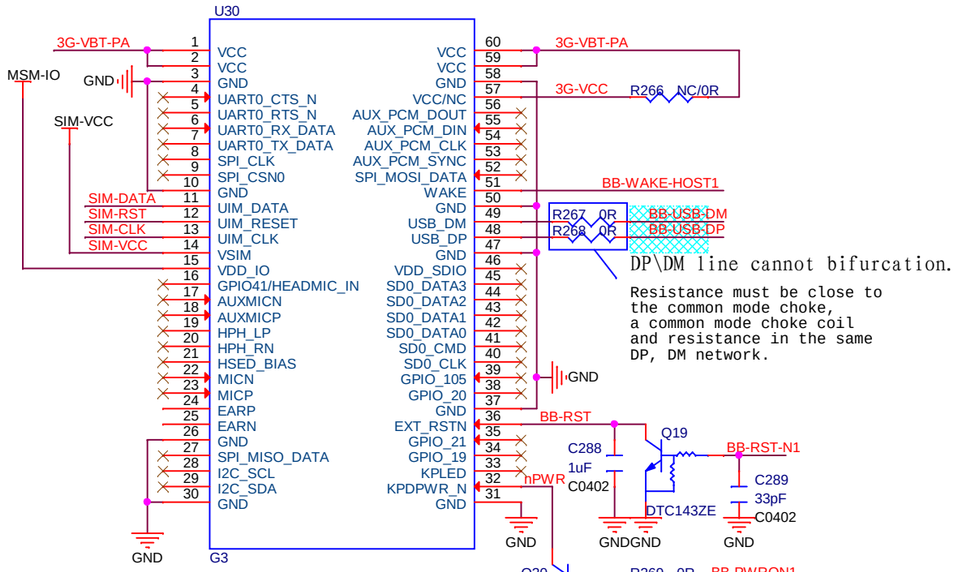
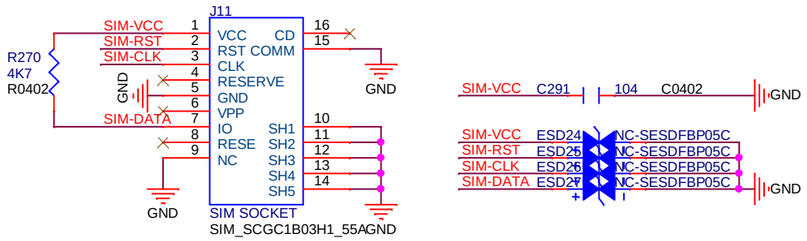
BASEBAND

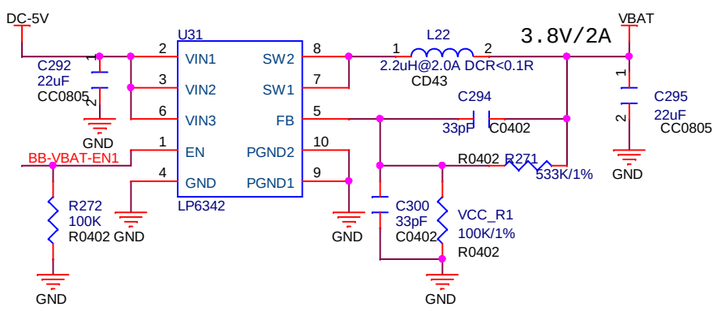


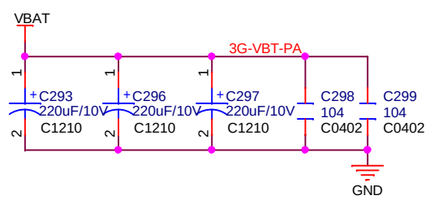


MSM-IO =2.8V



For the BBpower supply.





After AP Power-Down, VBAT-EXT still on,
IOs of BB should be still kept on the right level!!
Take Care of polarity of the Control Signals....

RF Microstrip
Z0= 50 ohm

Differential pairs
Z0= 90 ohm +/-5 ohm

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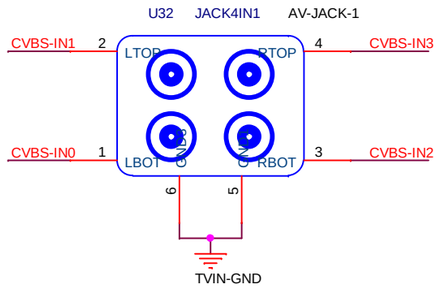
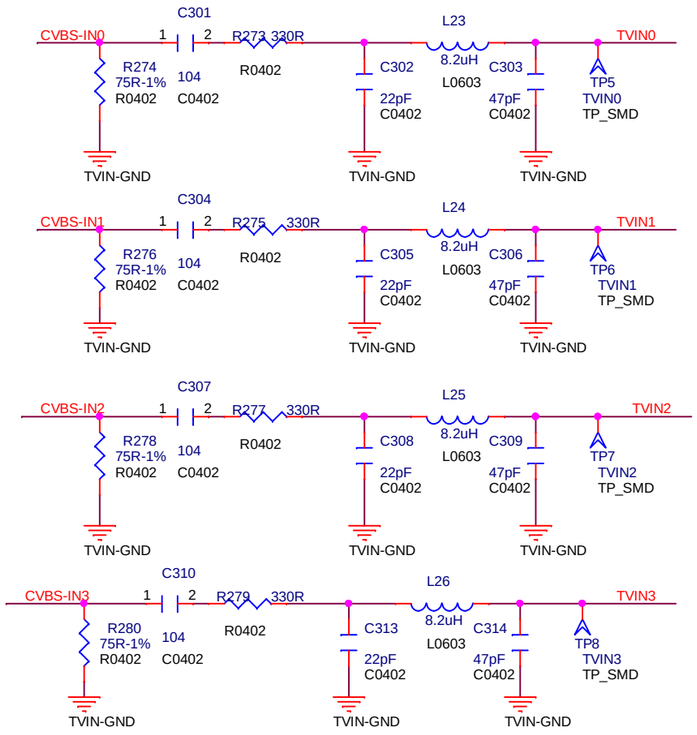
TVIN



No TVIN, resistors Ra =0R,
There is a TVIN, this circuit is deleted .



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