

RK1808

Hardware Design Guide

Rockchip Confidential

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Preface

Overview

This document mainly introduces key points and notes of hardware design for RK1808, aiming at helping customers to shorten product design period, improve stability and reduce failure rates. Please follow this guide strictly for hardware design, and use relative core boards released by RK. If you need to change for particular reasons, please strictly follow high-speed digital circuit design requirements and RK product PCB design requirements.

Chipset Model

The chipset model described in this document is: **RK1808**

Applicable to object

This document is mainly suitable for the following engineers:

- Hardware development engineers
- Field application engineers
- Test engineers

Revision history

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No.	Author	Revision Date	Revision Description	Notes
V1.0	RZF	2019.01.16	Initial Release	

Acronyms

Acronyms include abbreviations of commonly used phrases in this document.

DDR	Double Data Rate	双倍速率同步动态随机存储器
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I ² C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议 (IEEE 1149.1兼容)
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
PCIE	Peripheral Component Interconnect Express	高速串行扩展总线
MAC	Media Access Control	以太网媒体接入控制器
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
RK	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output	安全数字输入输出
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SPI	Serial Peripheral Interface	串行外设接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
USB	Universal Serial Bus	通用串行总线

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Chapter 1. System Overview

1.1 Overview

RK1808 is a high-performance, low-power processor with dual-core Cortex-A35 and a hardware neural network processing unit integrated. Its flexibility and compatibility make it one of the mainstream solutions for smart IoT devices.

RK1808 has a variety of powerful embedded hardware engines that provide superior performance for advanced applications, embedding a powerful neural network processing unit (NPU); supporting full-format H.264 1080p@60fps decoding and H.264 1080p@30fps encoding and high quality JPEG encoder/decoder.

RK1808 features a high-performance memory interface (DDR3/DDR3L/LPDDR3) that provides high memory bandwidth.

RK1808 chip operating temperature: 0-80 °C; RK1808K (wide temperature) chip operating temperature: -20-85 °C.

1.2 Block Diagram

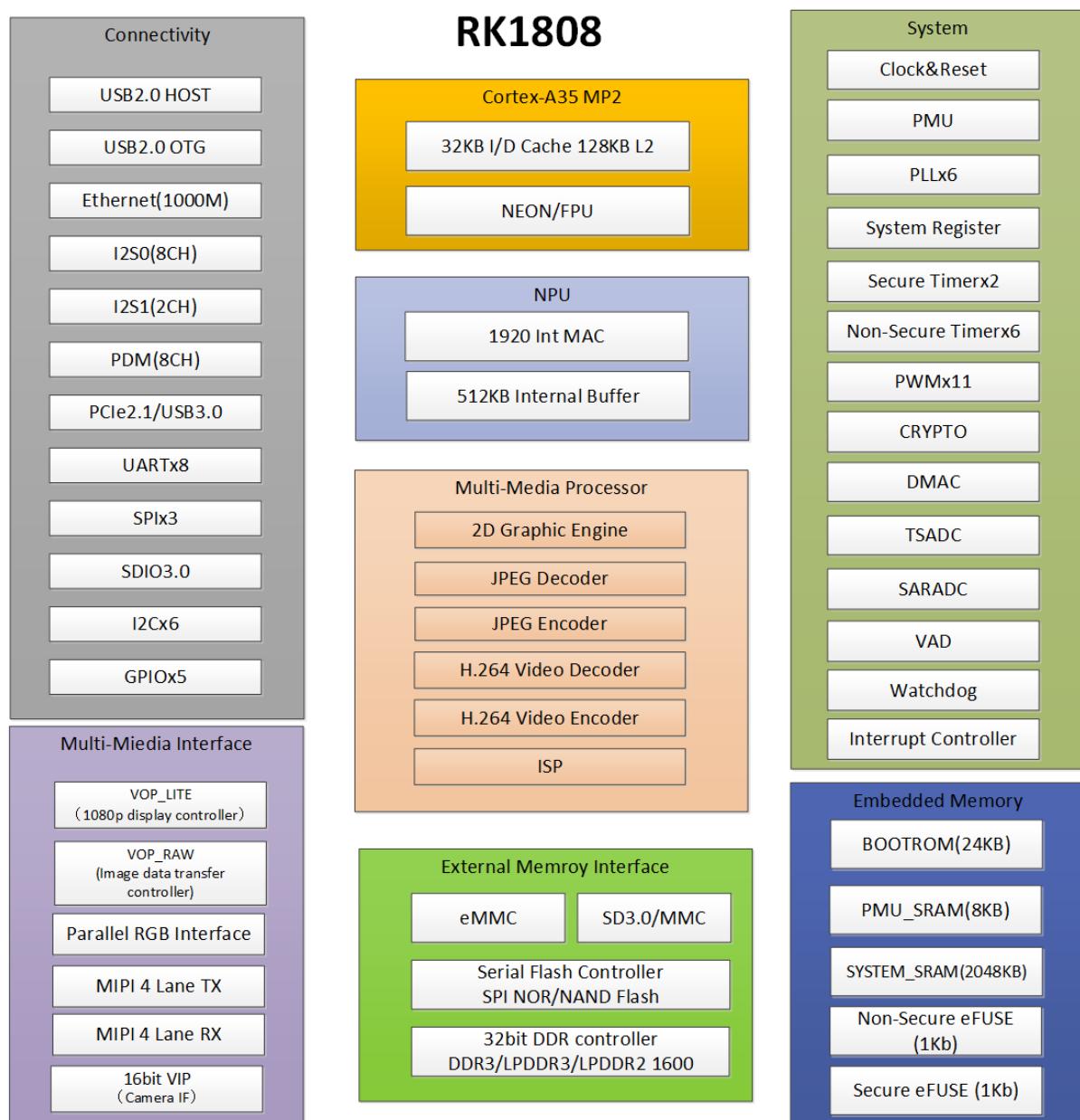


Figure 1-1 RK1808 Block Diagram

1.3 Application Block Diagram

1.3.1 RK1808 Single chip application block diagram

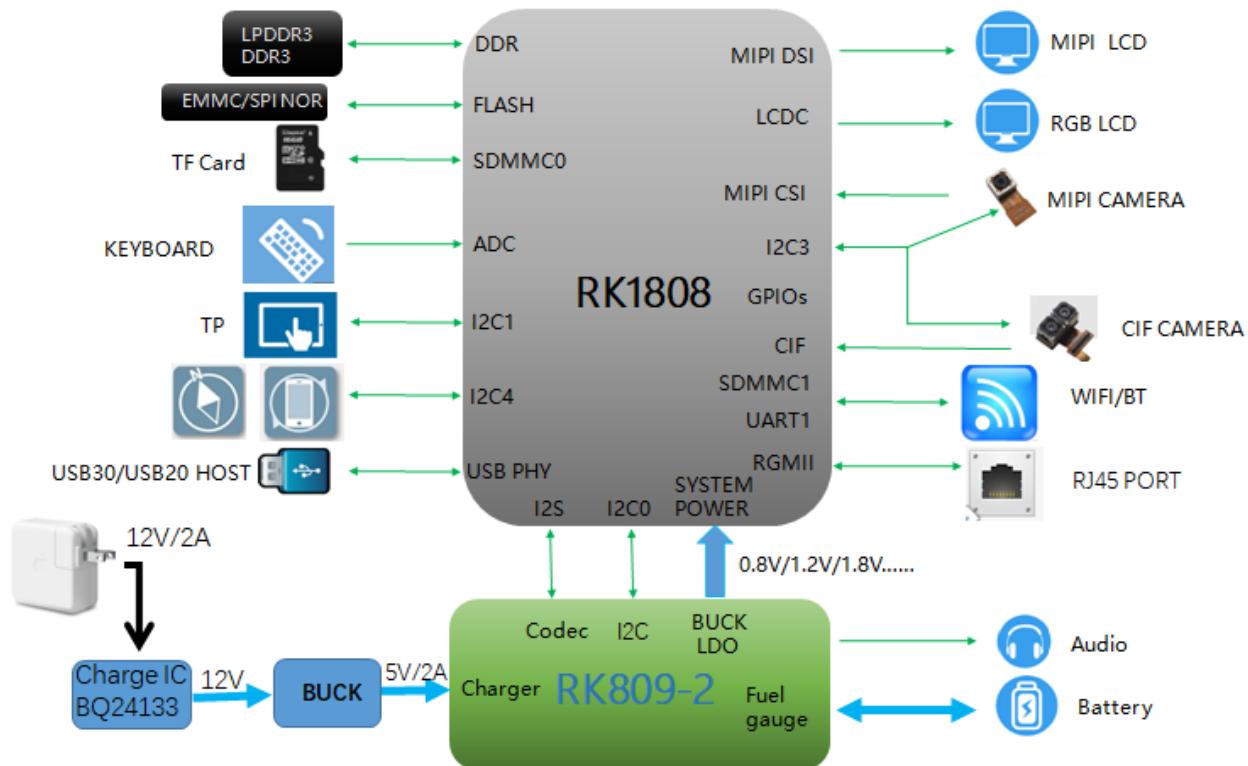


Figure 1-2 RK1808 single chip application block diagram

1.3.2 RK1808 EDGE COMPUTING application block diagram

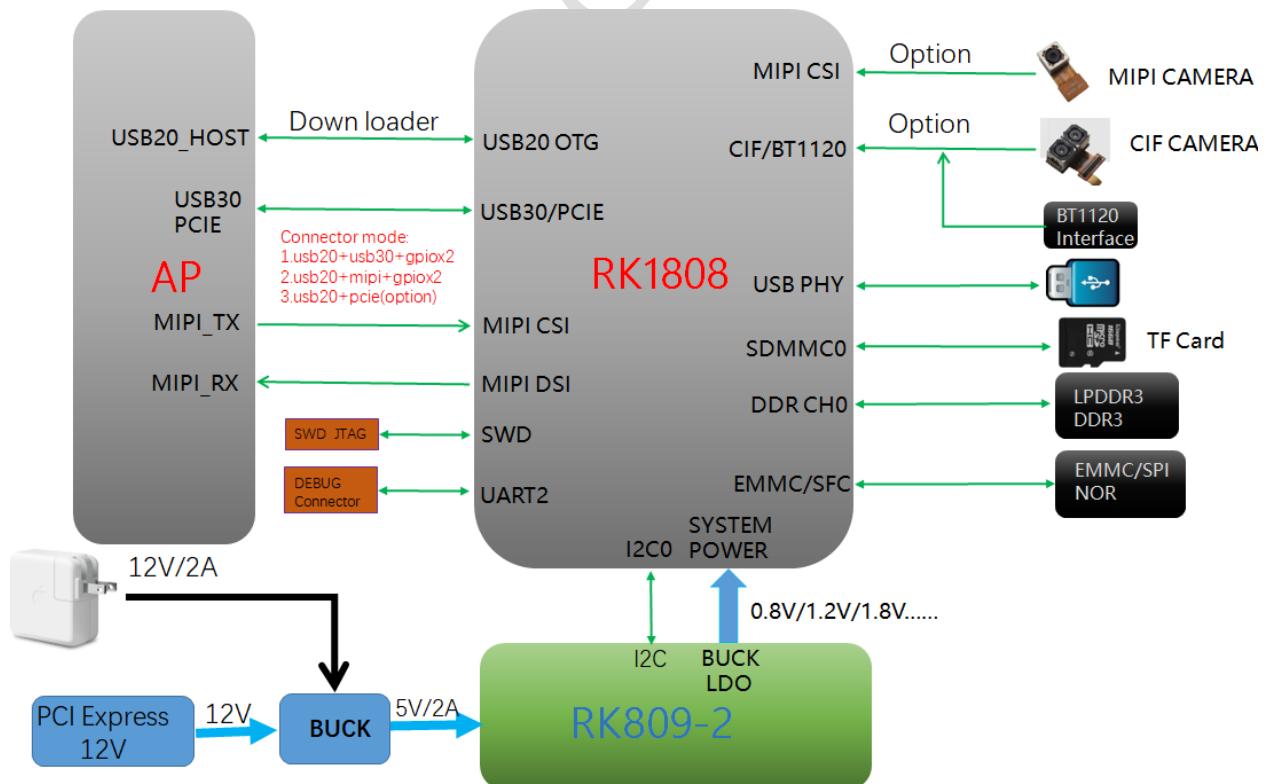


Figure 1-3 RK1808 edge computing application block diagram

Above are application block diagrams of RK1808, please refer to the reference design schematic released by RK.

Chapter 2. Schematic Design Recommendations

2.1 Minimum system design

2.1.1 Clock circuit

24M clock of RK1808 chip is provided in two ways. One is provided by 24M crystal oscillator, and the other 24M is provided from the OSC_24M_IN pin input of external clock source. These two clock inputs are configured by the pin OSC_BPASS (Pin AV24). When OSC_BPASS= 0, it is provided by 24M crystal oscillator, when OSC_BPASS=1, 24M clock is provided by external clock source input from OSC_24M_IN pin. As shown in Figure 2-1.

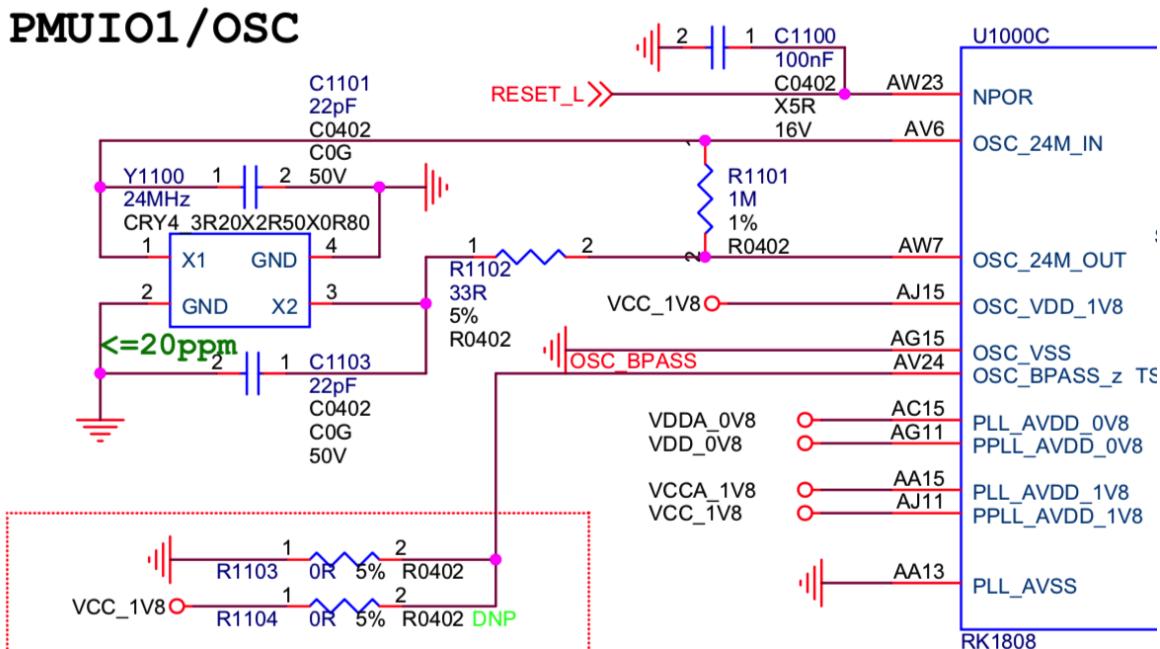


Figure 2-1 RK1808 Crystal connection method and device parameters



Note

The values of capacitors C1101 and C1103 need to be selected according to actual nominal load capacitance value of the crystal. 22pF is the capacitance value chosen by RK, not the common value.

24M clock parameters are shown in Table 2-1 below:

Table 2-1 RK1808 24MHz clock requirements

Parameter	Specification			Description
	Minimum	Maximum	Unit	
Frequency	24.000000		MHz	
Frequency deviation	+/-20		ppm	Frequency tolerance
Operating temperature	-20	70	°C	
ESR	/	40	Ohm	

When RK1808 chip is on standby mode, it will switch from 24M clock source to 32.768KHz clock of external input or 32.768K clock of the chip's internal PVTM output, by reducing system clock frequency to reduce system power consumption, the external 32.768K signal can be obtained from PMIC or external RTC clock source, as shown in Figure 2-2.

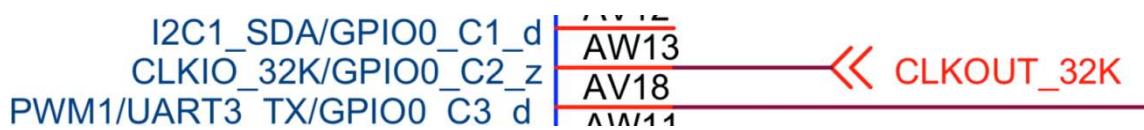


Figure 2-2 RK1808 Standby clock input

The external 32.768 kHz RTC clock parameters are shown in Table 2-2.

Table 2-2 RK1808 32.768KHz clock requirement

Parameter	Specification			Description
	Minimum	Maximum	Unit	
Frequency	32.768000		MHz	
Frequency deviation	+/-30		ppm	Frequency Tolerance
Operating temperature	-20	70	°C	
Duty cycle	45-55		%	

2.1.2 Reset circuit

RK1808 internally integrates a power-on reset circuit, POR (Power on Reset) for short, which is effective for low level, capacitor C1100 is used to eliminate jitter, please place it close to the NPOR pin of RK1808. The shortest reset time to ensure the chipset working stably and normally is 100 cycles 24MHz main clock period, that is 4us at least.

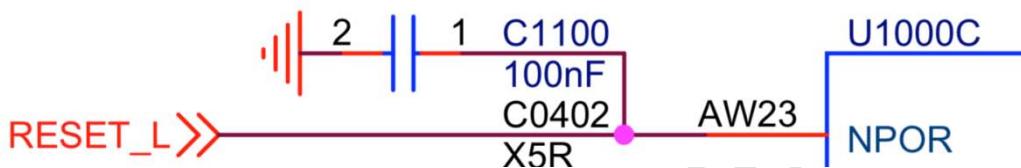


Figure 2-3 RK1808 reset input

2.1.3 System boot sequence

System boot sequence priority of RK1808 from high to low is as follow:

- SPI2APB interface(or named SPI0)
- eMMC interface
- SFC interface
- SDMMC interface
- USB OTG interface

2.1.4 System initialization configuration signal

There are two important signals in RK1808, which need to be configured before power-on. They are OSC_BPASS (clock source selection) and UART/JTAG/SDMMC reuse functions control pins.

The 24M clock source of RK1808 needs to be configured by OSC_BPASS pin. Table 2-3 lists the configuration.

RK1808 reuse JTAG\UART functions with SDMMC function to reduce IO pullout, you need to switch output mode through the pin. The configuration is shown in Table 2-3.

Table 2-3 RK1808 System initialization configuration signal description

Signal Name	Internal Pull up/down	Description
OSC_BPASS	High impedance	Clock source selection: 0: 24M crystal; (default) 1: External 24M clock is provided; (When RK1808 is used as a slave device, it is recommended to use this method)
SDMMCO_DET	pull up	JTAG pin reuse selection control signal: 0: Identified as SD card insertion, SDMMC/JATG/UART pin is reused as SDMMC output; 1: Identified as SD card no insertion, SDMMC/JATG/UART pin is reused as JTAG/UART output (default);

2.1.5 JTAG Debug circuit

JTAG interface of RK1808 is IEEE1149.1 standard. PC can connect DSTREAM simulator through SWD mode (two-wire mode) and debug ARM Core inside the chip.

Before connecting the emulator, you need to ensure that SDMMC0_DET pin is at a high level, otherwise you cannot enter JTAG debug mode. Interface description is shown as table 2-4:

Table 2-4 RK1808 JTAG Debug interface signal

Signal Name	Description
JTAG_TCK	AP JTAG clock input
JTAG_TMS	AP JTAG mode selection input

2.1.6 DDR circuit

- **2.1.6.1 DDR controller introduction**

RK1808 DDR controller interface supports JEDEC SDRAM standard, the controller has following features:

- Support DDR3-1600/DDR3L-1600/LPDDR3-1600 standard;
- Provide one 32 bit DDR controller interface, support data bus bitwidth 32bit/16bit configurable, address bus support up to 18bit max.
- Support DDR 2GB max.
- Support power down, self refresh etc. low power consumption mode;

- **2.1.6.2 DDR topology structure and connection method**

RK1808 SDRAM topology structure is shown as figure 2-5, taking LPDDR3 as an example:

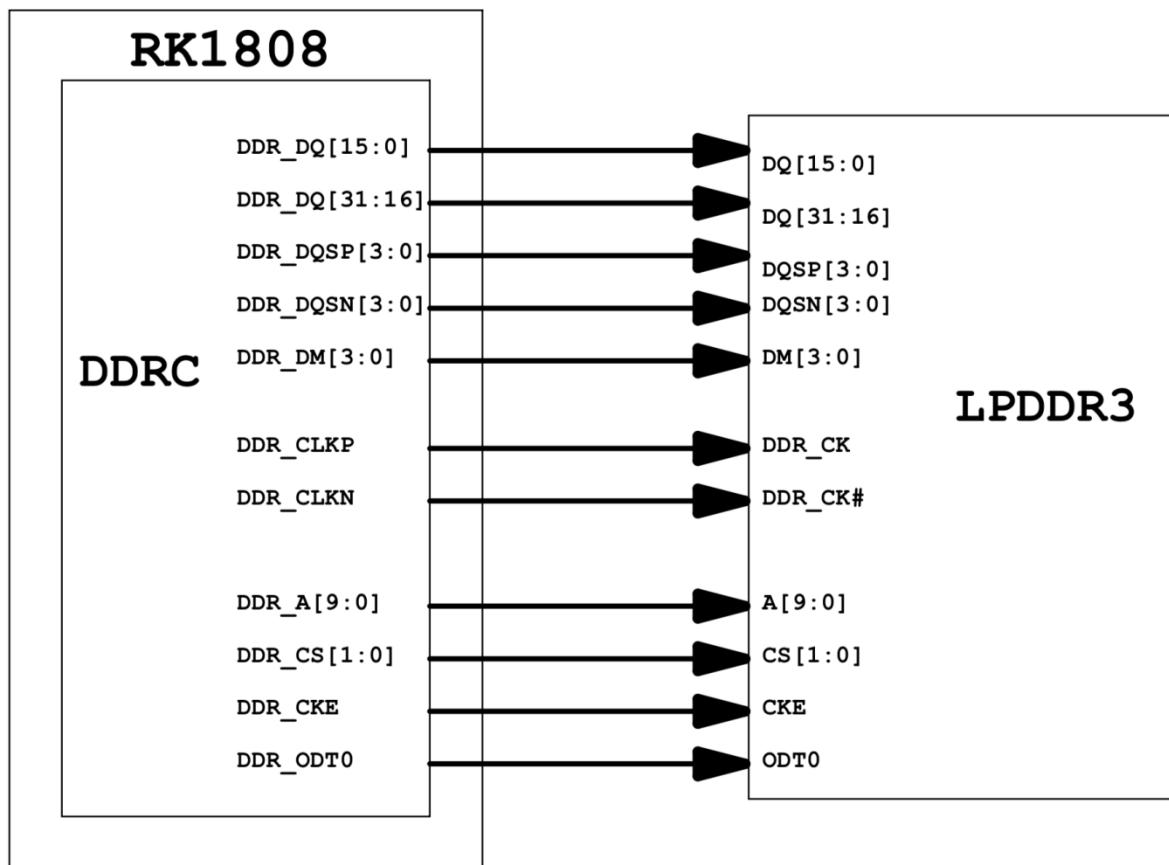


Figure 2-4 RK1808 LPDDR3 topology structure figure

- **2.1.6.3 DDR power up sequence requirement**

RK1808 DDR controller includes only one set of power supplies:

- DDRIO_VDD: Core power supply for DDR controller, I/O interfaces power supply,

and buffer power supply;
 DRAM includes two sets of power. For power-on sequence, please refer to JEDEC standard. For example, power-on sequence of LPDDR3 DRAM is shown in the following figure:

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2} —200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA} —200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ} —200mV
	V_{Ref} must always be less than all other supply voltages

Figure 2-5 LPDDR3 DRAM power up sequence

- **2.1.6.4 DDR support list**

RK1808 DDR supports DDR3/LPDDR3 interface, the max working frequency up to 800MHz. Please refer to "RK DDR Support List" for details.

2.1.7 eMMC circuit

- **2.1.7.1 eMMC controller introduction**

RK1808 eMMC interface supports eMMC 4.51 and is compatible with 4.41. The controller has the following features:

- Support SFC FLASH, eMMC FLASH, does not support parallel nand FLASH;
- Supports 1-bit, 4-bit and 8-bit three kinds of data bus width;
- The maximum transmission rate reaches 150MB/s;

- **2.1.7.2 eMMC topology structure and connection method**

Pulling up or down and matching design recommendations of eMMC interface as shown in Table 2-5..

Table 2-5 RK1808 eMMC interface signal design

Signal	Internal Pull up/down	Connection Method	Description(chip side)
eMMC_DQ[7:0]	pull up	direct connection	eMMC data send/receive
eMMC_CLK	pull up	in series with 22ohm resistor	eMMC clock send
eMMC_CMD	pull up	In series with 22ohm resistor	eMMC command send/receive

- **2.1.7.3 eMMC power up sequence requirement**

RK1808 eMMC controller only includes one set of power:

- VCCIO0: I/O power supply for eMMC controller;

There are two sets of power supply for eMMC. Please refer to JEDEC standard for power-on sequence:

- VCC and VCCQ have no power up sequence requirement.
- VCC and VCCQ must be powered up and keep stable working voltage before RK1808 sending out CMD command;
- After the component enters sleep mode, RK1808 can cut off VCC power to lower power consumption
- Before the component is waken up from sleep mode, VCC power must be on and keep stable working voltage;

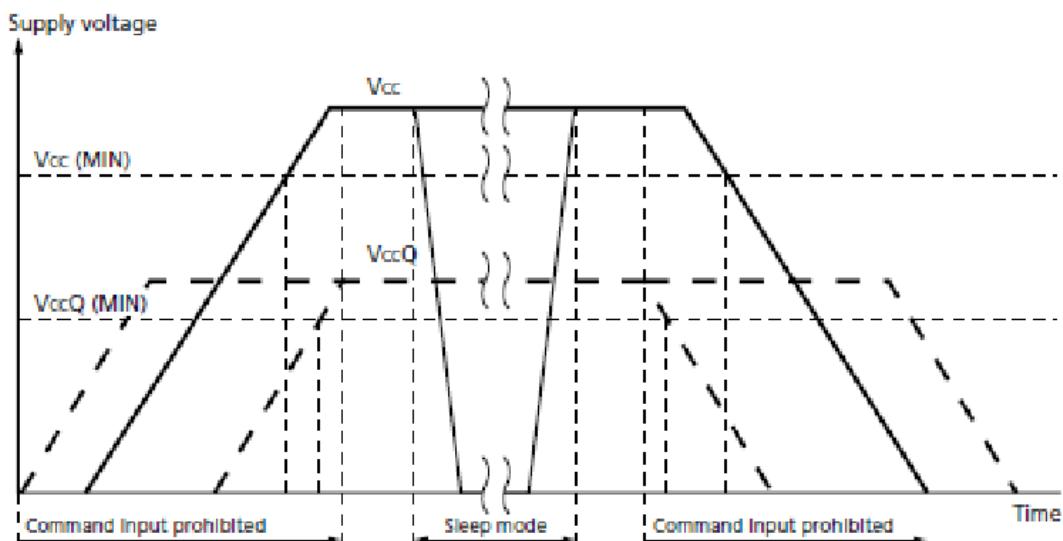


Figure 2-6 eMMC component power up/down sequence

- **2.1.7.4 eMMC support list**

Please refer to "RK eMMCSupportList" for RK1808 eMMC interface support list.

2.1.8 SPI circuit

- **2.1.8.1 SPI controller introduction**

There are three SPI controllers SPI0 (1CS), SPI1 (2CS) and SPI2 (1CS) in RK1808 chip, which can be used to connect to SPI devices. SPI0 is embedded in APB master interface, only supports slave mode, and is used for booting; SPI1 and SPI2 support both master and slave modes.

- **2.1.8.2 SPI0 topological structure and connection method**

Pulling up or down and matching design recommendations of SPI0 interface are shown in Table 2-6.

Table 2-6 RK1808 SPI0 interface signal

Signal	Internal Pull up/down	Connection Method	Description(chipset)
SPI0_MOSI	pull up	direct connection	SPI0 data reception
SPI0_MISO	pull up	direct connection	SPI0 data sending
SPI0_CLK	pull down	In series with 22ohm resistor	SPI0 clock input
SPI0_CS	pull up	direct connection	SPI0 chip select signal

- **2.1.8.3 SPI0 power up sequence requirement**

SPI0 controller power up requirement complies with power-up sequence requirements of GPIO power domain.

SPI0 has only one power supply, so there is no requirement for power-up sequence.

Power pin of SPI0 (VCCIO5): Power is required at all times (with or without SPI0).

When system boot up, SPI0 CS must be pulled up and cannot be pulled down. Otherwise, the system cannot boot normally.

2.1.9 GPIO circuit

For RK1808, GPIO type is 1.8V only or 1.8V/3.3V two configurable modes, only need to power supply 1.8V or 3.3V in the side of hardware, the voltage supplied by IO is automatically

detected in the chip, and corresponding registers are configured without software.

- **2.1.9.1 GPIO drive capability**

In RK1808, GPIO provides adjustable 4 levels of drive strengths, which are 2mA/4mA/8mA/12mA respectively. Depending on the type of GPIO, the initial default drive strength is also different. Please refer to chip TRM for configuration and modification.

- **2.1.9.2 GPIO power**

Power pins of GPIO power domain is described below:

Table 2-7 RK1808 GPIO power pins description

Power Domain	GPIO Type	Pin Name	Description
PMUIO1	1.8V only	PMU_VDD_0V8	0.8V logic power for this GPIO domain (group).
		PMUIO1_VDD_1V8	1.8V IO supply for this GPIO domain (group).
PMUIO2	1.8V/3.3V	PMUIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO0	1.8V/3.3V	VCCIO0	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO1	1.8V/3.3V	VCCIO1	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V/3.3V	VCCIO3	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO7	1.8V/3.3V	VCCIO7	1.8V or 3.3V IO supply for this GPIO domain (group).

2.2 Power design

2.2.1 Minimal system power introduction

- **2.2.1.1 Power requirement**

- PLL: PLL_AVDD_0V8、PLL_AVDD_1V8、PPLL_AVDD_0V8、PPLL_AVDD_1V8
- OSC: OSC_VDD
- CPU: CPU_VDD
- LOGIC: LOG_VDD
- NPU: NPU_VDD
- DDR: DDR_VDD
- GPIO: PMU_VDD_0V8、PMUIO1_VDD、PMUIO2_VDD、VCCIO0、VCCIO5

- **2.2.1.2 Power up sequence**

Theoretically comply with this rule: for the same module, power up from low voltage to high voltage, and the same module and same voltage power up at the same time. There is no power up requirement among different modules.

Reference power up sequence is recommended as below:

LL_AVDD_0V8&PPLL_AVDD_0V8&PMU_VDD_0V8&LOG_VDD&CPU_VDD->OSC_VDD&
DDR_VDD &PLL_AVDD_1V8&PPLL_AVDD_1V8&PMUIO1_VDD_1V8
&VCCIO0->PMUIO2->NPU_VDD

For more detailed power-up sequence, see "power diagram and sequence" page of RK1808 reference diagram.

(Note: The above power names are all named by the chip pins)

2.2.2 Power design suggestions

- **2.2.2.1 Standby circuit solution**

RK1808 board-level system adopts a standby solution, which is divided into a normal power supply area and a standby power-down area. The two parts are independently

powered, as shown in Figure 2-7.

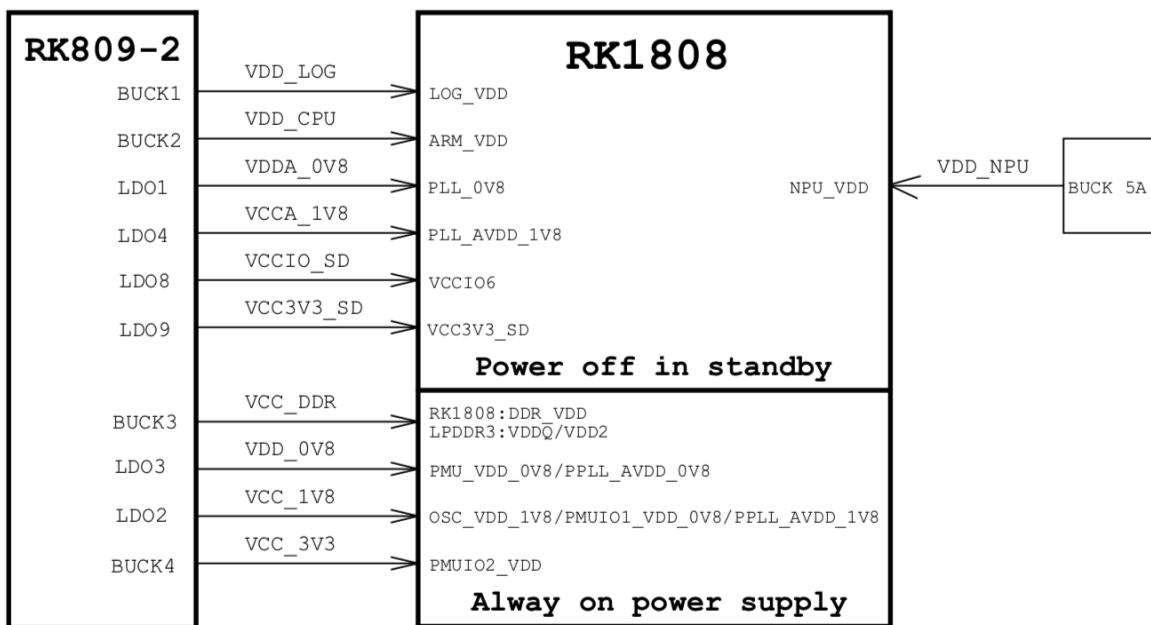


Figure 2-7 RK1808 standby circuit solution

Standby power off and constantly power supply areas are directly powered by RK809-2 (except NPU) and control each power supply to be turned off independently. Need to keep below four sets of power on at least in standby mode:

- VCC_DDR: Power for DDR self-refresh;
- VDD_0V8: Power for PMUIO & PPLL_AVDD and IO power for PMU output status and interrupt response.
- VCC_1V8: Power for PMUIO1 & PPLL_AVDD &OSC_VDD, and supply power for PMU, PPLL and OSC working.
- VCC_3V3: Power for PMUIO2 power domain

● 2.2.2.2 PLL power

There are 6 PLLs inside RK1808 chip, they are allocated as below:

Table 2-8 RK1808 internal PLL introduction

	Quantity	Power	Standby Status
PMU	1	PPLL_AVDD_0V8/PPLL_AVDD_1V8	Do not power off
Modules inside the chip	5	PLL_AVDD_0V8/PLL_AVDD_1V8	Can be powered off

It is recommended to use LDO to supply power to PLL separately. Especially for because PCIE/DDR operating frequency is high, stable PLL power supply is helpful to improve the operating stability at high frequencies, and decoupling capacitors should be placed close to the pins.

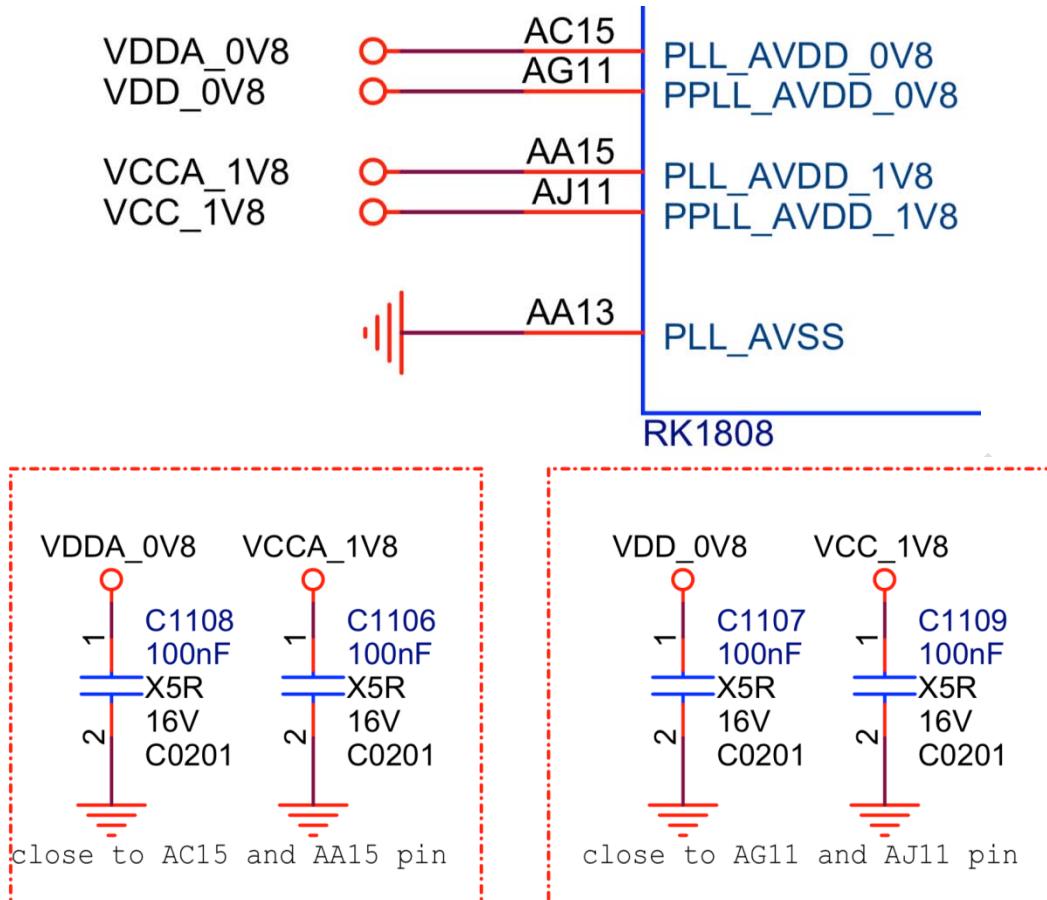


Figure 2-8 RK1808 chip PLL power

- **2.2.2.3 CPU power**

RK1808 uses independent power domain to supply power for CPU. VDD_CPU supply power for ARM Cortex-A53 core shown as below figure, support DVFS dynamic voltage and frequency scaling function, use BUCK2 of RK809-2 to supply power, the peak current can reach up to 850mA, so please do not delete or reduce capacitors in RK1808 reference design schematic. For layout, put big capacitors in the back side of RK1808 chip (or put it close to the chip if only one side) to ensure the power ripple within 60mV in case the power ripple becomes too big with heavy load. Capacitors are shown as figure 2-10.

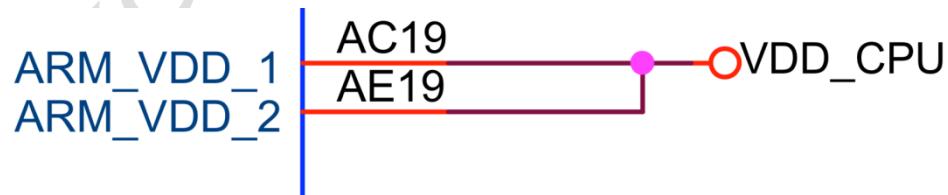


Figure 2-9 RK1808 chip VDD_CPU power

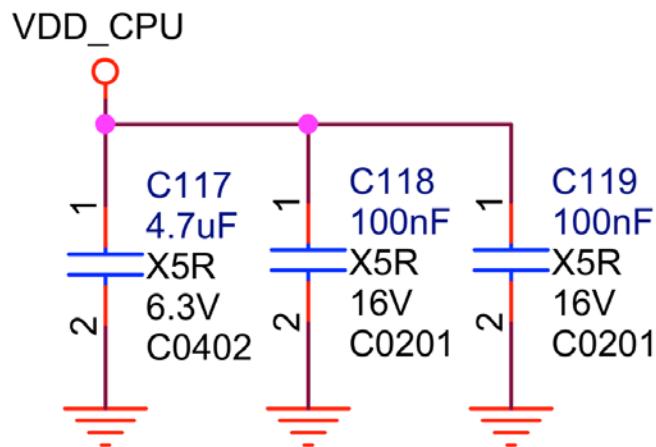


Figure 2-10 Decoupling of RK1808 chip VDD_CPU Power Supply

- 2.2.2.4 LOGIC power

RK1808 LOGIC power uses BUCK1 of RK809-2 to supply power, as shown in the figure below, VDD_LOG supports DVFS dynamic voltage and frequency scaling function, peak current up to 1A, so please do not delete or reduce capacitors in RK1808 reference design schematic. For layout, put big capacitors in the back side of RK1808 chip (or put it close to the chip if only one side) to ensure the power ripple within 50mV in case the power ripple becomes too big with heavy load. Capacitors are shown as picture 2-12.

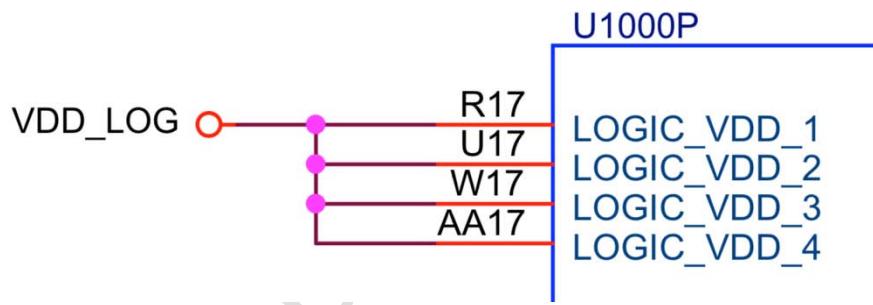


Figure 2-11 RK1808 chip VDD_LOG power

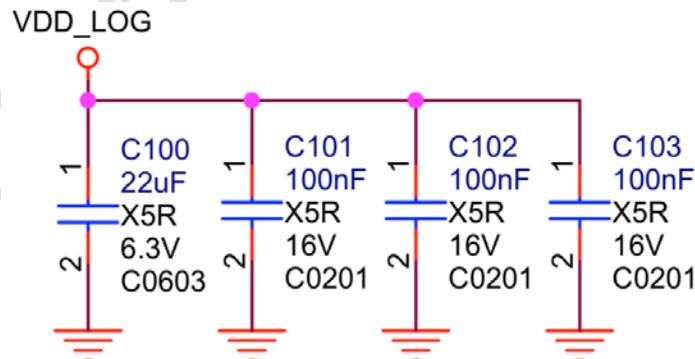


Figure 2-12 RK1808 chip power decoupling capacitors

- 2.2.2.5 DDR power

RK1808 DDR controller supports various types of DDR, such as DDR3/DDR3L/LPDDR3. Only need to provide DDRIO_VDD power, power levels are different when DDR components are difference, 1.2V/1.35V/1.5V three-level adjustable. This voltage is powered by RK809-2 BUCK3, for product design, adjust feedback resistances and confirm output voltage meets DDR component power requirements according to the actual usage cases.

RK1808 DDR controller internally integrates Vref circuit, which will output adjustable VREFO_DDR voltage for DDR component and save external voltage divider resistor circuit

(see Figure 2-14 below); when LOG is turned off, VREFO_DDR will also be Turn off. Vrefca at the component side must be kept powered at all times (self-refresh needs). Vrefdq can be turned off during DDR self-refresh. Therefore, VREFO_DDR output from RK1808 can only be used for Vrefdq of the component; unless DDR is not used for power-saving function and no need to enter self-refresh state.

On LPDDR3 DRAM side Vref_CA=VCC_DDR/2, and Vref_DQ needs to be adjusted according to ODT strategy, and the corresponding Vref voltage can be adjusted according to drive strength and ODT value.

For example, at the frequency of 800MHz, the drive strength of RK1808 chip side is 34ohm, and ODT of DRAM side is 240ohm. When ODT is enabled, DRAM Vref=0.562*VCC_DDR calculated according to the formula. Therefore, VREFO_DDR voltage of RK1808 only needs to set the output of 0.674V.

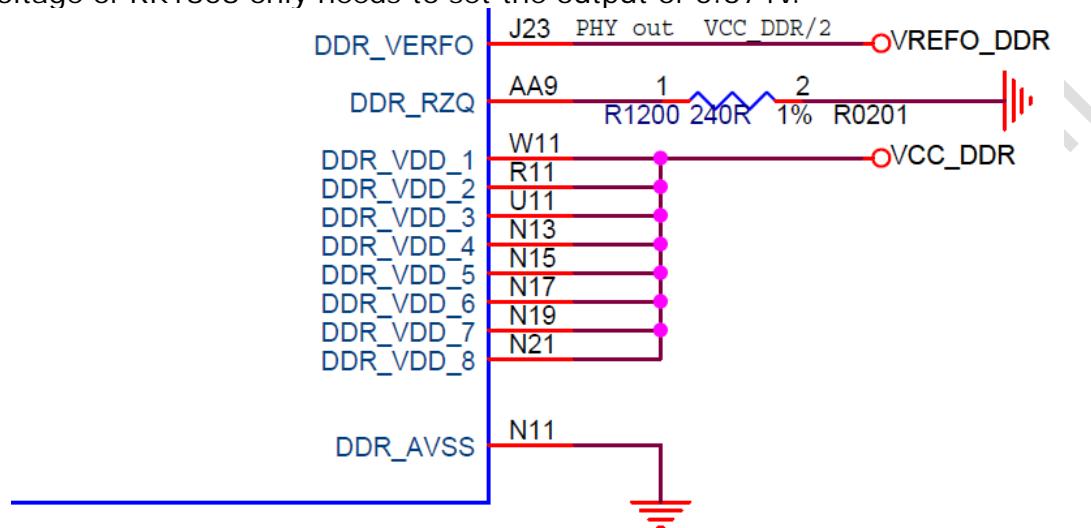
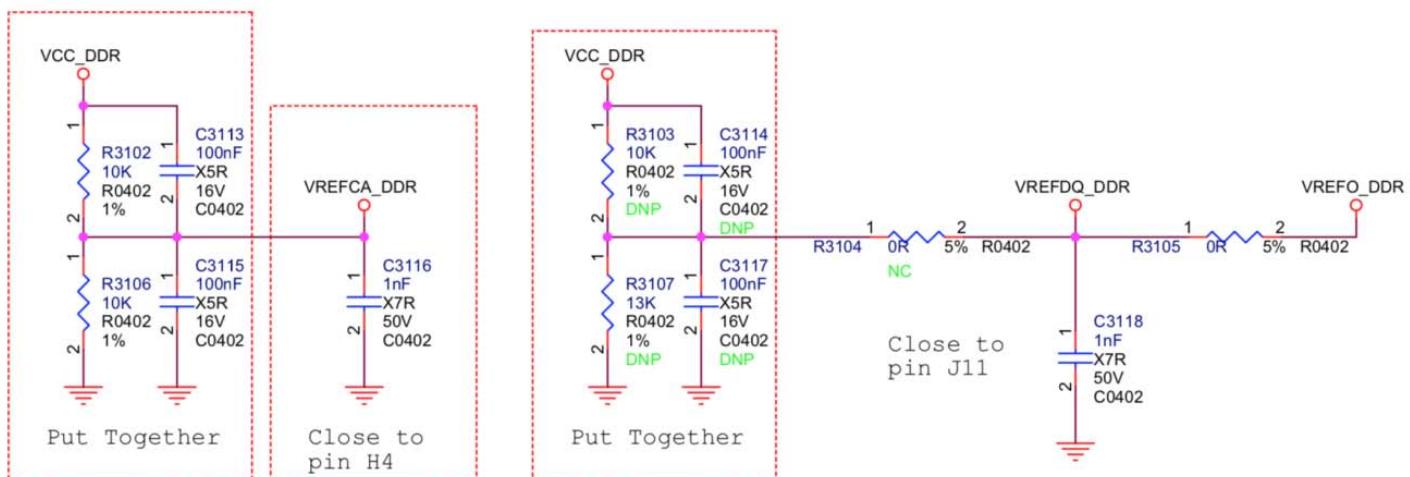


Figure 2-13 RK1808 chip DDR controller power



Note:
 $Vih = VCC$
 $Vil = VCC \cdot Ron / (Ron + Rodt)$
 $VREFDQ_DDR = (Vih + Vil) / 2$

eg: $VCC = 1.2V$, $Ron = 34\text{ohm}$, $Rodt = 240\text{ohm}$
so, $Vih = 1.2V$, $Vil = 0.149V$, $VREFDQ_DDR = 0.674V$

Figure 2-14 RK1808 LPDDR3 DRAM VREF power design



Note

Vref_DQ design for various types of DDR components:

LPDDR2 does not support ODT function; DDR4 Vref_DQ is adjusted inside the [DDR parts](#); while DDR3/DDR3L ODT function is enabled, it will pull up/down simultaneously internally,

Rockchip 瑞芯微电子	
Project:	RK1808_REF_V10
File:	31.RAM LPDDR3 1x3
Date:	Thursday, January 03, 2019
Designed by:	Rzf

$Vref_DQ = Vref_CA = VCC_DDR/2$; Only LPDDR3 needs to adjust $Vref_DQ$.

● 2.2.2.6 NPU power

NPU power of RK1808 uses external BUCK power supply, as shown in Figure 2-15 below, NPU power supports dynamic frequency and voltage scaling, and the peak current can reach 5A. This power supply current will instantaneously jump 3.5A/10uS, so it is required the selected BUCK transient response should be good enough, and the ability with load should be strong; For layout, should place 2x22uF large capacitors on the back of RK1808 chip (please place close to the chip if only one side) as shown in Figure 2-16; The total capacitance on this power supply path requires more than 220 UF. Please do not delete the capacitors in RK1808 reference design schematic to ensure that the power ripple is controlled within 90mV (when operating frequency is 800M), to prevent power ripple being too large under large load. The filter capacitors are shown in Figure 2-17.

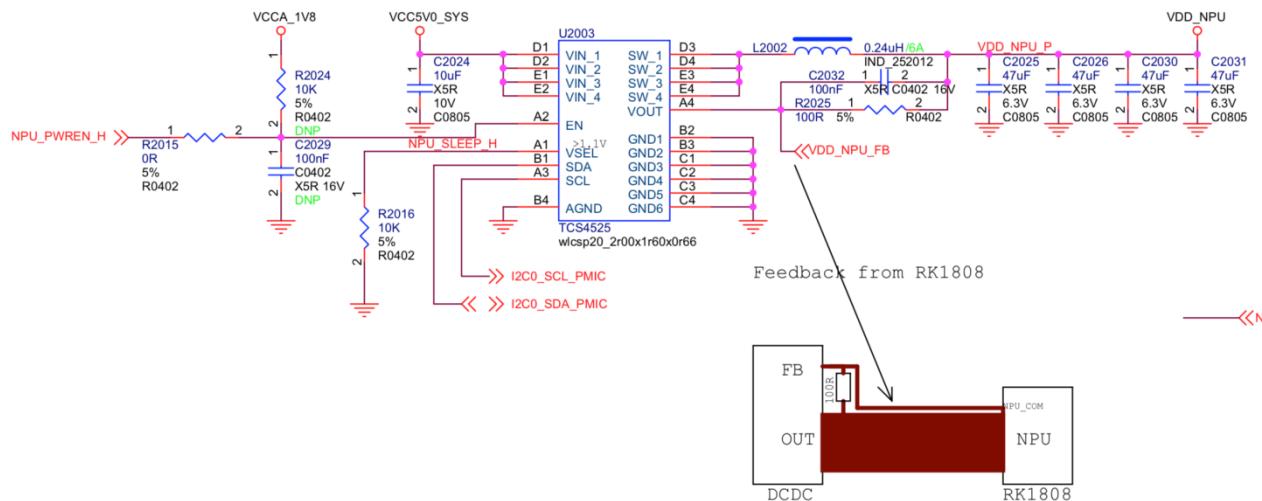


Figure 2-15 NPU Power design

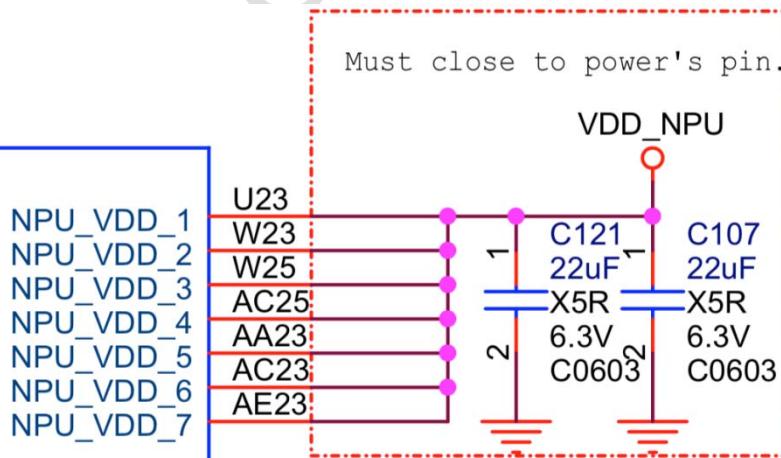


Figure 2-16 RK1808 NPU controller power

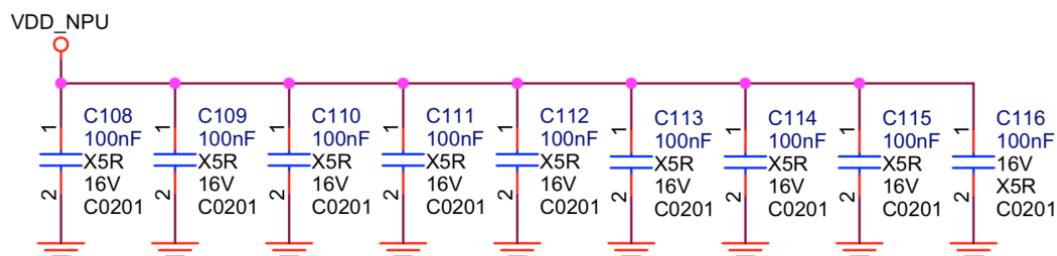


Figure 2-17 RK1808 NPU Power filter capacitors

- 2.2.2.7 GPIO power

Please refer to chapter 2.1.9 for GPIO power circuit. It is recommended to place a 100nF decoupling capacitor on each pin and place it close to power pin. For detailed design, please refer to RK1808 reference design schematic.

2.2.3 Introduction of RK809-2 solution

- 2.2.3.1 RK809-2 block diagram

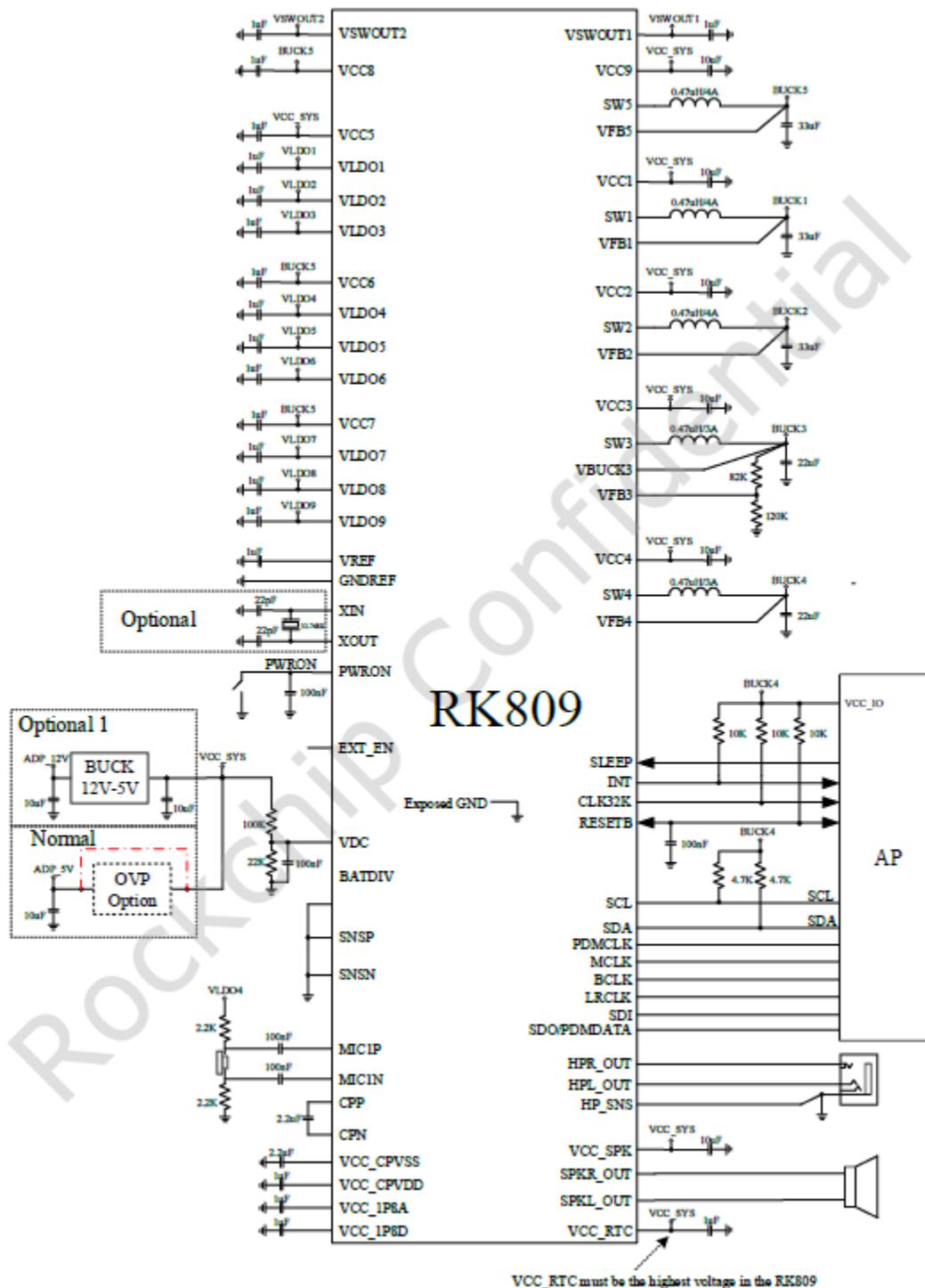


Figure 2-18 RK809-2 block diagram

- 2.2.3.2 RK809-2 features

- Power input range: 2.7V-5.5V
- Including accurate volt-ammeter for single battery voltage and current two ADC

- Built-in real time clock (RTC)
- Very low standby current of 25uA (at 32KHz clock frequency)
- Real-time output headphone drive
- Is a 1.3W Class D amplifier that does not require external filter inductors
- Programmable power supply power on sequence and voltage values
- Built-in high performance audio codec
 - ◆ Built-in independent PLL
 - ◆ Support microphone input
 - ◆ Support for programmable digital and analog gain
 - ◆ Support bit rate of 16bits-32bits
 - ◆ Sample rate up to 192kHz
 - ◆ Software supports master and slave two working mode configurations
 - ◆ Supports 3 I2S formats (standard, left aligned, right aligned)
 - ◆ Support PDM mode (external input PCLK)
- Power supply:
 - ◆ Channel 1: Synchronous Step-Down DC-DC Converter, 2.5A max
 - ◆ Channel 2: Synchronous Step-Down DC-DC Converter, 2.5A max
 - ◆ Channel 3: Synchronous Step-Down DC-DC Converter, 1.5A max
 - ◆ Channel 4: Synchronous Step-Down DC-DC Converter, 1.5A max
 - ◆ Channel 5: Synchronous Step-Down DC-DC Converter, 2.5A max
 - ◆ Channels 6-7, 9-14: Low Dropout Linear Regulator, 400mA max
 - ◆ Channel 8: Low-noise, high power rejection ratio Low Dropout Linear Regulator, 100mA max
 - ◆ Channel 15: Switch, 1.5A max
 - ◆ Channel 16: Switch, 3A max
- Package: 7mmx7mm QFN68

● 2.2.3.3 RK1808+RK809-2 Power Tree

RK1808 uses RK809-2+external buck power supply solution. The following figure shows the power architecture diagram.

See RK1808 reference diagram "Power diagram and Sequence" page for details.

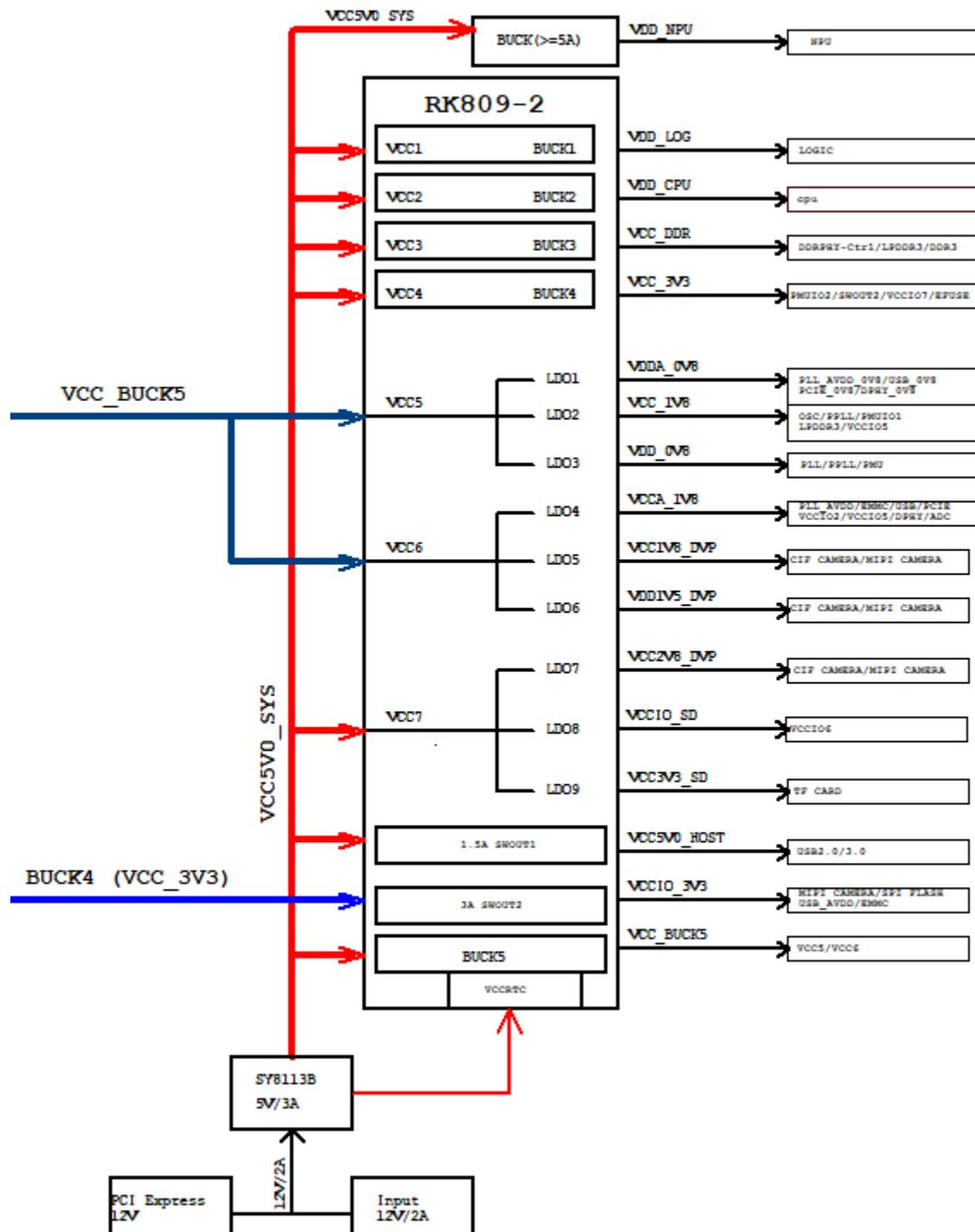


Figure 2-19 RK809-2 Power architecture

- 2.2.3.4 RK809-2 notes

- The recommended matching capacitance of 32.768 crystal is 22pF. Customers can fine tune this parameter according to the specifications of the crystal used.



Note

In order to reduce consumption, The crystal signal driving ability of PMIC RTC is weak, it is not able to measure oscillation signal in XOUT or XIN pin using normal oscilloscope, or oscillation will stop once the probe touch it. Please use CLK32K pin if need to measure 32.768k signal.

- VCC_RTC must be powered, and its voltage value must be the highest among RK809-2 power.
- BUCK1 and BUCK2 output capacitors must be over 30uF to guarantee good

decoupling effect, especially in high current and heavy load cases, it is better to increase output decoupling capacitor value.

- RK809-2 comes with USB OTG power supply function SWITCH1, with short circuit protection function, can be configured with 1.5A output current limit;
- The boot logic directly controlled by input power is as follows: When there is a power input, the primary DCDC buck outputs VCC5V0_SYS and VCC_RTC, the power is passed through the external voltage divider circuit and then input to VDC is greater than 0.55V. At this time, PMIC starts to work and output voltage;
- Boot and shutdown logic controlled by keys is as follows: PWRON pin has built-in 17K pull-up resistor, pull up to VCCRTC, it will automatically power on when it detects low level for more than 500ms; if PWRON pin is pulled low for more than 6s after boot, it will force shutdown (usually used for forced shutdown after system crashes, and then power on); during suspend and wake-up operations, low level of PWRON pin needs to be maintained for more than 20ms.
- RK809-2 basic working conditions:
 - ◆ VCC_RTC is powered;
 - ◆ VCC5V0_SYS is powered, ;
 - ◆ One of the following three cases is detected: RK809-2 automatically powers up: PWRON pin is low and maintains 500mS; VDC voltage exceeds 0.55V; internal RTC Alarm is boot enabled and time is up.
 - ◆ Start power up process, every timing interval is 2ms, the next timing will continue only after the former one voltage output meets the requirement, until all the timings power up, release reset, and then finish the process.

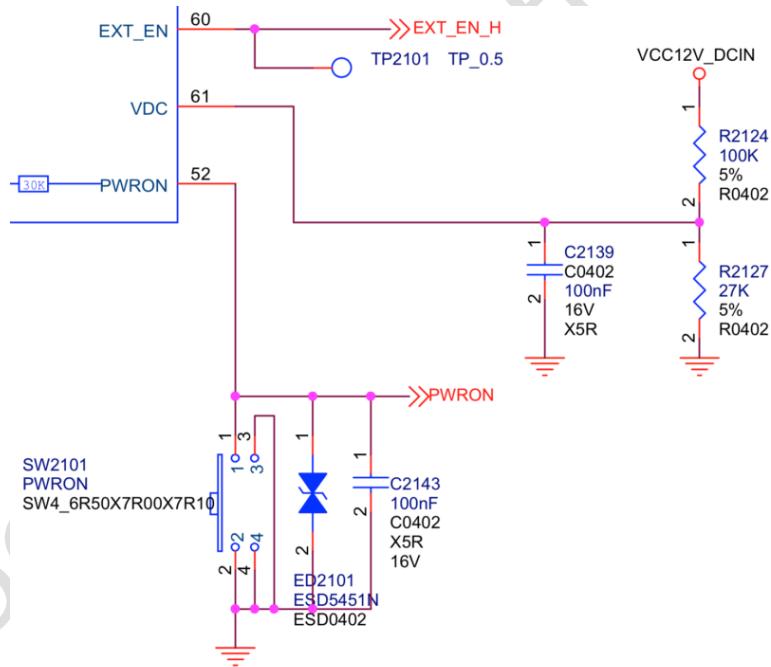


Figure 2-20 RK809-2 PWRON pins

- RK809-2 will power off automatically if any of the two cases below is detected:
 - ◆ I2C write DEVICE_OFF=1;
 - ◆ PWRON pin keeps low level over 6s
- After RK809-2 starts power-off process, it will pull down "reset" after one RTC clock cycle (after about 30.5us), and then turn off all power output at the same time after 2ms to complete the power-off process;

● 2.2.3.5 RK809-2 design introduction

For RK809-2 design details, please refer to RK PMIC related design document "RK809 application guide"

2.2.4 Others

- 2.2.4.1 over temperature protection circuit

When RK1808 chip's temperature is too high, crash or in other abnormal situations, TSADC_SHUT pin will output low level, reset RK809-2, control the power to down and clear the whole registers, and then restart:

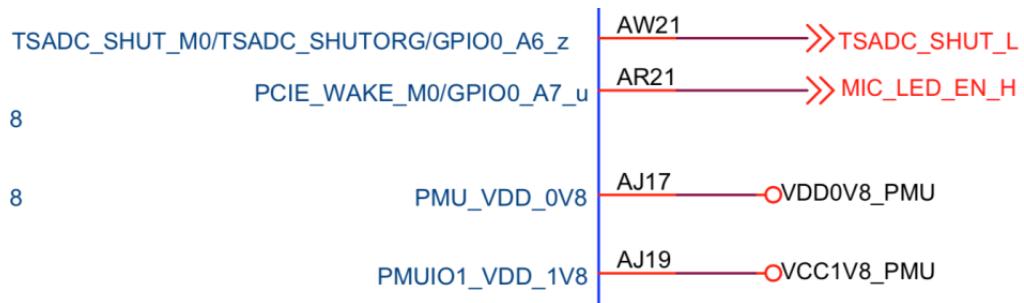


Figure 2-21 RK1808 TSADC_SHUT(OTP_OUT) protection output

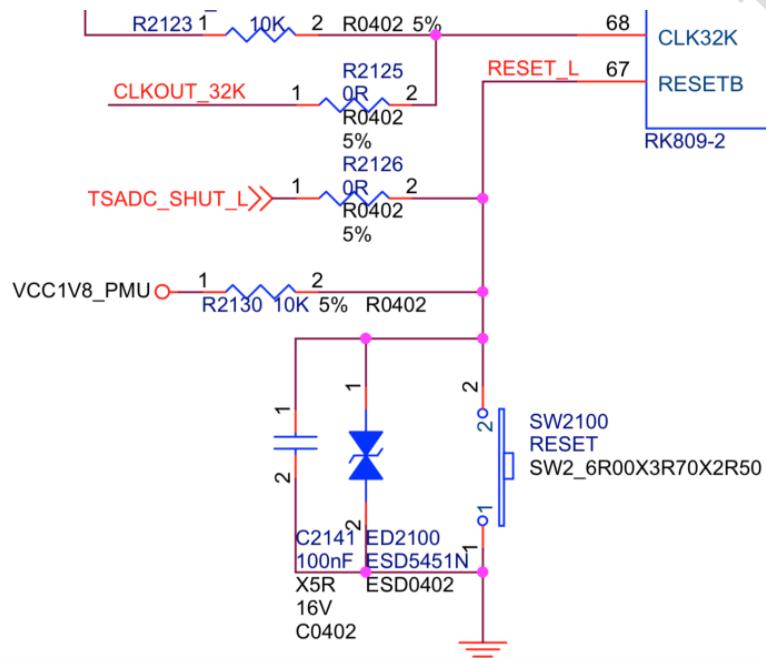


Figure 2-22 RK809-2 TSADC_SHUT(OTP_OUT) over temperature protection input

- 2.2.4.2 PMIC SLEEP circuit

When RK1808 is in normal working mode, the status pin PMIC_SLEEP will keep low level output.

When system enters standby mode, PMIC_SLEEP pin will output high level sleep indicator signal and at the moment PMIC will enter the standby mode as controlled by the signal. As configured in firmware dts file, some power will be cut off and some will set down voltage.

When system is waken up from standby mode, PMIC_SLEEP pin will output low level first, and then PMIC will restore back to the previous working status and recover all power outputs.

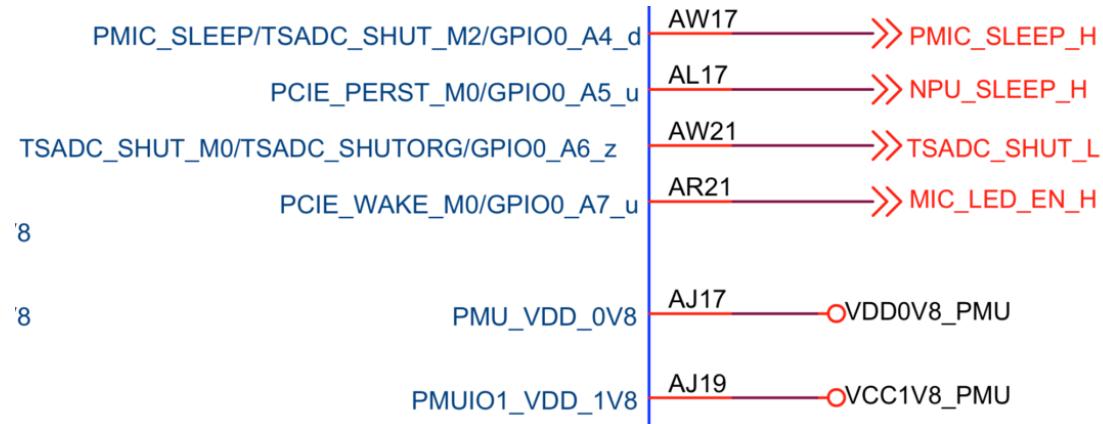


Figure 2-23 RK1808 PMIC_SLEEP output

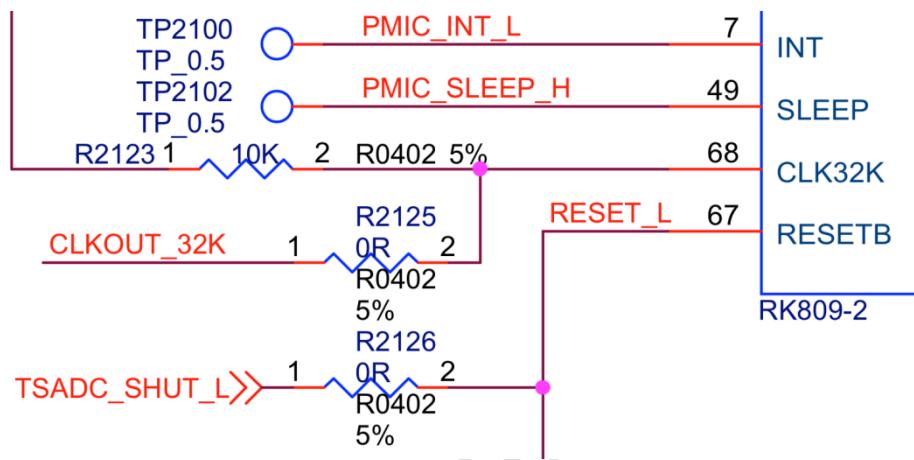


Figure 2-24 RK809-2 PMIC_SLEEP input

2.2.5 Power peak current table

Below table shows three main power peak current test results in high load, high temperature (88-90 degrees) mode based on RK1808 EVB V10, for reference only. Test condition is as below:

- APK version: ripple_peak_current_test;
- CPU max frequency: 1.6 GHz;
- NPU max frequency: 800 MHz;
- DDR max frequency: 1x32bit LPDDR3 K4E6E304EB-EGCF, 800 MHz;

Table 2-9 RK1808 peak current table

Power Name	Voltage (V)	Peak Current (mA)	Peak Ripple (mV)
VDD_CPU	0.9	826	26.3
VDD_LOG	0.8	786	9
VDD_NPU	0.85	2810	82

2.3 Function interface circuit design guide

2.3.1 Memory card circuit

RK1808 provides one SDMMC interface controller which can support SD v3.0 and eMMC v4.51 protocol, as shown in picture 2-25:

- SDMMC0 controller has a standalone power domain;
- SDMMC0 reuses with UART2, JTAG etc. Choose the function through SDMMC0_DET. Please refer to chapter 2.1.4 for details;
- VCCIO_SD is IO power which needs 3.3V power from external(SD 2.0 mode) or 3.3V/1.8V adjustable power(SD 3.0 mode);

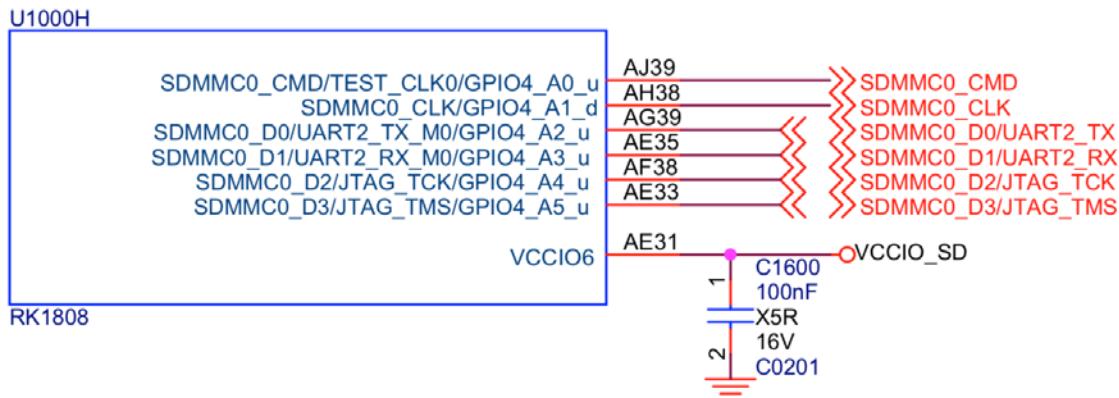


Figure 2-25 RK1808 SDMMC module circuit

SDMMC interface pull up/down and matching design recommendations are shown as below table 2-10.

Table 2-10 RK1808 SDMMC interface design

Signal	Internal Pull up/down	Connection Method (SD3.0 high speed mode)	Description(chip side)
SDMMC_DQ[3:0]	pull up	in series with 22ohm resistor Can delete if the line is short	SD data send/receive
SDMMC_CLK	pull down	in series with 22ohm resistor	SD clock send
SDMMC_CMD	pull up	in series with 22ohm resistor Can delete if the line is short	SD command send/receive

2.3.2 USB circuit

● 2.3.2.1 USB20 circuit

RK1808 has two sets of USB 2.0 interface, one is USB 2.0 HOST, and the other is USB2.0 OTG which is the only one that can be used to download firmware.

RK1808 USB 2.0 module circuit is shown in Figure 2-26.

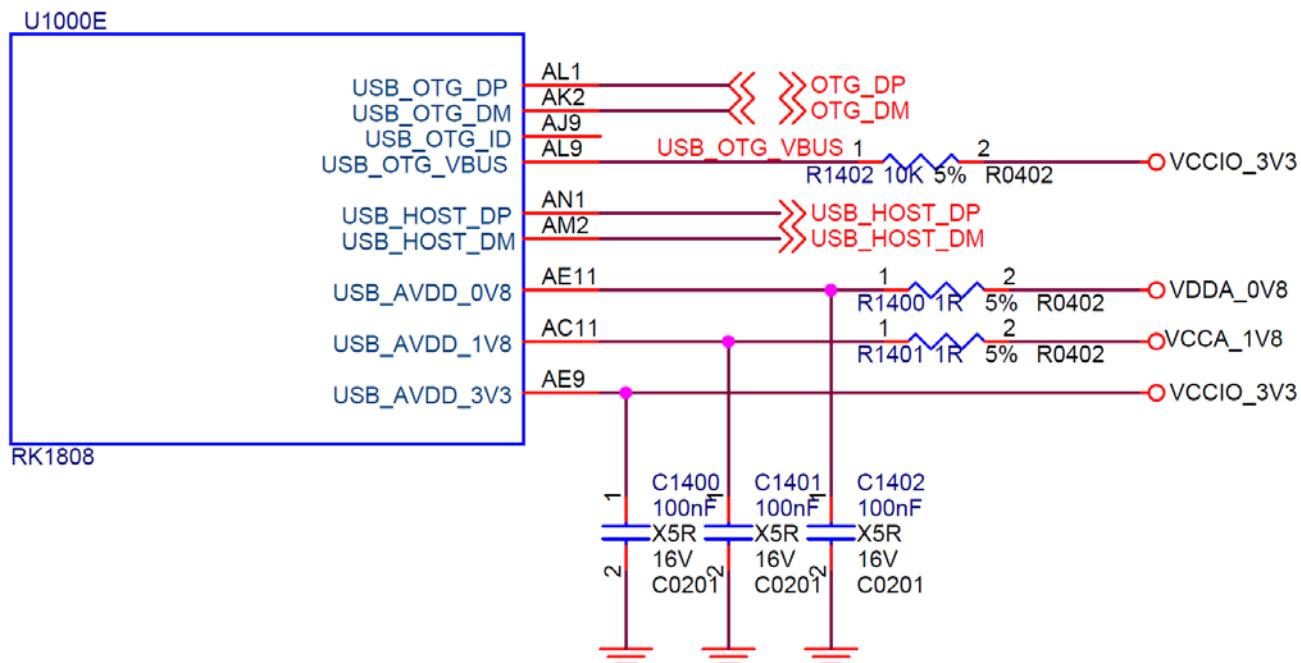


Figure 2-26 RK1808 USB 2.0 module circuit

● 2.3.2.2 USB3.0 circuit

RK1808 has built-in a USB3.0 signal that reuses the pin with PCIE V2.1 signal (see chapter 2.3.9 for details); USB3.0 signal can be combined with USB20 OTG to form a standard USB30 OTG connector that can be used to download firmware (also it can be programmed with a separate USB20 OTG micro connector for downloading).

- USB20 OTG interface is the system firmware downloading port by default. During debugging process, USB30 (USB30+USB20 OTG) interface or USB20 OTG interface must be reserved.

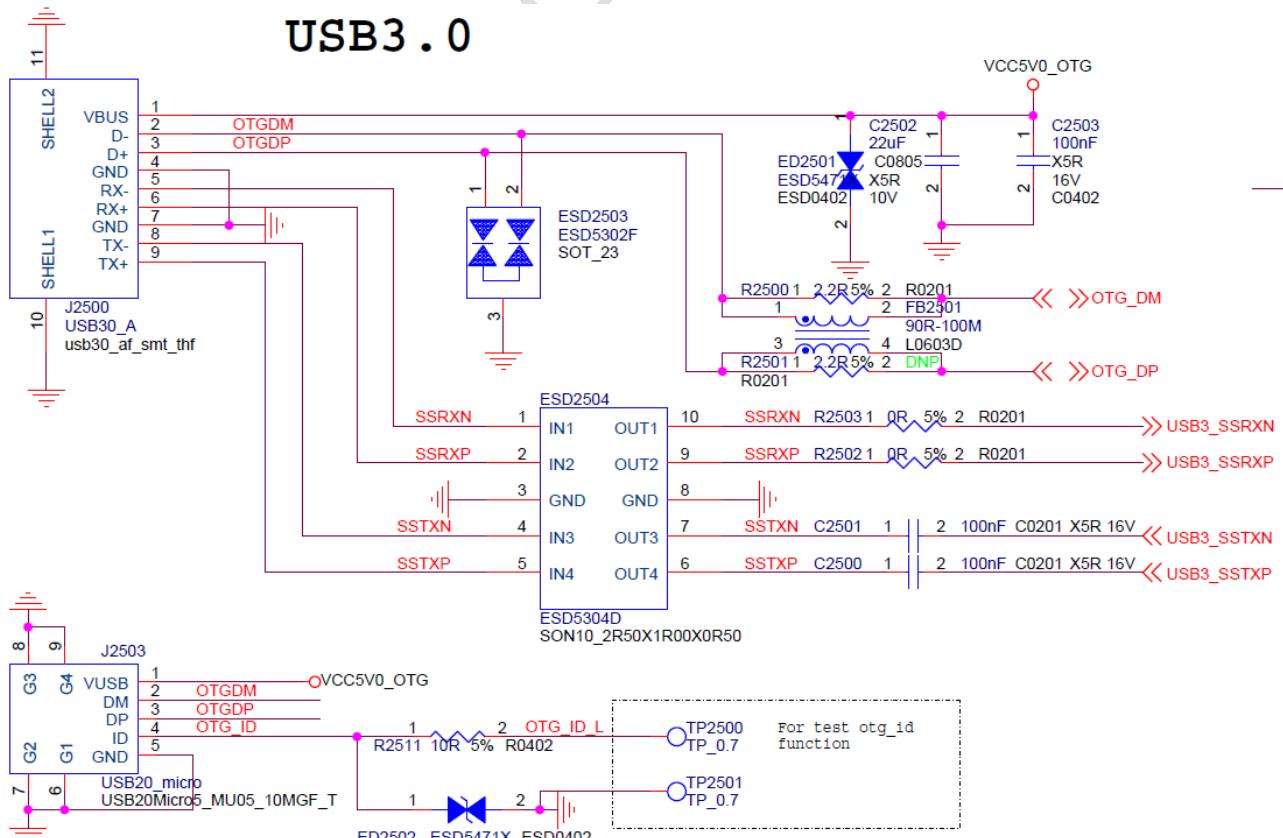


Figure 2-27 RK1808 USB3.0 circuit

- 2.3.2.3 USB other signal description

- USB_ID internally has a 200k pull up resistance which pull up to USB_AVDD_1V8, so OTG is used as Device mode by default;
- OTG_DET (USB_DET) is used to detect USB insertion. If a high level is detected, it means there is USB inserted;

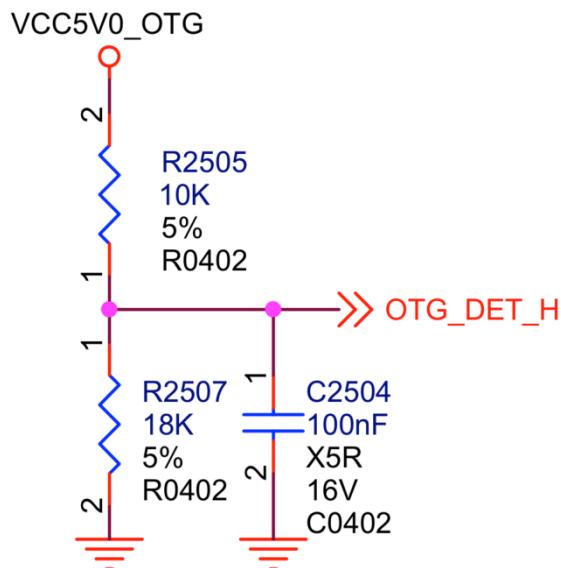


Figure 2-28 RK1808 USB insertion detection

- USB controller config reference resistor R1403 tolerance should be within 1% because the resistor will affect USB amplitude and eye diagram.



Figure 2-29 RK1808 USB/PCIE controller reference resistor

- In order to avoid surging shock to the chip, 1.0V/1.8V power of the controller need to be in series with 1ohm resistor.

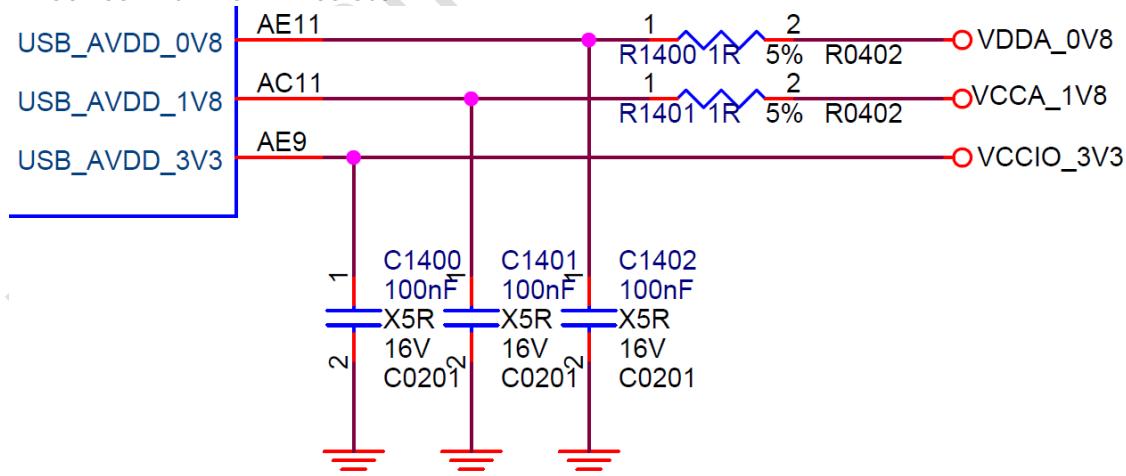


Figure 2-30 RK1808 USB controller power surge protection

- Please put controller power decoupling capacitors close to the pins to ensure USB performance.
- Consider to reserve a common mode choke in the signal line in order to restrain electromagnetic radiation. Choose to use the resistors or the common mode chokes according to the actual situation during debugging.

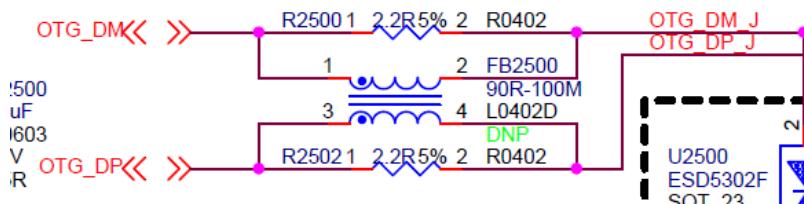


Figure 2-31 RK1808 USB reserved common mode choke

USB 2.0 interface pull up/down and matching design recommendations are shown as table 2-11.

Table 2-11 RK1808 USB2.0 OTG interface design

Signal	Connection Method	Description
USB_OTG_DP/DM	in Series with 2.2R resistor	USB OTG input/output
USB_OTG_ID	direct connection (internal with 1.8V pull up)	USB OTG ID identification, need to use when using Micro-B interface
USB_OTG_VBUS		USB OTG insert detection
USB_RBIAS		USB PHY config reference resistor, 2K ground connection(reused with PCIE)

2.3.3 Audio circuit

RK1808 provides 2 sets of standard I2S interfaces. They all support master and slave mode, max sampling rate up to 192kHz and the bit rate from 16bits to 32bits. Supports three I2S modes: normal, left-justified, right-justified; supports configurable 4 mode; early,late1,late2, Late3;I2S or PCM mode.

- 2.3.3.1 I2S0

I2S0 of RK1808 supports I2S, PCM, TDM I2S, TDM PCM functions

As shown in the figure, I2S0 interface includes independent 8 channels output and 8 channels input. To meet with the asynchronous sampling rate requirement of playback and recording, bit clock and frame clock also provide 2 sets (SCLKTX\LRCKTX, SCLKRX\LRCKRX) correspondingly. Need to notice that, in the case when SDOx and SDIx only refer to one set of bit/frame clock, prefer to use SCLKTX\LRCKTX as their common clock.

Need to notice that, the set of I2S interface belongs to VCCI04 power domain, The power supply is set to 1.8V by default. If I2S peripheral IO voltage is 3.3V, need to adjust the powers supply and note to match the voltage with relative IO in the same power domain.

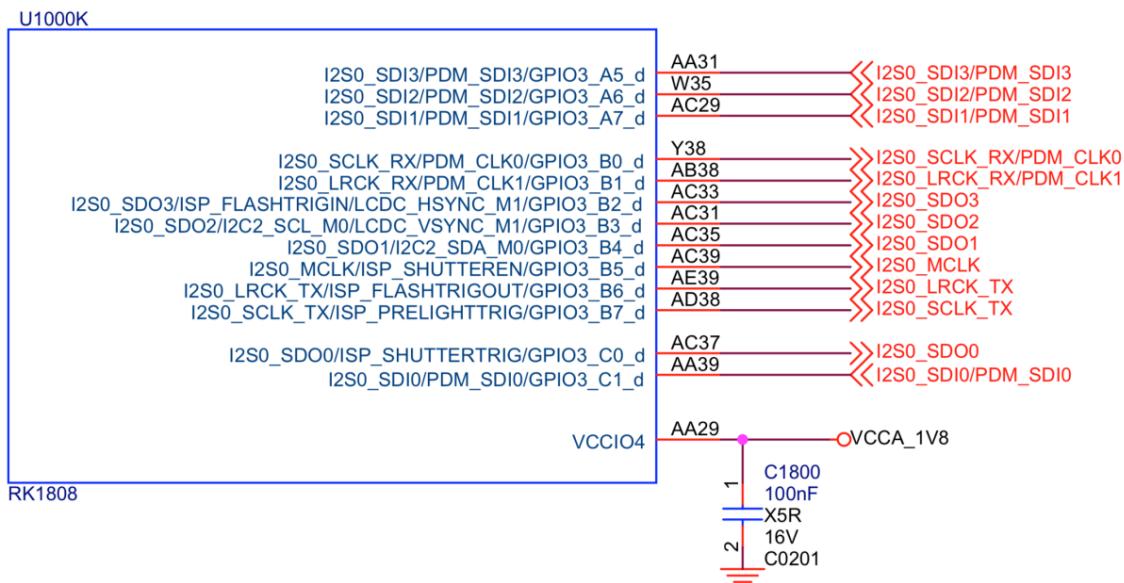


Figure 2-32 RK1808 I2S0 module circuit

I2S0 interface pull up/down and the matching design recommendations are shown as table 2-12.

Table 2-12 RK1808 I2S0 interface design

Signal	Internal Pull up/down	Connection Method	Description(chip side)
I2S0_8CH_MCLK	pull down	in series with 22ohm resistor	I2S0 system clock output
I2S0_8CH_SCLKTX	pull down	in series with 22ohm resistor	I2S0 bit clock(TX, associated with SDOx)
I2S0_8CH_LRCKTX	pull down	in series with 22ohm resistor	I2S0 frame clock, used for audio channel selection(TX, associated with SDOx)
I2S0_8CH_SDO0	pull down	in series with 22ohm resistor	I2S0 data output channel 0
I2S0_8CH_SDO1	pull down	in series with 22ohm resistor	I2S0 data output channel 1
I2S0_8CH_SDO2	pull down	in series with 22ohm resistor	I2S0 data output channel 2
I2S0_8CH_SDO3	pull down	in series with 22ohm resistor	I2S0 data output channel 3
I2S0_8CH_SCLKRX	pull down	in series with 22ohm resistor	I2S0 bit clock(RX, associated with SDIx)
I2S0_8CH_LRCKRX	pull down	in series with 22ohm resistor	I2S0 frame clock, used for audio channel selection(RX, associated with SDIx)
I2S0_8CH_SDIO	pull down	in series with	I2S0 data input channel 0

		22ohm resistor	
I2S0_8CH_SDI1	pull down	in series with 22ohm resistor	I2S0 data input channel 1
I2S0_8CH_SDI2	pull down	in series with 22ohm resistor	I2S0 data input channel 2
I2S0_8CH_SDI3	pull down	in series with 22ohm resistor	I2S0 data input channel 3

● 2.3.3.2 I2S1

I2S1 supports 2 channels input and 2 channels output.

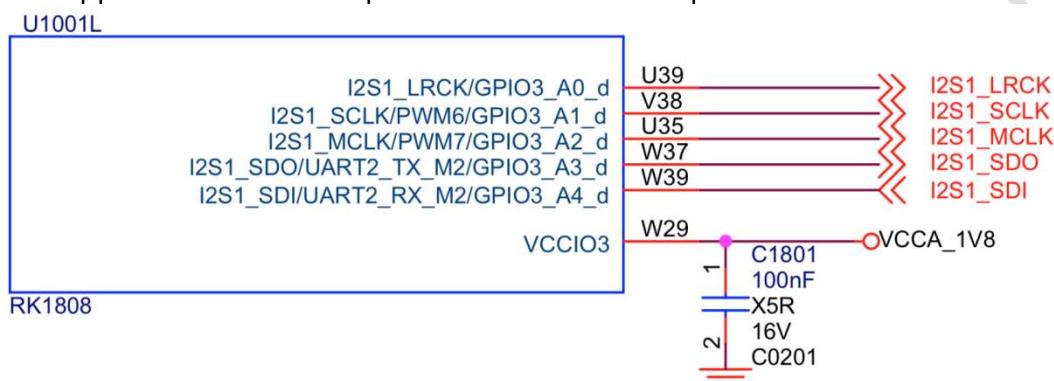


Figure 2-33 RK1808 I2S1 module circuit

I2S1 interface pull up/down and the matching design recommendations are shown as table 2-13.

Table 2-13 RK1808 I2S1 interface design

Signal	Internal Pull up/down	Connection Method	Description(chip side)
I2S1_MCLK	pull down	in series with 22ohm resistor	I2S1 system clock output
I2S1_SCLK	pull down	in series with 22ohm resistor	I2S1 bit clock
I2S1_LRCK_TXRX	pull down	in series with 22ohm resistor	I2S1 frame clock, used for audio channel to select clock
I2S1_SDO	pull down	in series with 22ohm resistor	I2S1 data output channel
I2S1_SDI	pull down	in series with 22ohm resistor	I2S1 data input channel

● 2.3.3.3 VAD(Voice Activity Detection)

RK1808 supports VAD function and voice wakeup.

Supports reading audio data from I2S/PDM, supports audio amplitude detection,
supports multi-MIC array data storage, and supports level combination interrupt.

● 2.3.3.4 PDM

RK1808 provides a group of PDM digital audio interfaces, supports up to 8 channels of PDM format audio input, max sampling rate up to 192KHz, bit rate ranges from 16bits to 32bits.

When use PDM MIC to capture audio, to simplify the software processing on audio recording data, also suggest to use PDM interface for loop back. Therefore in the normal cases with 2-6 PDM MIC audio recording and 1-2 loop back channels, just one whole 4-8 channel audio recording is enough to complete input, no need for software to do the additional splicing processing.

PDM pin reused with I2S0, as shown below:

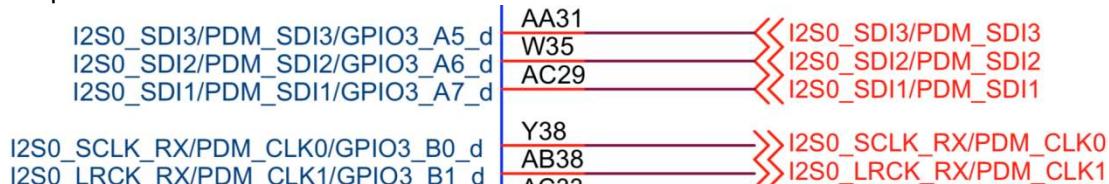


Figure 2-34 PDM interface of RK1808 I2S0 module

● 2.3.3.5 TDM

RK1808 provides a group of TDM digital audio interfaces supporting master or slave mode, up to 8 TDM format audio outputs and 8 TDM format audio inputs, max sampling rate up to 192kHz, bit rate from 16bits to 32bits; TDM signals and I2S0 signal pins reuse compatible.

● 2.3.3.6 Codec

RK809-2 comes with Codec and supports I2S and PCM interfaces. I2S/PCM audio digital interface is used to input or output data from a stereo DAC; I2S/PCM can be configured in master or slave mode, in master mode, BCLK and LRCLK are configured as outputs, MCLK is fixed as an input; in slave mode, BCLK and LRCLK are configured as inputs and MCLK is configured as an input too. RK1808 uses I2S1 interface to communicate with RK809-2 by default, RK1808 as a master device, and RK809-2 as a slave device.

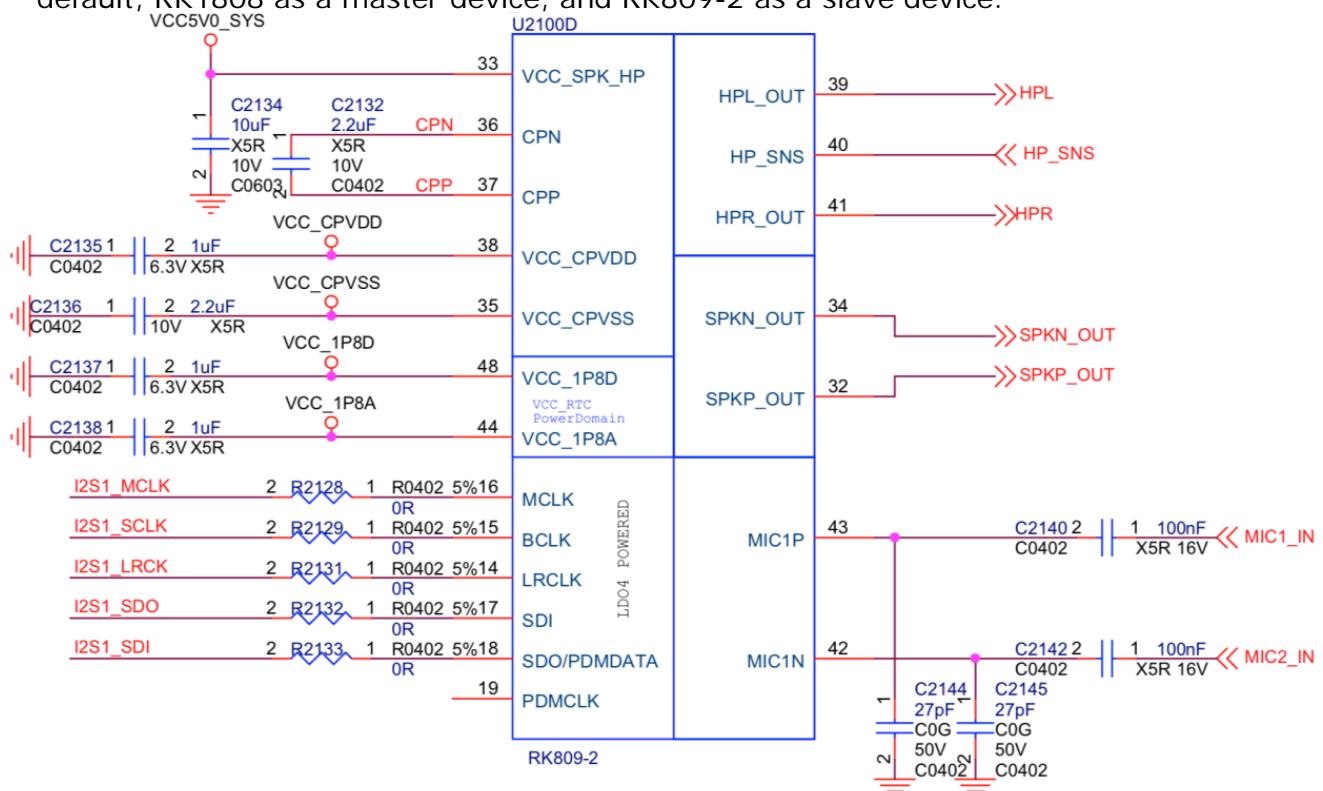


Figure 2-35 RK809-2 Codec circuit

The HP_SNS output from Codec is used as an internal reference for Offset. It needs to be connected with GND at the headphone connector to reduce voltage difference with headphone GND, and they should be routed concomitantly in the middle of HPR/HPL, so as to avoid interference from other signals. If Codec's GND and headphone's GND are on the same whole GND layer and devices layout are close, they can be connected directly to GND layer.

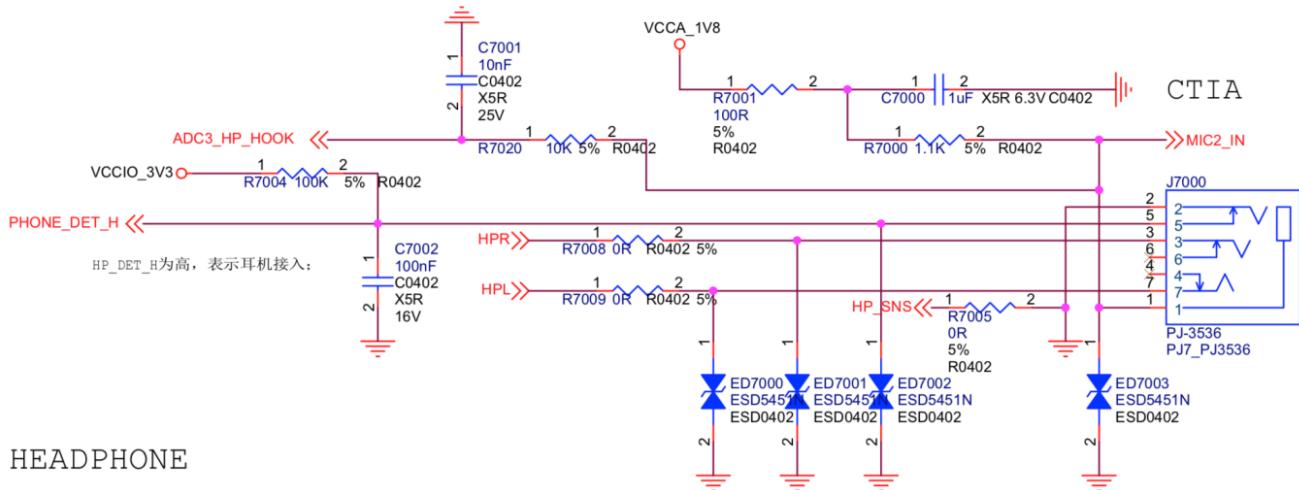


Figure 2-36 RK1808 Headphone circuit

Codec builds in a Mono filterless speaker driving circuit which can provide 1.3W@8ohm drive strength for low power and single audio channel application case to save the cost of additional external amplifier. If Codec built-in Mono speaker drive circuit cannot meet the requirements of the drive capability, a separate analog/digital amplifier can be added.

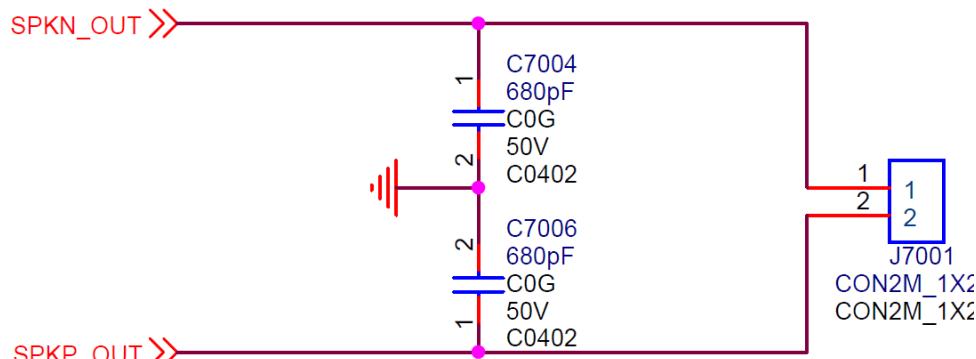


Figure 2-37 RK1808 Speaker circuit

● 2.3.3.7 MIC

MIC circuit is shown as figure 2-38. Please select appropriate bias resistor R7007 according to the electret microphone specification.

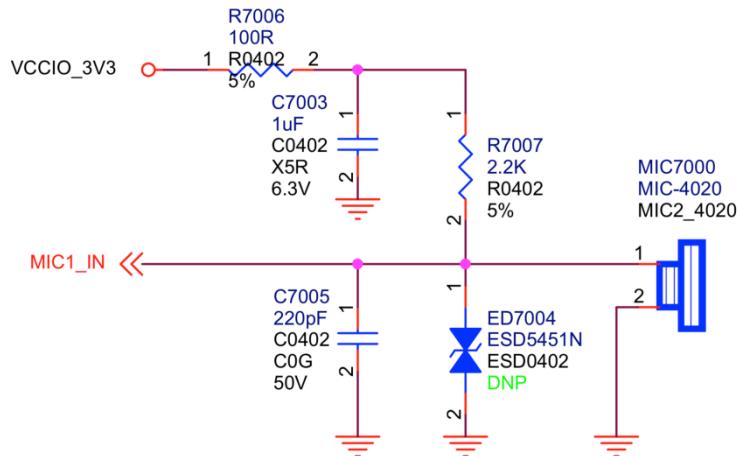


Figure 2-38 RK1808 MIC circuit

2.3.4 RGMII/LCDC/CIF(BT1120) circuit

RK1808 chip built-in a RGMII/CIF/LCDC controller. These three functions are pin-reused and only one function can be used at the same time. The schematic is shown in Figure 2-39 below:

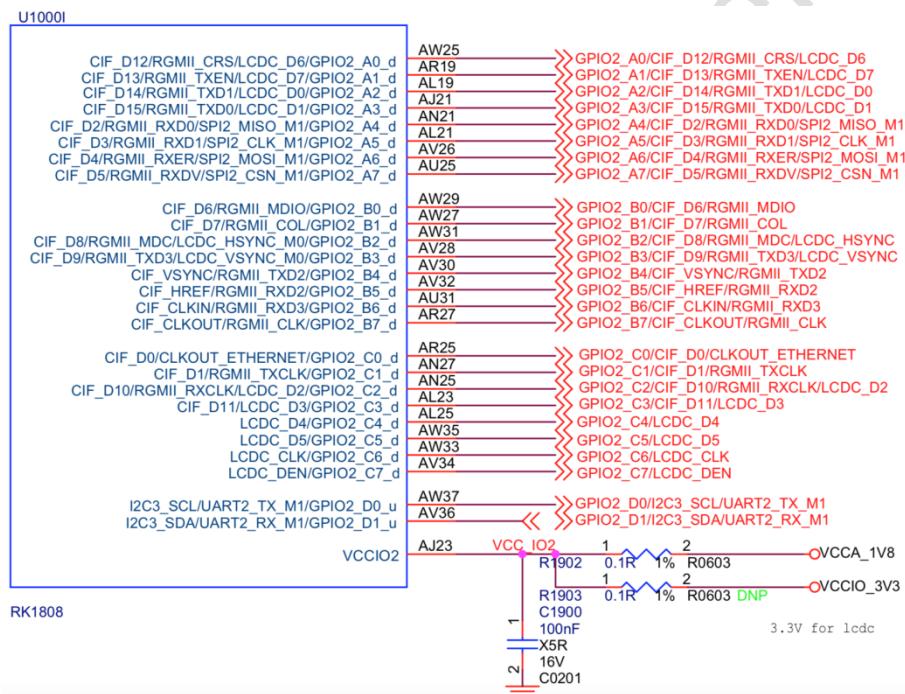


Figure 2-39 RK1808 RGMII/CIF/LCDC interface

● 2.3.4.1 Ethernet Circuit

RK1808 integrates a Gigabit Ethernet MAC, which can be connected to different Ethernet PHYs to achieve 100M/Gigabit network functions. Please refer to design documents of PHY vendor for detailed design and this guide will not introduce too much. The 25M working clock of PHY uses an external crystal, and RGMII_CLK (125M) of RK1808 is output from CLKOUT pin of PHY, as shown in Figure 2-40.

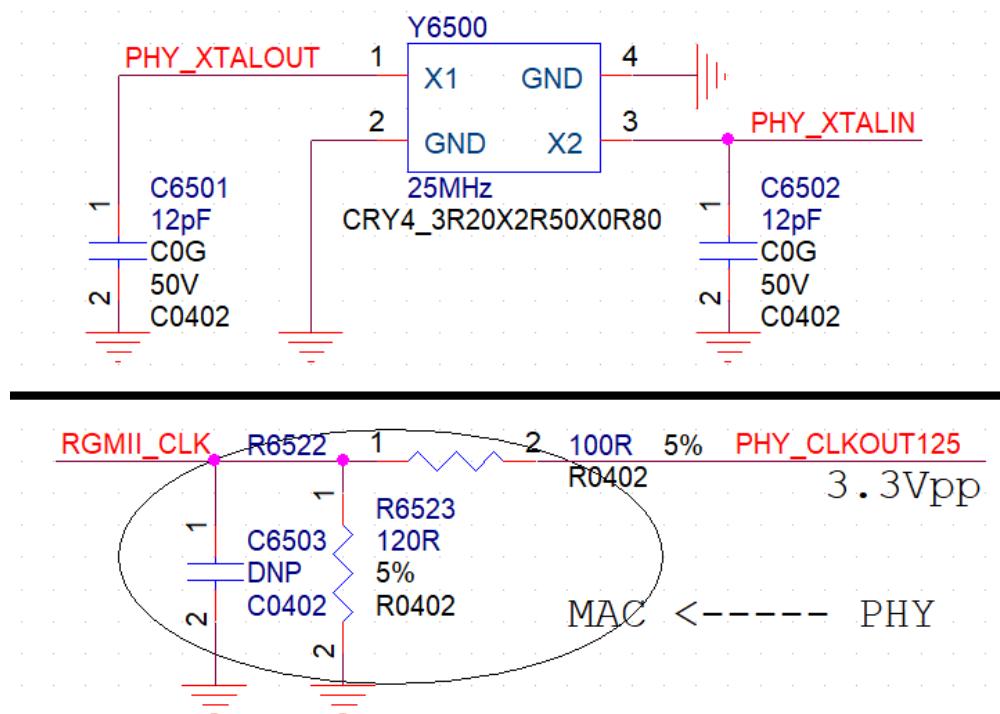


Figure 2-40 RK1808 PHY clock circuit

RK1808 supports 10/100/1000M Ethernet controller, 1000M GMAC design and its notes are as follows:

Signal	Internal Pull up/down	Connection Method	Description(chip side)
RGMII_TXCLK	pull down	in series with 22ohm resistor	Reference clock for data sending
RGMII_RXCLK	pull down	in series with 22ohm resistor	Reference clock for data reception
RGMII_TXD[3:0]	pull down	in series with 22ohm resistor	Data send
RGMII_RXD[3:0]	pull down	in series with 22ohm resistor	Data receive
RGMII_TXEN	pull down	in series with 22ohm resistor	Send data enable
RGMII_RXDV	pull down	in series with 22ohm resistor	Receive data valid indication
RGMII_MDC	pull down	in series with 22ohm resistor	Configure interface clock
RGMII_MDIO	pull down	in series with 22ohm resistor	Configure interface I/O
RGMII_CLK	pull down	in series with 22ohm resistor	MAC master clock output or input

- Power: RK1808 GMAC only needs one power supply VCCIO2, which can be configured to 1.8V or 3.3V. According to Ethernet PHY IO supply voltage configuration, it needs to be consistent with GMAC IO voltage level.
- On RK1808 RGMII interface transceiver signal line, TX_CLK and RX_CLK are 125MHz, TXD and RXD signal lines are sampled on both sides of clock to achieve 1000Mb transmission rate, data enable signal (RGMII_TXEN, RGMII_RXDV) must be enabled before data sending valid.
- Reset: RGMII resets PHY with GPIO. It can also use RC hardware reset circuit. Note that if RC hardware reset circuit is used, PHY power must be controllable.

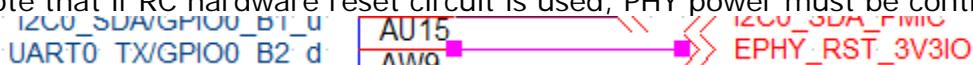


Figure 2-41 RK1808 RGMII Reset Circuit for PHY

- The control and status information between MAC layer and PHY are MDIO interface, clock MDC signal and data MDIO signal. It should be noticed that MDIO signal needs to be pulled up, as shown below:

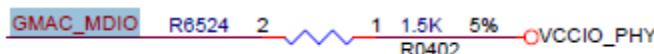


Figure 2-42 RK1808 RGMII MDIO signal

- 10/100M work and connection are similar to 1000M, the only different is RGMII_CLK=50M; note that 10/100M PHY_CRS_DV is connected to MAC_RXDV instead of MAC_CRS pin.

■ ESD protection

In order to meet the requirements of ESD protection and surge protection, it is recommended to design a protection circuit on RGMII PHY circuit during design. In order to avoid protection devices from affecting PHY routing signal and achieving good protection, it is recommended to adopt the following rules when designing PCB.

A: Protection devices are recommended to be placed inside transformer, between transformer and PHY, close to transformer.

B: Protection devices are recommended to use TVS transistor, the breakdown voltage is 8kV, and the response time is less than 1ns.

● 2.3.4.2 LCDC interface introduction

RK1808 supports 18bit RGB output, supports 18-bit (RGB666), 16-bit (RGB565), resolution is 1280X800; supports MCU interface, needs to configure the corresponding output mode by software. Pin assignments are shown in Figure 2-43:

- When using RGB666 18bit screen, only need to connect LCDC_D0-D17 data signal, the corresponding relationship is as follows:

Correspondence between LCDC DATA and RGB			
LCDC_D0	B2	LCDC_D9	G5
LCDC_D1	B3	LCDC_D10	G6
LCDC_D2	B4	LCDC_D11	G7
LCDC_D3	B5	LCDC_D12	R2
LCDC_D4	B6	LCDC_D13	R3
LCDC_D5	B7	LCDC_D14	R4
LCDC_D6	G2	LCDC_D15	R5
LCDC_D7	G3	LCDC_D16	R6
LCDC_D8	G4	LCDC_D17	R7

Figure 2-43 RK1808 18bit connection method

- Following is LCD screen connection schematic:

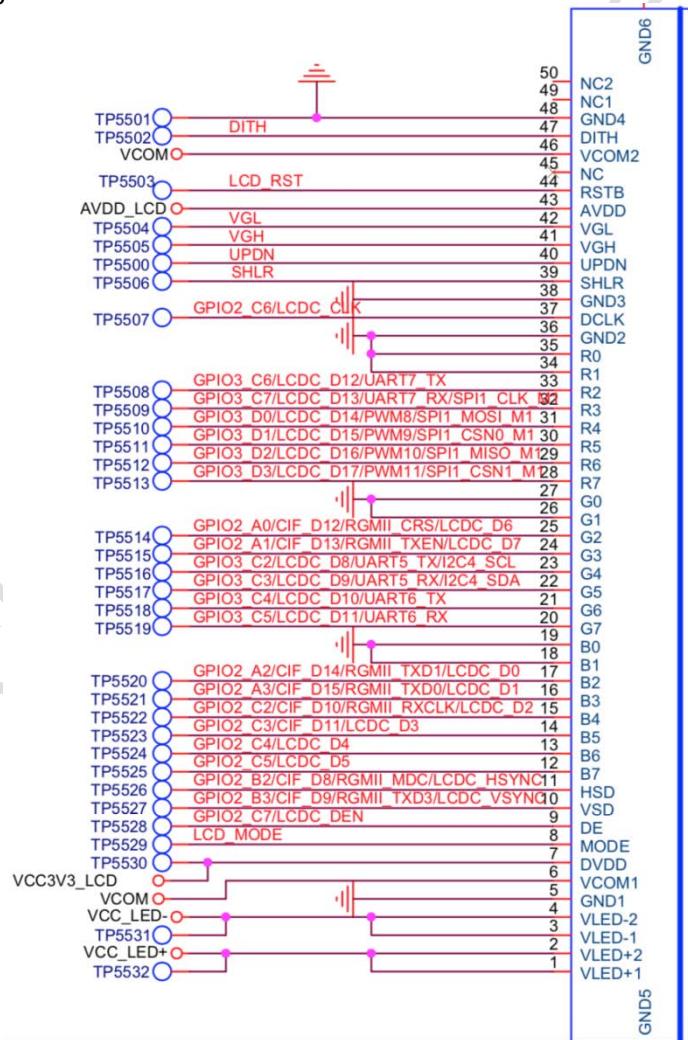


Figure 2-44 LCD connection circuit

- When using MCU screen, the relationship between LCDC's RGB and MCU interfaces is as follows:

Table 2-14 LCDC IO features description list

Interface	Pin Name	Direction	Description
LCDC	LCDC_DCLK	o	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_VSYNC	o	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LCDC_HSYNC	o	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
Interface	Pin Name	Direction	Description
	LCDC_DEN	o	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_Di ($i=0\sim17$)	o	LCDC data output/input

- 2.3.4.3 CIF(BT1120) interface introduction

RK1808 integrates a CIF interface, supports 8-bit input of BT601 YCbCr and BT656 YCbCr 422; supports UYVY/VYUY/YUYV/YVYU configuration, supports RAM 8/10/12 bit input; supports BT1120 16bit, single and double edge sampling .

CIF corresponds to different bits of DVP IO interfaces as follows:

Table 2-15 CIF interfaces corresponding DVP interfaces list

RK1808 Pin Name	ISP 8bit CIF 8bit	ISP 10bit CIF 10bit	ISP 12bit CIF 12bit	BT1120
CIF D0		CIF D0	CIF D0	CIF D0
CIF D1		CIF D1	CIF D1	CIF D1
CIF D2	CIF D2	CIF D2	CIF D2	CIF D2
CIF D3	CIF D3	CIF D3	CIF D3	CIF D3
CIF D4	CIF D4	CIF D4	CIF D4	CIF D4
CIF D5	CIF D5	CIF D5	CIF D5	CIF D5
CIF D6	CIF D6	CIF D6	CIF D6	CIF D6
CIF D7	CIF D7	CIF D7	CIF D7	CIF D7
CIF D8	CIF D8	CIF D8	CIF D8	CIF D8
CIF D9	CIF D9	CIF D9	CIF D9	CIF D9
CIF D10			CIF D10	CIF D10
CIF D11			CIF D11	CIF D11
CIF D12				CIF D12
CIF D13				CIF D13
CIF D14				CIF D14
CIF D15				CIF D15
CIF HREF	CIF HREF	CIF HREF	CIF HREF	CIF HREF
CIF VSYNC	CIF VSYNC	CIF VSYNC	CIF VSYNC	CIF VSYNC
CIF CLKIN	CIF CLKIN	CIF CLKIN	CIF CLKIN	CIF CLKIN
CIF CLKOUT	CIF CLKOUT	CIF CLKOUT	CIF CLKOUT	

Pin assignments are shown above in Figure 2-39.

CIF camera and BT1120 interface circuits are as follows:

CIF CAM

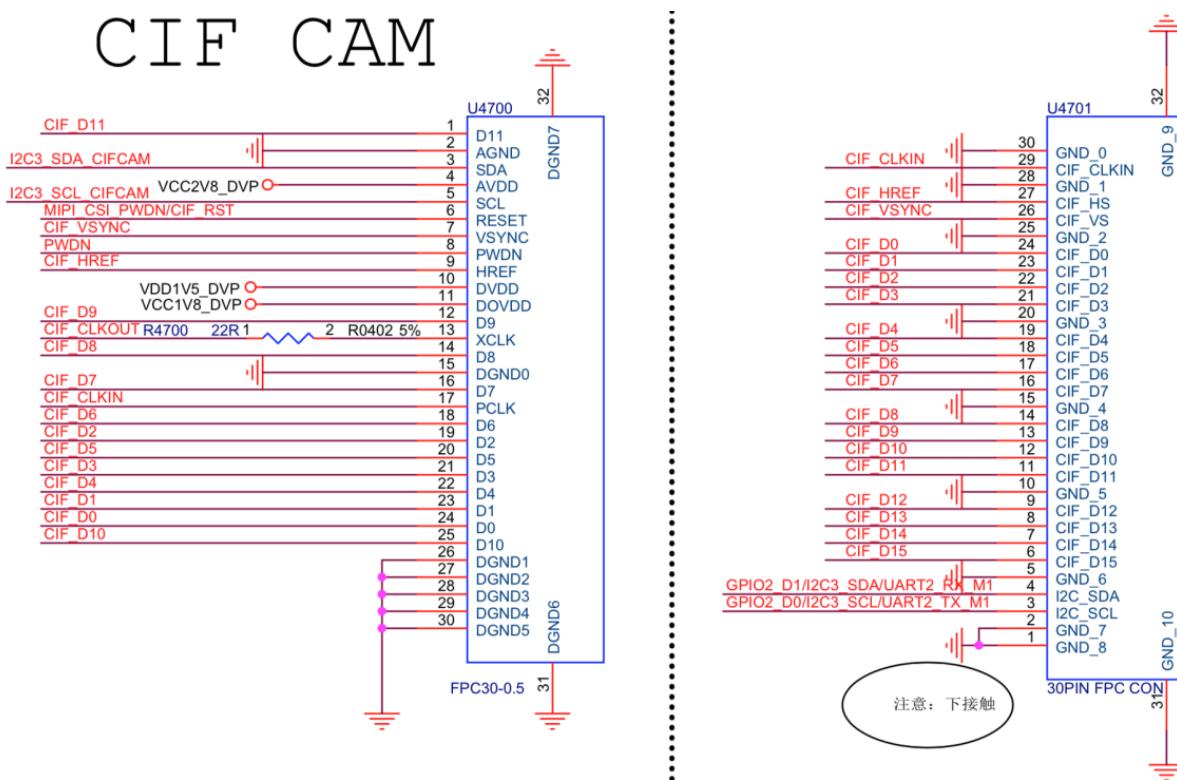


Figure 2-45 CIF/BT1120 connection circuit

2.3.5 Camera circuit

- **2.3.5.1 USB CAMERA**

Please refer to USB circuit in chapter 2.3.2. For USB CAMERA design, USB CAMERA is using standard USB protocol, and we will not introduce more here.

- **2.3.5.2 MIPI CSI**

RK1808 integrates a set of MIPI-CSI input interface, SPEC V1.0 version, supporting 4lane, max speed of each Lane reaches 2G bps, built-in ISP processor.

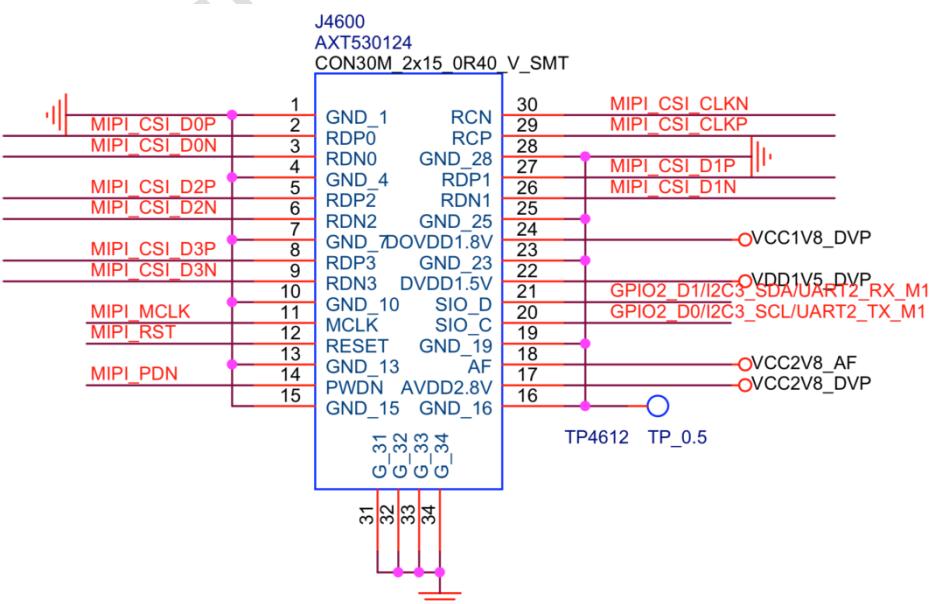


Figure 2-46 RK1808 MIPI-CSI CAMERA circuit

Note the following items when designing:

- Power of MIPI-CSI controller needs to be connected in series with 1 ohm resistor to avoid damage to the chip caused by surge.

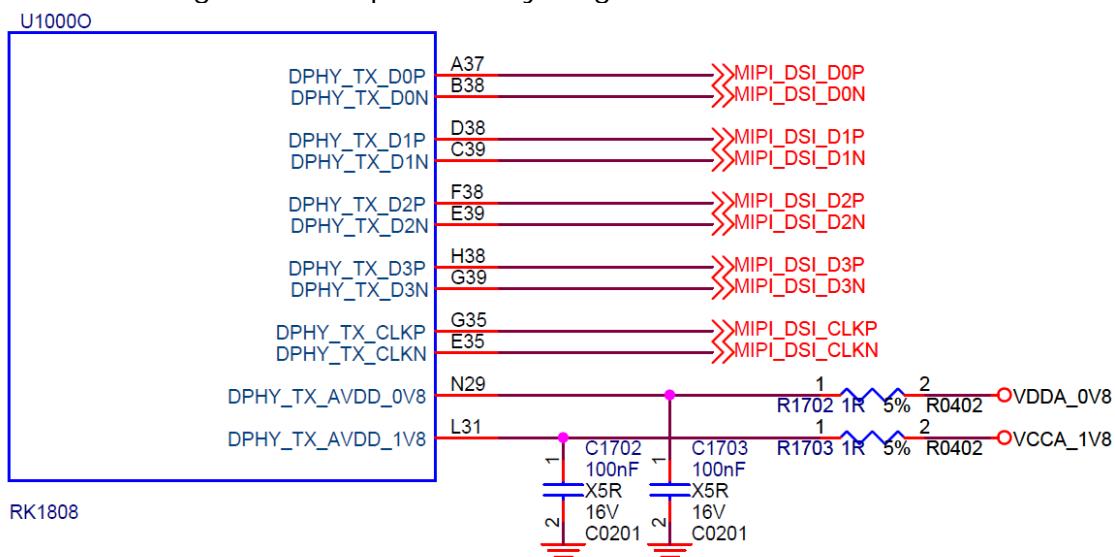


Figure 2-47 RK1808 DPHY_RX circuit

- Please place controller power decoupling capacitors close to the pins to improve MIPI-CSI performance.

● 2.3.5.3 CIF CAMERA

The circuit is shown in Figure 2-45

CIF interface power domain is VCCIO2 power supply. In actual product design, need to select the corresponding power supply according to the product camera actual IO power supply requirement (1.8V or 2.8V) and keep I2C pull up voltage level same as it, otherwise it will make camera working abnormally or can not work.

2.3.6 ADC circuit

RK1808 supports 4-channel SARADC with 10-bit resolution and sampling rate up to 1M/s.

RK1808 uses SARADC ADC_IN2 as keyboard input port and reuses it as RECOVERY mode (no need to upgrade LOADER), as shown in the follow figure. When system already downloaded image, pull down ADC2_KEY_IN to make ADC_IN2 keep 0V during system bootup, and then RK1808 enters Rockusb downloading mode. When PC identifies USB device, release the button to recover ADC_IN2 back to high voltage (1.8V), and then can start image downloading.

RK1808 SARADC sampling range is 0-1.8V and the sampling precision is 10 bits. Button array type is parallel and the input key value can be adjusted by increasing/decreasing button and adjusting divider resistance ratio to accomplish multikey input to meet with customer product requirements. Suggest any two button key values must be bigger than +/-35, that means the central voltage difference must be bigger than 123mV.

Note: If RK1808 LOG needs to be turned off during standby, the power of ADC_AVDD must also be turned off during standby. Otherwise, it will cause leakage and increase power consumption during standby.

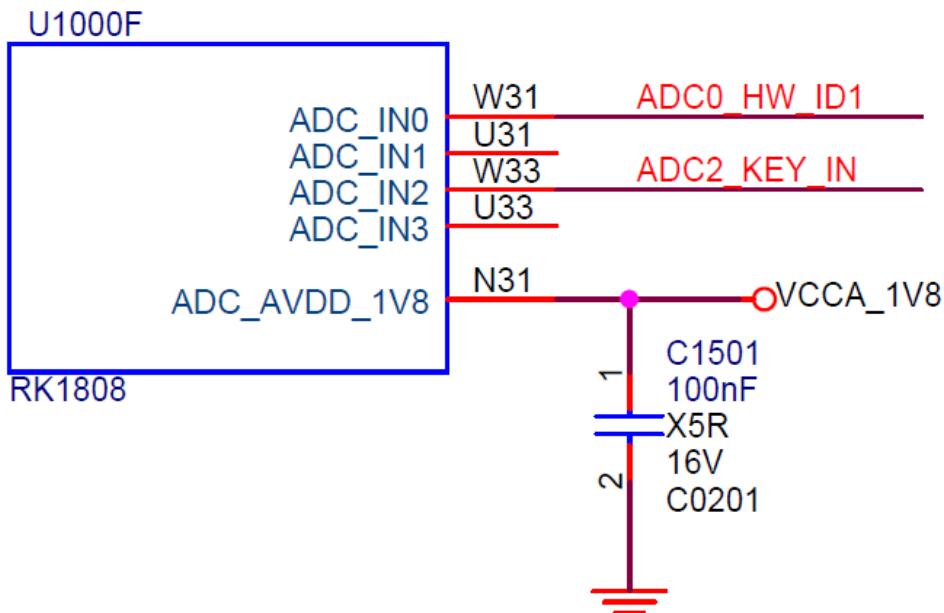


Figure 2-48 RK1808 SAR-ADC module

2.3.7 SDIO/UART/SWD JTAG circuit

RK1808 supports WIFI/BT module with SDIO 3.0 interface as shown in the figure 2-49. When using WIFI/BT modules with SDIO and UART interfaces, please note that RK1808 SDIO and UART controller power supply must keep same as the IO voltage level of the module.

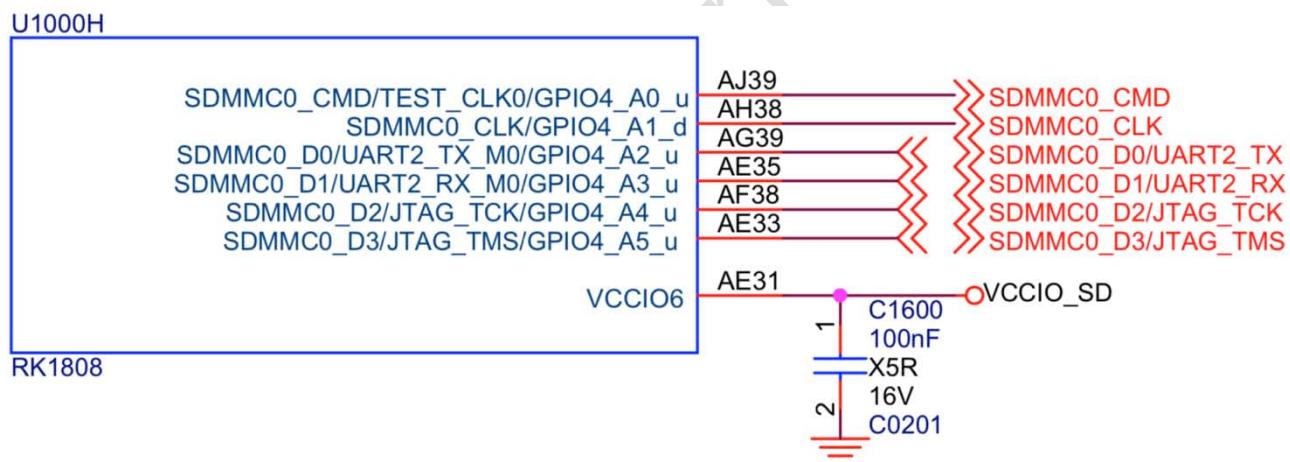


Figure 2-49 RK1808 SDIO/UART module circuit

- 2.3.7.1 SDIO

SDIO interface pull up/down and the matching design recommendations are shown as table 2-16.

Table 2-16 RK1808 SDIO0 interface design

Signal	Internal Pull up/down	Connection Method	Description(chip side)
SDIO_DQn[0:3]	pull up	in series with 22ohm resistor can be connected directly when the line is shorter.	SDIO data sending/receiving
SDIO_CLK	pull down	in series with 22ohm resistor	SDIO clock sending
SDIO_CMD	pull down	in series with 22ohm resistor	SDIO command

		can be connected directly when the line is shorter.	sending/receiving
--	--	---	-------------------

● 2.3.7.2 UART

UART2 interface pull up/down and the matching design recommendations are shown as table 2-17

Table 2-17 RK1808 UART2 interface design

Signal	Internal Pull up/down	Connection Method	Description(chip side)
UART2_RX	pull up	connected directly	UART2 data input
UART2_TX	pull up	connected directly	UART2 data output

2.3.8 Debug circuit

2.3.8.1 UART DEBUG instruction

RK1808 Debug UART2 is reused with SDMMC interface. You can connect external conversion board to convert UART to USB for debugging.

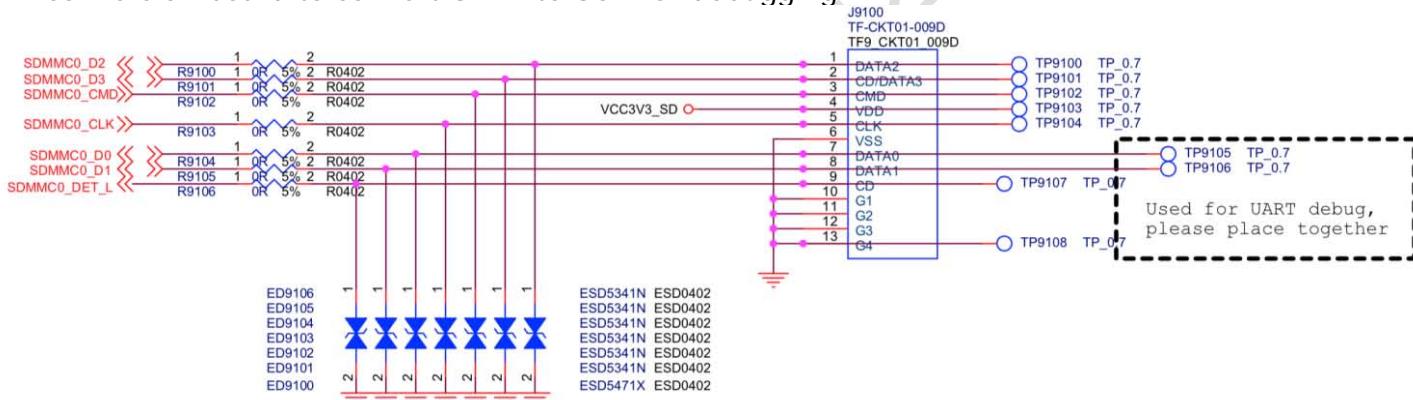


Figure 2-50 RK1808 UART2 reuse relationship

Please select the PC port which connected with the development board, select 1.5M baud rate and no need to select flow control RTS/CTS. If the built-in DB-9 port on PC does not support high speed mode, take the method of USB conversion to serial port.

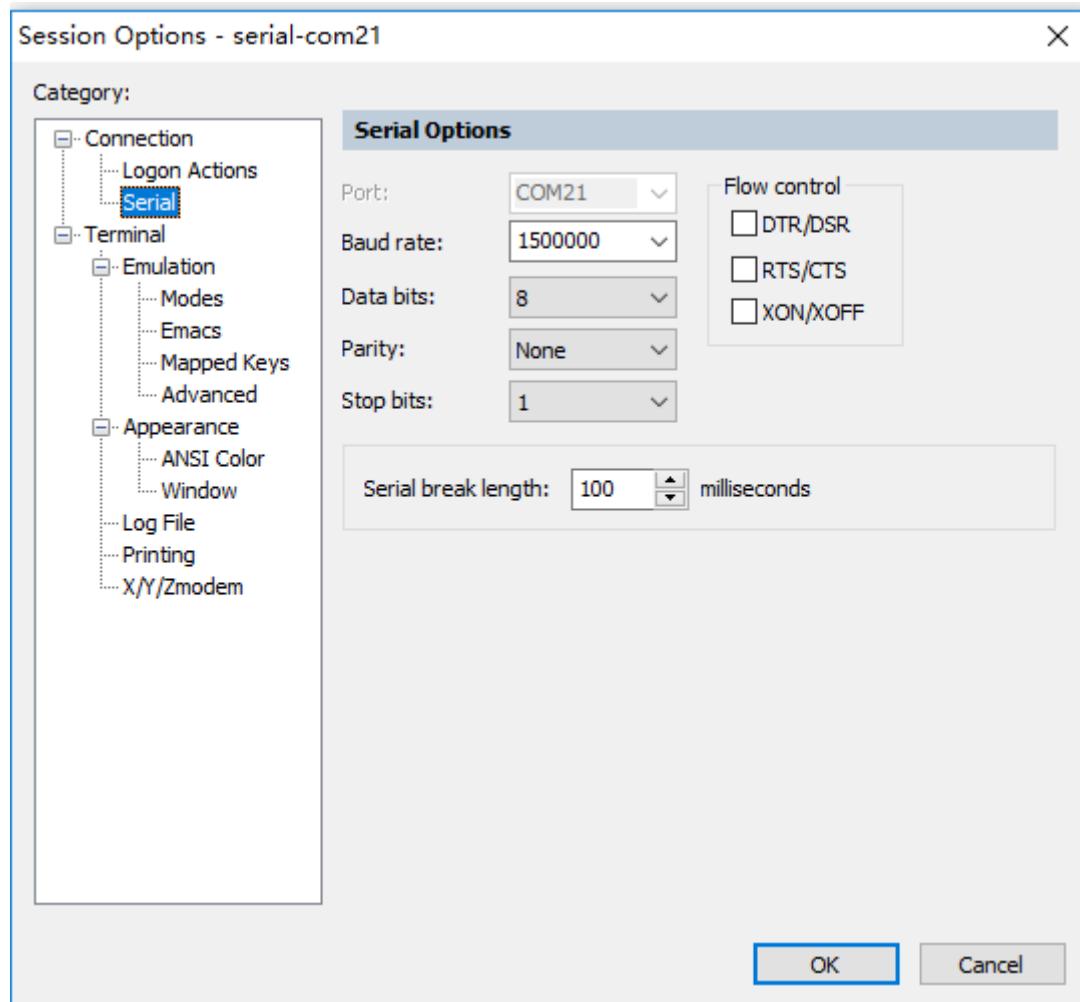


Figure 2-51 RK1808 serial port configuration

2.3.8.2 JTAG DEBUG instruction

RK1808 SWD JTAG reused with SDMMC interface, when debugging, a standard 20PIN JTAG socket can be externally connected and then connected to DSTREAM emulator for debugging the internal A35 CPU.

JTAG interface pull up/down and the matching design recommendations are shown as table 2-18

Table 2-18 RK1808 JTAG interface design

Signal	Internal Pull up/down	Connection Method	Description(chip side)
JTAG_TCK	pull up	connected directly	SWD JTAG clock input
JTAG_TMS	pull up	connected directly	SWD JTAG mode selection input

2.3.9 PCIE circuit

RK1808 supports one PCI Express V2.1 interface, supports both RC and EP two operation modes, and supports up to 2 lanes. Each lane supports 2.5G or 5G data transmission.

PCIE interface reused with USB3.0 interface, and only PCIE or USB3.0 can be used at the same time.

PCIE module circuit is as follows:

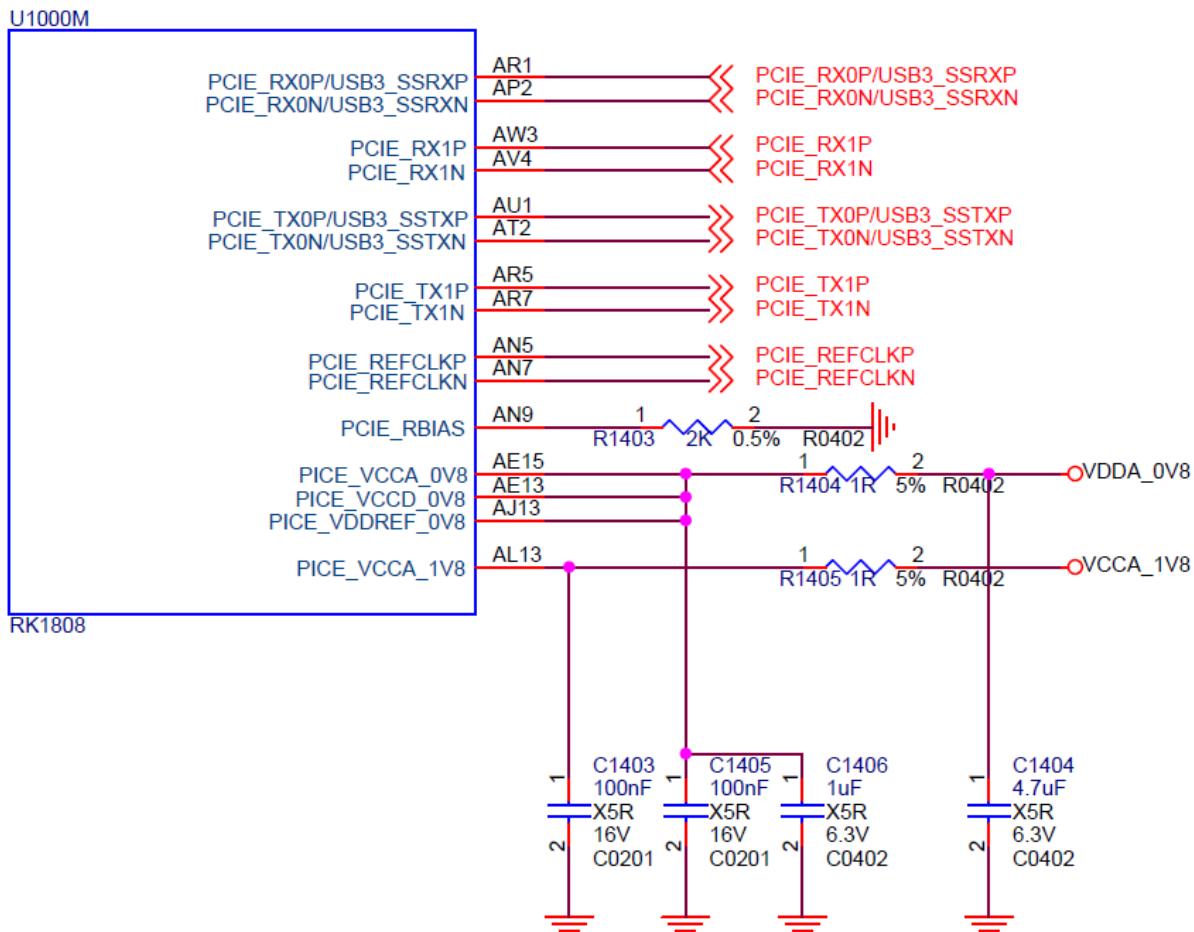


Figure 2-52 RK1808 PCIE/USB3.0 module circuit

RK1808 PCIE is used as EP interface circuit is as follows

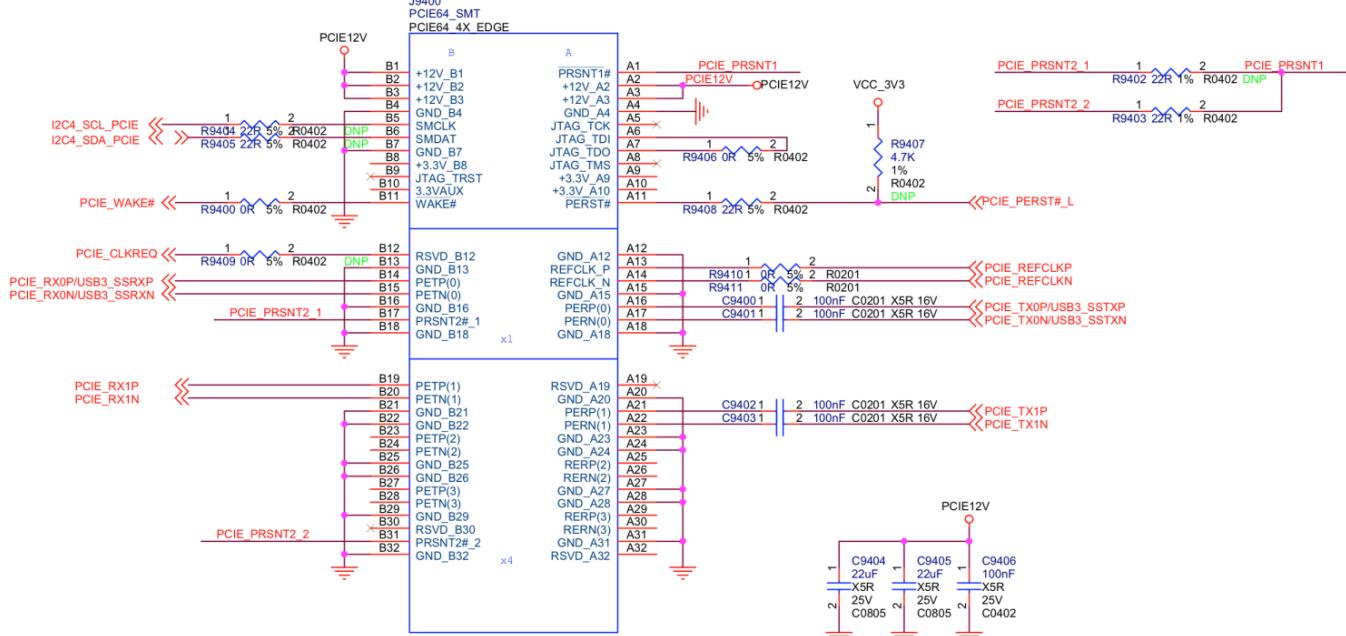


Figure 2-53 PCIE is used as EP interface circuit

RK1808 PCIE is used as RC interface circuit is as follows:

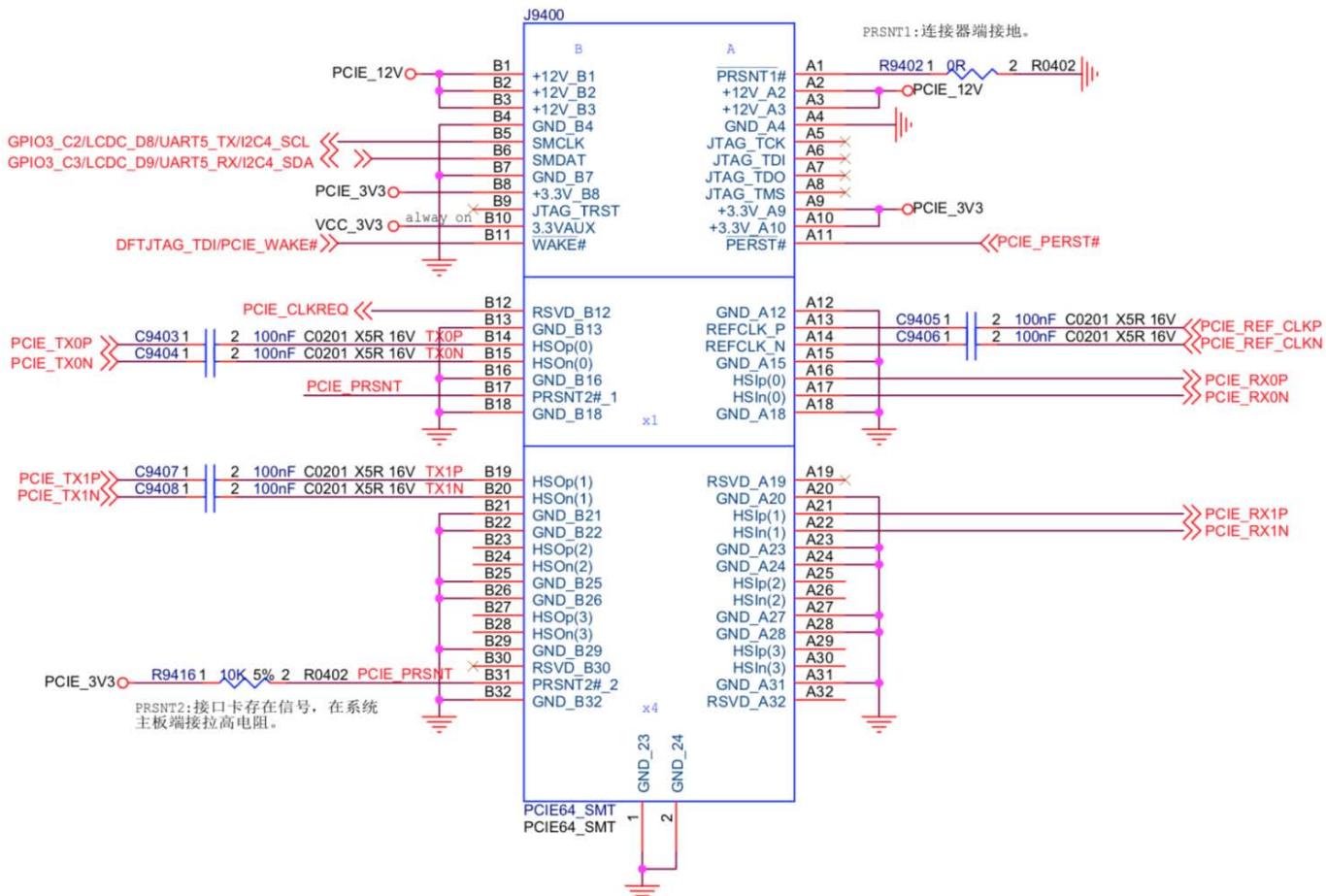


Figure 2-54 PCIE is used as RC circuit

PCIE design notes:

PCIE_PERST/PCIE_CLKREQN/PCIE_WAKE three signal networks in RK1808 MUX to M0 (PMUIO1) and M1 (PMUIO2), in RK1808 solution, PMUIO1 power is set to 1.8V, PMUIO2 power is set to 3.3V; PCIE peripheral signal requires a 3.3V power domain, so in RK1808 solution, these three pins can only be connected to the signal on M1 (PMUIO2) and cannot be connected to M0 (PMUIO1).

Circuit is as follow:

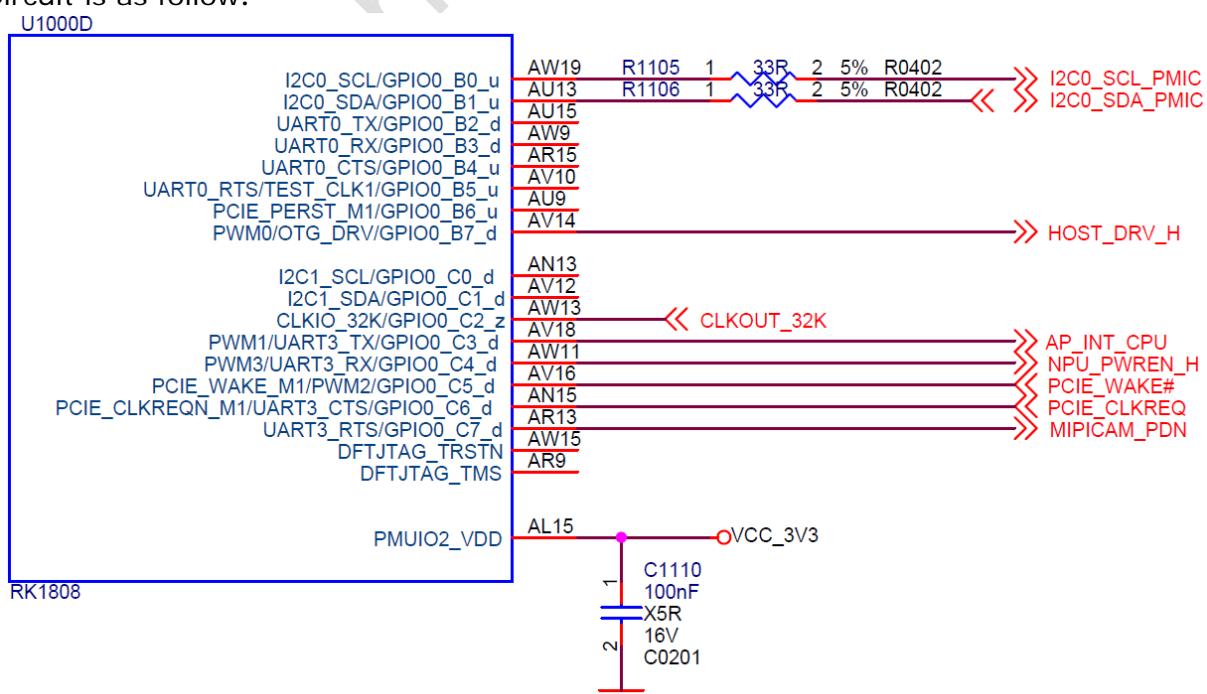


Figure 2-55 PCIE control signal

- In order to avoid damage to the chip caused by surge, 0.8V/1.8V power of the controller needs 1ohm resistor in series.

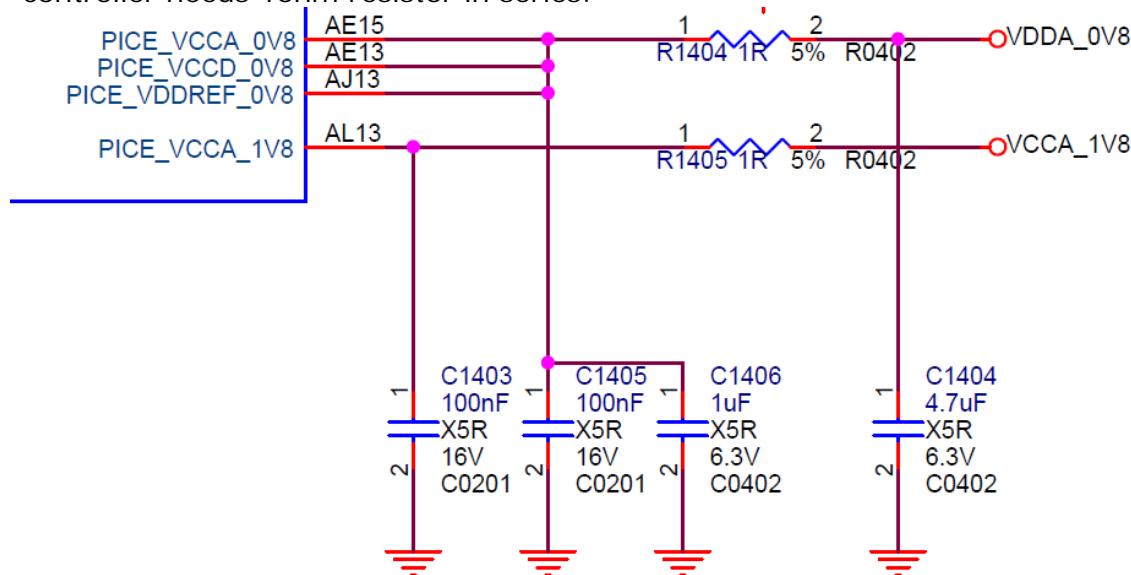


Figure 2-56 RK1808 USB3.0/PCIE controller power prevents surge

2.3.10 RK1808+AP interconnection

When RK1808 is used as a slave device, there are three connection methods for interconnection with AP.

(1) USB2.0+USB3.0+GPIOX2 connection mode: USB2.0 is used to download RK1808 firmware, USB3.0 is used to transfer big data, and GPIO is used to detect sleep and interrupt communication.

(2) USB2.0+MIPI+GPIOX2 connection mode: USB2.0 is used to download RK1808 firmware, MIPI is used to transfer big data, and GPIO is used to detect sleep and interrupt communication.

(3) USB2.0+PCIE connection mode: USB2.0 is used to download RK1808 firmware. PCIE is used to transmit big data, detect sleep and interrupt communication.

Above 1 and 2 connection methods are recommended.

Chapter 3. Thermal design suggestion

3.1 Thermal simulation result

Aiming at RK1808 FCCSP420 Pin package, based on EVB 6 layers PCB and JEDEC standard PCB, use Finite Element Modeling to get the thermal resistance simulation report. This report is achieved based on JEDEC 2S2P standard, but the system design and environment may be different from JEDEC 2S2P standard, need to analyze according to the application condition.



Note

Thermal resistance is the reference value when there is no heat sink on PCB. The detailed temperature is related with the single board's design, size, thickness, material and other physical factors.

3.1.1 Result overview

The thermal resistance simulation result is as below:

Table 3-1 RK1808 Thermal resistance simulation result

Package (FCCSP)	Power (W)	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)
EVB PCB		20.71	10.66	1.94

3.1.2 PCB description

The PCB structure of thermal resistance simulation is shown as below table:

Table 3-2 RK1808 PCB structure of the thermal resistance simulation

EVB PCB	PCB Dimension (L x W)	153.6 x 75mm
	PCB Thickness	1.6mm
	Number of Cu Layer	6-layers

3.1.3 Terms interpretation

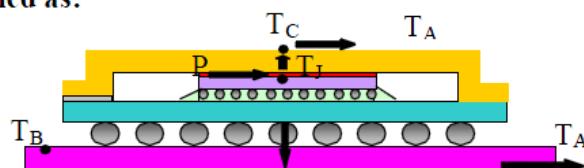
The terms of this chapter are as below;

- T_J : The maximum junction temperature;
- T_A : The ambient or environment temperature;
- T_c : The maximum compound surface temperature;
- T_B : The maximum surface temperature of PCB bottom;
- P : Total input power;

The thermal parameter can be define as following

1. Junction to ambient thermal resistance, θ_{JA} , defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P}; \quad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 3-1 θ_{JA} definition

2. Junction to case thermal resistance, θ_{JC} , defined as:

$$\theta_{JC} = \frac{T_J - T_C}{P}; \quad (2)$$

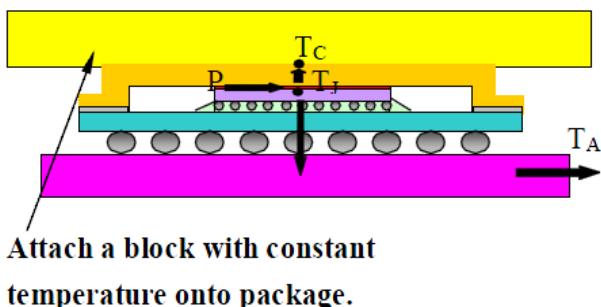


Figure 3-2 θ_{JC} definition

3. Junction to board thermal resistance, θ_{JB} , defined as:

$$\theta_{JB} = \frac{T_J - T_B}{P}; \quad (3)$$

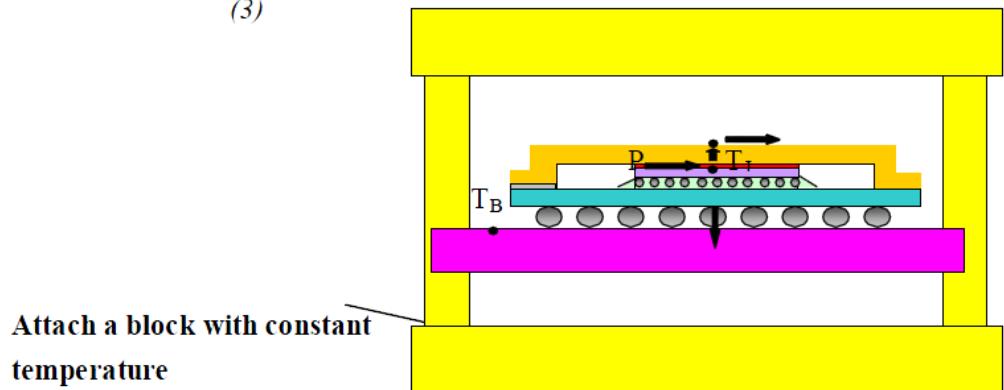


Figure 3-3 θ_{JB} definition

3.2 Thermal control method inside the chip

3.2.1 Thermal control strategy

In Linux kernel, it defines one set of thermal control frame Linux Generic Thermal System Drivers. It can control the system temperature through different strategies. Currently the following 3 strategies are commonly used:

- Power_allocator: Introduce PID (percentage-integral-differential) control to dynamically allocate power for modules according to current temperature, and convert power to frequency, so as to achieve the effect of limiting the frequency according to temperature.
- Step_wise: Limit the frequency step by step according to current temperature.
- Userspace: Do not limit frequency.

RK1808 uses T-sensor inside the chip to detect internal temperature. Use Power_allocator strategy by default and there are several working status as below:

- when temperature below the set value:
 - CPU frequency is not controlled by thermal, and is frequency-modulated according to system load;
- when temperature is over the set value:
 - Temperature tendency goes up, start to decrease frequency;
 - Temperature tendency goes down, start to increase frequency;
- If the temperature is still too high after decreasing frequency (such as poor heat dissipation), firmware will trigger restart when over 115 degrees. If the chip

temperature over 120 degrees caused by failing to restart due to deadlock or other reasons, it will trigger otp_out inside the chip for PMIC to power off directly or reset system by CRU. Please refer to chapter 2.2.5.1 for detailed operations.

**Note**

Temperature tendency is achieved by comparing the two values captured adjacently. When the device temperature is not over the threshold value, capture the temperature every 1 second; when the device temperature is over the threshold value, capture the temperature every 20 ms and limit the frequency.

3.2.2 Temperature control configuration

RK1808 SDK provides separate thermal control strategies for CPU and GPU. Please refer to "Rockchip thermal development guide" for detailed configuration.

Chapter 4. ESD/EMI protection design

4.1 Overview

This chapter provides ESD/EMI protection design suggestions for RK1808 product design to help customers improve the anti-static and anti-electromagnetic interference ability of the product.

4.2 Terms interpretation

The terms of this chapter are explained as below:

- Electro-Static discharge (ESD);
- Electromagnetic Interference (EMI): Electromagnetic interference, including conduction interference and radiation interference.

4.3 ESD protection

- Ensure reasonable mold design; reserve anti ESD components for port and connectors.
- Protect and isolate the sensitive components in PCB layout.
- Try best to put RK1808 and core components in the center of PCB layout. If it is not able to put them in the center, make sure that the shielding cover has 2mm at least from the board edge and is connected to GND safely.
- PCB layout should consider function module and signal flow direction, sensitive components should be mutually independent, and it is better to isolate the areas that are easy to interference.
- Place ESD components reasonably. Generally place at the source, that is, place ESD components in the junction or electrostatic discharge.
- Components layout should be away from the board edge and have some distance from the connectors.
- PCB surface must have good GND loop and all connectors need to have good GND connection loop on the surface layer. Shielding cover should try best to connect with the surface layer GND and make as many ground holes as possible in the soldering place to connect with GND. In order to achieve this point, it is required that the connecting parts should not go through the surface, and there should not be a wide range of cutting off the copper surface in layout.
- Do not go through the surface layer edge and make as many ground holes as possible.
- Isolate signal from ground if necessary.
- Expose copper as much as possible to enhance the electrostatic discharging effect or make it convenient to add remedial measures such as foam.

4.4 EMI protection

- Electromagnetic interference has three factors: interference source, coupling channel and sensitive devices. We cannot deal with sensitive devices, so need to handle EMI from interference source and coupling channel. The best way to resolve EMI issues is to eliminate interference source. If it cannot eliminate, try to cut off coupling channel or avoid antenna effect.
- It is difficult to eliminate interference source on PCB. We can take actions such as filtering, grounding, balancing, resistance controlling, improving signal quality (eg. butt joint) etc. Generally several methods will be applied together, but the basic requirement is good grounding.
- The commonly used EMI material include shielding cover, special filter, resistor, capacitor, inductor, magnetic bead, common mode choke/magnetic ring, wave-absorbing material, spread spectrum component etc.
- The rule to select filter: if the load (receiver) is high resistance (general single port signal interface is high resistance, such as SDIO, RGB, CIF etc.), select capacitive filter components and parallel connect to circuit; if the load (receiver) is low

resistance (such as power output interface), select inductive filter components and connect to circuit in series. If using filter components, should ensure the signal quality within its SI permission range. Differential interfaces usually use the common mode choke to suppress EMI.

- The shielding measures on PCB should have good grounding, otherwise it will cause radiation leakage or form antenna effect. The shielding of connectors should comply with the relative technical standard.
- RK1808 spread spectrum can be used in modules. The degree of spread spectrum should be determined according to the requirements of the relevant parts. For details, see RK1808 Spread Spectrum Description;
- EMI has the same high requirement as ESD on layout. The ESD Layout requirements described above are mostly suitable for EMI protection. Besides, add below requirements.
 - Try best to ensure the signal integrality.
 - Differential line should be in equal length and be tight coupling to ensure the symmetry of the differential signal and minimize the disorder and clock difference of the differential signal, to avoid converting to the common mode signal which will cause EMI issues.
 - Components with metal shell such as plug-in electrolytic capacitors should avoid coupling interference signals to radiate. Also need to avoid component interference signals coupling from shell to other signal lines.

Chapter 5. Soldering process

5.1 Overview

RK1808 is a ROHS-certified product, which is a Lead-free product. This chapter regulates basic settings of temperature for each period of time when customers use RK1808 chip SMT. It mainly introduces process control when using RK1808 chip reflow soldering: mainly lead-free process and mixed process.

5.2 Terms interpretation

Terms in this chapter are explained below:

- Lead-free: Lead-free process;
- Pb-free: Pb-free process, all devices (main board, all ICs, resistors and capacitors, etc.) are lead-free devices, and lead-free solder paste is used in pure lead-free processes;
- Reflow profile: Reflow soldering
- Restriction of Hazardous Substances (ROHS): the Restriction of the use of certain hazardous substances in electrical and electronic equipment
- Surface Mount Technology (SMT);
- Sn-Pb: Sn-Pb mixing process refers to use of lead solder paste and a mixed soldering process with both lead-free BGA and lead IC

5.3 Reflow soldering requirements

5.3.1 Solder composition requirements

The ratio of Solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerating temperature is 2~10°C, it should be warmed at room temperature before use, It will take 3~4 hours to warm-up and need to make a record.

The solder paste needs to be stirred before brushing, stirred by hand for 3 to 5 minutes or mechanically stirred for 3 minutes. After being stirred, it is naturally turbulent.

5.3.2 SMT profile

Since RK1808 chips are made of environmental protection materials, Pb-Free process is recommended. The reflow profile shown below is only recommended for JEDEC J-STD-020E process requirements, and customers need to adjust according to actual production conditions.

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Figure 5-1 Standard for heat resistance of lead process device packages

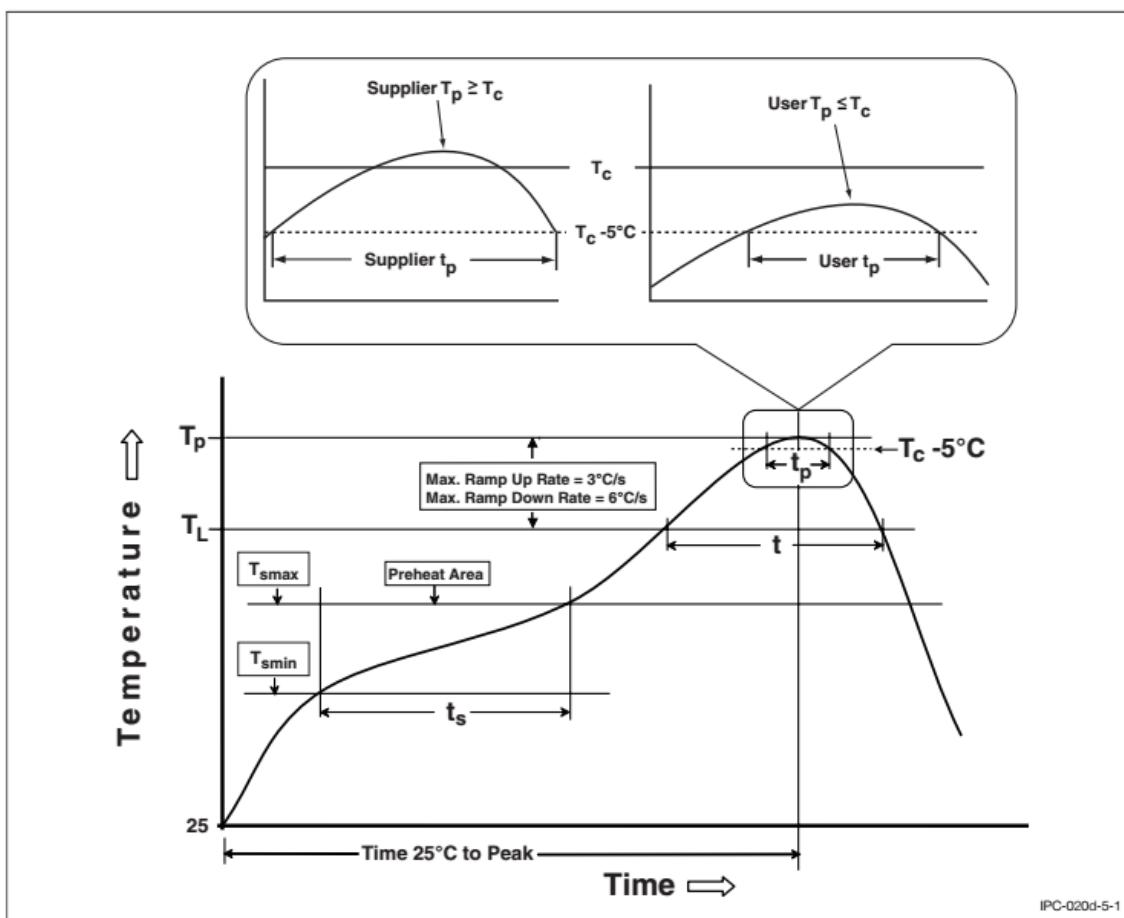
Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 5-2 Standard for heat resistance of lead-free process device packages

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Figure 5–3 Classification of reflow soldering profile



IPC-020d-5-1

5.3.3 SMT recommendation profile

The SMT profile recommended by RK is shown in Figure 5-5

Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp \leq 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above \geq 217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow \leq 10°C	Substrate MAX Temperature \leq 260°C Die Peak Temperature \leq 300°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above \geq 217°C spec's met.	PCB land/pad temperature needs to be at 100 – 130° \pm 5°C when removing board from rework machine bottom heater at end of component removal operation or \leq 80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

Figure 5-5 Lead-free reflow soldering process recommended profile parameters

Chapter 6. Packages and Storage Conditions

6.1 Overview

This chapter introduces the storage and directions for use of RK1808 to ensure the safety and correct use of products.

6.2 Terms interpretation

Terms in this chapter are explained below:

- Desiccant: a material used to adsorb moisture
- Floor life: the maximum time products are allowed to be exposed to environment, from before unpacking moisture barrier to reflow soldering;
- Humidity Indicator Card(HIC): humidity indicator card;
- Moisture Sensitivity Level(MSL)
- Moisture Barrier Bag(MBB)
- Rebake
- Solder Reflow
- Shell Life
- Storage environment

6.3 Moisture Barrier Bag

The dry vacuum packaging material of product is as follows:

- Desiccant;
- Six-point humidity card;
- Moisture-proof belt, aluminum foil, silver opaque, mark with moisture sensitivity level;



Figure 6-1 Chip dry vacuum packaging

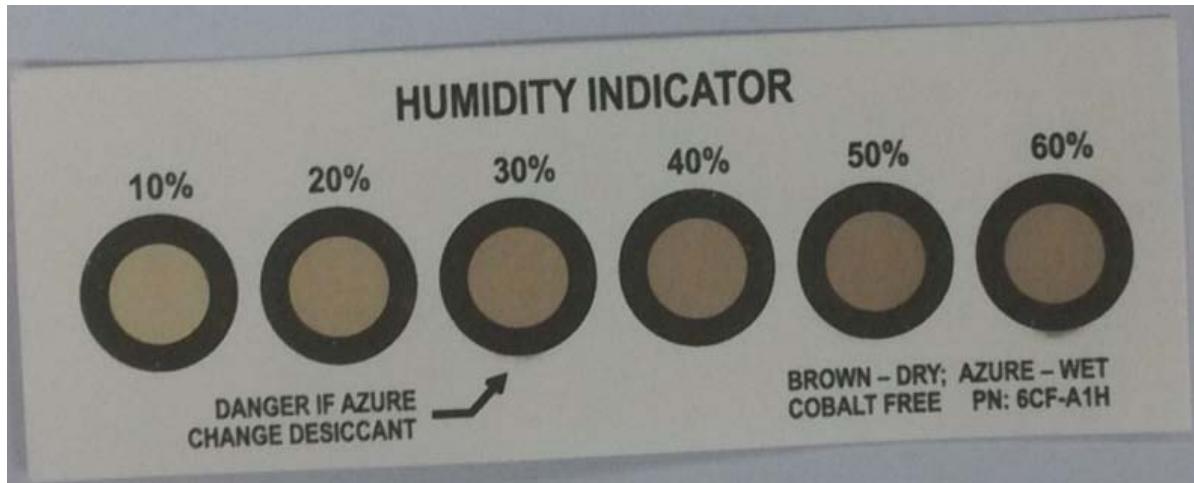


Figure 6-2 Six-point humidity card

6.4 Products storage

6.4.1 Storage environment

Products are stored in a vacuum packages and can be stored for up to 12 months with environment temperature $\leq 40^{\circ}\text{C}$ and a relative humidity $< 90\%$.

6.4.2 Exposure time

Under ambient conditions $< 30^{\circ}\text{C}$ and humidity 60%, please refer to Table 6-1 below.

RK1808 chip has an MSL rating of 3 and is very sensitive to humidity. If the chip is not used in time after unpacking, and if it is not baked and directly SMT after being left for a long time, there will be a high probability of chip failure.

Table 6-1 Moisture Sensitivity Levels (MSL)

MSL level	Exposure time	
	Factory environmental conditions: $\leq 30^{\circ}\text{C} / 60\% \text{RH}$	
1	Unlimited at $\leq 300^{\circ}\text{C} / 85\% \text{RH}$	
2	1 year	
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use, must be reflowed within the time limit specified on the label.	

6.5 Use of moisture sensitive products

After RK1808 chips packages are opened, the following conditions must be met before reflow soldering:

- Continuous or cumulative exposure time is within 168 hours, and factory environment is $\leq 30^{\circ}\text{C} / 60\% \text{RH}$;
- Stored in $< 10\% \text{RH}$ environment;

Chips must be baked to remove internal moisture under the following conditions to avoid delamination or popcorn problems during reflow:

- When humidity indicator card is at $23 \pm 5^{\circ}\text{C}$, $> 10\%$ dots have changed color. (Please refer to humidity indicator cards for color change);
- Does not meet the specifications of 2a or 2b;

Please refer to Table 6-2 below for the time for chip re-baking:

Table 6-2 RK1808 Re-bake reference table

Package Body	MSL	High Temp Bake @125°C + 10/-0°C		Medium Temp Bake @90°C +8/-0°C		Low Temp Bake @40°C +5/-0°C	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness ≤1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days



Note

*The table shows the minimum baking time necessary after damp.
Re-baking prefers low-temperature baking.*