AHB to APB Bridge Design

Project Report

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UNDER THE GUIDANCE OF:

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Abstract :

The AHB to APB Bridge project is a critical component in modern System-on-Chip (SoC) design, enabling seamless communication between high-performance and peripheral modules within the same integrated circuit. This project focuses on the design, development, and integration of a robust and efficient bridge to facilitate data and control signal transfers between the AHB and APB buses.

The AHB to APB bridge is a hardware module that allows AHB masters to communicate with APB slaves. The bridge is responsible for translating the AHB protocol to the APB protocol, and vice versa. This allows AHB masters to access APB peripherals without having to know the details of the APB protocol.

In this project, I have developed synthesizable design of AHB2APB bridge and testbench for the functional verification of the same in Verilog. The software tools that I have used are ModelSim - Intel FPGA Starter Edition 17.1.0.590

AMBA:-

AMBA (Advanced Microcontroller Bus Architecture) is a freely-available, open standard for the connection and management of functional blocks in a system-onchip (SoC). It facilitates right-first-time development of multi-processor designs, with large numbers of controllers and peripherals. An AMBA-based microcontroller typically consists of a highperformance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, onchip

memory and other Direct Memory Access (DMA) devices reside. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers. Also located on the high performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located.

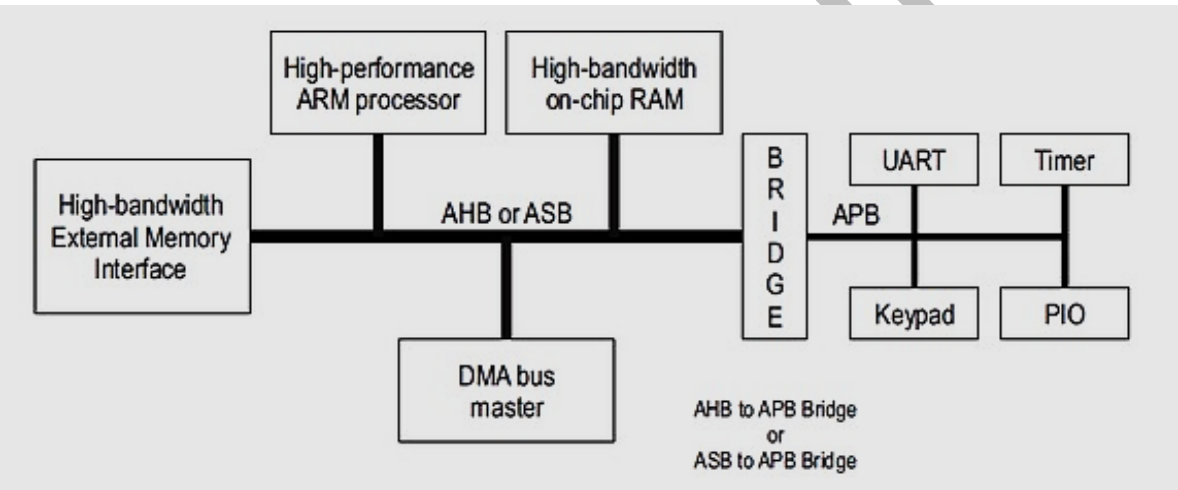


Fig.1. AMBA based AHB2APB Bridge

INTRODUCTION:-

In contemporary System-on-Chip (SoC) designs, integrating various components with distinct functionalities is a common practice. The Advanced Microcontroller Bus Architecture (AMBA) standard, developed by ARM, provides a framework for connecting these components, facilitating efficient communication and data transfer. One of the key challenges in SoC design is bridging the communication gap between the high-performance Advanced High-Performance Bus (AHB) and the low-power Advanced Peripheral Bus (APB). This project addresses this challenge by designing and implementing an AHB to APB Bridge.

This project has several blocks and each block has its respective work. In this project, the bridge samples the data and addresses and it sends to the APB controller and fulfills the transaction of data.

PROJECT BLOCKS:-

1)AHB_SLAVE_INTERFACE

2)APB_CONTROLLER

3)BRIDGE_TOP

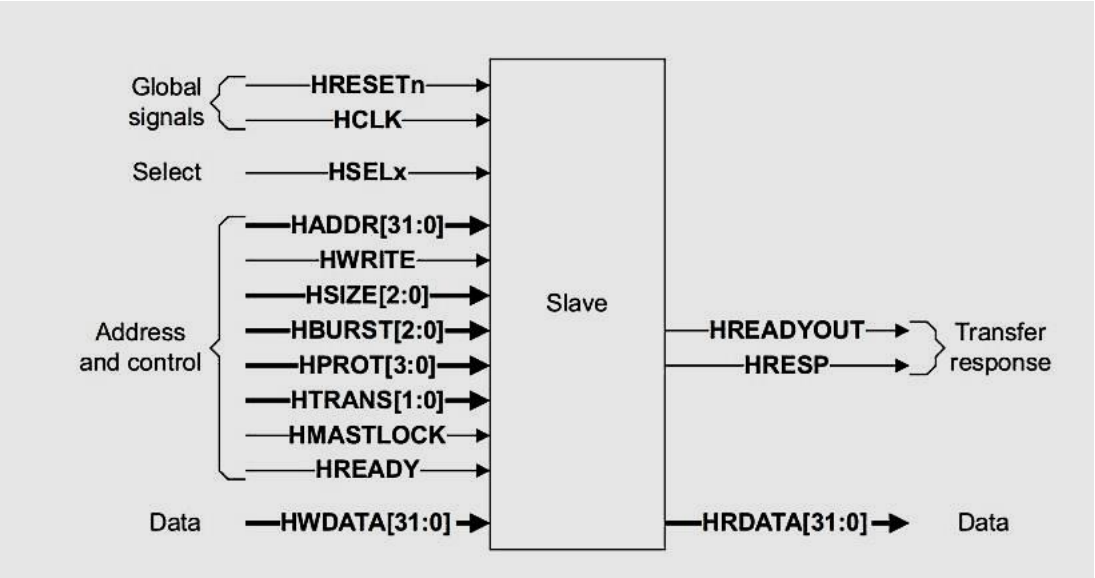
4)AHB_MASTER

5)APB_INTERFACE

6)TOP_TB

1)AHB_SLAVE_INTERFACE:-

DIAGRAM: -



Functionality:-This block is responsible for interfacing with the AHB bus. It acts as a slave to the AHB master, receiving transaction requests from the AHB side. It is the entry point for AHB transactions into the bridge.

Functionalities:-

Accept incoming AHB transactions.

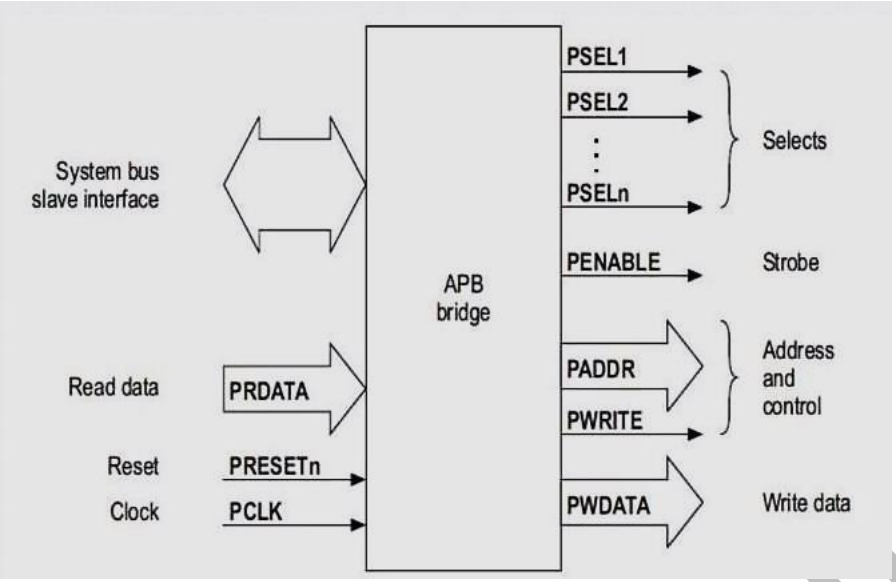
Decode the AHB address and determine the target peripheral on the APB side.

Translate AHB control signals into a format compatible with the bridge.

Handle read and write transactions from the AHB side.

2)APB_CONTROLLER:-

DIAGRAM: -



Functionality:- The APB Controller manages the interface between the bridge and the APB bus. It acts as a master on the APB bus, initiating transactions to access peripherals. It translates AHB transactions into APB transactions.

Functionalities:-

Generate and send APB transactions to the target peripheral.

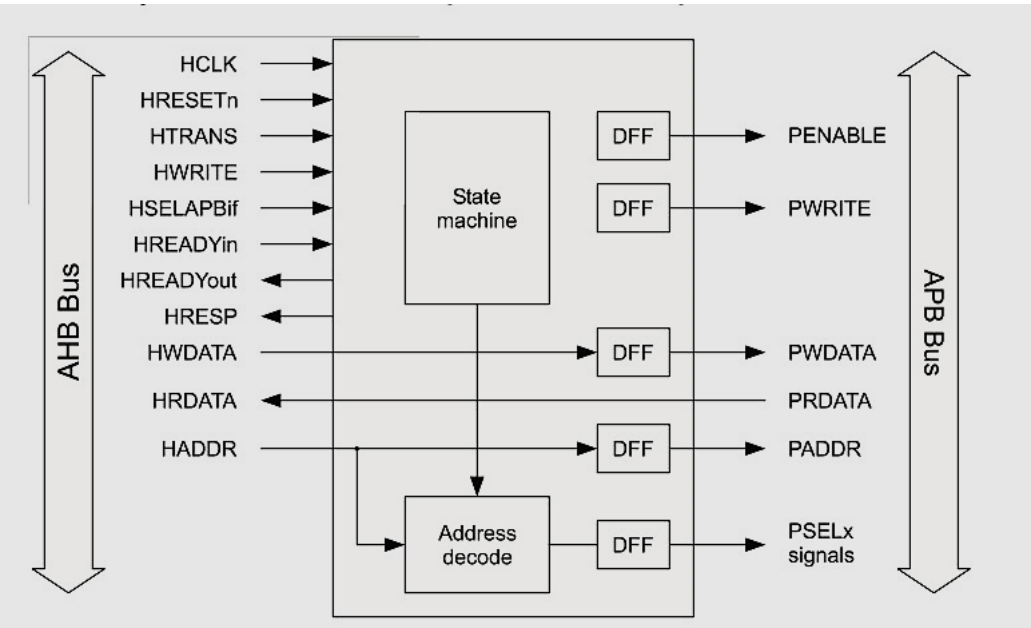
Manage the APB bus protocol, including control signals like PSEL, PENABLE, PWRITE, etc.

Handle APB read and write data transfers.

Provide acknowledgment and error reporting for transactions.

3)BRIDGE_TOP:-

DIAGRAM:-



Functionality: The bridge Top block is the central control unit that coordinates the overall operation of the AHB to APB Bridge. It manages data flow between the AHB Slave Interface and the APB Controller. It also handles arbitration, if necessary, and ensures proper transaction flow.

Functionalities: -

Coordinate the translation of AHB transactions into APB transactions.

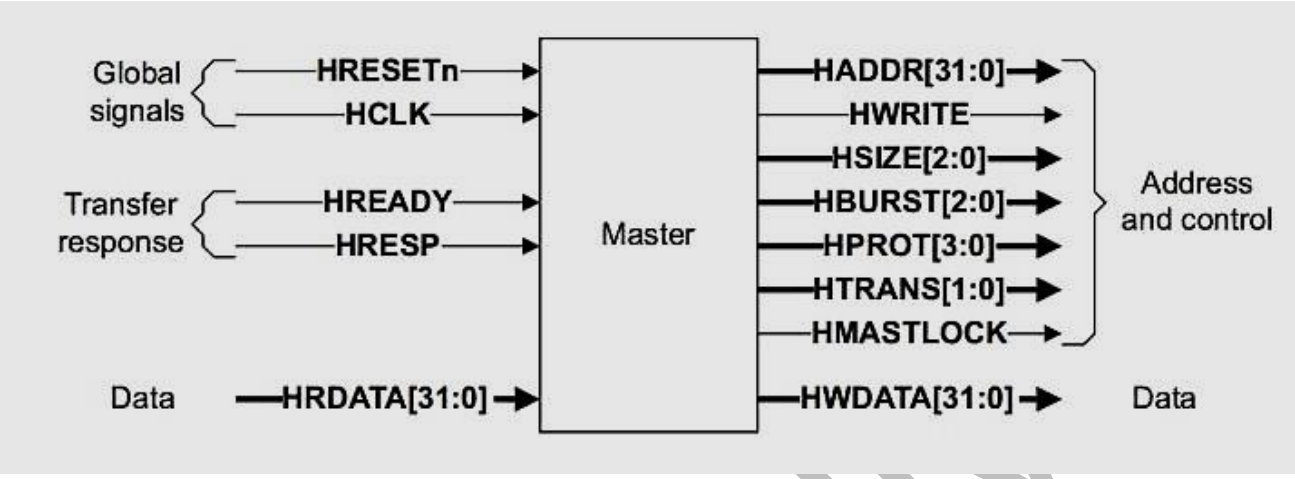
Manage the synchronization of data between AHB and APB domains.

Handle address decoding, directing transactions to the appropriate peripheral on the APB bus.

Arbitrate transactions when multiple masters on the AHB side are involved.

4)AHB_MASTER BLOCK:-

DIAGRAM:-



Functionality:-

The AHB Master block represents a component that acts as an AHB bus master. It initiates AHB transactions to access the AHB to APB Bridge.

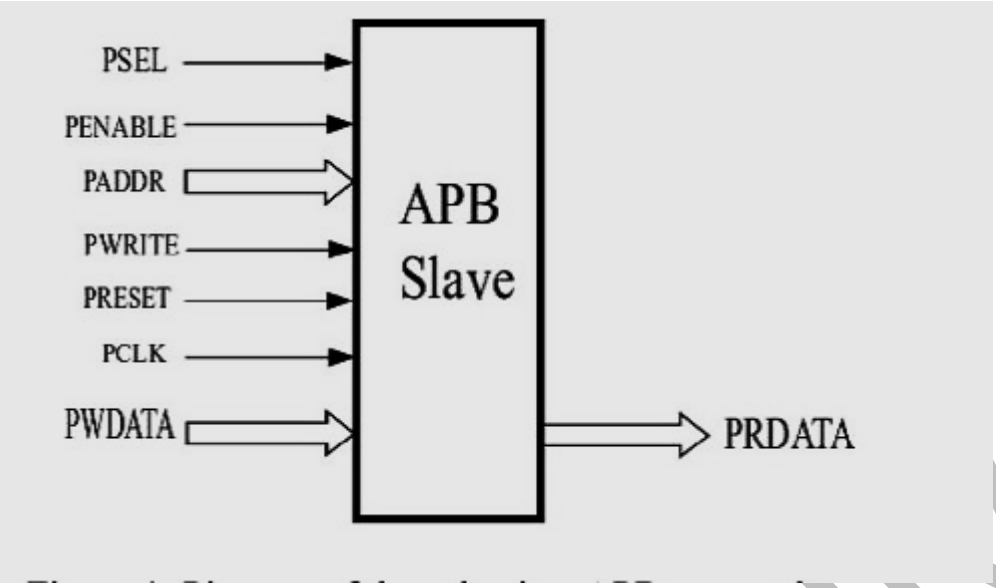
Functionalities:-

Generate AHB transactions to access peripherals or initiate communication.

Send AHB read and write requests to the AHB Slave Interface of the bridge.

5)APB_INTERFACE:-

DIAGRAM:-



APB Interface Functionality:-

The APB Interface block acts as the entry point to the APB bus, interfacing with the APB peripherals.

Functionalities:-

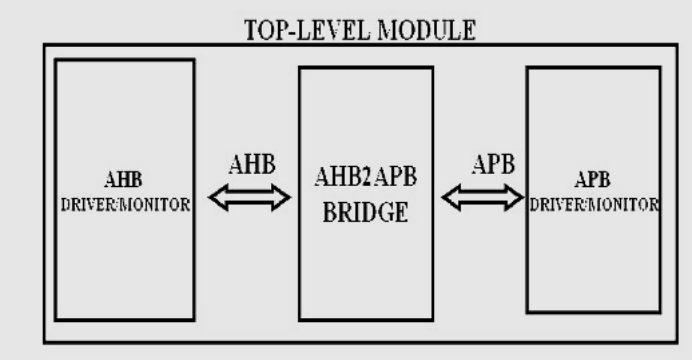
Provide an interface to APB peripherals for receiving APB transactions from the APB Controller.

Handle APB read and write operations for the attached peripherals.

Manage the APB peripheral's responses to transactions.

6)TOP_TB:-

DIAGRAM :



The top testbench is an essential component in the process of verifying and testing the AHB to APB Bridge design. It is a simulation environment that allows engineers to test the functionality, performance, and behaviour of the bridge under various scenarios and conditions without the need for physical hardware. Here's some information about the top testbench:

Purpose:-

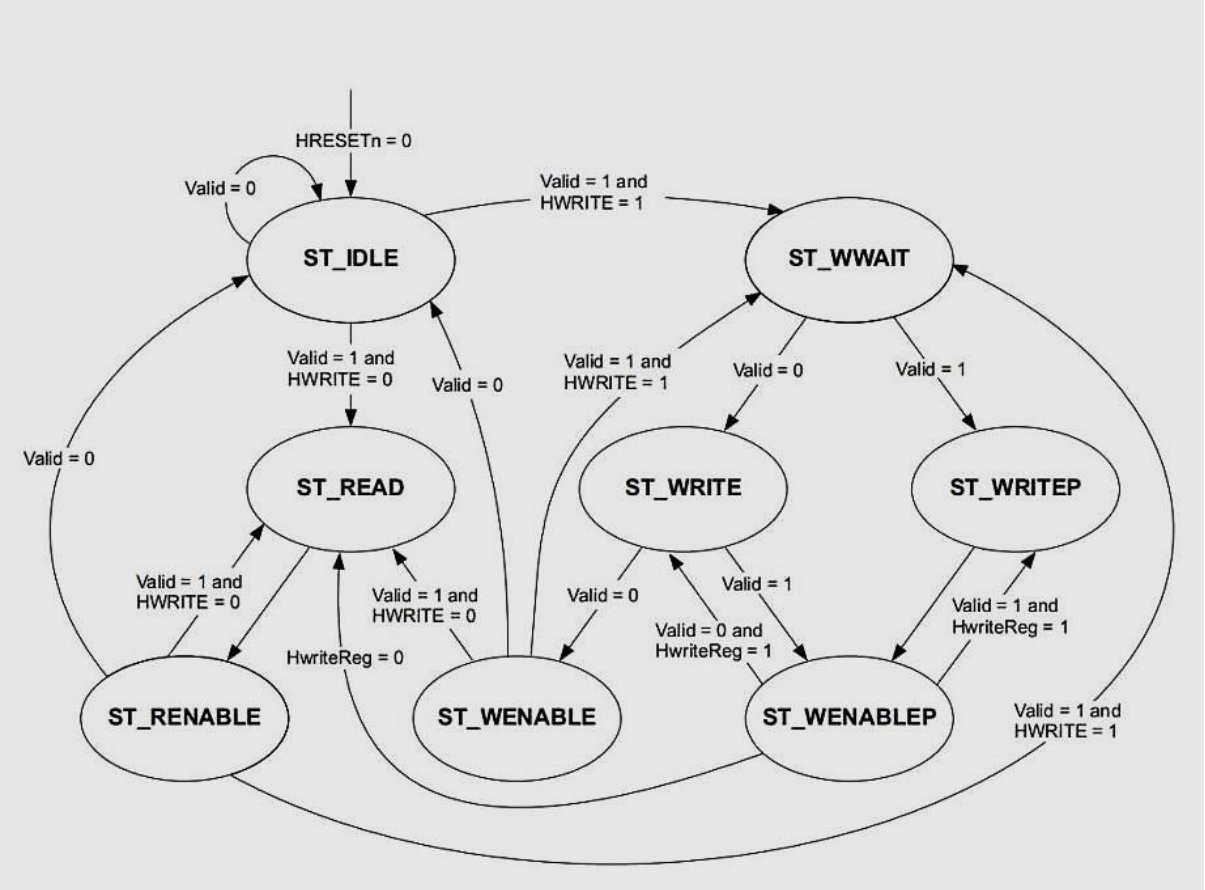
The top testbench is designed to verify that the AHB to APB Bridge functions correctly in a simulated environment.

It helps ensure that the bridge conforms to the AMBA standard and meets the project's objectives.

These blocks work in coordination to enable the AHB to APB Bridge to facilitate communication between the high-speed AHB bus and the low-speed APB bus. The AHB Slave Interface and APB Controller act as the interfaces to their respective buses, the Bridge Top controls and manages transaction flow, and the AHB Master and APB Interface allow the bridge to interact with other

components in the SoC. Together, they ensure efficient and reliable data transfer between different components in the system.

APB Controller State Diagram: -



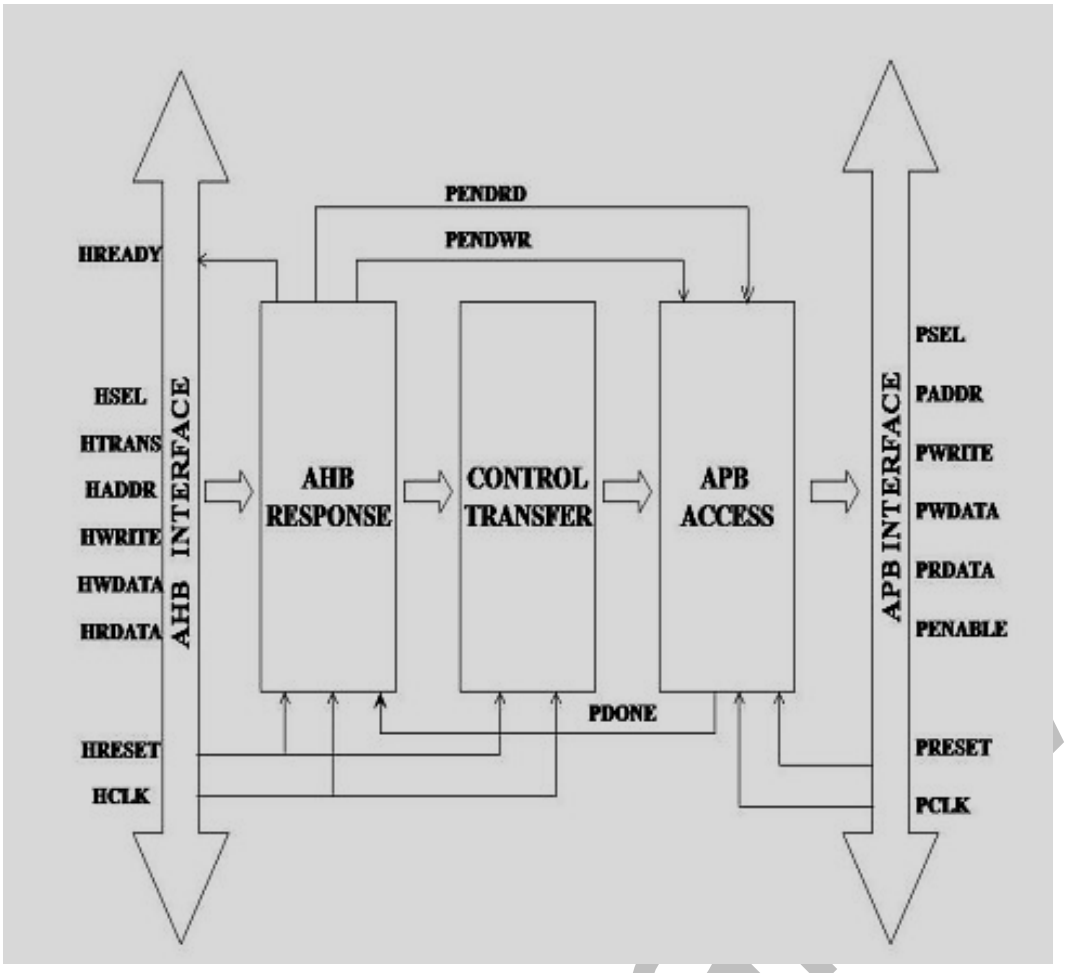
Signal Description: -

Signals	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HADDR[31:0]	Address bus	Input	The 32-bit system address bus.
HTRANS[1:0]	Transfer type	Input	This indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.

HWRITE	Transfer direction	Input	When HIGH this signal indicates a write transfer, and when LOW, a read transfer.
HWDATA[31:0]	Write data bus	Input	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HSELAPBif	Slave select	Input	Each APB slave has its own slave select signal, and this signal indicates that the current transfer is intended for the selected slave. This signal is a combinatorial decode of the address bus.
HRDATA[31:0]	Read data bus	Output	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HREADYin HREADYout	Transfer done	Input/output	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.
HRESP[1:0]	Transfer response	Output	The transfer response provides additional information on the status of a transfer. This module will always generate the OKAY response.
PRDATA[31:0]	Peripheral read data bus	Input	The peripheral read data bus is driven by the selected peripheral bus slave during read cycles (when PWRITE is LOW).
PWDATA[31:0]	Peripheral write data bus	Output	The peripheral write data bus is continuously driven by this module, changing during write cycles (when PWRITE is HIGH).
PENABLE	Peripheral enable	Output	This enable signal is used to time all accesses on the peripheral bus. PENABLE goes HIGH on the second clock rising edge of the transfer, and LOW on the third (last) rising clock edge of the transfer.

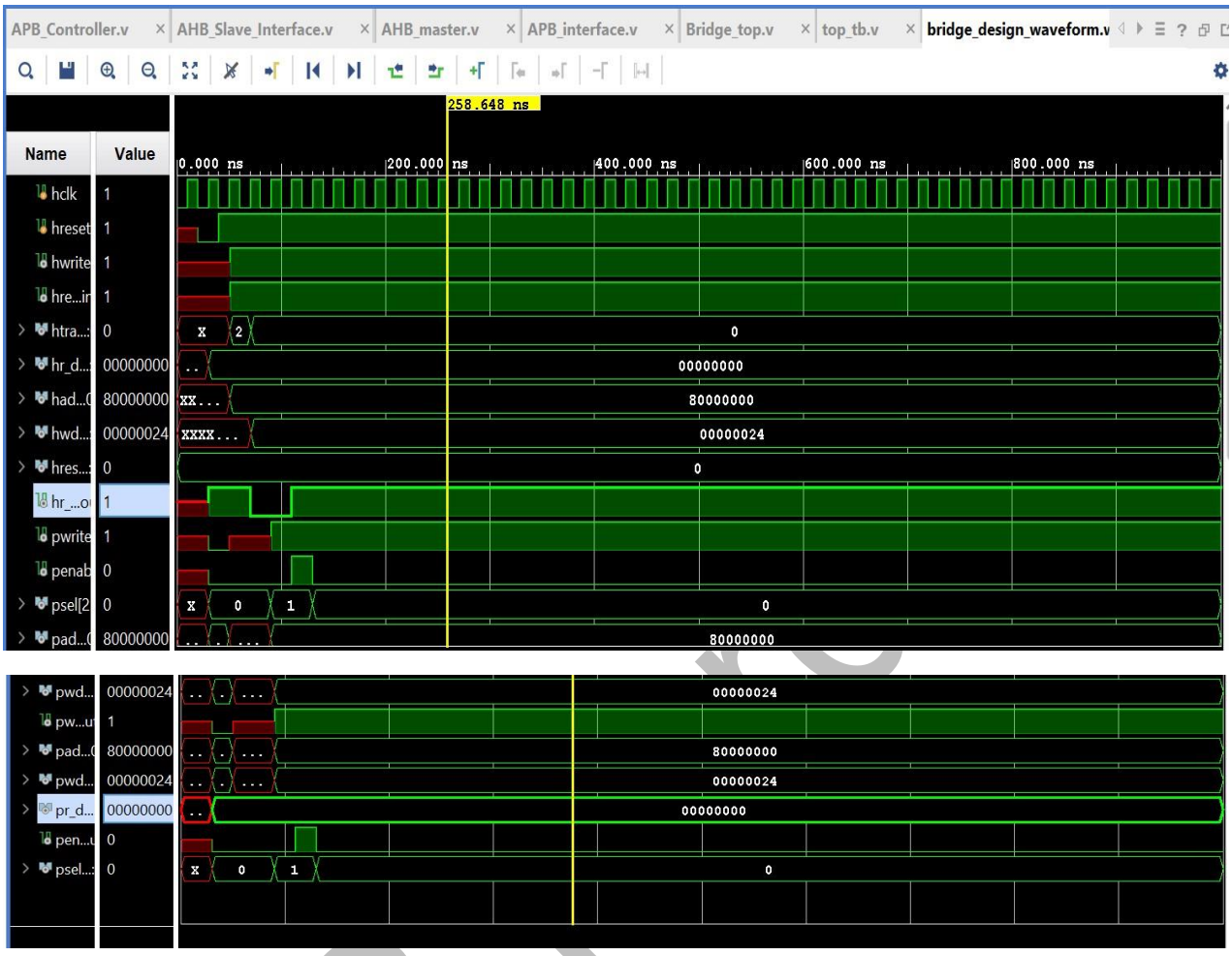
PSELx	Peripheral slave select	Output	There is one of these signals for each APB peripheral present in the system. The signal indicates that the slave device is selected, and that a data transfer is required. It has the same timing as the peripheral address bus. It becomes HIGH at the same time as PADDR, but will be set LOW at the end of the transfer.
PADDR[31:0]	Peripheral address bus	Output	This is the APB address bus, which may be up to 32 bits wide and is used by individual peripherals for decoding register accesses to that peripheral. The address becomes valid after the first rising edge of the clock at the start of the transfer. If there is a following APB transfer, then the address will change to the new value, otherwise it will hold its current value until the start of the next APB transfer.
PWRITE	Peripheral transfer direction	Output	This signal indicates a write to a peripheral when HIGH, and a read from a peripheral when LOW. It has the same timing as the peripheral address bus.

OVERALL ARCHITECTURE OF THE PROJECT:-

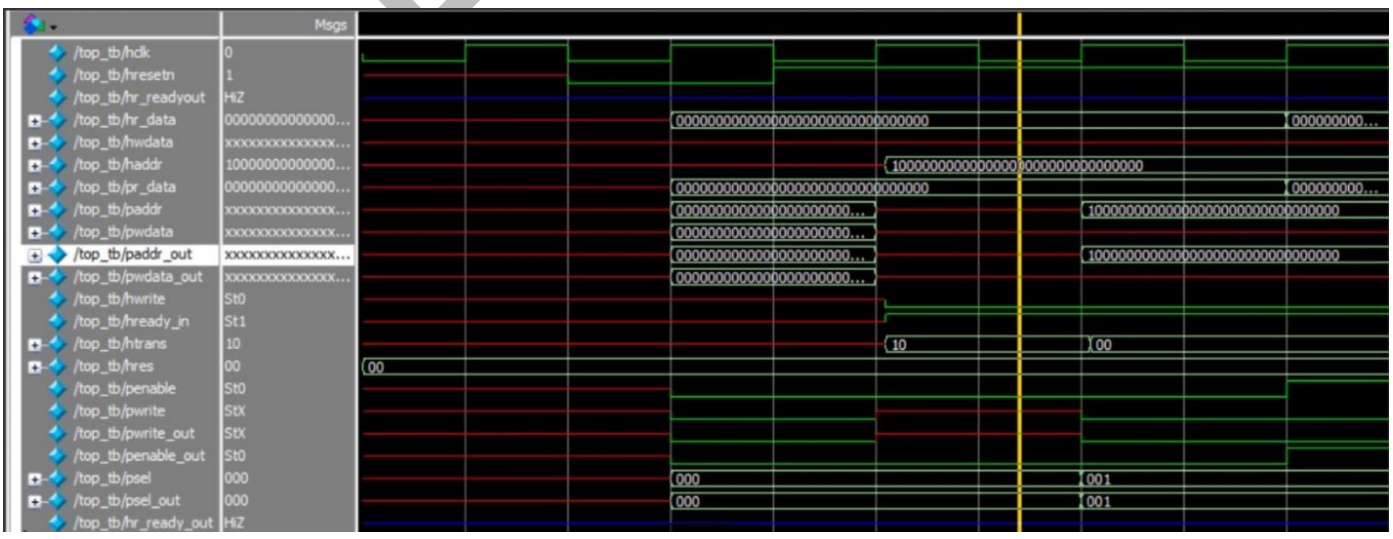


OUTPUT WAVEFORMS OF THE PROJECT: -

Single_Write transfer: -



Single read transfer: -



Conclusion:-

The development of the synthesizable AHB to APB Bridge in verilog HDL was done. The HCLK and PENABLE mechanism was implemented for making it the low-power consuming system. The functional verification of the bridge was done by driving various testcases to the design for testing the features. The multimaster and multislave AHB to APB bridge is one of the future scope.