CSE 206
DIGITAL LOGIC DESIGN SESSIONAL

Marks distribution:

Quiz	**35%**
Viva	**20%**
Report	**15%**
Experiment	**30%**

Viva:

- There will be one viva. We will announce the viva schedule two weeks prior.

Experiments:

- Each group must bring the design of circuits for the problems in an experiment to be held on that very day.

Reports:

- Students must submit one report for each group for each experiment.
- Each of the students of a group must write the reports one by one in **cyclic order** in ascending manner.
- All the reports must contain the given **top page**.
- Except for pending experiments, report of each experiment must be submitted the next week after the successful completion of that experiment.
- For late submission marks will be deducted from report.
- Report will not be accepted until successful completion of an experiment. In general, if any experiment (any part) is incomplete/ unsuccessful, the report has to be submitted after successfully finishing all the parts.

Quiz:

- One Quiz will be held at the end of the term.

References:

I. Micrprocessor Data Hand book.
II. Digital Logic and Computer Design by *M. Morris Mano*
III. Digital Design by *E. L. Johnson* and *M.A.Karim*
IV. Digital Fundamentals by *Thomas L. Floyd*
V. Switching and Finite Automata Theory by *ZVI Kohavi*

Report Top Sheet

CSE206 (Digital Logic Design Sessional)

Expt. No.

Name of the Expt.

Group No.	
Writer's Roll	
Section	
Department	
Other Group Members	
Date of Performace:	
Date of Submission:	

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 1

Topic: Implementing circuits with basic gates.

Implement the following problems.

Implement the following functions with basic gates.

1. $F(P, Q, R) = PR + \overline{Q}R$
2. $F(P, Q, R) = \underline{PR}(PQ + QR)$
3. $F(P, Q, R) = \overline{P + Q} + R$

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- Truth table.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 2

Topic: Truth tables and simplification using Boolean Algebra.

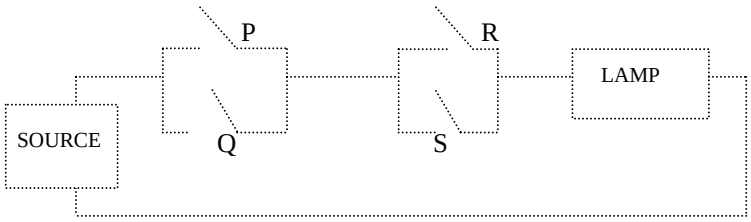
Implement the following problems.

1. Simplify the equation using Boolean algebra and implement it.

   F (P, Q, R, S) = PQR'S + P'QRS' + PQR + PQ'R'S' + PQS' + PQ'R

2. Derive the output equations for a 3-bit gray to binary code converter and implement it with required gates.

3. Deduce the truth table for the switching circuit shown below. Find the Boolean function from the truth table, minimize it and draw the logic circuit diagram.



Answer the following questions.

1. For the following logic function, find out the truth table, write down the logic expression and draw the logic circuit diagram. Simplify the logic expression as far as possible using Boolean algebra.
   F (*P, Q, R, S*) = Σ (6, 9, 13, 15)

2. There are three oscilloscopes *A, B, C* in a laboratory and you are to design an indicator circuit that will make an LED to glow when two or more of the oscilloscopes are malfunctioning. Derive the logic circuit diagram.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- Truth table.
- Required equation in minimized form with necessary steps.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 3

Topic: Truth tables and K-maps.

Implement the following problems.

1. Design and implement a circuit using gates that would take two 2-bit numbers as input and produces the sum of the inputs as its output.

2. Simplify and implement the Boolean function with gates.

   $f(V,W,X,Y,Z)=\Sigma(1,4,5,13,20,21,22,28) + d(6,9,11,12,14,29,30)$

Answer the following questions.

1. Design a circuit that takes a five bit BCD number (00 – 19) as input and produces its binary equivalent as output.

Report:

For each of the problems/questions report should the following points.

- Problem specification.
- Truth table.
- Required equation in minimized form with necessary steps.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 4

Topic: Arithmetic circuit design.

Implement the following problems.

1. Design a 1-bit full Subtractor circuit using logic gates.

2. Using basic gates design a 2-bit comparator to compare two 2-bit numbers X and Y. The circuit should provide 3 output lines to indicate X>Y, X = Y and X< Y.

Answer the following question.

1. Design a 4-bit Carry Look Ahead (**CLA**) adder circuit.

Report:
For each of the problems/questions report should cover the following points.

- Problem specification.
- Truth table.
- Required equation in minimized form with necessary steps.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 5

Topic: Circuit design using IC 7483.

Implement the following problems.

1. Design and implement an **Adder-Subtractor** circuit that would perform $P+Q$ (Addition) when a selection variable $S=0$ and would perform $P-Q$ (Subtraction) when $S=1$. Each of *P* and *Q* is a 4 bit number. Use IC 7483 and basic gates.

2. Design and implement the circuit for the following problem using XOR gates and one 7483 IC. You are not allowed use any ***inverter***.

Input	Output
00	X
01	$X+1$
10	X'
11	$X'+1$

   Here "+" means addition operation and *X* is a 4 bit number.

Answer the following questions.

1. Design a binary to BCD converter that would convert any of the number 0-19 to BCD. Use IC 7483 and basic gates.

2. Given two 3-bit binary number A ($a_2\, a_1\, a_0$) and B ($b_2\, b_1\, b_0$), design a circuit that produces the multiplication C ($c_5\, c_4\, c_3\, c_2\, c_1\, c_0$) of that two numbers using gates & Full Adder circuits.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- Truth table.(If required)
- Required equation in minimized form with necessary steps (if required).
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 6

Topic: Encoder and Decoder Circuits.

Implement the following problems.

1. Using gates design and implement a 4 to 2 priority encoder with the priority of data bit input as given below:
   (2,0,1,3 given in order of descending priority).

2. Implement the function given below using two 3 × 8 decoders and gates as required.

$$a)\ f = \sum(2,4,6,8,14)$$

$$b)\ f = \prod(1,2,4,7,12,15)$$

Answer the following questions.

1. Using **IC-74154** design a 2-bit comparator to compare two 2-bit numbers Y and Z. The circuit should provide 3 output lines to indicate Y>Z, Y = Z and Y< Z.

2. Study the use of **IC 7447** (BCD to 7-segment decoder / driver). Explain ripple blanking operation for 2 digits seven segment display.
   [You can see **"Digital Fundamentals"** by **Thomas L. Floyd**]

Report:

For each of the problems/questions report should the following points.

- Problem specification.
- Truth table.
- Required equation in minimized form with necessary steps.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 7

Topic: Design using Multiplexers.

Implement the following problems:

1. Design and implement the following two Boolean functions using 4×1 MUXs and necessary gates.

    a. $f(P,Q,R,S) = \sum(0,2,7,10,14,15)$
    b. $f(P,Q,R,S) = \prod(1,2,3,4,8,9,12)$

2. Design a 16×1 MUX using 4×1 MUXs only. Using this 16×1 MUX implement the Boolean function, $f(P,Q,R,S) = \sum(0,2,7,10,14,15)$

Answer the following question:

1. Design a Binary to Excess-3 code converter using one 8×1 MUX and basic gates as many as required.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- Truth table.
- Required equation in minimized form with necessary steps.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 8

Topic: Flip-Flops

Implement the following problems.

1. Design and implement an **SR flip-flop** with $\overline{\textbf{PRESET}}$ and $\overline{\textbf{CLEAR}}$ input, using only **NAND** gates.
2. Design and implement a **master-slave JK** flip-flop using only **NAND** gates.

Answer the following questions.

1. Design **JK FF** with **PRESET** and **CLEAR** and derive the excitation table.
2. Transform **JK FF** to **D** and **T FF** and also derive the excitation table.
3. Transform a **T FF** and a **D FF** to **JK FF**.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- Excitation Table.
- Truth table and function minimization (if required)
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 9

Topic: Registers

Implement the following problem.

1. Design and implement a 4-bit universal shift register.

Answer the following question.

1. Write down short notes on
    a. 7491A
    b. 74164.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

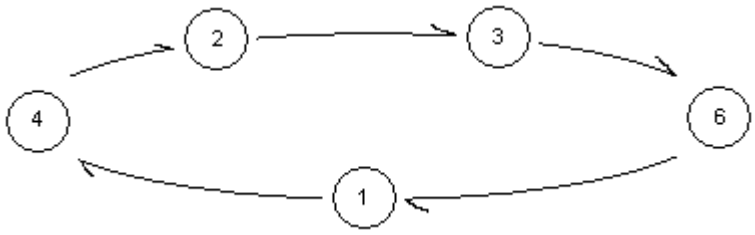
Course: CSE 206
Digital Logic Design Sessional

Experiment No. 10

Topic: Counters.

Implement the following problems.

1. Design a synchronous counter with the sequence given below by using **T** Flip Flops and basic gates:



2. Design 2-bit asynchronous up counter with the provision for mod-3 by using **D** Flip Flops and basic gates.

Answer the following questions.

1. Design mod-3 synchronous down counter using any type of Flip Flop.
2. Design a synchronous BCD counter with **JK** flip-flops (Don't convert JK to T)
3. Design a MOD 17 counter. Use any standard counter modules and gates.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- State table and Excitation table.
- Required equation in minimized form with necessary steps.(If required)
- Required instruments.
- Circuit diagram with pin number.

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering

Course: CSE 206N
Digital Logic Design Sessional

Experiment No. 11

Topic: Sequence Detector

Implement the following problems:

1. Design and implement a synchronous sequence detector that produces an output of 1 whenever the sequence 1101 occurs. The circuit resets to its initial state after 1 has been generated. Use **Moore model**. (Use any type of Flip Flop)

Answer the following question:

1. Solve the above mentioned problem by **Mealy model**. Write down a comparative study between the two designs.

2. How can a ring counter be implemented using a shift register? Show also the timing diagram.

Report:

For each of the problems/questions report should cover the following points.

- Problem specification.
- State diagram, State table and Excitation table.
- Required equation in minimized form with necessary steps.(If required)
- Required instruments.
- Circuit diagram with pin number.