CSE 206 (Digital Logic Design Sessional)

Exp No. 07

Name of The Exp:

Flip-flops and Registers.

Roll. 1905004

Section. A1

Dept: CSE

Date of Performance:
27.01.2022

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28.01.2022

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Problem 1:

Problem Specification:

Design and implement a master-slave JK flip-flop using only NAND gates.

Excitation Table:

CLK	J	K	Q_n	Q_{n+1}	Mode
0	x	x	x	Q_n	Hold
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	set
1	1	0	1	1	
1	1	1	0	1	Toggle
1	1	1	1	0	

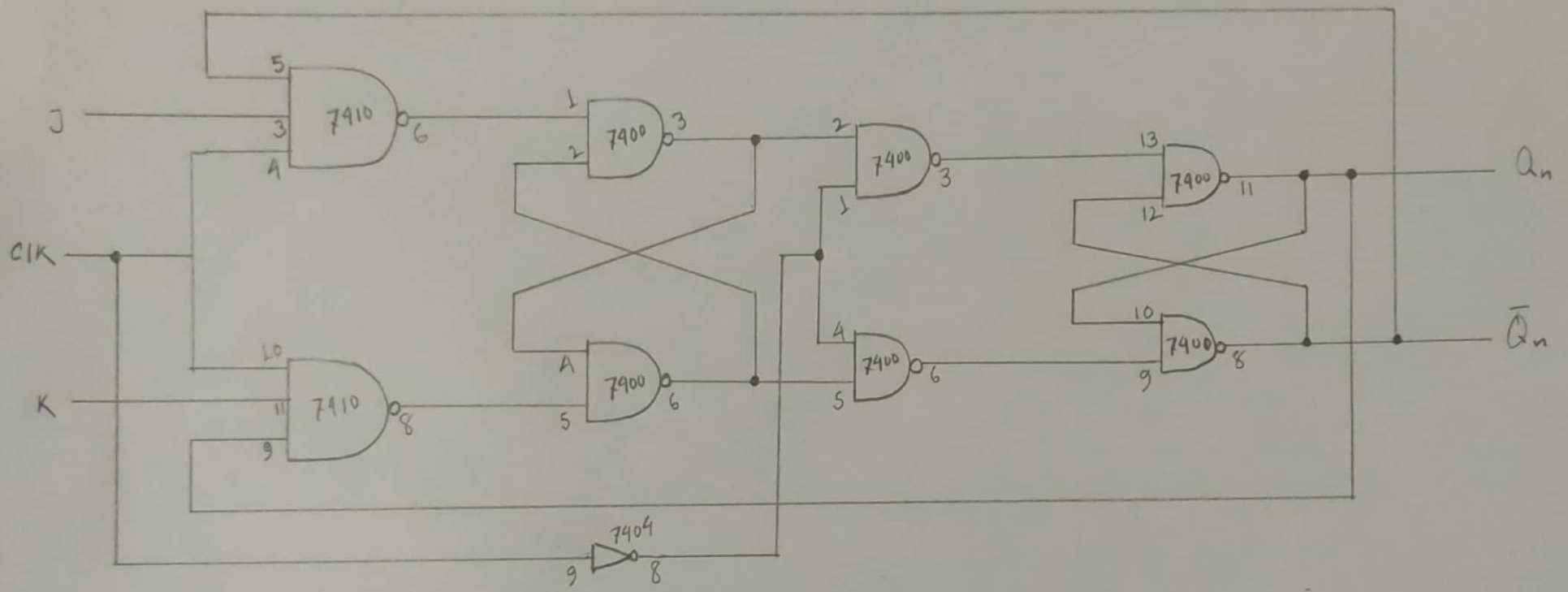

Fig: Circuit Diagram of Master-slave JK Flip Flop

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Problem 2:

Problem Specification:

We have to design and implement a 4-bit universal shift register.

* Excitation Table:

Input						Output				
$\overline{Clear}$	Preset	CLK	S_1	S_0	Internal signals	A_3	A_2	A_1	A_0	Mode
0	X	X	X	X	X	0	0	0	0	Asynchronous clear
1	1	X	X	X	X	1	1	1	1	Preset
1	0	X	0	0	X	A_3	A_2	A_1	A_0	Data hold
1	0	↑	0	1	A_{i+1}	MSB IN	A_3	A_2	A_1	Shift right
1	0	↑	1	0	A_{i-1}	A_2	A_1	A_0	LSB IN	Shift left
1	0	↑	1	1	i	I_3	I_2	I_1	I_0	Parallel load

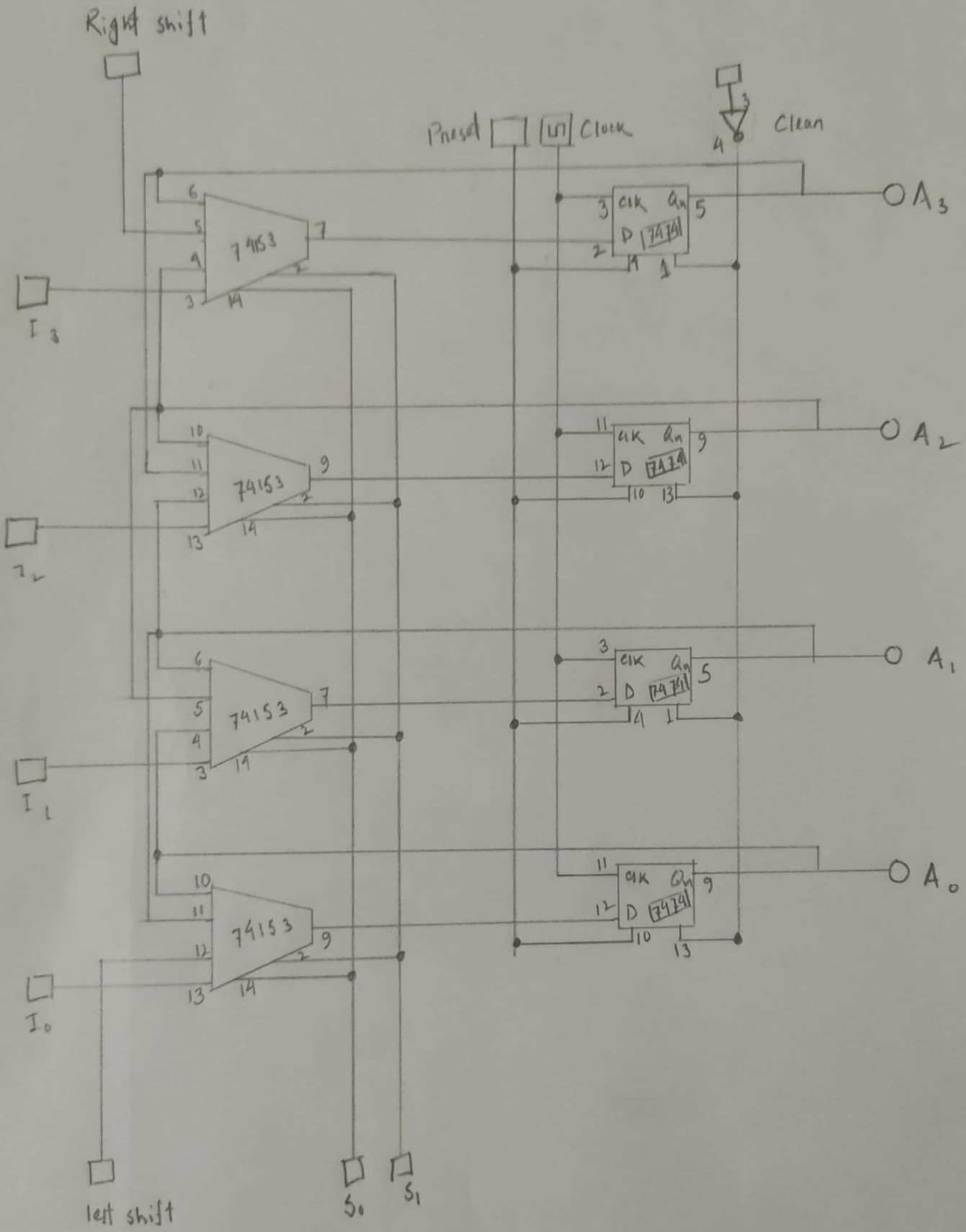

Fig: Circuit Diagram of 4-bit Universal shift Register