Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

Course: CSE 206 (Digital Logic Design Sessional)
Experiment No. 7
Topic: Flip-Flops and Registers

Implement the following problems:

1. Design and implement a **master-slave JK** flip-flop using only **NAND** gates.
2. Design and implement a 4-bit universal shift register.

Report:
For each of the problems above, the report should cover the following items:
1. Excitation Table.
2. Truth table and function minimization (if required)
3. Circuit diagram.

Submission Instruction:

1. Put all the items in a folder that is named as Roll_Number.
2. Zip the above folder, name it as Roll_Number.zip
3. Submit the zip file.
4. The submission deadline is 11:55pm, January 28, 2022.