

Nuvoton 8051 ISP Programmer

User Manual

Revision 7.15, 2015/Apr/15



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Revision History

Revision	Description	Date
v1.00	The first formal released version.	2009/07/08
v5.00	 (1) Improved data security of the Nuvoton standard ISP code for N78E366A, N78E055A, N78E059A and N78E517A. (Updated the ISP code version to v3.13.) (2) Updated the connection diagrams of Type-1~6. (Section 2.1~2.6) (3) Added new sections: Section 2.7, Section 6.2 and Section 6.3. (4) Updated the PC-site AP to v5.00. (The GUI display for "CONFIG Setting" becomes more user-friendly.) 	2010/08/13
v5.02	 (1) Fixed the HEX-to-BIN conversion error when the hex input file has a binary code size more than 64K. (Updated the application program to v5.02.) (2) Modified all the ISP codes to prevent from hanging in LDROM during powered on in an RS-485 application. (Updated the ISP code version to v3.20.) 	2010/11/15
v5.05	(1) Supported Tool Project (TPJ) file for management of GUI settings.(2) Fixed the ISP code bug when using 3.6864 MHz XTAL for 'ISP by COM Port' function. (Updated the ISP code version to v3.21.)	2011/01/18
v5.31	(1) Fixed some software bugs.(2) Updated the ISP code version to v3.23.	2011/04/08
v5.50	(1) Supported an advanced function: Limited Usage Times.(2) Updated the PC-site AP version to v5.50.	2011/06/15
v5.51	Fixed minor bugs in the PC-site AP of v5.50.	2011/07/26
v5.52	(1) Changed the maximum 'Limited Usage Times' from 9,999 to 60,000.(2) Supported to save the 'Limited Usage Times' setting in the TPJ file.	2011/09/28
v5.60	Renamed the parts W78E051D~W78E516D.	2011/10/20
v5.70	Updated the PC-site AP version to v5.70.	2011/11/07
v6.00	Supported chip counter for successfully programmed chips. (cf. Section 9.2)	2011/12/20
v6.02	Fixed some minor software bugs.	2012/02/01
v6.04	Updated the document version to v6.03.	2012/02/29
v6.10	Updated the document version to v6.10.	2012/03/26
v6.12	Fixed a software bug that sometimes makes "Auto Synchronization of Buffer Data" failed. (cf. Section 3.4)	2012/04/26
v7.10	Removed support for W77E(L)516, W77E(L)532, W78E051D, W79E201, W79E217, W79E225, W79E226, W79E227, W79E(L)632, W79E(L)633, W79E(L)648, W79E(L)649, W79E(L)658 and W79E(L)659.	2014/01/15



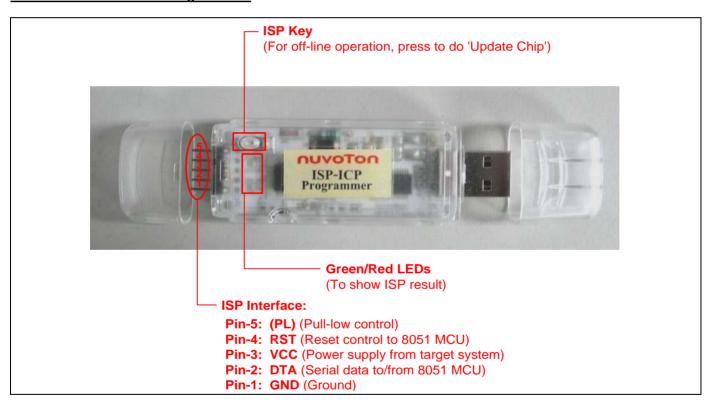
1 Introduction

ISP is the acronym of **In-S**ystem **P**rogramming, which makes it possible that the user can update the MCU's program memory under software control without removing the mounted MCU chip from the actual end product. The USB-stick-like tool "8051 ISP Programmer", as shown in the following picture, is used to perform the ISP function when the LDROM of the MCU is pre-programmed with the *Nuvoton Standard ISP Code* and CONFIG bits are properly configured. In addition, since this tool can save the programming data downloaded from the host, it is able to perform the off-line operation. This feature is especially useful in the field without a host PC.

Note:

The ISP function can work only when the ISP code has resided in LDROM of the MCU. To let users easily use the ISP function, some of the 8051 MCU products have the "Nuvoton Standard ISP Code" pre-programmed in LDROM and CONFIG bits properly configured before shipping. Please contact Nuvoton for detailed product information. (The "Nuvoton Standard ISP Code" is also included in the folder [(3) Nuvoton Standard ISP Code]. The user may program it with a universal programmer.)

Picture of the "8051 ISP Programmer"



The ISP Interface

PL: Pull-low control.

Some 8051 MCU parts need its special I/O pins to be tied to ground to boot from LDROM for ISP operation. Using pull-low control can release these I/O pins for their normal function. In other words, these pins do not need to be tied to ground in the target system but pulled low by the ISP Programmer for ISP operation.

RST: Reset control to the 8051 MCU.

The ISP Programmer will send reset signal to control the 8051 MCU for ISP operation.

VCC: Power supply from the target system. In off-line operation, the programmer is powered by the target system.

DTA: Serial data to/from the 8051 MCU. (Single-wire Communication Interface)

GND: Ground.



2 Hardware

According to the I/O pins used for booting from LDROM after reset, there are several connection types between the 8051 MCU and the ISP Programmer, as shown in the following table. Some parts do not need any I/O pins, but need CONFIG to be properly configured, such as W78E(I)051D, W78E(I)052D and W78E(I)054D. Some parts need only I/O pins, such as W78E(I)058D, W78E(I)516D, etc. Some parts not only need I/O pins, but also need the CONFIG to be properly configured, such as W78E(I)RD2A. The following sub-sections will show the connection diagrams for these connection types.

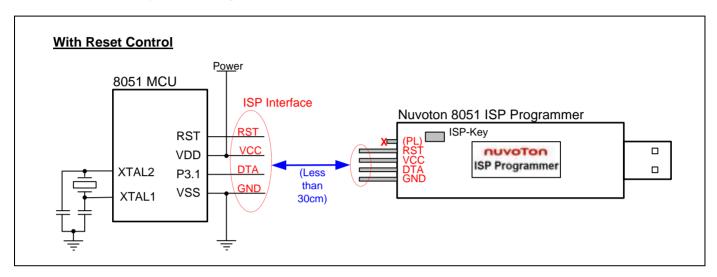
I/O Pins and CONFIG Bit for Booting from LDROM after Reset

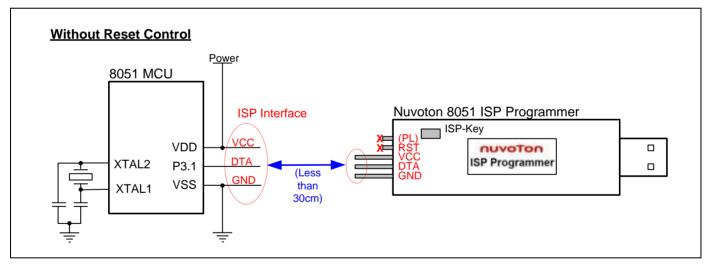
Part No.	I/O Pins Tied to Ground for Booting from LDROM	CONFIG Setting for Booting from LDROM	Connection Type
W78E052D W78E054D N78I054DFN	(Not Need)	'CBS' configured as LDROM	Type-1
W78E058D W78E516D W78E(L)365A	P2.6 & P2.7 (for 40-pin package)	(Not Need)	Type-2
W78E(E)363A W78E065A W78E858A	P4.3 (for 44-pin package)	(Not Need)	Type-3
W78E(I)RD2A	P2.6 & P2.7 (for 40-pin package)	'Reboot P2.6/P2.7' configured as Enabled	Type-2
	P4.3 (for 44-pin package)	'Reboot P4.3' configured as Enabled	Type-3
W925EP01	P4.7	'Reboot P4.7' configured as Enabled	Type-6
N78E366A N78E055A N78E059A N78E517A	(Not Need)	'CBS' configured as LDROM	Type-1



2.1 Type-1 Connection (No I/O Pins Used for Booting from LDROM)

In this type of connection, the PL-pin of the ISP interface is not used. The following figures show the hardware connection for "With Reset Control" and "Without Reset Control" configuration. The former is adopted when the RST-pin of the MCU can be controlled by the ISP Programmer; the latter is adopted when the RST-pin of the MCU cannot be controlled by the ISP Programmer. Refer to Chapter 5: Reset Control.

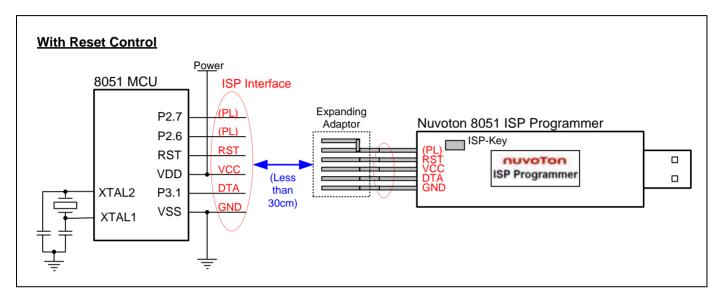


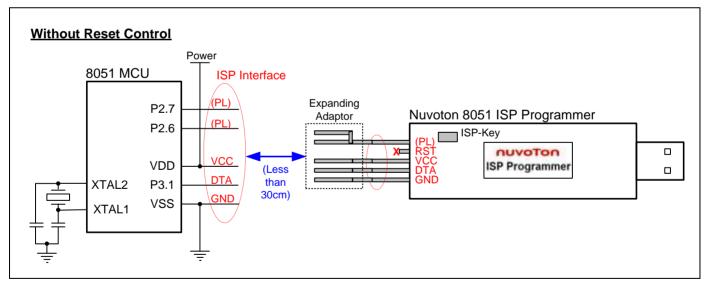




2.2 Type-2 Connection (P2.6 & P2.7 Used for Booting from LDROM)

In this type of connection, P2.6 and P2.7 are to be pulled low to let the 8051 MCU boot from LDROM after hardware reset. The PL-pin in the ISP interface can automatically pull low P2.6 and P2.7 when the ISP Programmer is connected to the 8051 MCU. So, the user does not always need pull P2.6 and P2.7 low in the target system. The following figures show the hardware connection for "With Reset Control" and "Without Reset Control" configuration. The former is adopted when the RST-pin of the MCU can be controlled by the ISP Programmer; the latter is adopted when the RST-pin of the MCU cannot be controlled by the ISP Programmer. Refer to Chapter 5: Reset Control.

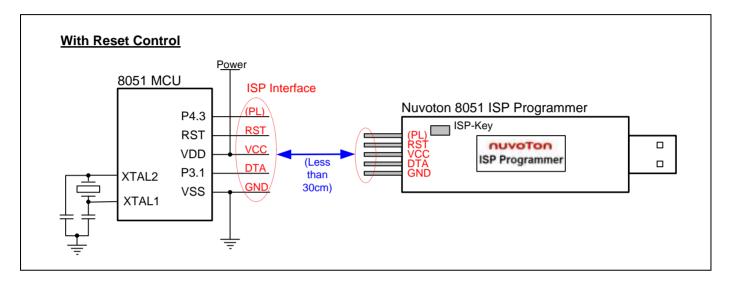


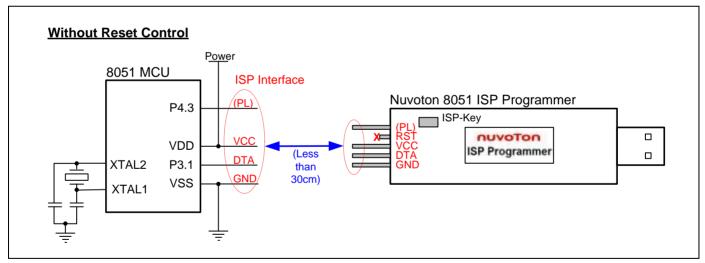




2.3 Type-3 Connection (P4.3 Used for Booting from LDROM)

In this type of connection, P4.3 is to be pulled low to let the 8051 MCU boot from LDROM after hardware reset. The PL-pin in the ISP interface can automatically pull P4.3 low when the ISP Programmer is connected to the 8051 MCU. So, the user does not always need to pull P4.3 low in the target system. The following figures show the hardware connection for "With Reset Control" and "Without Reset Control" configuration. The former is adopted when the RST-pin of the MCU can be controlled by the ISP Programmer; the latter is adopted when the RST-pin of the MCU cannot be controlled by the ISP Programmer. Refer to Chapter 5: Reset Control.

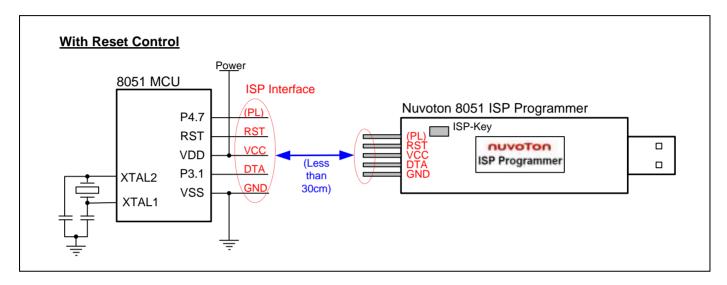


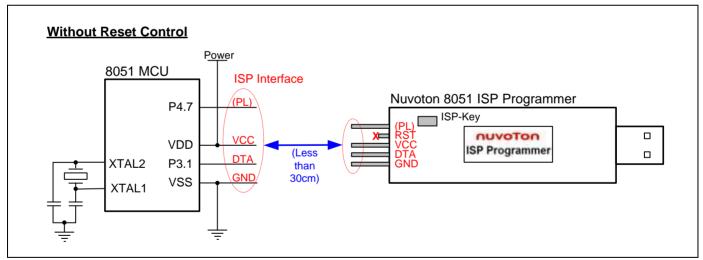




2.6 Type-6 Connection (P4.7 Used for Booting from LDROM)

In this type of connection, P4.7 is to be pulled low to let the 8051 MCU boot from LDROM after hardware reset. The PL-pin in the ISP interface can automatically pull low P4.7 when the ISP Programmer is connected to the 8051 MCU. So, the user does not always need to pull P4.7 low in the target system. The following figures show the hardware connection for "With Reset Control" and "Without Reset Control" configuration. The former is adopted when the RST-pin of the MCU can be controlled by the ISP Programmer; the latter is adopted when the RST-pin of the MCU cannot be controlled by the ISP Programmer. Refer to Chapter 5: Reset Control.





2.7 Requirement on the XTAL Frequency

There is no restriction on the XTAL frequency for ISP operation. All frequencies between 2 MHz and 40 MHz are acceptable. The MCU will automatically build a proper transmission rate to communicate with the ISP Programmer during ISP operation.



3 Software

3.1 Installing the Driver

This ISP Programmer has the USB-to-Serial bridge chip (PL-2303) built inside. When connected to host, it will appear as a *USB-to-Serial COM port* in the System\Hardware\Device Manager. Before starting to use this programmer, the user has to install the driver if the PL-2303 driver has never been installed in this host. The user can also find this driver in the folder [(1) Driver].

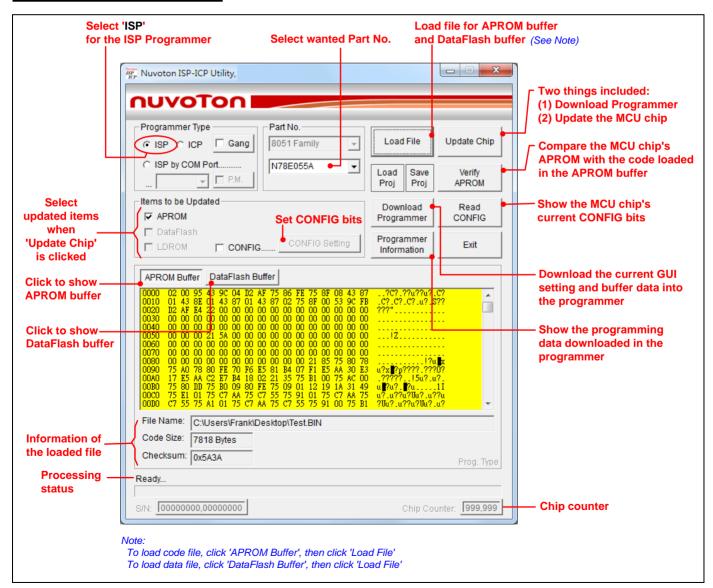
Note: Do not plug the ISP Programmer to the host before the driver is installed.

3.2 Installing the Application Program

The application program setup file is stored in the folder [(2) Application Program]. Using the default installation setting, you will find the item "Nuvoton Tools \ Nuvoton ISP-ICP Utility, v?.??" appears in the Windows START-menu after the application program is successfully installed.

Note: ISP-ICP means this application program is designed for both the ISP Programmer and the ICP Programmer.

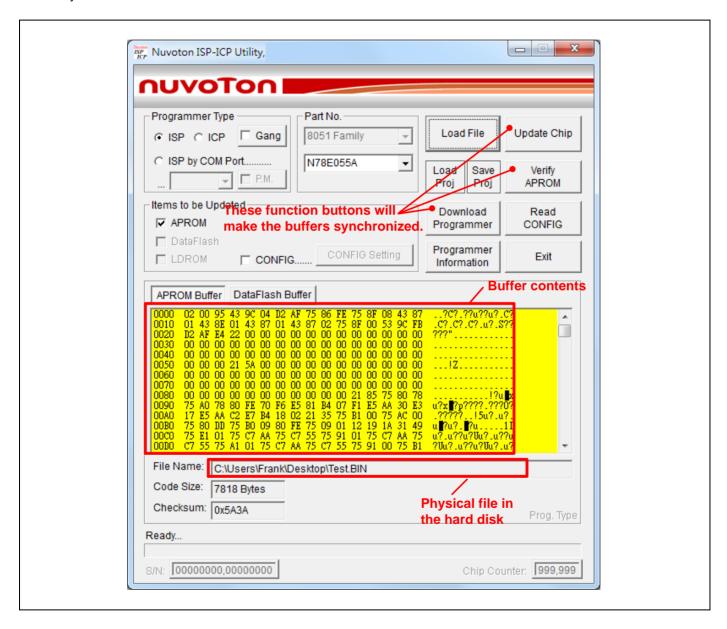
3.3 Introduction to the GUI





3.4 Auto Synchronization of Buffer Data

The buffer contents will be automatically synchronized with the physical file in the hard disk when the function buttons 'Download Programmer', 'Update Chip' or 'Verify Chip' is clicked, as shown below. Thus, the user does not need to manually reload the files for APROM buffer and Data Flash buffer when the physical files are updated externally.

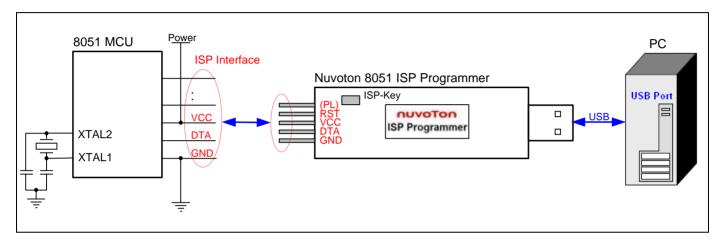




4 Operation Modes

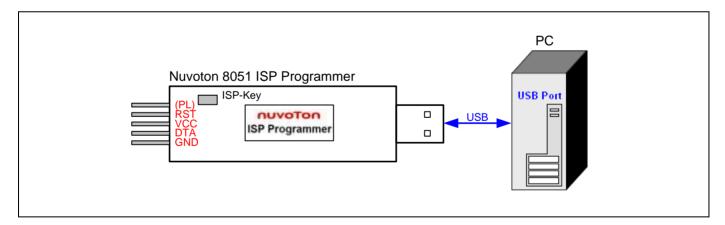
4.1 On-line Mode

The system diagram for **On-line Mode** is shown below. In this mode, both the host and MCU chip are connected. The user may directly update the MCU chip or download the programming data into the programmer for use in Offline Mode. After updating the MCU chip, the user may disconnect the programmer to let the MCU chip run the new application code.



4.2 Download Programmer Mode

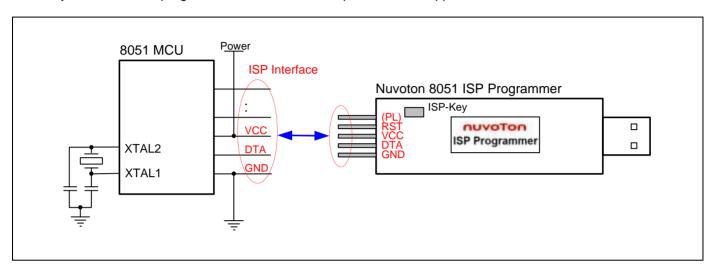
The system diagram for **Download Programmer Mode** is shown below. In this mode, only the host is connected. The user may download the programming data into the programmer for use in Off-line Mode.





4.3 Off-line Mode

The system diagram for **Off-line Mode** is shown below. In this mode, only the MCU chip is connected. This mode is especially useful in the field without a PC. After the programmer has been downloaded, it can perform the off-line operation. Press the ISP-Key to start an ISP operation to update the MCU chip. After updating the MCU chip, the user may disconnect the programmer to let the MCU chip run the new application code.





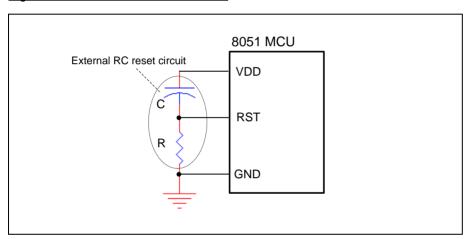
5 Reset Control

Normally, the 8051 RST-pin of the MCU with external RC reset circuit (see Figure 5a) can be controlled by the ISP Programmer. At this time, the user may adopt the "With Reset Control" configuration for ISP operation. However, the RST-pin cannot be controlled by the ISP Programmer when the RST-pin is connected to a reset IC (such as MAX810, ADM810, AIC810 and FP6810, etc., see Figure 5b). Now the user should adopt the "Without Reset Control" configuration for ISP operation.

External RC Reset Circuit

The general external RC reset circuit is shown in Figure 5a. The resistance of R should be larger than $47k\Omega$ to have the RST-pin be successfully controlled by the ISP Programmer. Normally, $\{47k\Omega,\ 2.2uF\}$ and $\{100k\Omega,\ 1uF\}$ are recommended for $\{R,C\}$.

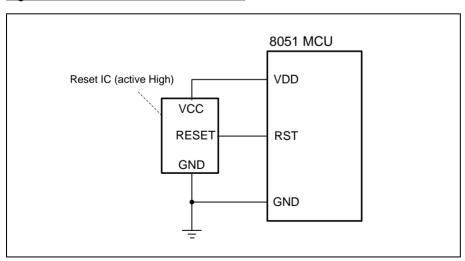
Figure 5a. External RC Reset Circuit



Reset Circuit with a Reset-IC

In this condition, the RST-pin cannot be controlled by the ISP Programmer.

Figure 5b. Reset Circuit with a Reset-IC





5.1 With Reset Control

For the "With Reset Control" configuration, the ISP Programmer will always keep the 8051 MCU in reset state until the ISP operation is triggered, such as "Update Chip" button is clicked or ISP-Key is pressed. At this time, the ISP Programmer will release the 8051 MCU to let it reboot from LDROM to run the ISP code. After ISP operation is completed, the ISP Programmer keeps the 8051 MCU in reset state again. When the ISP Programmer is disconnected from the 8051 MCU, the 8051 MCU will automatically reboot from APROM to run the new application code. With reset control, the user may do the ISP operation as long as the ISP Programmer is connected to 8051 MCU when the 8051 MCU is in powered-on state.

Note: "With Reset Control" is strongly recommended for ISP operation.

5.2 Without Reset Control

For the "Without Reset Control" configuration, to successfully let the 8051 MCU boot from LDROM to run the ISP code, the user should follow the steps listed below.

- Step 1: Connect the ISP Programmer to the 8051 MCU.
- Step 2: Connect the ISP Programmer to the host. (This step is only for On-line Mode and may be exchanged with Step1.)
- Step 3: Make the 8051 MCU boot from LDROM by the following two methods:
 (1) Send reset a reset pulse to the RST-pin, or (2) power off the and power on again.
- Step 4: Now, the 8051 MCU will boot from LDROM and start to run the ISP code for ISP operation.

Note: Step 3 shows the "Without Reset Control" is somewhat inconvenient for the user to have the 8051 MCU boot from LDROM. That is why it is strongly recommended to adopt the "With Reset Control" configuration.

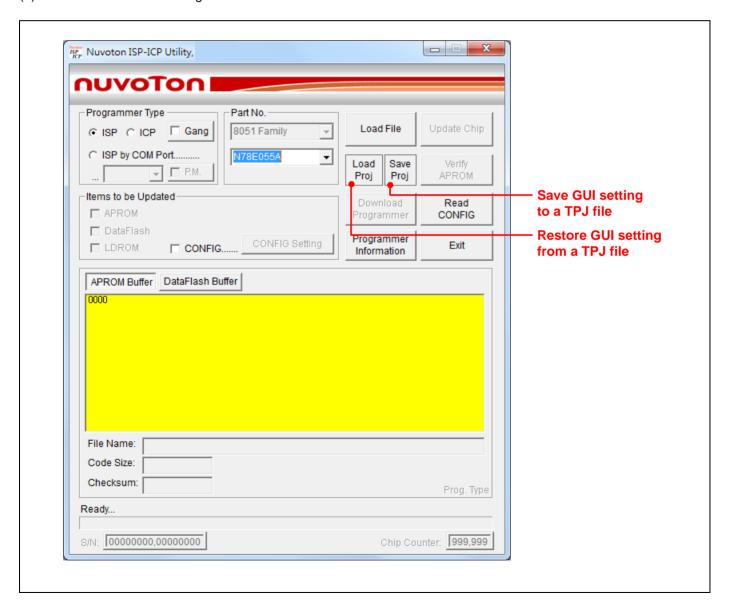


6 Tool Project File (TPJ)

The user may save all the GUI settings to the Tool Project (TPJ) file, and retrieve the GUI settings by loading the TPJ file previously saved. It is much helpful to the user to manage a variety of programming data by the 'project' type.

The GUI settings or the contents of the TPJ file include:

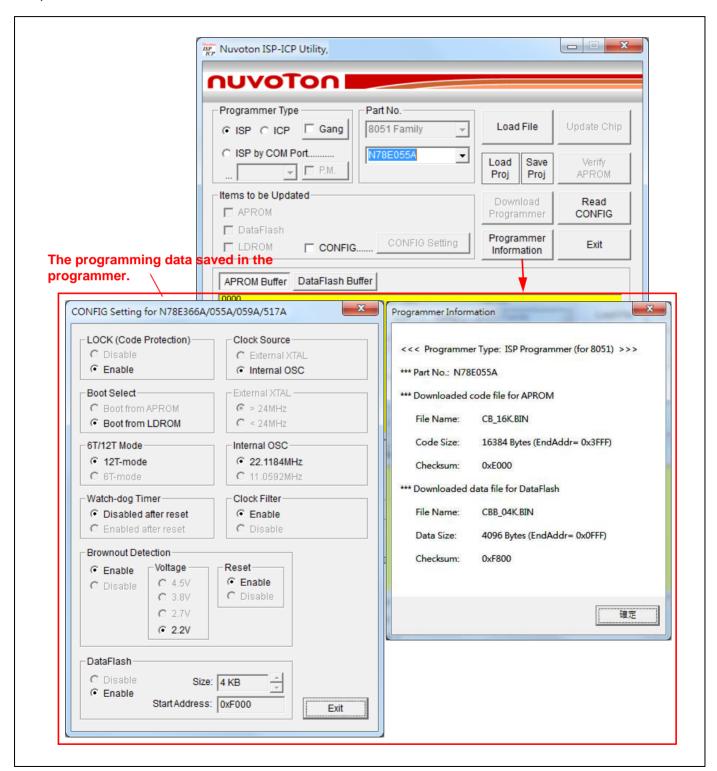
- (1) Programmer type
- (2) Part number
- (3) Items to be updated
- (4) APROM buffer data if APROM is one of the updated items
- (5) Data Flash buffer data if Data Flash is one of the updated items
- (6) CONFIG setting if CONFIG is one of the updated items
- (7) Advanced functions setting





7 Programmer Information

To check the programming data downloaded in the programmer, click the 'Programmer Information' button when the programmer is connected to PC. Note the 'CONFIG Setting' dialog box appears only when the CONFIG bits are to be updated.





8 Notes for the ISP Function

8.1 Requirement on P3.1

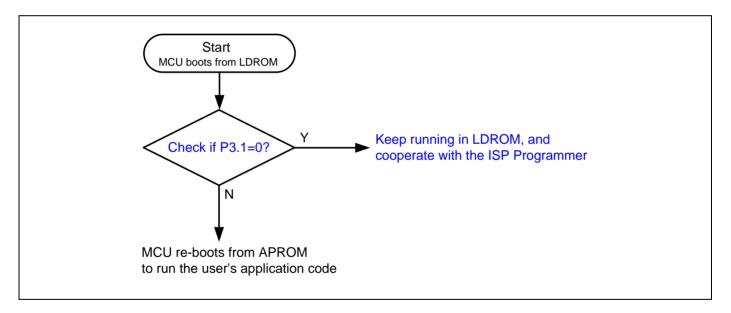
During ISP operation, the P3.1-pin of the MCU behaves as 'DTA' (serial data). When ISP is not requested, P3.1 can function as its normal general purpose I/O pin as long as P3.1 conforms to the following requirements:

- * The state of P3.1 must be logic-1 before the MCU is just released from reset condition.
- * During the ISP operation, P3.1 cannot be pulled low by the other components connected to it.

Because when the MCU boots from its LDROM and starts to run the *Nuvoton standard ISP code*, the MCU will sample P3.1 to determine the next action. If logic-0 is sampled, it means the ISP Programmer is connected, and the MCU will stay in LDROM for further ISP operation; if logic-1 is sampled, the MCU will automatically re-boot from APROM (by internal software reset) to run the user's application code.

During the operating of ISP, P3.1 functions as bi-directional I/O for serial data transfer. It may output logic-1 or logic-0 to the ISP Programmer, and receive logic-1 or logic-0 from the ISP Programmer. Thus the user should check if there is any side effect on the other components connected to P3.1 during ISP operation.

The following flow chart shows how the MCU determines to cooperate with ISP Programmer or to reboot from APROM when the MCU starts to run the *Nuvoton standard ISP code* in LDROM.





8.2 About the ISP Code

For the 8051 MCU products with ISP function, there are two program memories: one is APROM and the other is LDROM. APROM contains the user's application code for normal operation while LDROM contains the ISP code (cooperating with the ISP Programmer) for programming of APROM. To use the ISP Programmer to update APROM, the ISP code should have resided in LDROM. If the ISP code disappears from LDROM because of accidentally being erased by a universal programmer, the ISP function will become failed. To recover the ISP function, please use a universal programmer to reprogram the *Nuvoton standard ISP code* into LDROM, and have its CONFIG setting properly configured (cf. Chapter 2).

Why can the ISP code be easily/accidentally erased by a universal programmer? Because the universal programmers usually use chip-erase operation to erase APROM, and chip-erase will also erase LDROM. So, we strongly recommend the user to use our proprietary ISP Programmer to program APROM in the beginning of development. Do not use any universal programmer to program APROM unless the ISP function will not be used.

8.3 Comparison with the 'ICP'

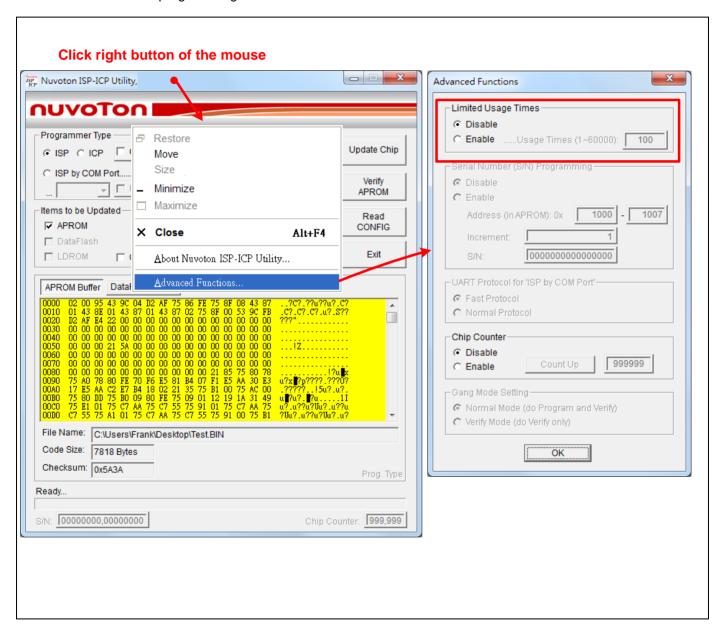
The difference between ISP (In-System Programming) and ICP (In-Circuit Programming) is that ISP is implemented by software control of MCU itself while ICP is implemented by hardware control. So, before updating the MCU chip, ISP needs a software code (the ISP-code) pre-programmed in LDROM of the MCU to function as software control while ICP does not need any software code pre-programmed.



9 Advanced Functions

9.1 Limited Usage Times

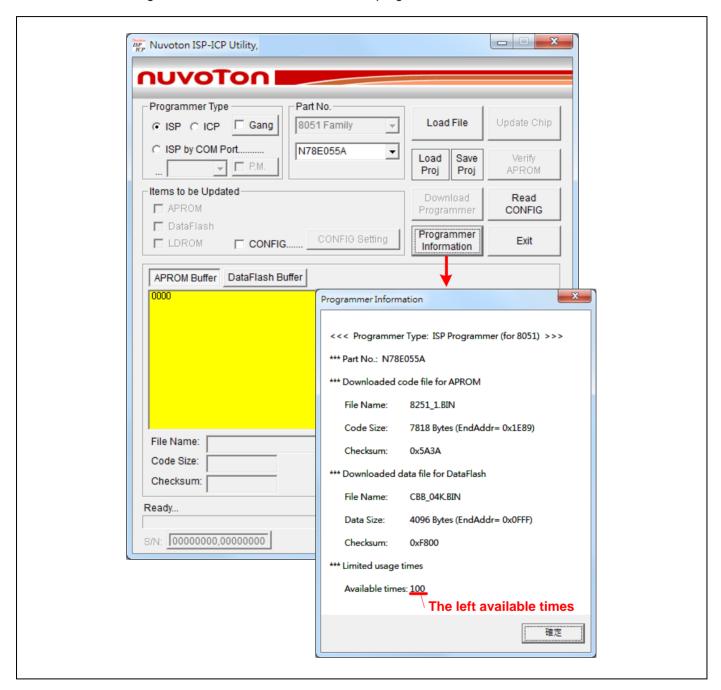
An advanced function, *Limited Usage Times*, is supported for the customer who wants to limit the usage times of the ISP Programmer. Once this function is enabled and the wanted times value is filled, as shown below, the usage times of this programmer will be limited after finishing 'Download Programmer'. Provided that 100 is filled, then the programmer will be no longer available when reaching 100 times of successful programming. That is to say, only 100 times of successful programming are available.





Checking the Left Available Times

To check the left available times of the programmer, which was previously downloaded with *Limit Usage Times* enabled, click the 'Programmer Information' button when the programmer is connected to PC, as shown below.





9.2 Chip Counter

The chip counter is used to calculate the successfully programmed chips. The user may configure the counter as up counter or down counter, and set the initial counter value. The following figure shows how to enable the chip counter and its various configuration.

