SONY®

CXA1362Q

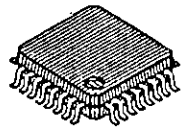
Read/Write Amplifier for Floppy Disk Drive with Built-in Filter

For the availability of this product, please contact the sales office.

Description

The CXA1362Q is designed for FDD (Floppy Disk Drive) use. This IC combines such functions as Read, Write, Erase and Supply voltage detection circuits in a single chip.

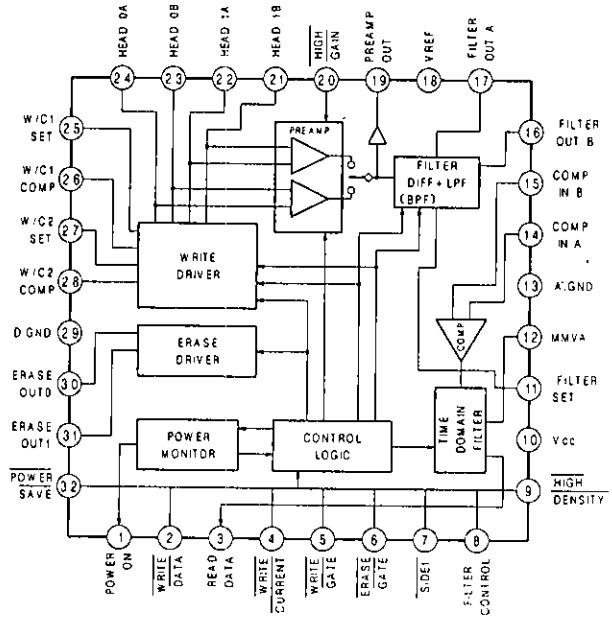
32pin QFP (Plastic)



Features

- 5V single power supply operation.
- Built-in filter permits switching to 4 modes 1M/2M, inner and outer tracks. This contributes to a drastic reduction of the external parts originally meant for the differentiator constant, low pass filter, select switches and others (Down to 1/2 the original number).
- Filter characteristics can be customized.
- Preamplifier input equivalent noise voltage as low as 2.2 nV/$\sqrt{\text{Hz}}$ (Typ.) keeps read data output jitter to a minimum. The preamplifier voltage gain can be selected at either 100 or 200 times.
- Built-in function to select the pulse width of the 1st monostable multivibrator in the time domain filter enables selection through 1M/2M mode.
- Built-in write current selection function allows for 4 mode write current selections: 1M/2M, inner and outer tracks (Other than the filter inner/outer track).
- Built-in supply voltage detection circuit prohibits irregular write during power supply rise, fall or abnormal voltage.
- Power consumption is kept to low 120 mW (Typ.) making suitable for battery drive FDD.
- Built-in capacitor of the time constant in the 1st and 2nd monostable multivibrator (The 2nd monostable multivibrator pulse width is fixed).
- Built-in power saving function to reduce power consumption when not in use. In power saving mode only power ON/OFF detector is in operating condition (5 mW Typ.).
- Built-in reset circuit in the write driver. As a result, when mode selection is switched from read to write, should head side 0 be selected, write current sinks from head side 0A. Similarly, if head side 1 is selected, write current sinks from head 1A.

Block Diagram and Pin Configuration



E89818A9Z-YA

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc		7		V
• Digital signal input pin (*Note) Input voltage		- 0.5	to	Vcc +0.3	V
• POWER ON output voltage applied			Vcc +0.3		V
• ERASE OUTPUT voltage applied			Vcc +0.3		V
• Head 0A, 0B, 1A and 1B voltage applied			15		V
• POWER ON output SINK current			7		mA
• ERASE OUTPUT SINK current			150		mA
• Operating temperature	Topr	-20	to	+75	°C
• Storage temperature	Tstg	-65	to	+150	°C
• Allowable power dissipation	PD		500		mW

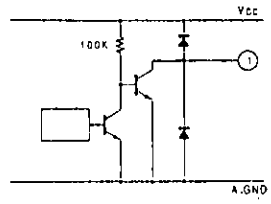
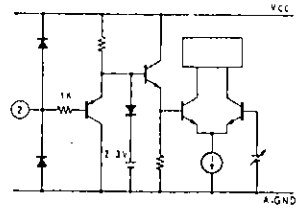
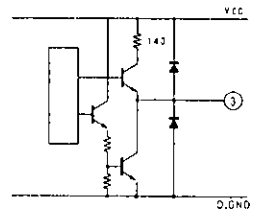
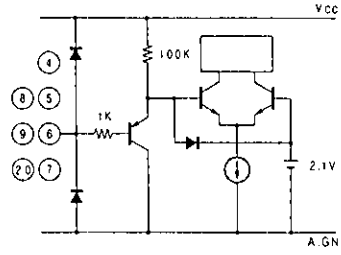
Supply Voltage Range

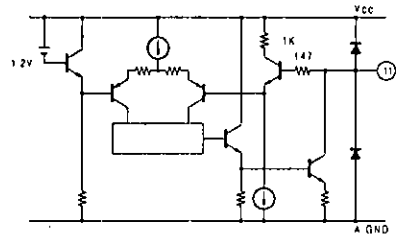
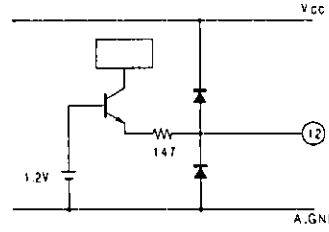
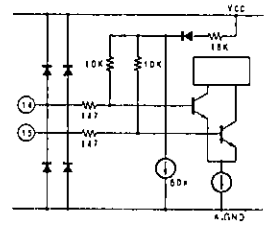
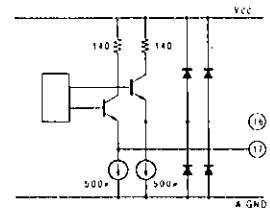
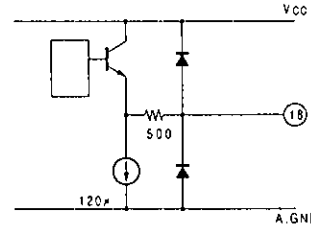
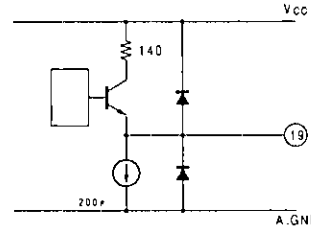
	Vcc	4.4	to	6.0	V

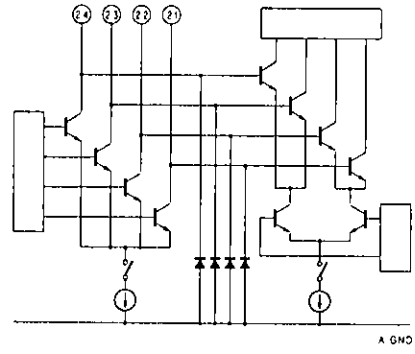
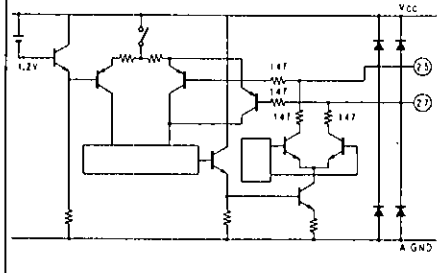
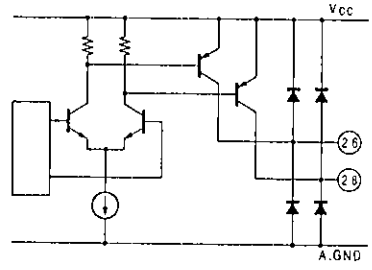
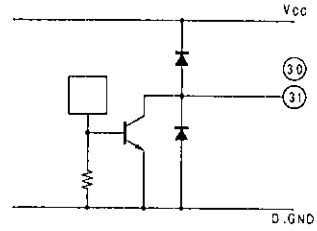
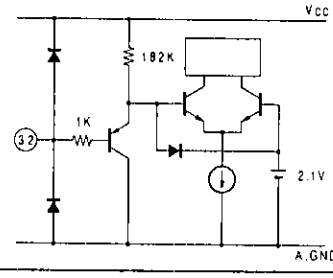
*Note) $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE CURRENT}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{ERASE GATE}}$
$\overline{\text{SIDE1}}$, FILTER CONTROL, $\overline{\text{HIGH DENSITY}}$, $\overline{\text{HIGH GAIN}}$, $\overline{\text{POWER SAVE}}$

Pin Description

(Ta=25°C, Vcc=5V)

No.	Symbol	Voltage	Equivalent Circuit	Description
1	POWER ON	—		Output pin for supply voltage decrease detection. Open collector pin that outputs "L" when Vcc is below normal value.
2	$\overline{\text{WRITE DATA}}$	—		Write data input pin. A schmitt type input triggered when logic voltage shifts from "H" to "L".
3	READ DATA	—		Read data output pin. Activated when either write gate signal or erase gate signal logic voltage is at "H".
4	$\overline{\text{WRITE CURRENT}}$	—		Write current control pin. Write current increases at logic voltage "L".
5	$\overline{\text{WRITE GATE}}$	—		Write gate signal input pin. Write system is activated at logic voltage "L".
6	$\overline{\text{ERASE GATE}}$	—		Erase gate signal input pin. Erase system is activated at logic voltage "L".
7	$\overline{\text{SIDE 1}}$	—		Head side switching signal input pin. This pin is activated only when logic voltage of both write and erase gates are at "H". At logic voltage "L", HEAD 1 system is selected while HEAD 0 is selected at logic voltage "H".
8	FILTER CONTROL	—		Control pin for filter inner/outer tracks. Inner track mode ON at logic voltage "L".
9	$\overline{\text{HIGH DENSITY}}$	—		1M, 2M mode control pin for filter, time domain filter and write current. 2M mode ON at logic voltage "L".
20	$\overline{\text{HIGH GAIN}}$	—		Voltage gain select pin of the preamplifier. 100 times at logic voltage "H" and 200 times at logic voltage "L".

No.	Symbol	Voltage	Equivalent Circuit	Description
10	Vcc	–		Power supply (5V) connection pin.
11	FILTER SET	3.8V		Resistance connecting pin that sets the filter cut off frequency. Connect resistance R_F for filter cut off setting between this pin and Vcc, then set cut off frequency.
12	MMVA	0.5V		Pulse width setting pin for the 1st monostable multivibrator of the time domain filter. Connect 1st monostable multivibrator pulse width setting resistance R_A between this pin and A. GND.
13	A. GND	–		GND connecting pin for analog system.
14	COMP IN A	3.3V		Comparator differential input pin.
15	COMP IN B	3.3V		
16	FILTER OUT B	3.3V		Filter differential output pin.
17	FILTER OUT A	3.3V		
18	VREF	2.8V		Connecting pin for the decoupling capacitor of the internal reference voltage. Decoupling capacitor C_{REF} is connected between this pin and A. GND.
19	PREAMP OUT	2.8V		Preamplifier output pin.

No.	Symbol	Voltage	Equivalent Circuit	Description
21	HEAD 1B	—		Magnetic heads I/O connecting pin. Connects magnetic heads for both Rec/PB use. Center tap is connected to Vcc. When Pin 7 ($\overline{\text{SIDE 1}}$) logic voltage is at "L", HEAD 1 system is activated. At "H", HEAD 0 system is activated.
22	HEAD 1A	—		
23	HEAD 0B	—		
24	HEAD 0A	—		
25	W/C1 SET	At $\overline{\text{WG}}$= "H", 5V		Resistance connecting pin for 1M write current setting. Connect R_{W1} resistance for write current setting between this pin and Vcc, then set write current.
27	W/C2 SET	At $\overline{\text{WG}}$= "L", 3.8V		Resistance connecting pin for 2M write current setting. Connect R_{W2} resistance for write current setting between this pin and Vcc, then set write current.
26	W/C1 COMP	—		Resistance connecting pin for 1M write current compensation. Connect resistance R_{WC1} for write current compensation between this pin and Pin 25 (W/C1 SET), then set write current increase volume.
28	W/C2 COMP	—		Resistance connecting pin for 2M write current compensation. Connect resistance R_{WC2} for write current compensation between this pin and Pin 27 (W/C2 SET), then set write current increase volume.
29	D. GND	—		GND connecting pin for digital system.
30	ERASE OUT 0	—		Erase current output pin for HEAD 0 system.
31	ERASE OUT 1	—		Erase current output pin for HEAD 1 system.
32	$\overline{\text{POWER SAVE}}$	—		Input pin for power saving signal. When logic voltage is at "L", power saving is ON. In power saving condition only the power supply ON/OFF detector operates.

Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
Consumption current for Read	ICCR	Vcc=5V $\overline{WG}$="H"	—	—	14.0	24.0	34.0	mA
Consumption current for Write and Erase	ICCWE	Vcc=5V $\overline{WG}$="L", $\overline{EG}$="L"	—	—	10.5	18.0	25.5	mA
Consumption current for Power saving	ICCPS	Vcc=5V $\overline{PS}$="L"	—	—		0.9	1.8	mA

Power Supply Observation System

(Ta=25°C)

Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
Power supply ON/OFF detector threshold voltage	VTH		—	—	3.5	3.9	4.3	V
Power ON output saturation voltage	VSP	Vcc=3.5V I=1mA	—	—			0.5	V

Read System

(Ta=25°C, Vcc=5V)

Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
Preamplifier voltage gain SIDE 0*	GV0	f=100kHz SW4=a,b	1	G	38.1 /44.1	40 /46	41.6 /47.6	dB
Preamplifier voltage gain SIDE 1*	GV1	f=100kHz SW4=a,b SW1,5=b						
Preamplifier frequency characteristics SIDE 0*	BW0	A_V/A_{V0}=−3dB SW4=a,b	1	G	5			MHz
Preamplifier frequency characteristics SIDE 1*	BW1	A_V/A_{V1}=−3dB SW4=a,b SW1,5=b						
Preamplifier input equivalent noise voltage SIDE 0	EN0	Bandwidth=400Hz to 1MHz SW4=b	1	G		2.2	3.1	μVrms
Preamplifier input equivalent noise voltage SIDE 1	EN1	Bandwidth=400Hz to 1MHz SW4=b SW1,5=b						

* When SW4=a Vi=10mVp-p
When SW4=b Vi=5mVp-p

Read System

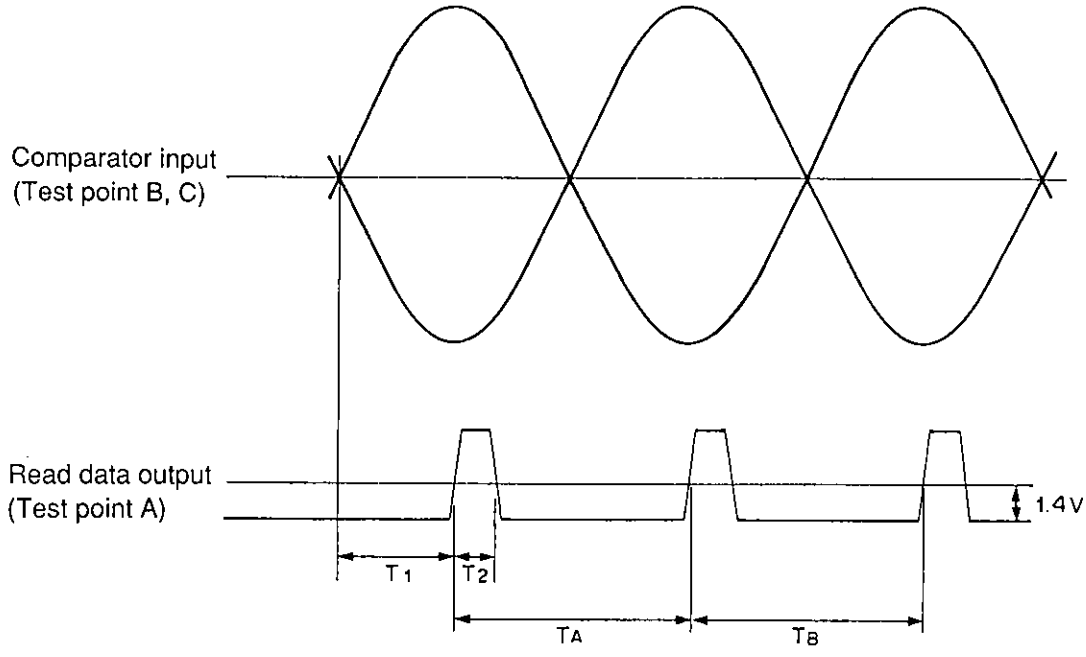
(Ta=25°C, Vcc=5V)

Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
Preamplifier output offset voltage (vs. VREF)	VOFSP	Vi=0 SW4=a,b SW1,5=a,b	1	F, G	−500		+500	mV
Preamplifier output voltage amplitude**	VOP	f=100kHz SW4=a,b SW1,5=a,b	1	G	1.8			Vp-p
Filter differential output offset voltage	VOFSF	Vi=0	1	D, E	−100		+100	mV
Filter differential output voltage amplitude	VOF	f=100kHz Vi=60mVp-p	1	D, E	2.8			Vp-p
Time domain filter 1st monostable multivibrator pulse width accuracy	ETM1 ETM1'	R_A=27kΩ See Fig. 1	1	B, C A	−10		+10	%
Time domain filter 2nd monostable multivibrator pulse width (fixed)	T2	R_A=27kΩ See Fig. 1	1	A	260	400	540	ns
Read data output "L" output voltage	VOL	I_{OL}=2mA	1	A			0.5	V
Read data output "H" output voltage	VOH	I_{OH}=−0.4mA	1	A	2.8			V
Read data output rise time	TR	R_L=2kΩ C_L=20pF	1	A			100	ns
Read data output fall time	TF	R_L=2kΩ C_L=20pF	1	A			100	ns
Peak shift***	PS	Vi=0.25mVp-p to 10mVp-p f=62.5kHz See Fig. 1	1	A			1	%

** When SW4=a Vi=60mVp-p
When SW4=b Vi=30mVp-p

*** When Vi=0.25mVp-p to 5mVp-p, SW4=b (Preamplifier voltage gain 46dB)
When Vi=0.5mVp-p to 10mVp-p, SW4=a (Preamplifier voltage gain 40dB)

Fig. 1 1st and 2nd Monostable Multivibrator Pulse Width Accuracy and Peak Shift Test Conditions



- 1st monostable multivibrator pulse width accuracy
  When $\overline{HD}$="H",

$$ETM1 = \left(\frac{T_1}{2.45\mu S} - 1 \right) \times 100\,(\%)$$

  When $\overline{HD}$="L",

$$ETM1' = \left(\frac{T_1}{1.25\mu S} - 1 \right) \times 100\,(\%)$$

- 2nd monostable multivibrator pulse width = T_2
- Peak shift

$$PS = \frac{1}{2} \left| \frac{T_A - T_B}{T_A + T_B} \right| \times 100\,(\%)$$

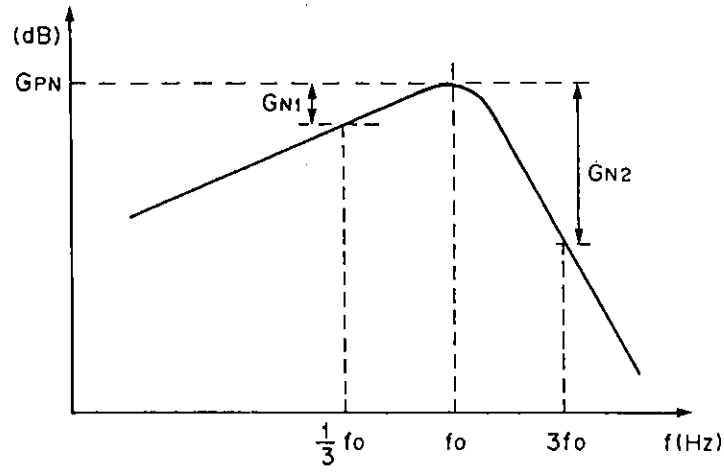
Read System (FILTER)

(Ta=25°C, Vcc=5V)

	Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
1M/Outer track	Peak frequency	f_{o1}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="H" FC="H"	1	D, E	153.0	170.0	187.0	kHz
	Peak voltage gain****	G_{P1}	See Fig. 2 at f_{o1}	1	G D, E	3.6	5.5	7.1	dB
	Frequency characteristics (1)	G_{11}	See Fig. 2 at 1/3 f_{o1}	1	D, E	−7.6	−7.1	−6.6	dB
	Frequency characteristics (2)	G_{12}	See Fig. 2 at 3f_{o1}	1	D, E	−25.0	−23.1	−21.5	dB
1M/Inner track	Peak frequency	f_{o2}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="H" FC="L"	1	D, E	163.8	182.0	200.2	kHz
	Peak voltage gain****	G_{P2}	See Fig. 2 at f_{o2}	1	G D, E	3.6	5.5	7.1	dB
	Frequency characteristics (1)	G_{21}	See Fig. 2 at 1/3 f_{o2}	1	D, E	−7.6	−7.1	−6.6	dB
	Frequency characteristics (2)	G_{22}	See Fig. 2 at 3f_{o2}	1	D, E	−25.0	−23.1	−21.5	dB
2M/Outer track	Peak frequency	f_{o3}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="L" FC="H"	1	D, E	288.0	320.0	352.0	kHz
	Peak voltage gain****	G_{P3}	See Fig. 2 at f_{o3}	1	G D, E	3.6	5.5	7.1	dB
	Frequency characteristics (1)	G_{31}	See Fig. 2 at 1/3 f_{o3}	1	D, E	−7.6	−7.1	−6.6	dB
	Frequency characteristics (2)	G_{32}	See Fig. 2 at 3f_{o3}	1	D, E	−25.0	−23.1	−21.5	dB
2M/Inner track	Peak frequency	f_{o4}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="L" FC="L"	1	D, E	310.5	345.0	379.5	kHz
	Peak voltage gain****	G_{P4}	See Fig. 2 at f_{o4}	1	G D, E	5.3	7.2	8.8	dB
	Frequency characteristics (1)	G_{41}	See Fig. 2 at 1/3 f_{o4}	1	D, E	−8.6	−8.1	−7.6	dB
	Frequency characteristics (2)	G_{42}	See Fig. 2 at 3f_{o4}	1	D, E	−36.2	−34.3	−32.7	dB

**** $G_{PN}=20\text{Log}\ (V_{Filterout}/V_{Preout})$
$V_{Filterout}$: Filter differential output voltage
(N=1 to 4)

Fig. 2 Filter Frequency Characteristics Test Conditions



(N = 1 to 4)

Write and Erase System

(Ta=25°C, Vcc=5V)

Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
Write current output accuracy*	EW	$\overline{WG}$="L" Rw=4.3kΩ	2	LKJI	−7		+7	%
Write current output unbalance	DW	$\overline{WG}$="L" Rw=4.3kΩ	2	LKJI	−1		+1	%
Write current compensation current accuracy**	EWC	$\overline{WG}$="L" Rw=4.3kΩ Rwc =12kΩ	2	LKJI	−10		+10	%
Head I/O pin leak current during write	ILKW	$\overline{WG}$="L"	2	LKJI			10	μA
Head I/O pin saturation voltage during write	VSW	$\overline{WG}$="L" SW1=b	2	L'K'J'I'			1	V
Erase current switch leak current	ILKE	$\overline{EG}$="L"	2	MN			10	μA
Erase current switch output saturation voltage	VSE	$\overline{EG}$="L" I=100mA SW2=b	2	M'N'			500	mV

* Write current output accuracy $E_W = \left(\frac{I_W}{2.70mA} - 1 \right) \times 100\ (\%)$

** Write current compensation current accuracy $E_{WC} = \left(\frac{I_W' - I_W}{0.90mA} - 1 \right) \times 100\ (\%)$

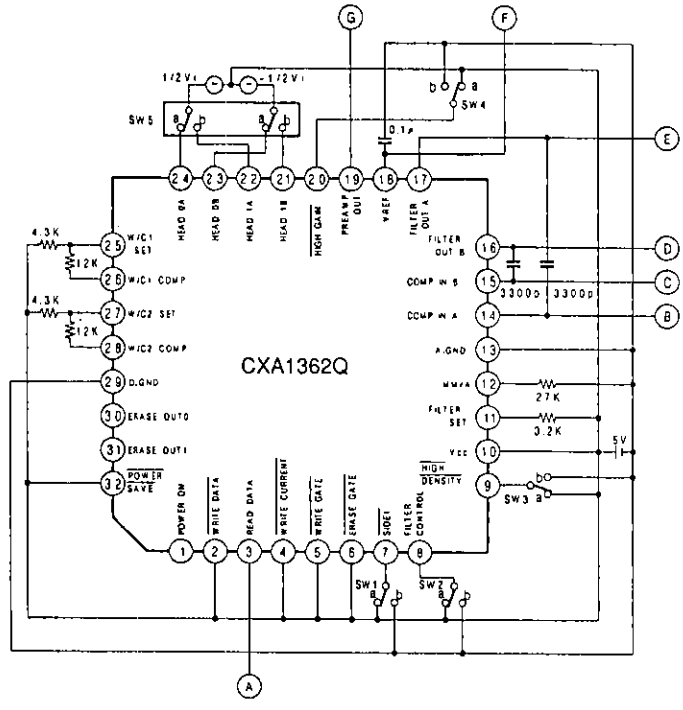
I_W : $\overline{\text{WRITE CURRENT}}$="H"
I_W' : $\overline{\text{WRITE CURRENT}}$="L"

Logic Input Section

(Ta=25°C, Vcc=5V)

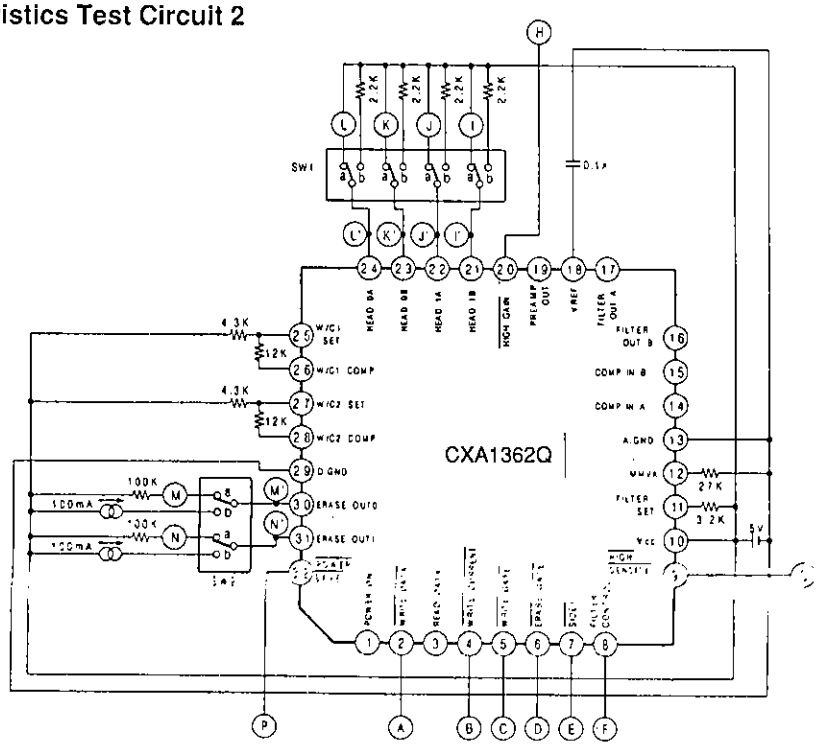
Item	Symbol	Conditions	Test circuit	Test point	Min.	Typ.	Max.	Unit
Digital signal input "L" input voltage	VLD		2	BCDE FGHP			0.8	V
Digital signal input "H" input voltage	VHD		2	BCDE FGHP	2.0			V
Schmitt type digital signal input "L" input voltage	VLSD		2	A			0.8	V
Schmitt type digital signal input "H" input voltage	VHSD		2	A	2.0			V
Digital signal input "L" input current	ILD	V_L=0V	2	ABCD EFGHP	−20			μA
Digital signal input "H" input current	IHD	V_H=5V	2	ABCD EFGHP			10	μA

Electrical Characteristics Test Circuit 1



Note) SWs are on side "a", unless otherwise specified.

Electrical Characteristics Test Circuit 2



Note) SWs are on side "a", unless otherwise specified.

Operation

(1) Read system

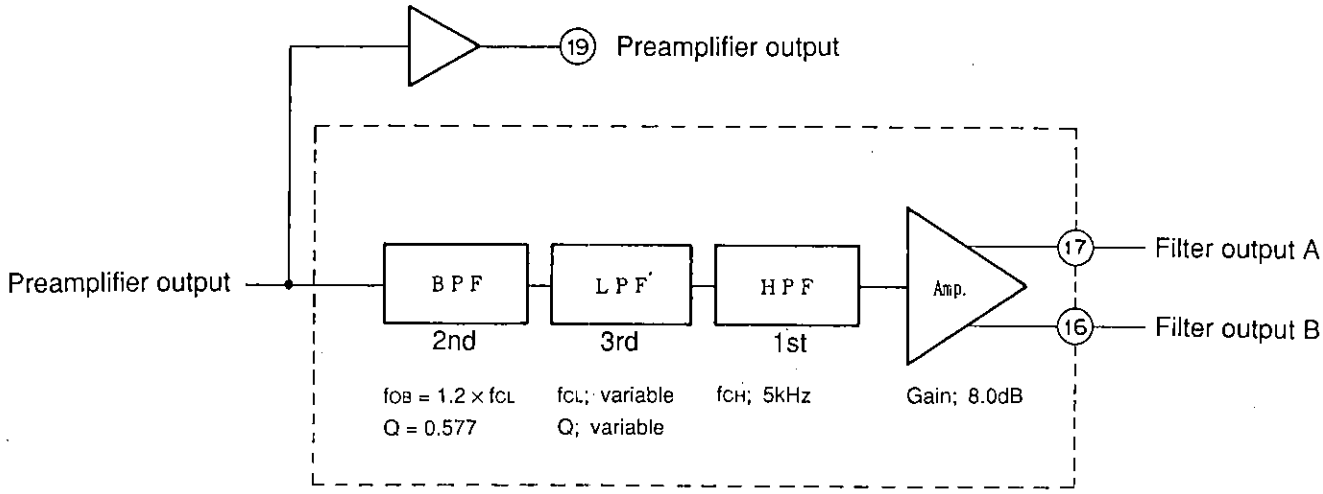
Preamplifier

The input signal is amplified.
Voltage gain can be switched to 40dB, 46dB by means of Pin 20.

Filter

The signal amplified at the preamplifiers is differentiated.
High band noise components are attenuated by means of a low pass filter.
Switching to the filter 4 modes is possible by setting Pins 8 and 9. 1M/outer track mode peak frequency f_{01} is set at the external R_F resistance.
The 3 other f_0 modes are switched according to the value set inside the IC with f_{01} (1.00) as standard.
An explanation on the filter follows.

① Active filter block



Filter characteristics

Pin 8	Pin 9	LPF characteristics	f_0 ratio
H	H	1M/Outer track mode: Butterworth	1.00
L	H	1M/Inner track mode: Butterworth	1.07
H	L	1M/Outer track mode: Butterworth	1.88
L	L	1M/Inner track mode: Chebychev 1dB ripple	2.03

Table 1

The calculation formula can be explained as follows.

$f_{01}=527/R_F+5.8$ (kHz) f_{01}: 1M/Outer track mode peak frequency
R_F: Filter setting resistance (kΩ)

Relation between f_{01} and f_0 with respect to the 4 modes.

1M/Outer track $f_{01} = 1.0 \times f_{01}$
1M/Inner track $f_{02} = 1.07 \times f_{01}$
1M/Outer track $f_{03} = 1.88 \times f_{01}$
1M/Inner track $f_{04} = 2.03 \times f_{01}$

This filter can be applied to the customer's requirements.
Application to the customer's requirements is given in pages 16 to 17.

Comparator
Detects the filter differential output cross point.

Time domain filter
Converts the comparator output into read data.
Features 2 monostable multivibrators. The first one eliminates unnecessary pulses. The second determines the read data pulses width. The first monostable multivibrator pulse width T_A is set by means of resistance R_A between Pin 12 and A. GND.
Through the setting of Pin 9, T_A can be switched as follows.

$\overline{\text{HIGH DENSITY}}$ = "H" $T_{A\,LOW} = 84R_A + 180$ (nS) R_A (kΩ)
$\overline{\text{HIGH DENSITY}}$ = "L" $T_{A\,HIGH} = 42R_A + 110$ (nS)

The 2nd monostable multivibrator width is fixed at 400 (nS).

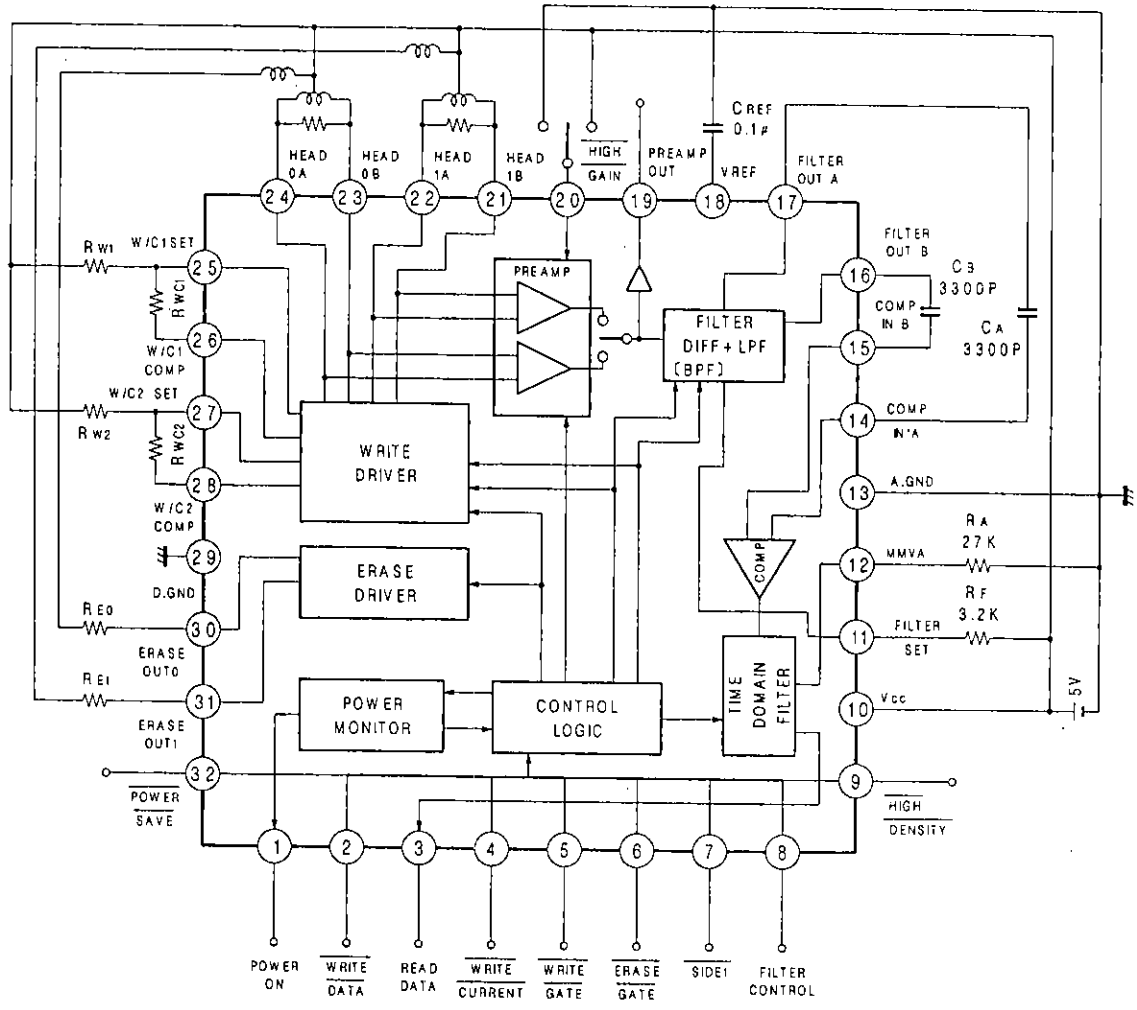
(2) Write system
Write data input from Pin 2 is divided frequency by means of a T flip flop to form the head recording current.
Switching the recording current becomes possible by setting Pin 9. Write current I_W is set by means of resistors R_W between Pin 25 and Vcc, Pin 27 and Vcc.
$I_W = 11.6/R_W$ (mA) R_W (kΩ)
Write current compensation I_{WC} is set by means of resistors R_{WC} between Pins 25 and 26, 27 and 28.
$I_{WC} = 10.8/R_{WC}$ (mA) R_{WC} (kΩ)

(3) Erase system
Pins 30 and 31 are open collector outputs. Erase current is set through the resistance between these pins and the erase head.

(4) Power supply ON/OFF detection system
Detects reduced supply voltage.
When Vcc value is below normal, write and erase operations are stopped, which recording and erase functions are prohibited.

Notes and Operation
- Select voltage gain so as to obtain a preamplifier output amplitude of 1Vp-p or less.
  Should the preamplifier output amplitude exceed 1Vp-p, the filter output waveform would get distorted.
- To mount this device, please take the following precautions.
  - Use a Vcc decoupling capacitor of about 0.1 μF and connect it as close to the device as possible.
  - Set as wide GND as possible.

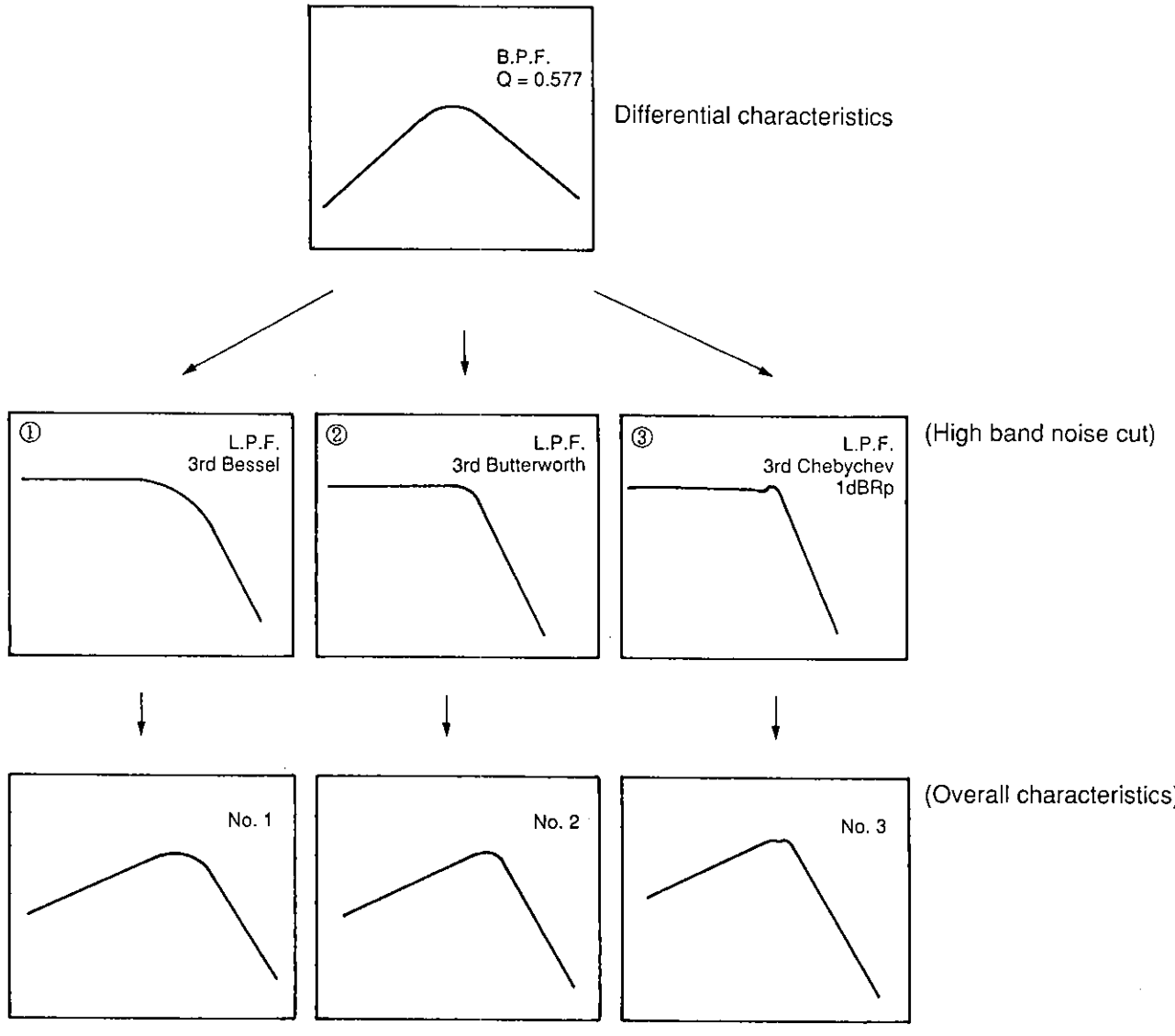
Application Circuit (for 1M/2M devices)



Customer Requirements

Filter frequency characteristics

- 4 modes: 1M/Outer track, 1M/Inner track, 2M/Outer track, and 2M/Inner track can vary the filter frequency characteristics.
- The combinations shown below are possible.



* No. 1's Bessel characteristics applicable only in 1M/outer track mode.

Filter and Customized Selection/Combination

For the filter setting, as shown in Table 1, LPF cut off frequency f_{c1} in 1M/outer track mode is set at 1.00. For the 3 other modes, f_c ratio and the type of LPF are open to selection. LPF selection can be effected from Bessel/Butterworth/Chebychev 1dB ripple. However, for Bessel only the selection of 1M/outer track is possible. BPF center frequency f_{oB} is fixed at 1.2 times LPF cut off frequency f_c. Also, the relation between peak frequencies f_o and f_c as regards overall characteristics, is set by the following formula according to the LPF difference in type.

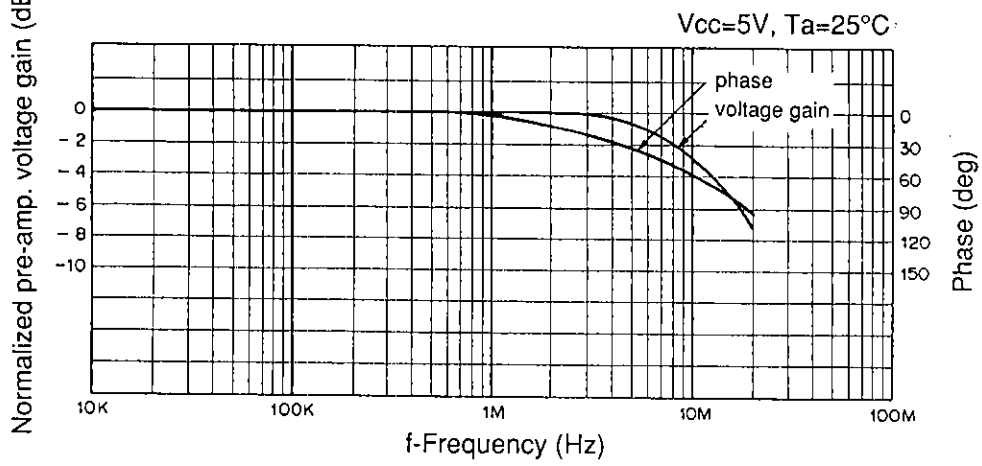
Butterworth characteristics $f_c = 1.28\ f_o$
Chebychev 1dB ripple characteristics $f_c = 1.12\ f_o$

Table 1. LPF f_c ratio and Type

Mode	LPF type	f_c ratio when f_{c1} is set to 1.00
1M/Outer track	① Bessel [② Butterworth] ③ Chebychev (1dB ripple)	[1.00]
1M/Inner track	[② Butterworth] ③ Chebychev (1dB ripple)	[1.07] 1.14 1.23 1.33 1.45 1.60 2.00
2M/Outer track	[② Butterworth] ③ Chebychev (1dB ripple)	1.33 1.39 1.45 1.52 1.60 1.68 1.78 [1.88] 2.00 2.13 2.29 2.46 2.67
2M/Inner track	② Butterworth [③ Chebychev (1dB ripple)]	1.33 1.39 1.45 1.52 1.60 1.68 [1.78] 1.88 2.00 2.13 2.29 2.46 2.67

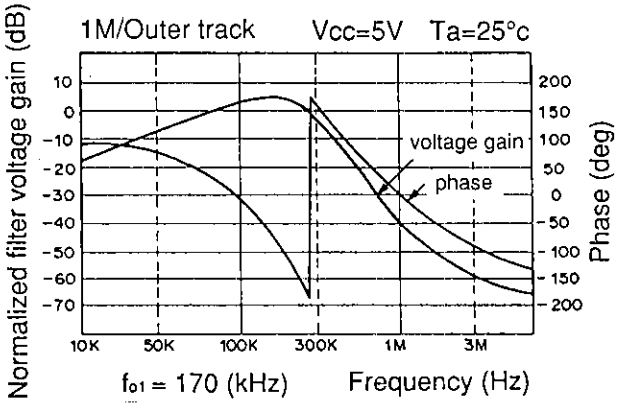
Note) In [ ] is the setting for CXA1362Q.

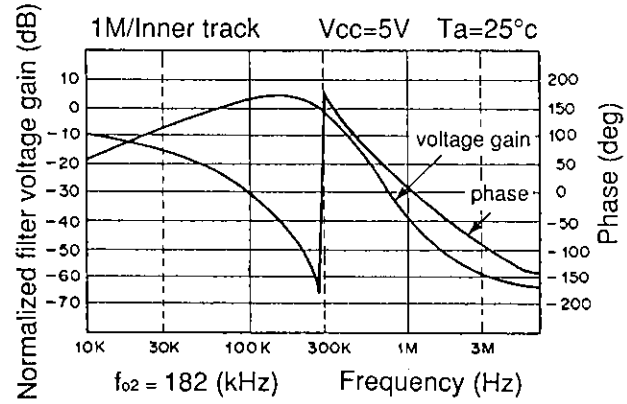
Normalized pre-amp. voltage gain, phase vs. Frequency

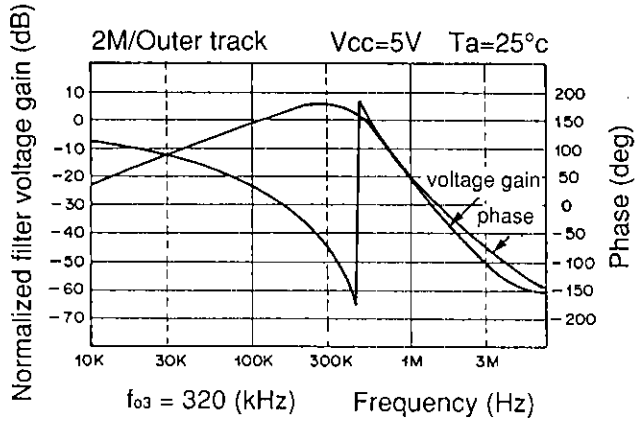


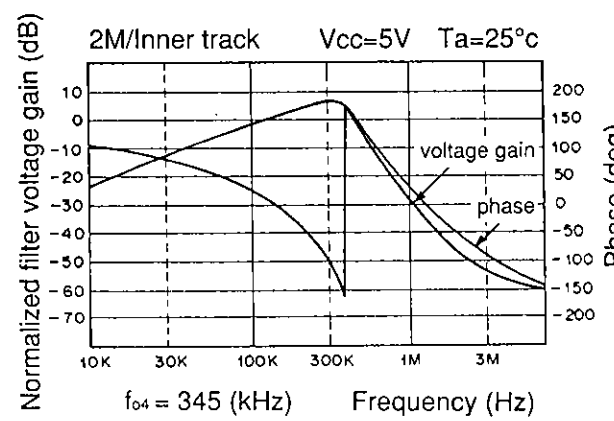
Filter 4 modes characteristics

(Characteristics where pre-amp. output is normalized. 0dB = pre-amp. output level)

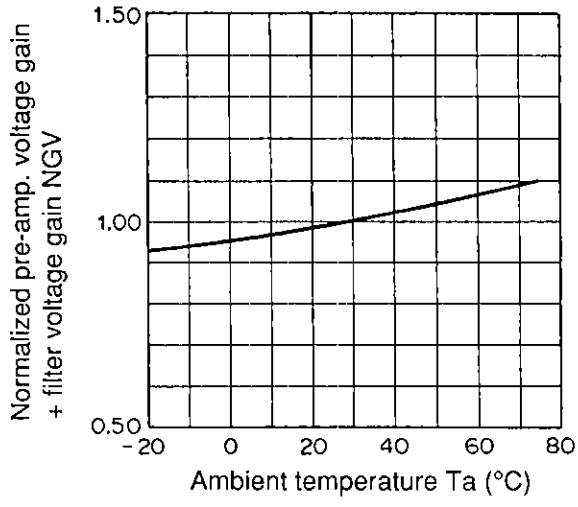




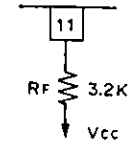




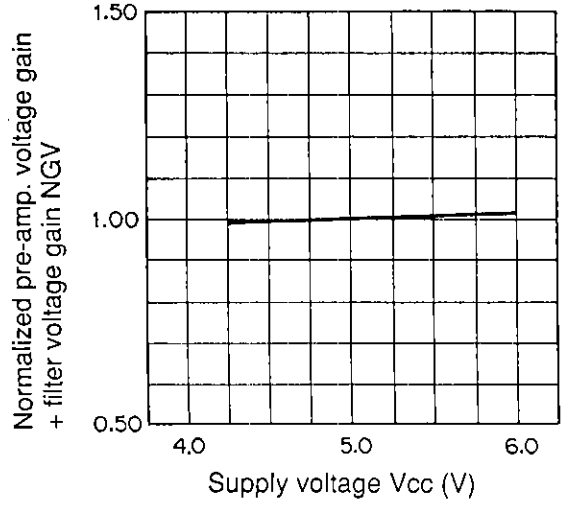
Normalized pre-amp. voltage gain + filter voltage gain NGV vs. Ambient temperature Ta



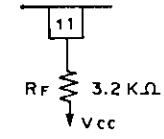
f=100kHz Vcc=5V
Vin=10mVp-p ($\overline{HG}$="H")
Vin=5mVp-p (HG="L")
NGV=GV/GV (Ta=25°C)



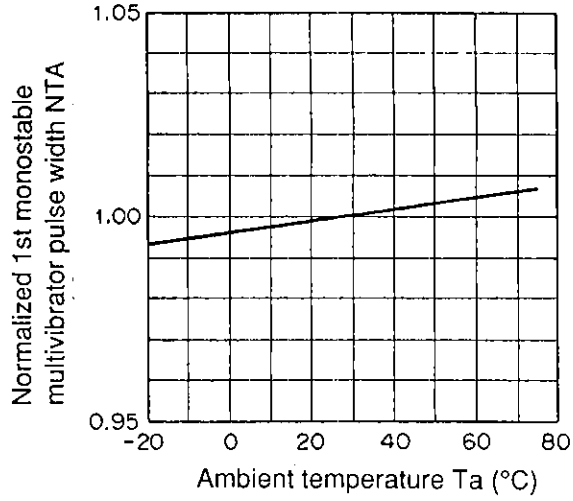
Normalized pre-amp. voltage gain + filter voltage gain NGV vs. Supply voltage Vcc



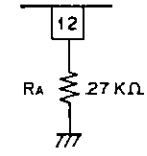
Ta=25°C
f=100kHz
Vin=10mVp-p ($\overline{HG}$="H")
Vin=5mVp-p ($\overline{HG}$="L")
NGV=GV/GV (Vcc=5V)



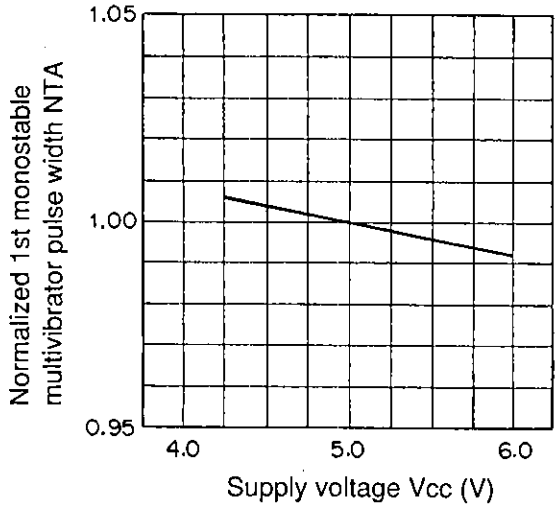
Normalized 1st monostable multivibrator pulse width NTA vs. Ambient temperature Ta



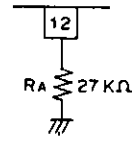
Vcc=5V
NTA=TA/TA (Ta=25°C)
at $\overline{HD}$ = "H", "L"



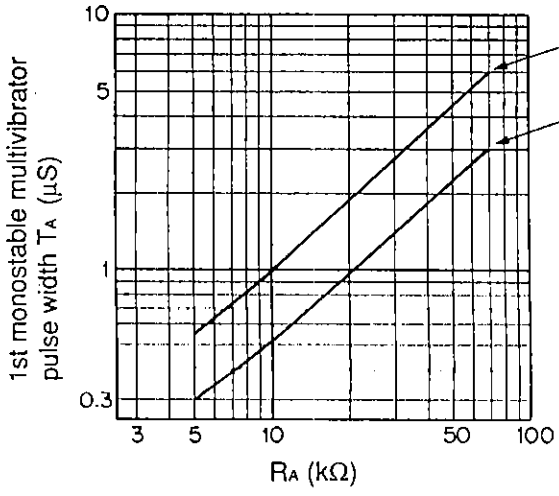
Normalized 1st monostable multivibrator pulse width NTA vs. Supply voltage Vcc



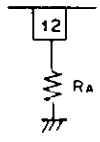
Ta=25°C
NTA=TA/TA (Ta=25°C)
at $\overline{HD}$ = "H", "L"



1st monostable multivibrator pulse width T_A vs. R_A

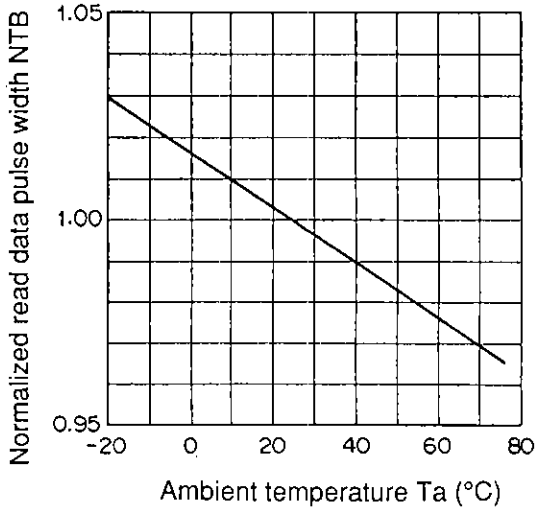


Vcc=5V
Ta=25°C



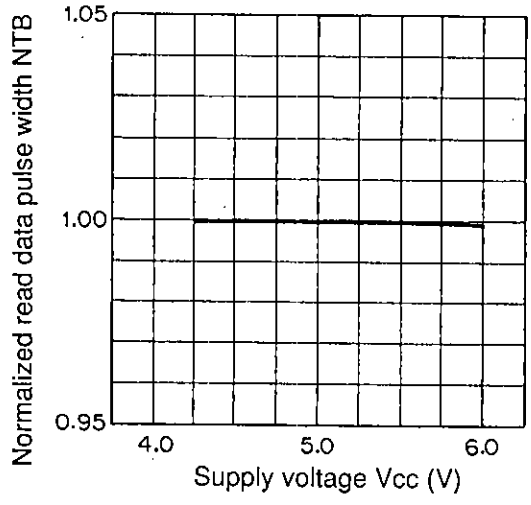
$T_{A\,LOW}$ = 84R_A + 180 (nS)
$T_{A\,HIGH}$ = 42R_A + 110 (nS)
R_A (kΩ)

Normalized read data pulse width NTB vs. Ambient temperature Ta



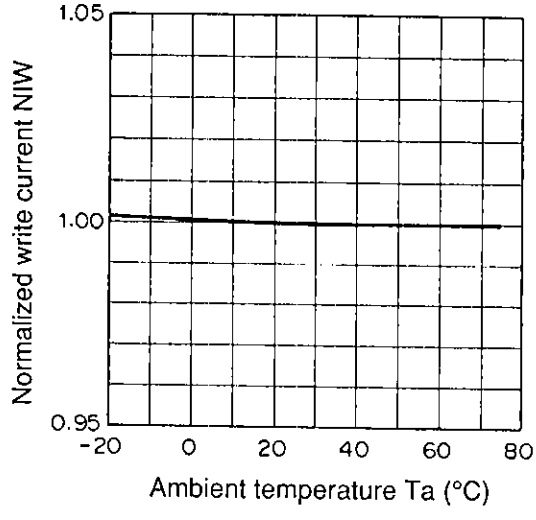
Vcc=5V
NTB=TB/TB (Ta=25°C)

Normalized read data pulse width NTB vs. Supply voltage Vcc

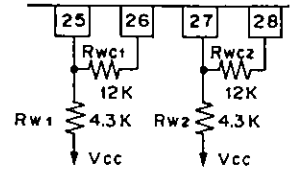


Ta=25°C
NTB=TB/TB (Vcc=5V)

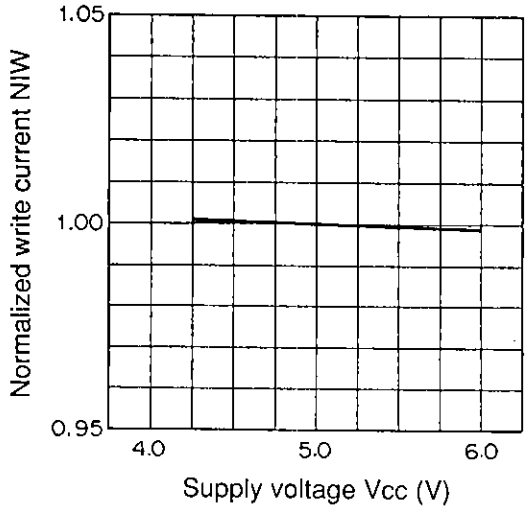
Normalized write current NIW vs. Ambient temperature Ta



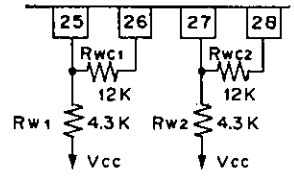
Vcc=5V
NIW=IW/IW (Ta=25°C)



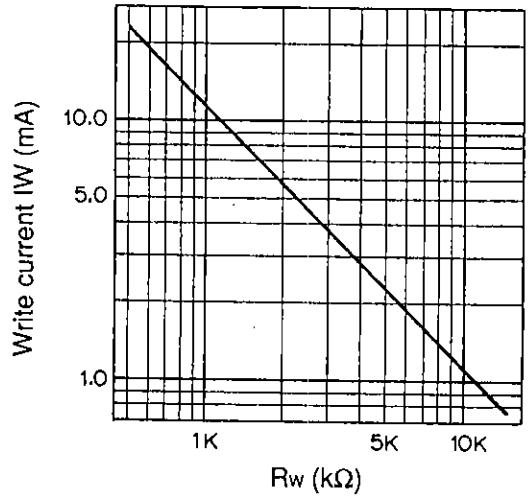
Normalized write current NIW vs. Supply voltage Vcc



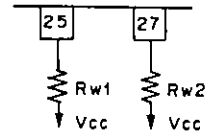
Ta=25°C
NIW=IW/IW (Vcc=5V)



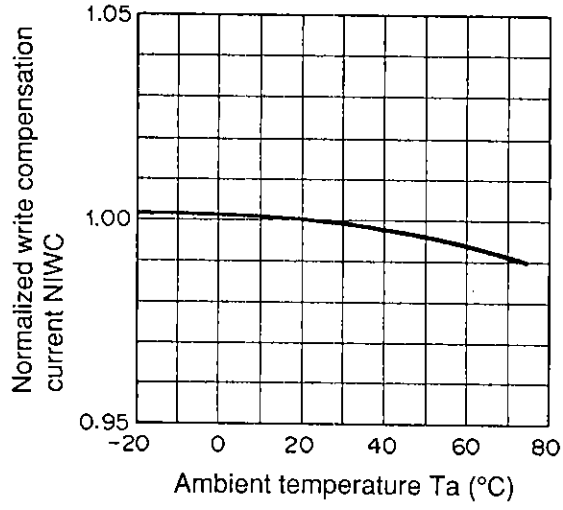
Write current IW vs. Rw



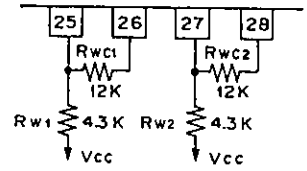
Vcc=5V
Ta=25°C
IW=11.6/ Rw (mA)
Rw (kΩ)



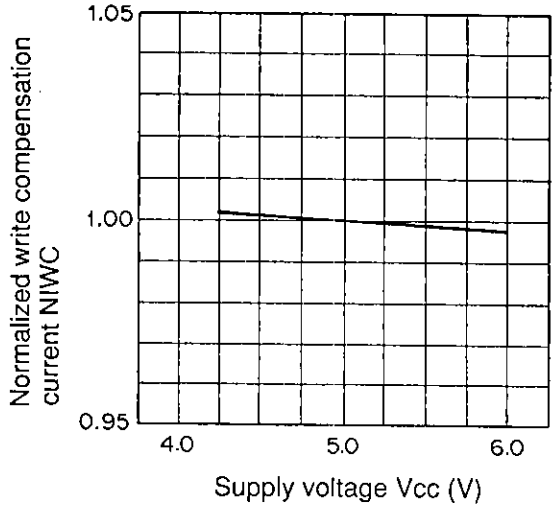
Normalized write compensation current NIWC vs. Ambient temperature Ta



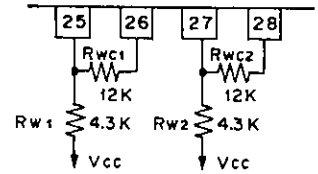
Vcc=5V
NIWC=IWC/IWC (Ta=25°C)



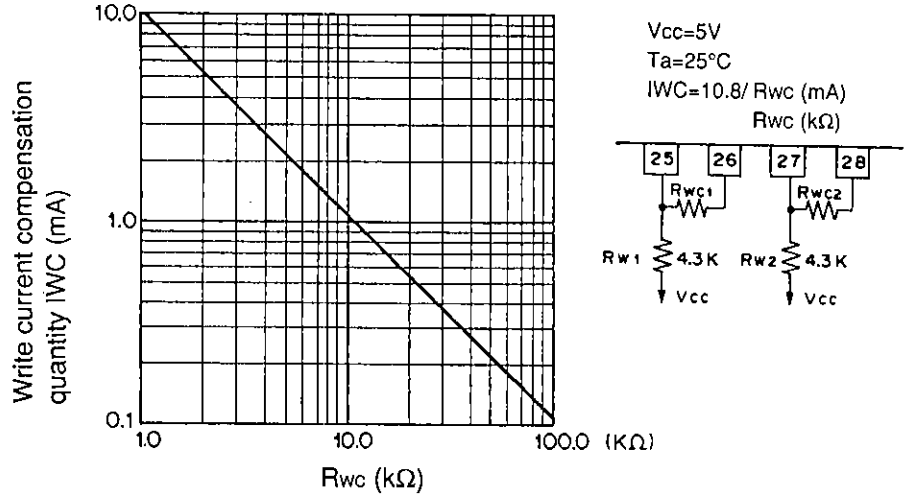
Normalized write compensation current NIWC vs. Supply voltage Vcc



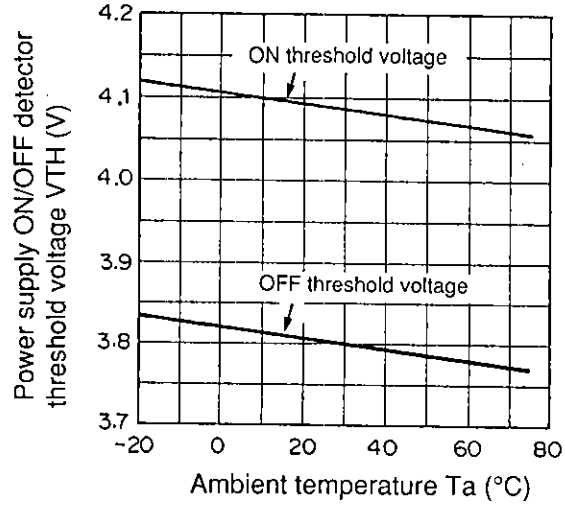
Ta=25°C
NIWC=IWC/IWC (Vcc=5V)



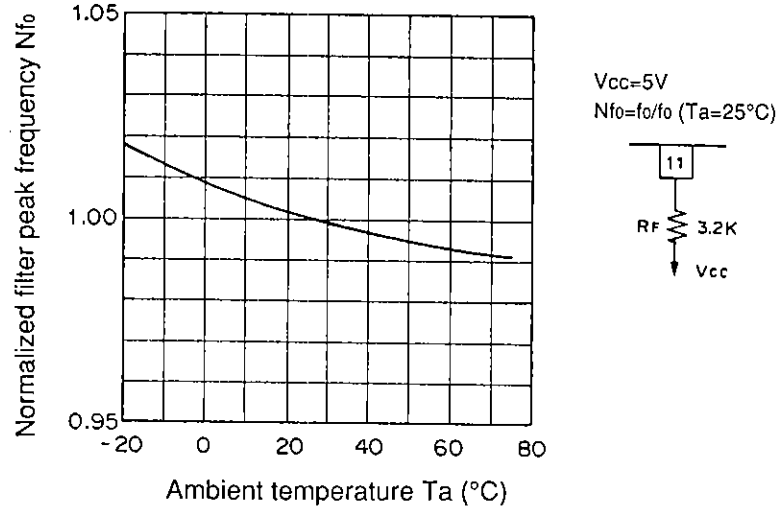
Write current compensation quantity IWC vs. Rwc



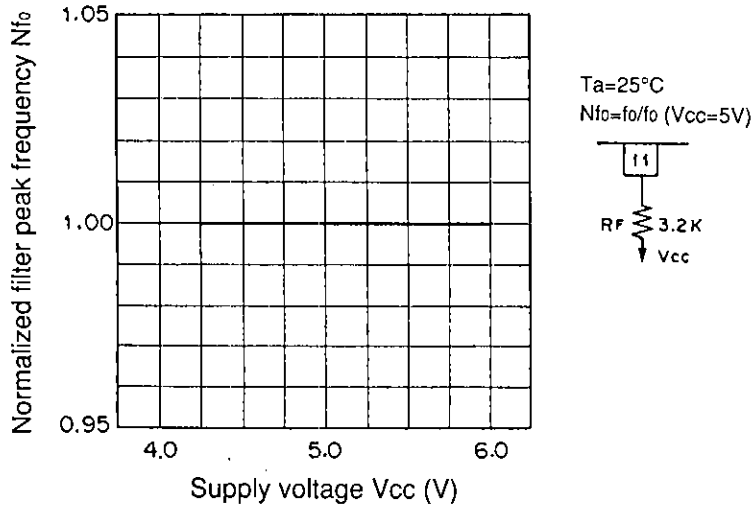
Power supply ON/OFF detector threshold voltage VTH vs. Ambient temperature Ta



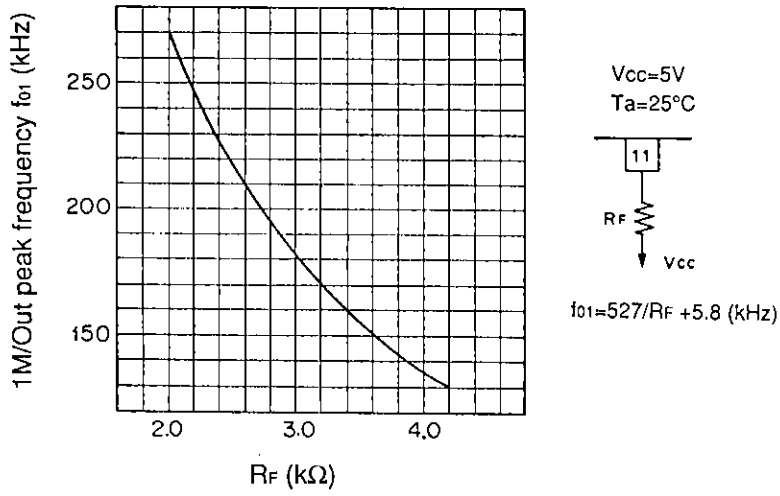
Normalized filter peak frequency Nfo vs. Ambient temperature Ta



Normalized filter peak frequency Nf_0 vs. Supply voltage characteristics Vcc

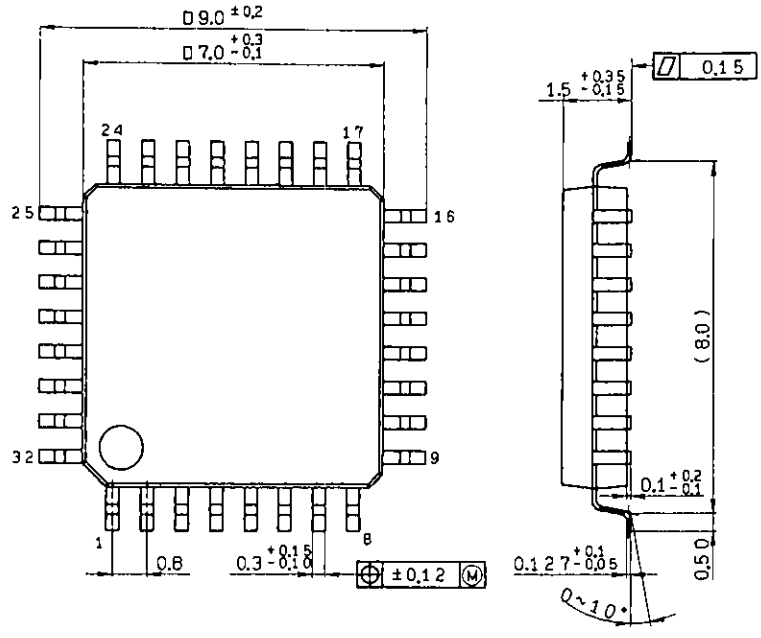


1M/Outer track peak frequency f_{01} vs. R_F



Package Outline Unit: mm

32pin QFP (Plastic) 0.2g



QFP-32P-L01