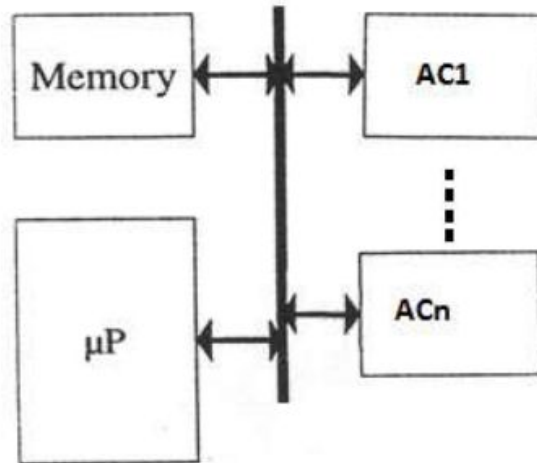


Project Context of Hardware Software Co-Design

Simulating a system contains Microprocessor/Accelerator/Bus and their connection via SystemC



1. Design a cpu (micro-processor) in [SystemC](#) language consists of the instructions below:

- [ALU instructions](#) according to the Opselect codes determined below

Operation select				Operation	Function
S_3	S_2	S_1	S_0		
0	0	0	0	$F = A$	Transfer A
0	0	0	0	$F = A+1$	Increment A
0	0	0	1	$F = A+B$	Addition
0	0	0	1	$F = A+B+1$	Add with carry
0	0	1	0	$F = A+B$	Subtract with borrow
0	0	1	0	$F = A+B+1$	Subtraction
0	0	1	1	$F = A - 1$	Decrement A
0	0	1	1	$F = A$	Transfer A
0	1	0	0	$F = A \wedge B$	AND
0	1	0	1	$F = A \vee B$	OR
0	1	1	0	$F = A \oplus B$	XOR
0	1	1	1	$F = A$	Complement A
1	0	×	×	$F = \text{shr } A$	Shift right A into F
1	1	×	×	$F = \text{shl } A$	Shift left A into F

- ``load`` and ``store`` operations with arbitrary opcodes
- In this cpu, we can also stop the current task after calling an accelerator to do some other task.

This accelerator can have an internal implemented algorithm (pure c++ code)

This accelerator is connected to the bus just like the shared memory

So if we wanna access the accelerator, we need to have an additional signal which we name it ``call`` signal.

2. This cpu works as a `pipeline` architecture

3. Implement an `8 KB Memory` and connect it to the bus. Each row of the memory is 8 bits.

4. By writing a testbench, simulate a real algorithm.

**

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UNIVERSITY: KHAJE NASIR TOOSI UNIVERSITY (@KNTU)

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