Precision Current Source: 0-1mA

Input: Digital PWM Signal from Microcontroller with voltage range 0-3.3V, frequency range: 1kHz to 10kHz.

Output: 0-1mA constant current across resistive load 10Ω to 500Ω.

Resolution: 10µA per step, with 100 steps.

Current error: ±2µA across temperature.

INTRODUCTION

This document outlines the design process for a precision constant current source with an adjustable output range of 0 to 1mA. The input to the source would be a PWM signal from the Microcontroller, defining voltage range as 0 to 3.3V. Output is a constant current source with 0 to 1mA range of 10µA resolution. For a resolution of 10µA and 0 to 1mA range, 100 control steps are required, which we get from changing the Duty cycle from 0-100% in the PWM signal. Explored design approaches, are discussed in detail in following sections

ASSESMENT OF EXPLORED DESIGN APPROACHES

Howland current pump: As shown in Fig1, is a circuit that accepts an input voltage v_I, converts it to an output current $i_O = Av_I$, with A as the transconductance gain, and pumps i_O to a load, regardless of the voltage v_L developed by the load itself.

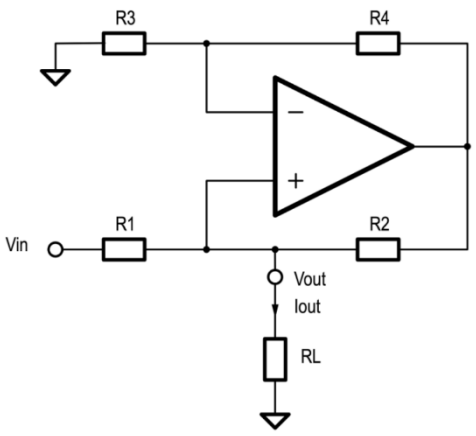


Fig1: Howland Current Pump

The Howland current pump is a voltage controlled current source, which satisfies the requirement criteria of our current source. Howland circuit relies on a balanced bridge configuration. Mismatched resistors break this balance, causing the circuit to behave more like a voltage source than a current source. As the input voltage is analog, the smallest non-zero voltage you can apply determines the smallest current. Although the exact Howland design is not used in the final design, it has been built using the Howland concept.

Precision 4-20 mA Source: 0–1 VDC input.

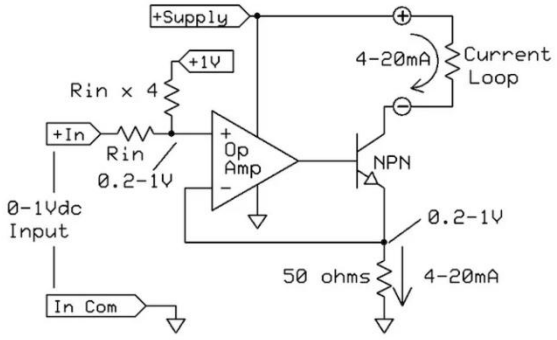


Fig2: Precision Current Source 4-20mA

The two input resistors convert it to 0.2-1.0 V, creating the 4mA output offset. Op-amp

feedback holds the emitter output equal to the 0.2–1.0 V input. The 50 Ω resistor converts this to the 4–20 mA output current. While this design can be brought to range 0-1 mA, the practical circuit of this design requires 24V supply, while it can work on 5V. The 24 V output supply supports output resistance up to about 1100 Ω (22 V at 20 mA). Transistors can exhibit non-linear behavior at low collector currents, especially below 1 mA, which may affect accuracy. Transistor parameters (like V_BE) vary with temperature, and this variation becomes more pronounced at low currents. The requirement is low current, and transistor is a hinderance to this low current requirement, because of these limitations, this design is not suitable for 0–1 mA operation.

FINALIZED CORE DESIGN

Current requirement being low 0-1mA, a simplified design without transistor has been finalized. The op-amp is configured as a **voltage-controlled current source.** It adjusts its output to ensure the voltage across the sense resistor R_{sense} matches the control voltage $V_{control}$. Since the op-amp forces the voltage across R_{sense} to be equal $V_{control}$ *[virtual short]*, the output current I_{out} through the load is:

$$I_{out} = \frac{V_{control}}{R_{sense}}$$

Given:

$$V_{control}=3.3\ \text{V}$$

$$R_{sense} = 3.3\ \text{k}\Omega$$

$$I_{out} = \frac{3.3V}{3.3\ k\Omega}$$

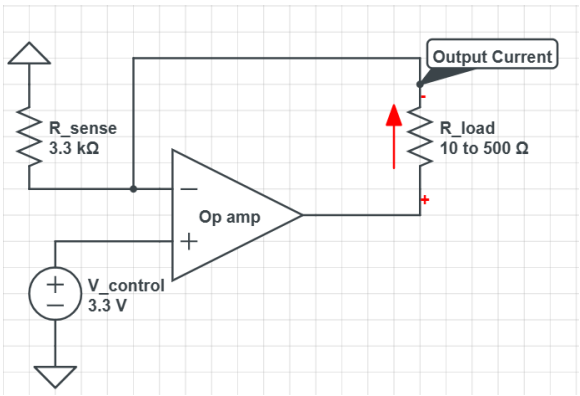


Fig3: Current Source Core Design

To maintain the desired current, the op-amp must provide an output voltage:

$$V_{out} = I_{out} \times R_{load}$$

This means the op-amp must be able to swing its output voltage from:

V_{out}(min) =1mA×10Ω=10mV

to

V_{out}(max) =1mA×500Ω=0.5V

Thus, the op-amp must be capable of outputting at least 0.5 V to support the full range of R_{load}.

VOLTAGE CONTROL THROUGH PWM DUTY CYCLE

To convert a digital PWM signal to Analog, we need a Digital to Analog Converter. Here the design uses an RC Low Pass Filter. For a smooth DC, cut off frequency of Low Pass Filter is chosen to be 1Hz, with R=10kΩ and C=15µF components. The output voltage from the RC filter (treated as a simple DAC) is directly proportional to the duty cycle of the input PWM signal:

$$V_{dc} = D \times V_{on}$$

Where:

- $V_{dc}$is the filtered DC voltage
- D is the PWM duty cycle (0 to 100)
- V_{on}=3.3 V

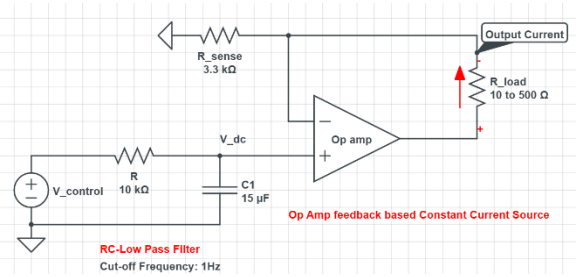


Fig 4: PWM-Analog Circuit

Settling Time of the RC Filter

The RC filter introduces a delay in the response of the system. The **settling time** (to within 1% of the final value) for an RC low-pass filter is approximately:

$$t_s \approx 5RC$$

Given:

R=10kΩ

C=15µF

$$t_s \approx 5 \times 10000 \times 15 \times 10^{-6} = 0.75s$$

This means that after any change in PWM duty cycle, the output voltage—and hence the regulated current—will stabilize within approximately **1s**.

Parameter	Value
Control Range (Current)	0–1 mA
Resolution	10µA (100 steps)
$V_{control}$ Resolution	~33 mV per step
RC Filter Cutoff Frequency	~1 Hz

Table1: Design Specifications achieved by the end of this section.

CHOICE OF OP AMP

Parameter	Requirement	Purpose/ Impact
Supply Voltage (V+)	5 V ±5%	Standard single-supply operation
Input Bias Current	<100 pA (ideally <10 pA)	Minimizes error in low-current sensing circuits
Input Offset Voltage	<10 µV (ideally <5 µV)	Ensures accurate control of small voltage differences
Offset Voltage Drift	<0.05 µV/°C	Maintains precision across temperature variations
Output Drive Capability	≥1 mA	Source/sink required current without distortion
Output Swing from Rails	Typ ≥10 mV, Max ≤30 mV (no load)	Allows near full-range output for better control resolution
Architecture	Rail-to-Rail Output, CMOS or Zero-Drift	Ensures low noise, high precision, and full-range output swing

Based on above parameters, Op Amp selected for circuit simulation testing are:

1. AD8675
2. AD8628
3. OPA192
4. ADA4522-1
5. OPA387

Expected results were observed in the simulation with these op amps. From the lab

inventory, precision op amps were listed and verified for a match with the above op amp criteria, in this case on board circuit testing could be performed immediately. **AD8574** was found to match the criteria and thus simulation testing was performed using **AD8574.** Note that AD8571/AD8572 could also be used as they belong to the same AD857 series. AD8574 was used as it was available.

LT-SPICE SIMULATION

On the next step, the finalized circuit as shown in Fig4 is simulated in LTspice.

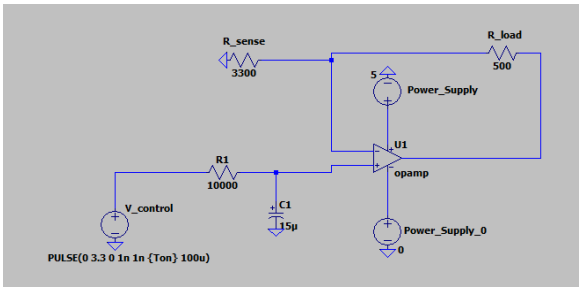


Fig 5: LTspice simulation circuit

PWM signal is generated using a Pulse voltage source. AD8574 op amp is selected from components in LTspice. Circuit connections are made and tested for validation of circuit working across the range of 0 to 1mA, using $\{T_{on}\}$ as parameter, command: .step param Ton 10u 100u 1u.

Here 100u period is equal to 10kHz frequency. Duty cycle change is simulated by varying pulse on Time, Ton step wise, start value 1u to 100u in 1u steps. The same was simulated for 1000u period and 1kHz frequency of PWM. After verification that circuit works through 0 to 1mA. Worst Case Analysis and Monte Carlo Analysis with consideration of resistance tolerances, temperature co-efficient has been performed which will is in further sections of the document.

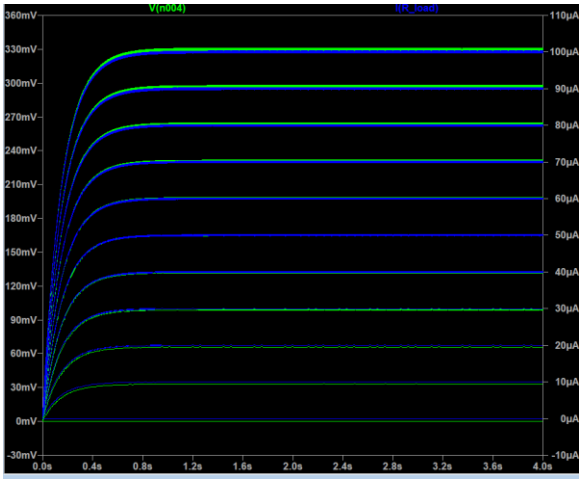


Fig 6: Graph of output current in range 0-100µA with 10µA steps.

CIRCUIT CHARACTERIZATION:

Circuit Characterization is done in four steps as below:

- Step1: Output Range Verification, here 0-1mA
- Step2: Only Tolerances of the circuit components are to be considered.
- Step3: Keeping input constant, change in Load across 10Ω to 500Ω, i. Without Tolerance in R, C ii. With Tolerance in R, C.
- Step4: Add all variables to circuit tolerances, temperature co-efficient, load regulation.

Step1 is performed in above section and results have been recorded.

Step2: Effect on current, with Tolerance of circuit components

To determine and ensure the circuit performs reliably across real-world variations in component values and environmental conditions, simulation of circuit elements resistance and capacitance with **tolerance** and **temperature coefficient** in LTspice is performed. Worst Case analysis across various values has been recorded and presented below.

Note: Simulation is performed across temperature -40°C to 85°C. Below readings are of extreme deviations from expected values for 10µA and 1000µA i.e extreme values for 0 to 1mA. With Constant Load = 500Ω.

SL. No	R_{sense}(Ω)	Duty Cycle, I_load Expected (%, µA)	I_load (µA)
1	3352.33	1, 10	9.851
2	3245.11	1, 10	10.172
3	3352.33	100, 1000	984.388
4	3245.11	100, 1000	1016.910

Table2: R_{sense} tolerance = 1%, Temperature Co-efficient = 100ppm.

For 10µA across temperature a deviation of ±0.172µA is observed and for 1000µA across temperature a deviation of ±16.910µA is observed. According to the requirements, ±2µA is acceptable, which is not seen in the observed readings. As per equations of circuit, accuracy of R_{sense} determines the accuracy of Current. Based on this we move on to a 0.1% tolerance resistance for R_{sense} Recorded observations are below.

SL. No	R_{sense} (Ω)	Duty Cycle, I_load Expected (%, µA)	I_load (µA)
1	3322.46	1, 10	9.940
2	3274.61	1, 10	10.080
3	3322.46	100, 1000	993.239
4	3274.61	100, 1000	1007.750

Table3: R_{sense} tolerance = 0.1%, Temperature Co-efficient = 100ppm.

For 10µA across temperature a deviation of ±0.080µA is observed and for 1000µA across temperature a deviation of ±7.750µA is observed. These specifications do not satisfy ±2µA, across temperature. The effect of temperature co-efficient is significant, now we change temperature co-efficient to lower value and see the effect on current.

SL. No	R_{sense}(Ω)	Duty Cycle, I_load Expected (%, µA)	I_load (µA)
1	3308.09	1, 10	9.983
2	3291.18	1, 10	10.029
3	3308.09	100, 1000	997.553
4	3291.18	100, 1000	1002.680

Table4: R_{sense} tolerance = 0.1%, Temperature Co-efficient = 25ppm.

For 10µA across temperature a deviation of ±0.029µA is observed and for 1000µA across temperature a deviation of ±2.680µA is observed. These observations are close to the ±2µA, we require.

Further testing with R_{sense} tolerance = 0.01% and temperature co-efficient = 10ppm,

5ppm, 2ppm has been simulated and recorded. Link to observations attached here: Link.

Step3: Keeping input constant, change in Load across 10Ω to 1500Ω

i. Without Tolerance in R, C.

SL. No	R_{load} (Ω)	Duty Cycle, I_{load} Expected (%, µA)	I_{load} (µA)
1	10	1, 10	10.002
2	1500	1, 10	10.008
3	10	100, 1000	999.999
4	1500	100, 1000	999.998

Table5: R_{sense} = 3.3kΩ, R_{sense} tolerance = 0.1%, Temperature Co-efficient = 25ppm.

For 10µA across temperature a deviation of 0.6% is observed and for 1000µA across temperature a deviation of 0.0001% is observed.

ii. With Tolerance in R, C.
Here observations are made by changing load from 10Ω to 1500Ω in a excel sheet with link attached here: Link.

Two important observations made here are change in resistance from 10Ω to 1500Ω has an effect of ±0.01µA across all values of range 10µA to 1000µA. This conclusion is drawn from comparison between current values at 10Ω and 1500Ω. These values are consistent with the values observed at R_{sense} tolerance = 0.1%, Temperature Co-efficient = 25ppm which is expected as the tolerance values considered were the same. But the goal here is to observe the effect on current because of change in resistance which is recorded as ±0.01µA.

Step4: Add all variables to circuit tolerances, temperature co-efficient, load regulation.
In this step, goal is to observe the effect on current for Duty Cycle change. To verify this Monte-Carlo Analysis approach was used with mc(value, tolerance). The maximum deviation from Duty Cycle and Current is 0.00000001, which is not significant deviation. Link to the observations made along with Step2, Step3 and Step4 in monte carlo analysis for 250 steps is attached here: Link.

ON BOARD CIRCUIT TEST
The Finalized circuit as in Fig4 was built on breakout board.

Setup:

- AFG: Generation of PULSE signal - PWM.
- DSO: Measurement of generated Pulse signal
- DMM: Measurement of V_dc and I_load current
- Power Supply: 5V for Op Amp

After building the circuit and testing, it was found that the voltage generated by AFG as measured on DMM was not accurate. For values with duty cycle set to 0-10% and 90-100%, there is a increase in voltage generated upto 8.8%. In PWM generated from the MCU, accuracy of the voltage value is dependent on LDO output which has an accuracy of 2%. This will impact output current accuracy. To solve the above problem of accuracy, use of

a comparator and V_{ref} IC design was employed.

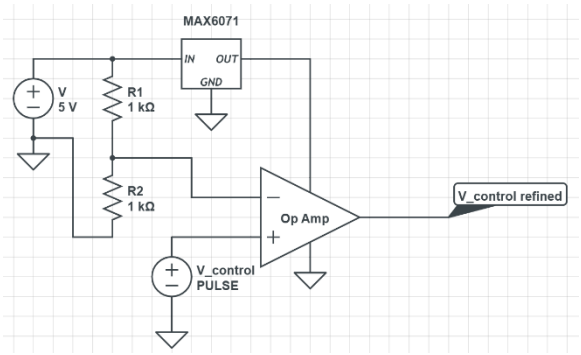


Fig 7: V_{ref} IC, comparator circuit

A Voltage Reference IC which gives constant output voltage of 3.3V, with ±0.04% initial accuracy is used in a comparator design. The $V_{control}$ refined output of this part is given as input to Low Pass filter. This addresses the error in voltage of $V_{control}$. For testing of this circuit, available IC in lab was MAX6071 with 3V constant output. For purpose of testing of this circuit the same IC is used. Op Amp is chosen to be the one already in use AD8574. Initial testing showed the expected result where 3V constant output is generated at Voltage Reference IC.

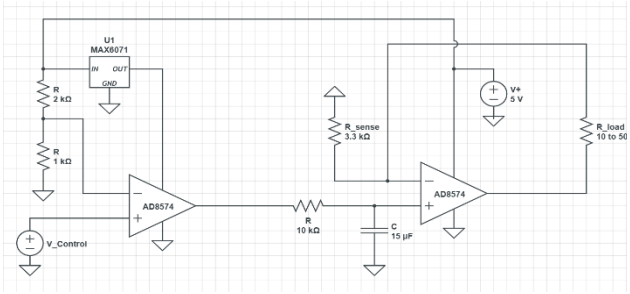


Fig8: Circuit On-Board

Fig8 circuit was built on board with AD8574-Op Amp, MAX6071 IC. Measurements were taken at 4 points as shown in Fig8.

1. Input: DSO measures the input from AFG. Voltage, Frequency, Duty Cycle, Positive Width of Pulse are measurements made.
2. V_{ref} [3V pulse signal]: Output at comparator. DSO measures Voltage, Frequency, Duty Cycle, Positive Width of Pulse.
3. V_{dc}: DMM measures the DC Voltage at point 3
4. Current: Output current across load is measured using DMM, DC current.

Link attached to observations made in this circuit at 4 points is here: Link.

Key observations from this testing stage are:

- AD8574 is not the correct Op Amp choice for comparator as there is distortion of frequency from input to output of comparator, with maximum error in positive pulse width being 1.24µs.
- Current output is consistent with Duty Cycle at point 2.
- Increase in AFG output voltage as measured in point 1 for Duty Cycle 0-10% and 90-100%.

Selection of appropriate Op Amp for comparator, part 1 of the circuit was carried out next.

Op Amp required in comparator needed to have high slew rate as to not have distortion in frequency, the frequency range in requirement is 1kHz to 10kHz. In LTspice AD8574 was replaced with Universal Op Amp and it was observed that the difference in frequency between point 1 and point 2 i.e input to comparator and output at comparator.

Parameter	Specification	Purpose
Slew Rate	≥7V/µs	Eliminate distortion in input and output of comparator
Rail-to-Rail I/O	Yes	A pulse signal is to be generated with range 0-3.3V, thus rail to rail I/O is required
Power Supply	2.7V to 5V	Op amp should be powered by 3.3V

Table6: Comparator Op Amp specifications

Simulations were performed in LTspice of Op Amps for comparators MAX4230, OPA4342, AD8040 and AD8031. AD8031 had the best results thus AD8031 was chosen as the final Op Amp for Comparator part of circuit.

AUTOMATION OF INSTRUMENTS

The Setup of ADF, DSO and DMM was automated using **Python and PyVisa**. USB-B cable was connected to the instrument and USB-A to Laptop/PC. NI-Visa software was installed for instrument recognition by Laptop/PC. VS Code used for python code editing and command panel. This setup was used in two ways:

1. DSO and DMM were connected to Laptop/PC and automation was used to read the measurements, Input Duty Cycle from 1-99% was given manually.
2. AFG-DSO and AFG-DMM, here AFG was automated to give input Pulse and vary Duty Cycle from 1-99%, DSO and DMM were used for measurements automation in different setups.

All measurements made were after a settling time of ~2-3s, this can be modified in the code and for each measurement a sample of 10 values in intervals of 0.1s were taken, returned value was averaged value of the 10 samples. These samples and intervals in which the samples were recorded can also be modified in the code. The final output was stored in a CSV file which was further used to draw conclusions.

FINALIZED CIRCUIT COMPONENTS

SL.No	Description	Part number (Quantity-1)
1	Op Amp	AD8571
2	Op Amp	AD8031
3	V_{ref} IC	MAX6070_33
4	Resistor RC filter	10kΩ, 1%
5	Capacitor RC filter	15µF
6	Voltage Divider Resistor	1kΩ, 1% - Quantity-2
7	R_{sense} Resistor	3.3kΩ, 0.1%, 10ppm

Table7: Final Circuit components

With the finalized components, the required components order was placed, and components were procured.

FINALIZED CIRCUIT TESTING

Circuit was built on breakout board as per Fig.9, and testing was done at 4 points as shown in the figure.
1. Input signal – DSO measurement
2. Input signal after Voltage Regulator – DSO measurement

3. V_{dc} – Average voltage after low-pass filter

4. Output current – constant current across load

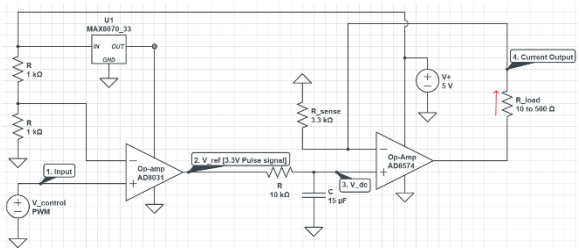


Fig 9. Current source design – finalized tested circuit

At points 1 and 2 measurements were made of the PWM control signal, it's accuracy in terms of voltage level i.e 3.3V, frequency tested at 1kHz and duty cycle. The recorded values of these parameters are tallied against expected values. At point 3 average voltage value after conversion from digital to analog are made which should span from 0, 0.033 to 3.3V. At point 4 current is measured, and direction of current is shown in circuit diagram Fig.9.

Circuit built on breakout board is shown in Fig.10. This circuit is implemented in 2 stages, first the Voltage regulator and comparator, second the current source design using Op-amp and R_{sense} resistor along with low-pass filter.

File with recorded observations: Link

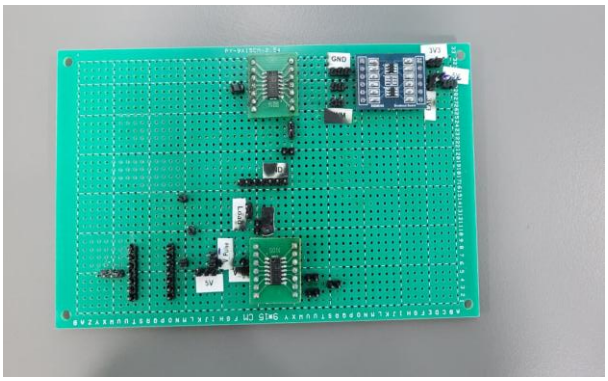


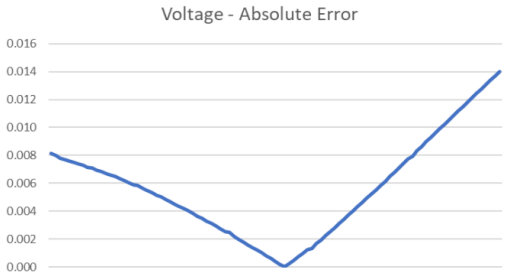
Fig.10 - Circuit on board

KEY OBSERVATIONS FROM CIRCUIT TESTING

1. At point 1, the voltage level can be anything from 1.85V - 3.3V depending on the input device used, for a nucleo board it is 1.85V for a ESP it is 3.3V and using AFG it can be set to any level.
   Note: The comparator –ve input should be less than the voltage level of input device. This can be configured by changing the resistor in voltage divider circuit.
   Duty cycle should be accurate at this stage.
   With ESP we notice a deviation of 0.05-0.08% and with Nucleo board we notice a deviation of $\pm$0.02%.
2. At point 2, i.e after the comparator, we need to check for the voltage level accuracy as this is the goal of introducing a comparator in the circuit. Also the op-amp with higher slew rate was chosen as to not distort the duty cycle.
   Duty cycle in both ESP and Nucleo board inputs is same as point 1, thus the choice of higher slew rate op-amp was found to be correct.

The voltage level – was found to lie between 3.24V-3.28V accounting for the rail-to-rail output after 0.05V and 0.2V voltage swing characteristic from AD8031 op-amp (from datasheet).
However an interesting observation here was that on the initial and final duty cycles, i.e 0-5% and 95-100%, there is a peak in measured voltage level compared to all other duty cycles voltage measurement – 3.9-3.68V for ESP and 3.47V for nucleo board. After consistently observing this pattern, a compelling explanation was accepted: at low and high duty cycle extremes, fast and sharp transitions during high switching activity cause voltage spikes, which are captured by the DSO and reflected in the peak-to-peak measurement.

3. V_{dc}: Voltage value should be from 0-3.3V with increments of 0.033V at each level, giving 100 levels, we can see the absolute error in measured values across 0.008-0.014V for nucleo board and 0.011-0.017V for ESP. This error is due to the combination of error from voltage level and duty cycle. However, the acceptable error in range is for 23-88% duty cycle in ESP and 23-80% in nucleo board.
4. Output current: The direction of output current is given in the diagram, in application case where this design will be used, a load of range 10-500Ω tested or up to 2kΩ as per simulations can attached and a constant current as per input duty cycle control value would be seen. Error in current acceptable would be ±2µA. This is observed across duty cycle range 23-80% in nucleo board and 23-88% in ESP.



SUMMARY

A PWM signal is given as input and an output current source, which is controlled by the duty cycle of the PWM signal. The current output level ranges from 0 to 1 mA with increments of 10 µA. Circuit design, simulations in LT spice, Monte Carlo Analysis, Worst case analysis, and circuit testing on board, automation testing instruments DSO, AFG, DMM, using Python and PyVISA, analysis of on-board testing measurements. The above tasks were performed under this design task.