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Computer Organization & Assembly Language

Assignment # 3

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Q. No 1 Compare characteristics

	Intel 4004	Intel 8080	Intel 8086	Intel 80286	Intel 80386
Data bus	4 bits	8 bits	16 bits	16 bits	32 bits
Address bus	12 bits	16 bits	20 bits	24 bits	32 bits
Size of Cache (if any)					
clock rate	400-800 KHz	2 MHz	5-10 MHz	20 MHz	16-33 MHz

Q. No 2 Define the following and mention microprocessors

- Interrupts
  Interrupts are signals which tell the CPU to stop the current task and begin the new task.
  Introduced with : Intel 8008 (1972)
- Protected Memory
  Protected Memory is the concept of preventing processes from accessing memory improperly or accessing unallocated memory
  Introduced with : Intel 80286 (1982)
- DMA Controller
  A DMA Controller is a piece of hardware which allows data transmission between I/O devices and main memory through direct memory access
  Introduced with : Intel 80286 (1982)
- Memory Paging and Virtual Memory
  Memory Paging allows computers to access data from secondary storage. Virtual memory is the amount of memory a computer can access which is more than the amount of physical memory already installed
  Introduced with : Intel 80386 (1985)

- Super-Scalar Architecture

  The superscalar architecture allows parallel computing for a processor using multiple instruction pipelines to execute several instructions during a clock cycle

  Introduced with: Intel 80486 (1989)

- Streaming SIMD Extension

  SSE is the Single Instruction multiple data instruction set extension to the x86 architecture

  Introduced with: Intel-P6 (1997)

- Out of order execution

  Out of order execution allows a processor to make use of instruction cycles which would have been wasted

  Introduced with: Intel-P6 (1997)

- Register Renaming

  It is a form of ~~pipling~~ pipelining that abstracts virtual registers from physical registers

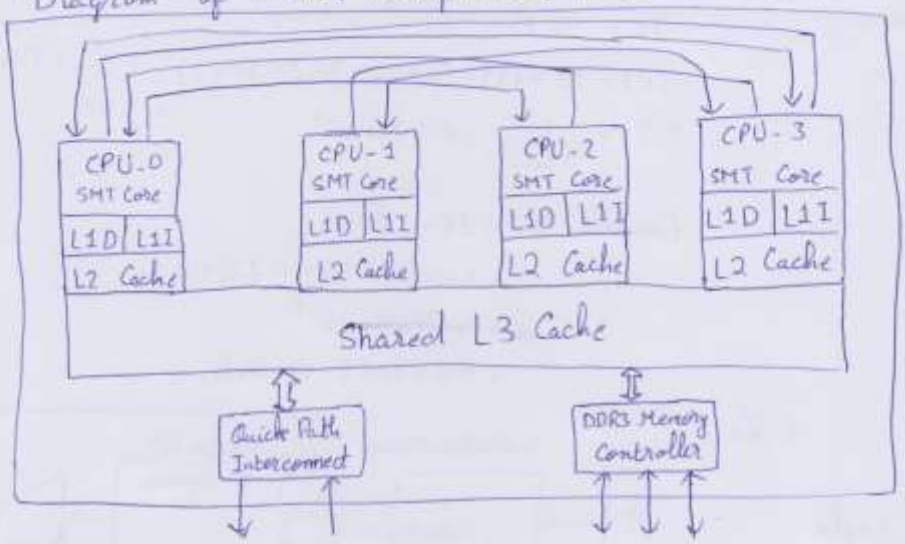
  Introduced with: Intel P6 (1997)

- Branch Prediction

  Branch Prediction is a piece of hardware which predicts the direction of the branch before real time execution

  Introduced with: Intel P6 (1997)

Q. No 3 Diagram of Intel microprocessor Basic Architecture



Q. No 4

- Core i3
  - ↳ Slow speed w/o turbo boost
  - ↳ normally having 2cores
  - ↳ 4 threads
  - ↳ HT enabled
- Core i5
  - ↳ Has turbo boost
  - ↳ normally having 4cores
  - ↳ 4 threads
  - ↳ HT disabled
- Core i7
  - ↳ More cache and clock speed
  - ↳ Normally having 8 cores
  - ↳ 16 threads
  - ↳ HT enabled

Q. No 5

$IC = 50M = 50 \times 10^6 = 5 \times 10^7$

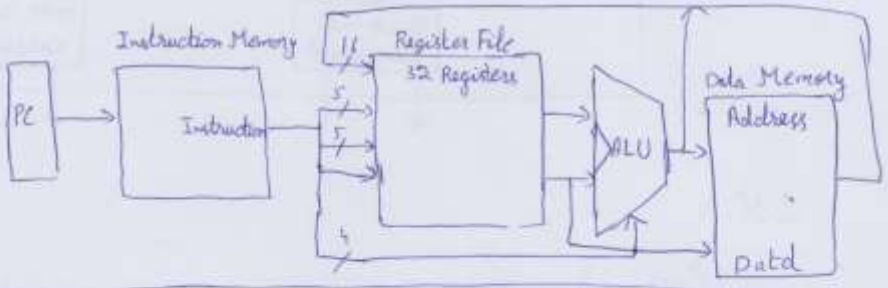
$CPI = (0.4 \times 3) + (0.35 \times 5) + (0.25 \times 2) = 1.2 + 1.75 + 0.5$
$= 3.45$

$CT = \frac{1}{3.6 \times 10^9} = 0.278 \times 10^{-9}$

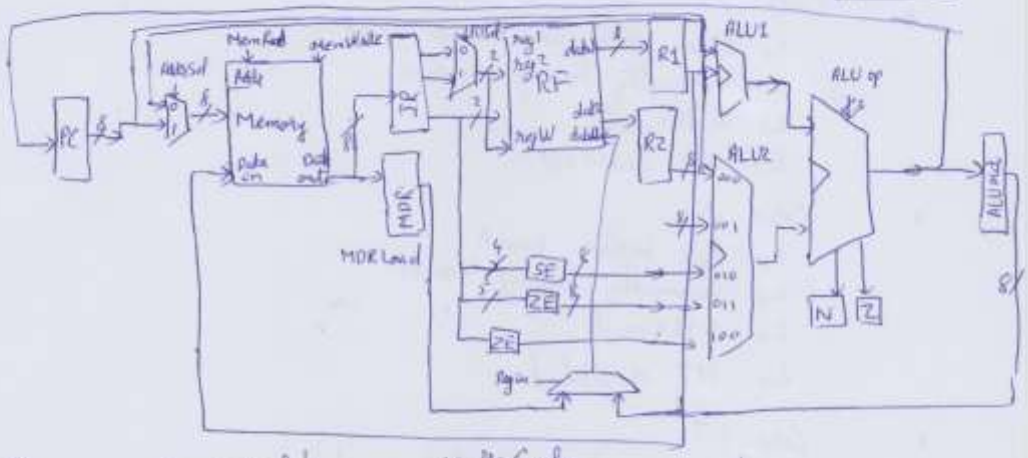
Execution time = $IC \times CPI \times CT$
$= 5 \times 10^7 \times 3.45 \times 0.278 \times 10^{-9}$
$= 4.7955 \times 10^{-2}$
$= 0.047955$ seconds

Q. No. 6

Single Cycle



Multi Cycle



	Single Cycle	Multi Cycle
Pros	Simple, Easy to design	Shorter clock cycles. Instructions are divide
Cons	Long cycle, poor data throughput	Complex, Require more resources

CPU Designers prefer multicycle CPU is because it reduces the clock cycle time and it allows reuse of different components/units

Q No 7 MIPS R3000

MIPS R3000 implements pipline in five phases.

- Istruction Fetch: Fetch instruction from memory
- Instruction Decode: Decode instruction and fetch operand from register.
- EXecution Stage(EX): Execute the instruction or calculate operand address
- Memory Access Stage(MEM): Access an operand from data memory
- Write Back Stage(WB): Write the result into a register

Q. No. 8 Uneven Pipeline

Pipeline in which all phases of the pipeline are uneven and take different time to perform tasks, such pipelines are called uneven pipeline.

Disadvantages of uneven pipelines are

- Irregular flow of data.
- Wasted clock cycles

Q No. 9 Intermediate registers

In an n-stage pipline, intermediate registers store the output of the previous stage. This allows the next stage to perform its task easily by taking input from the intermediate register.

Q No. 10 Classes of pipeline hazards

There are three classes of pipeline hazards.

- Structural Hazard
- Data Hazard
- Control Hazard

- Structural Hazard occurs when multiple instructions try to access same resource

```
ADD  R1, R2, R3
LOAD R1, 5
```

- Data Hazard occurs when instruction depends on result of a previous instruction which is still in the pipeline

```
ADD  R1, R2, R3
SUB  R4, R5, R1
```

- Control Hazard occurs when the value of program counter is changed

```
CMP  R1, R2
JEQ  loop/1048
```

Q. No 11 Out of order execution

Control hazard occurs in case of out of order execution as the program counter changes its address for next instruction

Following are some solutions

- Flush the pipeline
- Delayed Branch
- Dynamic Branch Prediction

Q. No 12 Pipeline Flushing

Pipeline Flushing is an effective solution because if the program counter value is rewriten then the next instruction will be somewhere else from the current instruction and the instruction after that will not be needed. Hence the pipline is flushed and new instructions are added to the pipline from the new PC address

	Clock Cycle	1	2	3	4	5	6
4	CMP R1, R2	IF	ID	EX	MEM	WB	
8	JEQ 1048		IF	ID	EX	MEM	WB
12	↓						
16							
20	Instructions						
24	are flushed						

	1	2	3	4	5	6	7	8
4	IF	ID	EX	MEM	WB			
8		IF	ID	EX	MEM	WB		
12			IF	ID	EX	MEM	WB	
16				IF	ID	EX	MEM	WB
20					IF	ID	EX	MEM
24						IF	ID	EX

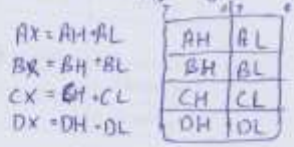
Q No. 13

RISC	CISC
Simple and less number of instructions, easy to decode and implement	Complex and more number of instructions, difficult to decode and implement
Instruction size is fixed and small (32 bits)	Instruction size is variable (1-15 bytes)
CPU control is hardwired without control memory	CPU is microcoded using control memory (ROM)
More general purpose registers (32-192)	Less general purpose registers (8-24)
Pipelining is easy to implement	Pipelining is difficult to implement
Examples: RISC-V, MIPS, ARM	Examples: PDP-11, IBM 370/168, Intel 86

Q No. 14 Segmented Memory Model of Intel 8086

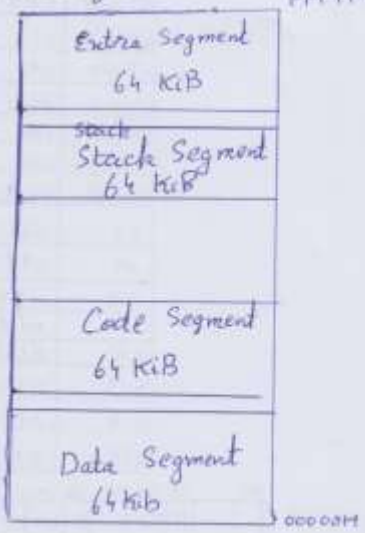
- Addressable memory of 1 MiB
- Can run assembly of 8080
- Memory is segmented into size of 64 KiB.
- Segment registers contain pointers for these segments
- Code, data, stack appear as three distinct units in memory

General Purpose Registers

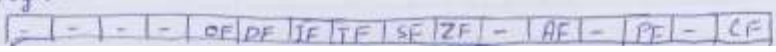


Special Purpose Registers

Memory



Flag Register



b) 0x94F4 : 0xA8C7

~~CS = 0x94F7~~

SS = 0x94F7

IP = 0xA8C7

Physical Address = $SS * 10_{(16)} + IP$

= $0x94F4 * 10_{(16)} + 0xA8C7$

= 0x94F40 + 0xA8C7

= 0x9F807

Q. No. 15 20 bits address in 16 bits IP Register.

Intel 8086 uses 16 bit IP Register to address the 20 bit memory with the help of special purpose segment registers. These segment registers contain the initial starting address of 4 MSBs and the IP register uses these registers to access the memory.

Q. No. 16

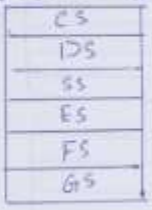
General Purpose Registers

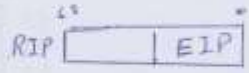
64 bit	32 bit	16 bit	8 bit
r0/rax	eax	ax	al
r1/rbx	ebx	bx	bl
r2/rcx	ecx	cx	cl
r3/rdx	edx	dx	dl
r4/rsi	esi	si	sil
r5/rdi	edi	di	dil
r6/rbp	ebp	bp	bpl
r7/rsp	esp	sp	spl
r8	r8d	r8w	r8b
r9	r9d	r9w	r9b
r10	r10d	r10w	r10b
r11	r11d	r11w	r11b
r12	r12d	r12w	r12b
r13	r13d	r13w	r13b
r14	r14d	r14w	r14b
r15	r15d	r15w	r15b

SSE Media Registers

Memory

Segment Registers





RFLAGS

63	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-		ID	VIP	VIF	AC	VM	RF	-	NT	IOPL	IOPL	OF	DF	IF	TF	SF	ZF	-	AF	-	PF	-	CF

The logical address of x86-64 microprocessor is of 48 bits while the physical address is of 40 bits. The reason behind the logical memory of 48 bits rather than 64 bits is because in today's technology there is no need of a complete 64 bit address. The maximum address a computer may need is only upto 48 bits Hence the remaining bits are unused

Q. No. 17 Flags

- CF : Holds carryout after addition or borrow out after subtraction
- PF : ~~Check~~ Contains Parity bit to check data correctness during transfer
- AF : Works same as CF but for BCD operations
- ZF : If result of ALU is 0 then this flag is set to 1
- SF : Holds MBS (Signed bit) of result after operation from ALU
- TF : Used to enable single step mode
- ~~IF~~ : Used to enable external interrupt from I/O devices
- DF : Used for moving or comparing data (string type)
- OF : Used to detect overflow
- IOPL : Protected mode for I/O devices with privellage 0
- IOP1 : Protected mode for I/O devices with privellage 1
- NT : Indicates nesting of current task
- RF : Used in debugging. Toggles certain exceptions in the process
- VM : Allows the Processor to behave like a different architecture (8086)
- AC : Used to ~~check~~ toggle data alignment check. In case of activation and misalignment an interrupt is issued
- VIF : Used with VMFlag. Acts as IF for 8086 behavior
- VIP : Used to check for pending interrupts for 8086 behavior
- ID : ~~Add~~ Enables use of CPUID instruction